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TEWS TECHNOLOGIES

TIP672

24 Differential I/O Lines with Interrupts

Version 1.0

User Manual

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TIP672-10

24 Differential I/O lines with interrupts

TIP672-10-ET

24 Differential I/O lines with interrupts, operating temperature -40°C to +85°C

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Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

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1.0	First Issue	May 2002
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1.2	Correction “IP Bus Address Map”	December 2002
1.3	Correction “IP Bus Address Map” and “Output Enable Register”	September 2003
1.4	Correction Description “Line Output Enable Register”	March 2004
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1.6	Adding Technical Specifications	February 2006
1.7	New address TEWS LLC	September 2006
1.0.8	New notation of User Manual Issue	March 2009

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1 Product Description

The TIP672 is an IndustryPack® compatible module providing 24 digital differential I/O lines using EIA-422 / EIA-485 compatible, ESD protected line driver and receiver. Each line can be individually configured as differential input or differential output.

Determining the state of the I/O line at any time, the differential receivers are always enabled. This can be used as read back function for lines configured as output.

All 24 input lines can generate an interrupt. Each input interrupt can individually be enabled and cleared. The signal edge handling is programmable.

Configuring an I/O line as output enables the differential transmitter and the I/O line reflects the state programmed in the Output Register.

Optional the I/O lines can be configured for simultaneous update internally and across several IP's by an external clock source. The polarity of the external clock source is programmable.

6 resistor networks (4 x 120 ohms) mounted in sockets are used to terminate the differential I/O lines. The resistor networks can be removed or changed in value.

After power-on or reset all I/O lines are configured as input and all pending interrupts are cleared.

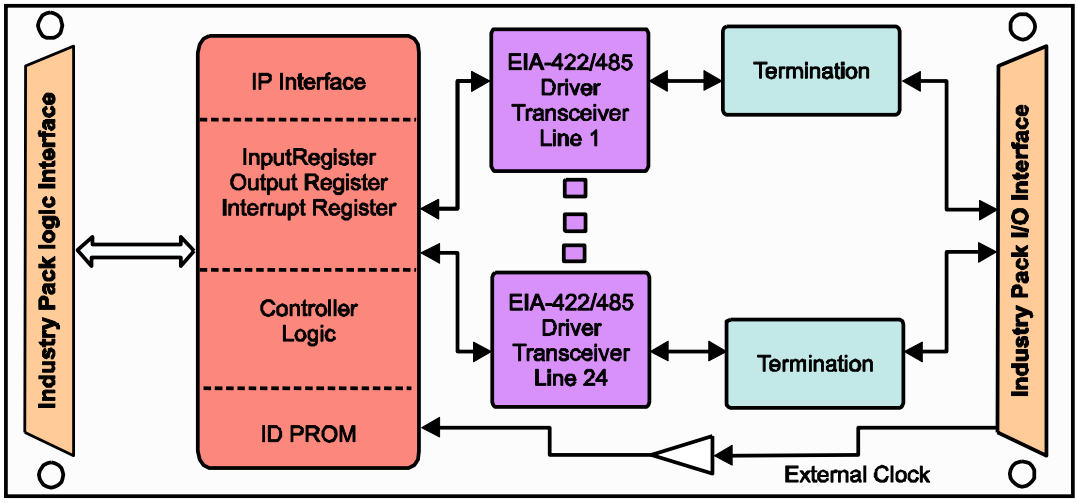


Figure 1-1 : Block Diagram

2 Technical Specification

IP Interface	Single Size IndustryPack® Logic Interface	
Module Specific Data		
Number of diff. I/O Lines	24 differential I/O lines	
Physical Interface	Based on the SP485E ESD protected differential half duplex RS485 transceiver from Sipex	
Termination	120 ohms resistor networks Changeable and removable in groups of four resistors	
TTL Input	Programmable simultaneous update feature by external clock	
Interrupts	One IP Interrupt for all 24 I/O lines Three registers for individual interrupt handling	
Wait States	No wait states	
Interface Connector	50-conductor flat cable	
Power Requirements	All I/O lines Input (reset state) All I/O lines Output – no load	40mA typical @ +5V DC 600mA typical @ +5V DC
Temperature Range	Operating Storage	0 °C to +70 °C -40°C to +85°C (TIP672-10-ET) -40°C to +125°C
MTBF	429000 h	
Humidity	5 – 95 % non-condensing	
Weight	36 g	

Table 2-1 : Technical Specification

3 ID PROM Content

Address	Function	Content
0x01	ASCII 'I'	0x49
0x03	ASCII 'P'	0x50
0x05	ASCII 'A'	0x41
0x07	ASCII 'C'	0x43
0x09	Manufacturer ID	0xB3
0x0B	Model Number	0x34
0x0D	Revision	0x10
0x0F	Reserved	0x00
0x11	Driver ID low byte	0x00
0x13	Driver ID high byte	0x00
0x15	Number of bytes used	0x0C
0x17	CRC	0x3B

Table 3-1 : ID PROM Contents

4 Address Map

4.1 IP Bus Address Map

The TIP672 is accessed in the I/O space through the following set of direct accessible register.

All registers of the TIP672 can be read/write by word (16 bit) or byte (8 bit) accesses.

4.1.1 Word access to TIP672 registers

Register Name	I/O lines	Register Symbol	Size	Address
Line Output Register	1 – 16 17 – 24	OUT_REG	16 bit 16 bit	0x00 0x02
Line Input Register	1 – 16 17 – 24	IN_REG	16 bit 16 bit	0x04 0x06
Line Output Enable Register	1 – 16 17 – 24	ENA_REG	16 bit 16 bit	0x08 0x0A
Control Register		CNT_REG	8 bit	0x0D
Interrupt Vector Register		VEC_REG	8 bit	0x11
Interrupt Enable Register	1 – 16 17 – 24	INT_ENA_REG	16 bit 16 bit	0x12 0x14
Interrupt Polarity Register	1 – 16 17 – 24	INT_POL_REG	16 bit 16 bit	0x16 0x18
Interrupt Status Register	1 – 16 17 – 24	INT_STA_REG	16 bit 16 bit	0x1A 0x1C

Table 4-1 : I/O Space Register / word access

4.1.2 Byte access to TIP672 registers

Register Name	I/O lines	Register Symbol	Size	Address
Line Output Register	9 – 16 1 – 8 17 – 24	OUT_REG	8 bit 8 bit 8 bit	0x00 0x01 0x03
Line Input Register	9 – 16 1 – 8 17 – 24	IN_REG	8 bit 8 bit 8 bit	0x04 0x05 0x07
Line Output Enable Register	9 – 16 1 – 8 17 – 24	ENA_REG	8 bit 8 bit 8 bit	0x08 0x09 0x0B
Control Register		CNT_REG	8 bit	0x0D
Interrupt Vector Register		VEC_REG	8 bit	0x11
Interrupt Enable Register	9 – 16 1 – 8 17 – 24	INT_ENA_REG	8 bit 8 bit 8 bit	0x12 0x13 0x15
Interrupt Polarity Register	9 – 16 1 – 8 17 – 24	INT_POL_REG	8 bit 8 bit 8 bit	0x16 0x17 0x19
Interrupt Status Register	9 – 16 1 – 8 17 – 24	INT_STA_REG	8 bit 8 bit 8 bit	0x1A 0x1B 0x1D

Table 4-2 : I/O Space Register / byte access

To process all 24 bit of one register, at least two 16 bit or three 8 bit accesses are necessary.

All registers are cleared and set each bit to default value after IP reset. All bits of Line Output Enable Register are set to '1'. All other registers set to '0'.

5 Register Description

5.1 Line Output Register

The Line Output Register is a two word wide read/write register. The status of the digital output channels can be set or reset directly by writing to the Line Output Register.

Line Output Register – IP Base Address + 0x00 / 0x02				
Bit Number	**0x00**	**0x02**	**Access**	**Description**
15 (MSB)	OUTPUT 16	-	R/W	To set an output channel active, write a ‘1’ to the corresponding bit. For the inactive state write a ‘0’ to the corresponding bit. 0 : inactive 1 : active
14	OUTPUT 15	-		
13	OUTPUT 14	-		
12	OUTPUT 13	-		
11	OUTPUT 12	-		
10	OUTPUT 11	-		
9	OUTPUT 10	-		
8	OUTPUT 9	-		
7	OUTPUT 8	OUTPUT 24		
6	OUTPUT 7	OUTPUT 23		
5	OUTPUT 6	OUTPUT 22		
4	OUTPUT 5	OUTPUT 21		
3	OUTPUT 4	OUTPUT 20		
2	OUTPUT 3	OUTPUT 19		
1	OUTPUT 2	OUTPUT 18		
0 (LSB)	OUTPUT 1	OUTPUT 17		

Table 5-1 : Line Output Register / word access

Line Output Register – IP Base Address + 0x00 / 0x01 / 0x03					
Bit Number	**0x00**	**0x01**	**0x03**	**Access**	**Description**
7 (MSB)	OUTPUT 16	OUTPUT 8	OUTPUT 24	R/W	To set an output channel active, write a '1' to the corresponding bit. For the inactive state write a '0' to the corresponding bit. 0 : inactive 1 : active
6	OUTPUT 15	OUTPUT 7	OUTPUT 23		
5	OUTPUT 14	OUTPUT 6	OUTPUT 22		
4	OUTPUT 13	OUTPUT 5	OUTPUT 21		
3	OUTPUT 12	OUTPUT 4	OUTPUT 20		
2	OUTPUT 11	OUTPUT 3	OUTPUT 19		
1	OUTPUT 10	OUTPUT 2	OUTPUT 18		
0 (LSB)	OUTPUT 9	OUTPUT 1	OUTPUT 17		

Table 5-2 : Line Output Register / byte access

Normally the output line is loaded with Line Output Register value directly after IP write access. This process is controlled by 8 MHz IP clock.

With the simultaneous update feature the user is able to control the output switch moment by external clock. For more information please refer to chapter "Control Register".

To set one differential line as output, the corresponding bit in the Output Enable Register must be set to '0'.

5.2 Line Input Register

The Line Input Register is a two word wide read only register that reflects the actual state of all 24 differential I/O lines.

Line Input Register – IP Base Address + 0x04 / 0x06				
Bit Number	**0x04**	**0x06**	**Access**	**Description**
15 (MSB)	INPUT 16	-	R	0 : differential I/O line logic low 1 : differential I/O line logic high
14	INPUT 15	-		
13	INPUT 14	-		
12	INPUT 13	-		
11	INPUT 12	-		
10	INPUT 11	-		
9	INPUT 10	-		
8	INPUT 9	-		
7	INPUT 8	INPUT 24		
6	INPUT 7	INPUT 23		
5	INPUT 6	INPUT 22		
4	INPUT 5	INPUT 21		
3	INPUT 4	INPUT 20		
2	INPUT 3	INPUT 19		
1	INPUT 2	INPUT 18		
0 (LSB)	INPUT 1	INPUT 17		

Table 5-3 : Line Input Register / word access

Line Input Register – IP Base Address + 0x04 / 0x05 / 0x07					
Bit Number	**0x04**	**0x05**	**0x07**	**Access**	**Description**
7 (MSB)	INPUT 16	INPUT 8	INPUT 24	R	0 : differential I/O line logic low 1 : differential I/O line logic high
6	INPUT 15	INPUT 7	INPUT 23		
5	INPUT 14	INPUT 6	INPUT 22		
4	INPUT 13	INPUT 5	INPUT 21		
3	INPUT 12	INPUT 4	INPUT 20		
2	INPUT 11	INPUT 3	INPUT 19		
1	INPUT 10	INPUT 2	INPUT 18		
0 (LSB)	INPUT 9	INPUT 1	INPUT 17		

Table 5-4 : Line Input Register / byte access

Normally the input lines are latched into Line Input Register every rising edge of the IP 8 MHz clock.

With the simultaneous update feature the user is able to control this latch moment by external clock. For more information please refer to chapter “Control Register”.

5.3 Line Output Enable Register

The Line Output Enable Register is a two word wide read/write register. To enable the output lines the corresponding bit of the Line Output Enable Register must be set to logic level '0'. To disable the output lines the logic level '1' has to be written into the Line Output Enable Register.

Line Output Enable Register – IP Base Address + 0x08 / 0x0A				
Bit Number	**0x08**	**0x0A**	**Access**	**Description**
15 (MSB)	ENABLE 16	-	R/W	1 : Disable diff. output line 0 : Enable diff. output line
14	ENABLE 15	-		
13	ENABLE 14	-		
12	ENABLE 13	-		
11	ENABLE 12	-		
10	ENABLE 11	-		
9	ENABLE 10	-		
8	ENABLE 9	-		
7	ENABLE 8	ENABLE 24		
6	ENABLE 7	ENABLE 23		
5	ENABLE 6	ENABLE 22		
4	ENABLE 5	ENABLE 21		
3	ENABLE 4	ENABLE 20		
2	ENABLE 3	ENABLE 19		
1	ENABLE 2	ENABLE 18		
0 (LSB)	ENABLE 1	ENABLE 17		

Table 5-5 : Line Output Enable Register / word access

Line Output Enable Register – IP Base Address + 0x08 / 0x09 / 0x0B					
Bit Number	**0x08**	**0x09**	**0x0B**	**Access**	**Description**
7 (MSB)	ENABLE 16	ENABLE 8	ENABLE 24	R/W	1 : Disable diff. output line 0 : Enable diff. output line
6	ENABLE 15	ENABLE 7	ENABLE 23		
5	ENABLE 14	ENABLE 6	ENABLE 22		
4	ENABLE 13	ENABLE 5	ENABLE 21		
3	ENABLE 12	ENABLE 4	ENABLE 20		
2	ENABLE 11	ENABLE 3	ENABLE 19		
1	ENABLE 10	ENABLE 2	ENABLE 18		
0 (LSB)	ENABLE 9	ENABLE 1	ENABLE 17		

Table 5-6 : Line Output Enable Register / byte access

The reset value of the Line Output Enable Register is 0xFFFFFF. That means all differential output lines are disabled.

5.4 Control Register

The Control Register is a byte wide read/write register. The both used bits of the Control Register serve to enable and to switch the polarity of the external clock. I/O interface pin 49 is used as TTL compatible external clock input.

After enable this external clock all 24 input latches and all 24 output drivers of the TIP672 change the state simultaneous on positive or negative edge of this external clock. Several TIP672 in the system could be synchronized in this way.

Control Register – IP Base Address + 0x0D			
Bit Number	**Bit Symbol**	**Access**	**Description**
7 (MSB)	-		Not used by the TIP672
6	-		
5	-		
4	-		
3	-		
2	-		
1	EX_CLK_POL	R/W	External clock polarity 0 : positive edge 1 : negative edge
0 (LSB)	EX_CLK_ENA	R/W	External clock enable 0 : disable 1 : enable

Table 5-7 : Control Register

5.5 Interrupt Vector Register

The Interrupt Vector Register is a byte wide read/write register.

The value of the Interrupt Vector Register could be read/write during I/O cycle and also be read during an interrupt acknowledge cycle.

Interrupt Vector Register – IP Base Address + 0x11			
Bit Number	**Bit Symbol**	**Access**	**Description**
7 (MSB)	IVEC7	R/W	Used for IP interrupt acknowledge cycle
6	IVEC6		
5	IVEC5		
4	IVEC4		
3	IVEC3		
2	IVEC2		
1	IVEC1		
0 (LSB)	IVEC0		

Table 5-8 : Interrupt Vector Register

5.6 Interrupt Enable Register

The Interrupt Enable Register is a two word wide read/write register. To enable interrupt for one I/O line the corresponding bit must be set to logic level '1'.

Interrupt Enable Register – IP Base Address + 0x12 / 0x14				
Bit Number	**0x12**	**0x14**	**Access**	**Description**
15 (MSB)	INT_ENA 16	-	R/W	0 : Interrupt for I/O line disabled 1 : Interrupt for I/O line enabled
14	INT_ENA 15	-		
13	INT_ENA 14	-		
12	INT_ENA 13	-		
11	INT_ENA 12	-		
10	INT_ENA 11	-		
9	INT_ENA 10	-		
8	INT_ENA 9	-		
7	INT_ENA 8	INT_ENA 24		
6	INT_ENA 7	INT_ENA 23		
5	INT_ENA 6	INT_ENA 22		
4	INT_ENA 5	INT_ENA 21		
3	INT_ENA 4	INT_ENA 20		
2	INT_ENA 3	INT_ENA 19		
1	INT_ENA 2	INT_ENA 18		
0 (LSB)	INT_ENA 1	INT_ENA 17		

Table 5-9 : Interrupt Enable Register / word access

Interrupt Enable Register – IP Base Address + 0x12 / 0x13 / 0x15					
Bit Number	**0x12**	**0x13**	**0x15**	**Access**	**Description**
7 (MSB)	INT_ENA 16	INT_ENA 8	INT_ENA 24	R/W	0 : Interrupt for I/O line disabled 1 : Interrupt for I/O line enabled
6	INT_ENA 15	INT_ENA 7	INT_ENA 23		
5	INT_ENA 14	INT_ENA 6	INT_ENA 22		
4	INT_ENA 13	INT_ENA 5	INT_ENA 21		
3	INT_ENA 12	INT_ENA 4	INT_ENA 20		
2	INT_ENA 11	INT_ENA 3	INT_ENA 19		
1	INT_ENA 10	INT_ENA 2	INT_ENA 18		
0 (LSB)	INT_ENA 9	INT_ENA 1	INT_ENA 17		

Table 5-10: Interrupt Enable Register / byte access

After enable the interrupt for one I/O line the TIP672 generates IP interrupts after rising or falling edge received on this I/O line. The edge which releases an interrupt depends on the value of the corresponding bit in the Interrupt Polarity Register.

Also an interrupt is generated by setting the Interrupt Enable Register, if there is a trigger edge before enable the interrupt for the I/O line.

5.7 Interrupt Polarity Register

The Interrupt Polarity Register is a two word wide read/write register. The Interrupt Polarity Register is used to set the positive or negative transition which generates IP interrupts.

The third source for IP interrupts is, if the Interrupt Polarity Register is switched and the corresponding I/O line is already in active state.

Example: I/O line is active (‘1’), the interrupt is enabled and the Interrupt Polarity Register is switched from negative to positive transition.

Interrupt Polarity Register – IP Base Address + 0x16 / 0x18				
Bit Number	**0x16**	**0x18**	**Access**	**Description**
15 (MSB)	INT_POL 16	-	R/W	0 : negative transition 1 : positive transition
14	INT_POL 15	-		
13	INT_POL 14	-		
12	INT_POL 13	-		
11	INT_POL 12	-		
10	INT_POL 11	-		
9	INT_POL 10	-		
8	INT_POL 9	-		
7	INT_POL 8	INT_POL 24		
6	INT_POL 7	INT_POL 23		
5	INT_POL 6	INT_POL 22		
4	INT_POL 5	INT_POL 21		
3	INT_POL 4	INT_POL 20		
2	INT_POL 3	INT_POL 19		
1	INT_POL 2	INT_POL 18		
0 (LSB)	INT_POL 1	INT_POL 17		

Table 5-11: Interrupt Polarity Register / word access

Interrupt Polarity Register – IP Base Address + 0x16 / 0x17 / 0x19					
Bit Number	**0x16**	**0x17**	**0x19**	**Access**	**Description**
7 (MSB)	INT_POL 16	INT_POL 8	INT_POL 24	R/W	0 : negative transition 1 : positive transition
6	INT_POL 15	INT_POL 7	INT_POL 23		
5	INT_POL 14	INT_POL 6	INT_POL 22		
4	INT_POL 13	INT_POL 5	INT_POL 21		
3	INT_POL 12	INT_POL 4	INT_POL 20		
2	INT_POL 11	INT_POL 3	INT_POL 19		
1	INT_POL 10	INT_POL 2	INT_POL 18		
0 (LSB)	INT_POL 9	INT_POL 1	INT_POL 17		

Table 5-12: Interrupt Polarity Register / byte access

Additionally to the Interrupt Polarity Register the corresponding bit in the Interrupt Enable Register must be enabled to generate an IP interrupt.

5.8 Interrupt Status Register

The Interrupt Status Register is a two word wide read/write register.

A pending interrupt request for a specific I/O line is cleared by writing a '1' to the according bit of the Interrupt Status Register.

Interrupt Status Register – IP Base Address + 0x1A / 0x1C				
Bit Number	**0x1A**	**0x1C**	**Access**	**Description**
15 (MSB)	INT_STA 16	-	R/W	**Read access** 0 : no interrupt request pending 1 : interrupt request pending **Write access** 1 : clear pending interrupt request
14	INT_STA 15	-		
13	INT_STA 14	-		
12	INT_STA 13	-		
11	INT_STA 12	-		
10	INT_STA 11	-		
9	INT_STA 10	-		
8	INT_STA 9	-		
7	INT_STA 8	INT_STA 24		
6	INT_STA 7	INT_STA 23		
5	INT_STA 6	INT_STA 22		
4	INT_STA 5	INT_STA 21		
3	INT_STA 4	INT_STA 20		
2	INT_STA 3	INT_STA 19		
1	INT_STA 2	INT_STA 18		
0 (LSB)	INT_STA 1	INT_STA 17		

Table 5-13: Interrupt Status Register / word access

Interrupt Status Register – IP Base Address + 0x1A / 0x1B / 0x1D					
Bit Number	**0x1A**	**0x1B**	**0x1D**	**Access**	**Description**
7 (MSB)	INT_STA 16	INT_STA 8	INT_STA 24	R/W	**Read access** 0 : no interrupt request pending 1 : interrupt request pending **Write access** 1 : clear pending interrupt request
6	INT_STA 15	INT_STA 7	INT_STA 23		
5	INT_STA 14	INT_STA 6	INT_STA 22		
4	INT_STA 13	INT_STA 5	INT_STA 21		
3	INT_STA 12	INT_STA 4	INT_STA 20		
2	INT_STA 11	INT_STA 3	INT_STA 19		
1	INT_STA 10	INT_STA 2	INT_STA 18		
0 (LSB)	INT_STA 9	INT_STA 1	INT_STA 17		

Table 5-14: Interrupt Status Register / byte access

6 Installation TIP672

6.1 Termination

Six resistor networks (4 x 120 ohms) mounted in sockets are used to terminate the differential I/O lines. The resistor networks can be removed or changed in value.

A resistor network is made out of four individual resistors in one serial package.

Groups of resistors:

N3 : I/O line 1,2,3,4

N2 : I/O line 5,6,7,8

N5 : I/O line 9,10,11,12

N4 : I/O line 13,14,15,16

N7 : I/O line 17,18,19,20

N6 : I/O line 21,22,23,24

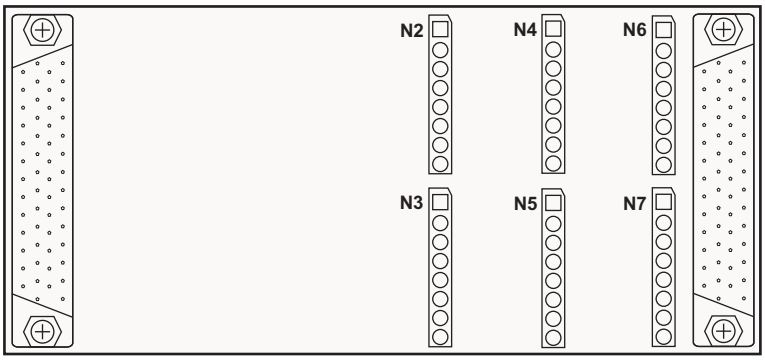


Figure 6-1 : Location of Termination Resistors

Resistor pining:

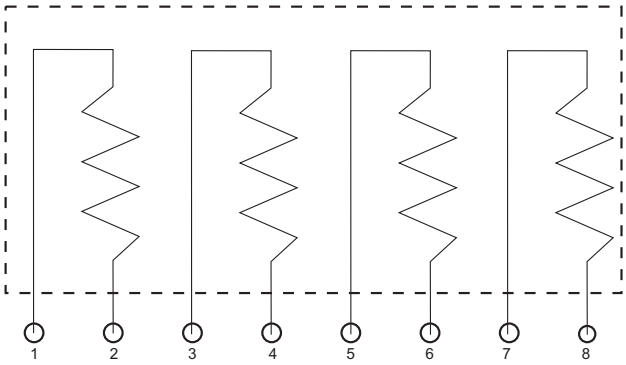


Figure 6-2 : Pining of Termination Resistors

6.2 Differential I/O Interface

The 24 differential I/O Lines are realized with a standard differential RS485 driver with transmit enable.

Each pair of differential I/O lines has a removable or changeable 120 ohms termination resistor.

See the following figure for more information about electrical circuitry.

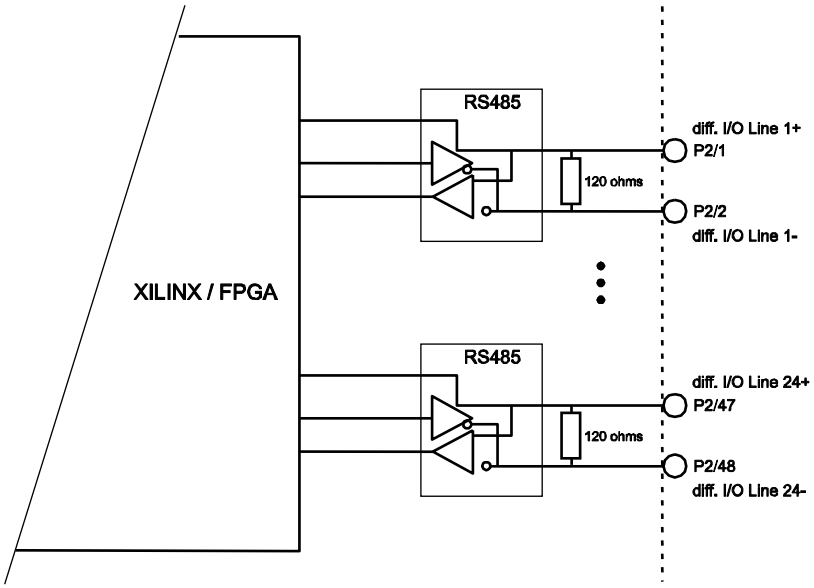


Figure 6-3 : Differential I/O Interface

7 I/O Pin Assignment

I/O Pin Number	Function	Signal Name
1	Differential I/O Line 1+	I/O 1+
2	Differential I/O Line 1-	I/O 1-
3	Differential I/O Line 2+	I/O 2+
4	Differential I/O Line 2-	I/O 2-
5	Differential I/O Line 3+	I/O 3+
6	Differential I/O Line 3-	I/O 3-
7	Differential I/O Line 4+	I/O 4+
8	Differential I/O Line 4-	I/O 4-
9	Differential I/O Line 5+	I/O 5+
10	Differential I/O Line 5-	I/O 5-
11	Differential I/O Line 6+	I/O 6+
12	Differential I/O Line 6-	I/O 6-
13	Differential I/O Line 7+	I/O 7+
14	Differential I/O Line 7-	I/O 7-
15	Differential I/O Line 8+	I/O 8+
16	Differential I/O Line 8-	I/O 8-
17	Differential I/O Line 9+	I/O 9+
18	Differential I/O Line 9-	I/O 9-
19	Differential I/O Line 10+	I/O 10+
20	Differential I/O Line 10-	I/O 10-
21	Differential I/O Line 11+	I/O 11+
22	Differential I/O Line 11-	I/O 11-
23	Differential I/O Line 12+	I/O 12+
24	Differential I/O Line 12-	I/O 12-
25	Differential I/O Line 13+	I/O 13+
26	Differential I/O Line 13-	I/O 13-
27	Differential I/O Line 14+	I/O 14+
28	Differential I/O Line 14-	I/O 14-
29	Differential I/O Line 15+	I/O 15+
30	Differential I/O Line 15-	I/O 15-
31	Differential I/O Line 16+	I/O 16+
32	Differential I/O Line 16-	I/O 16-
33	Differential I/O Line 17+	I/O 17+
34	Differential I/O Line 17-	I/O 17-
35	Differential I/O Line 18+	I/O 18+
36	Differential I/O Line 18-	I/O 18-

I/O Pin Number	Function	Signal Name
37	Differential I/O Line 19+	I/O 19+
38	Differential I/O Line 19-	I/O 19-
39	Differential I/O Line 20+	I/O 20+
40	Differential I/O Line 20-	I/O 20-
41	Differential I/O Line 21+	I/O 21+
42	Differential I/O Line 21-	I/O 21-
43	Differential I/O Line 22+	I/O 22+
44	Differential I/O Line 22-	I/O 22-
45	Differential I/O Line 23+	I/O 23+
46	Differential I/O Line 23-	I/O 23-
47	Differential I/O Line 24+	I/O 24+
48	Differential I/O Line 24-	I/O 24-
49	External Clock	EX_CLK
50	Ground	GND

Table 7-1 : I/O Pin Assignment

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