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TEWS TECHNOLOGIES

# TIP675

## 48 TTL I/O Lines with Interrupts

Version 1.0

## User Manual

Issue 1.0.6

May 2012

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## TIP675-10

48 TTL I/O Lines with Interrupts

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### Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

| | |
|---|---|
| W | Write Only |
| R | Read Only |
| R/W | Read/Write |
| R/C | Read/Clear |
| R/S | Read/Set |

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| Issue | Description | Date |
|---|---|---|
| 1.0 | First Issue | September 2002 |
| 1.1 | Correction I/O Pin Assignment | January 2003 |
| 1.2 | Completion of technical Information and new Hardware Revision | February 2003 |
| 1.3 | New address TEWS LLC | September 2006 |
| 1.0.4 | New notation of User Manual Issue | December 2008 |
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# 1 Product Description

The TIP675 is an IndustryPack® compatible module providing 48 digital TTL tri-state I/O lines with pull up resistors. Each of the 48 I/O lines is ESD protected and protected against overvoltage.

The line inputs are always enabled, allows determining the state of the I/O line at any time. This can be used as read back function for lines configured as outputs.

All 48 input lines can generate an interrupt. Each input interrupt can individually be enabled and cleared. Interrupts for negative and positive transitions could be used together with separate interrupt pending registers.

All interrupt inputs have an electronic debounce circuit to prevent short spikes on input lines to cause an IP interrupt.

Optional the I/O lines can be configured for simultaneous update internally and across several IP's by an external clock source. The polarity of the external clock source is programmable.

6 resistor networks mounted in sockets are used to pull the tri-state I/O lines to a logic high value. The resistor networks can be removed or changed in value.

After power-on or reset all I/O lines are configured as input and all pending interrupts are cleared.

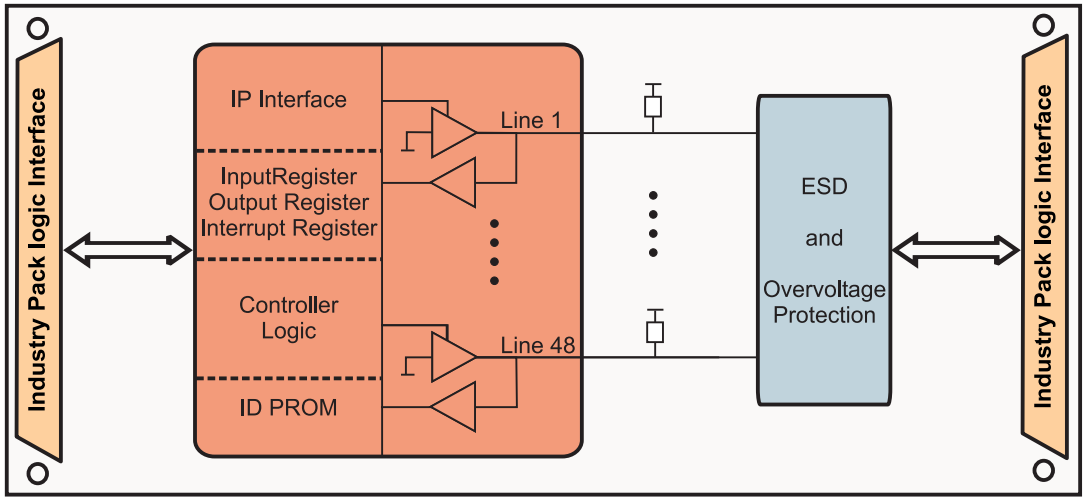



Figure 1-1 : Block Diagram

# 2 Technical Specification

| | | |
|---|---|---|
| **IP Interface** | | |
| **Interface** | Single Size IndustryPack® Logic Interface compliant to ANSI/VITA 4-1995 | |
| **ID ROM Data** | Format I | |
| **I/O Space** | used with no wait states | |
| **Memory Space** | not used | |
| **Interrupts** | IP interrupt (Int1) for all 48 I/O lines;<br>4 registers for individual interrupt handling | |
| **DMA** | Not supported | |
| **Clock Rate** | 8 MHz | |
| **Module Type** | Type I | |
| **I/O Interface** | | |
| Number of TTL I/O Lines | 48 lines | |
| Termination | 4.7k ohms resistor network as pull up for each tri-state I/O line;<br>Changeable and removable in groups of eight resistors | |
| Output 'Low' Current | –12mA maximum | |
| Output 'High' Current | Limited by 4k7 pull up to 1mA | |
| TTL Input / External Clock | Programmable simultaneous update feature by external clock | |
| External Clock Frequency | 8 MHz | |
| Interrupts | IP interrupt 0 for all 48 I/O lines;<br>4 registers for individual interrupt handling | |
| Interface Connector | 50-conductor flat cable | |
| **Physical Data** | | |
| **Power Requirements** | 40mA typical @+5V DC all lines are inputs | |
| **Temperature Range** | Operating<br>Storage | -40 °C to +85 °C<br>-65°C to +150°C |
| **MTBF** | 198000 h<br>MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: $G_B$ 20°C.<br>The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation. | |
| **Humidity** | 5 – 95 % non-condensing | |
| **Weight** | 30 g | |

Table 2-1 : Technical Specification

# 3 ID PROM Contents

| Address | Function | Contents |
|---|---|---|
| **0x01** | ASCII 'I' | **0x49** |
| **0x03** | ASCII 'P' | **0x50** |
| **0x05** | ASCII 'A' | **0x41** |
| **0x07** | ASCII 'C' | **0x43** |
| **0x09** | Manufacturer ID | **0xB3** |
| **0x0B** | Model Number | **0x36** |
| **0x0D** | Revision | **0x10** |
| **0x0F** | Reserved | **0x00** |
| **0x11** | Driver-ID Low - Byte | **0x00** |
| **0x13** | Driver-ID High - Byte | **0x00** |
| **0x15** | Number of bytes used | **0x0C** |
| **0x17** | CRC | **0xD8** |
| **0x19 to 0x3F** | Reserved | **0x00** |

Table 3-1 : ID PROM Contents

# 4 IP Addressing

## 4.1 I/O Addressing

The TIP675 is accessed in the I/O space though the following set of direct accessible registers.

All register of the TIP675 can be read/write by word (16 bit) or byte (8 bit) accesses.

| Address | Symbol | Description | Size (Bit) | Access |
|---|---|---|---|---|
| 0x00 | OUT_REG | Output Register Line 1- 16 | 16 | R/W |
| 0x02 | | Output Register Line 17 - 32 | 16 | R/W |
| 0x04 | | Output Register Line 33 - 48 | 16 | R/W |
| 0x06 | IN_REG | Input Register Line 1- 16 | 16 | R |
| 0x08 | | Input Register Line 17 - 32 | 16 | R |
| 0x0A | | Input Register Line 33 - 48 | 16 | R |
| 0x0C | DIR_REG | Direction Register Line 1- 16 | 16 | R/W |
| 0x0E | | Direction Register Line 17 - 32 | 16 | R/W |
| 0x10 | | Direction Register Line 33 - 48 | 16 | R/W |
| | IP_STA_REG | Rising Edge Interrupt Status Register | | |
| 0x12 | | Line 1- 16 | 16 | R/W |
| 0x14 | | Line 17 - 32 | 16 | R/W |
| 0x16 | | Line 33 - 48 | 16 | R/W |
| | IP_ENA_REG | Rising Edge Interrupt Enable Register | | |
| 0x18 | | Line 1- 16 | 16 | R/W |
| 0x1A | | Line 17 - 32 | 16 | R/W |
| 0x1C | | Line 33 - 48 | 16 | R/W |
| | IN_STA_REG | Falling Edge Interrupt Status Register | | |
| 0x1E | | Line 1- 16 | 16 | R/W |
| 0x20 | | Line 17 - 32 | 16 | R/W |
| 0x22 | | Line 33 - 48 | 16 | R/W |
| | IN_ENA_REG | Falling Edge Interrupt Enable Register | | |
| 0x24 | | Line 1- 16 | 16 | R/W |
| 0x26 | | Line 17 - 32 | 16 | R/W |
| 0x28 | | Line 33 - 48 | 16 | R/W |
| 0x2B | CNT_REG | Control Register | 8 | R/W |
| 0x2D | VEC_REG | Interrupt Vector Register | 8 | R |

Table 4-1 : I/O Register Set

## 4.2 Output Register

The Line Output Register is subdivided into three word wide read/write registers. The status of the digital output channels can be set or reset directly by writing to the Line Output Register.

| Bit | Symbol | Description | Access | Reset Value |
|---|---|---|---|---|
| 15:0 | OUT_REG | 16 bit Output Data<br>Bit 0 represents Output Line 1 and bit 15 represents Output Line 16.<br><br>0 : inactive<br>1 : active / tri-state | R/W | 0xFF |

Table 4-2 : Output Register Line 1 -16

| Bit | Symbol | Description | Access | Reset Value |
|---|---|---|---|---|
| 15:0 | OUT_REG | 16 bit Output Data<br>Bit 0 represents Output Line 17 and bit 15 represents Output Line 32.<br><br>0 : inactive<br>1 : active / tri-state | R/W | 0xFF |

Table 4-3 : Output Register Line 17 -32

| Bit | Symbol | Description | Access | Reset Value |
|---|---|---|---|---|
| 15:0 | OUT_REG | 16 bit Output Data<br>Bit 0 represents Output Line 33 and bit 15 represents Output Line 48.<br><br>0 : inactive<br>1 : active / tri-state | R/W | 0xFF |

Table 4-4 : Output Register Line 33 -48

**After power-on and reset all bits of Line Output Register are set to active / tri-state value.**

Normally the output line is loaded with Line Output Register value direct after IP write access. This process is controlled by 8 MHz IP clock.

With the simultaneous update feature the user is able to control the output switch moment by external clock. For more information please refer to chapter “Control Register”.

**To set a TTL line as output, the corresponding bit in the Direction Register must be set to ‘1’.**

# 4.3 Input Register

The Line Input Register is subdivided into three word wide read only registers that reflects the actual state of all 48 digital TTL I/O lines.

| Bit | Symbol | Description | Access | Reset Value |
|---|---|---|---|---|
| 15:0 | IN_REG | 16 bit Input Data<br>Bit 0 represents Input Line 1 and bit 15 represents Input Line 16.<br><br>0 : TTL I/O line logic low<br>1 : TTL I/O line logic high | R | |

Table 4-5 : Input Register Line 1 -16

| Bit | Symbol | Description | Access | Reset Value |
|---|---|---|---|---|
| 15:0 | IN_REG | 16 bit Input Data<br>Bit 0 represents Input Line 17 and bit 15 represents Input Line 32.<br><br>0 : TTL I/O line logic low<br>1 : TTL I/O line logic high | R | |

Table 4-6 : Input Register Line 17 -32

| Bit | Symbol | Description | Access | Reset Value |
|---|---|---|---|---|
| 15:0 | IN_REG | 16 bit Input Data<br>Bit 0 represents Input Line 33 and bit 15 represents Input Line 48.<br><br>0 : TTL I/O line logic low<br>1 : TTL I/O line logic high | R | |

Table 4-7 : Input Register Line 33 -48

## 4.4 Line Direction Register

The Line Direction Register is subdivided into three word read/write registers. To enable the output lines the corresponding bit of the Line Direction Register must be set to logic level ‘1’. To disable the output lines and switch to an only input line the logic level ‘0’ has to be written into the Line Direction Register.

| Bit | Symbol | Description | Access | Reset Value |
|---|---|---|---|---|
| 15:0 | DIR_REG | 16 bit Line Direction Register<br>Bit 0 represents the direction for I/O Line 1 and bit 15 represents the direction for I/O Input Line 16.<br><br>0 : TTL I/O line as Input<br>1 : TTL I/O line as Output | R | 0x00 |

Table 4-8 : Line Direction Register Line 1 -16

| Bit | Symbol | Description | Access | Reset Value |
|---|---|---|---|---|
| 15:0 | DIR_REG | 16 bit Line Direction Register<br>Bit 0 represents the direction for I/O Line 17 and bit 15 represents the direction for I/O Input Line 32.<br><br>0 : TTL I/O line as Input<br>1 : TTL I/O line as Output | R | 0x00 |

Table 4-9 : Line Direction Register Line 17 -32

| Bit | Symbol | Description | Access | Reset Value |
|---|---|---|---|---|
| 15:0 | DIR_REG | 16 bit Line Direction Register<br>Bit 0 represents the direction for I/O Line 33 and bit 15 represents the direction for I/O Input Line 48.<br><br>0 : TTL I/O line as Input<br>1 : TTL I/O line as Output | R | 0x00 |

Table 4-10: Line Direction Register Line 33 -48

## 4.5 Rising Edge Interrupt Status Registers

The Rising Edge Interrupt Status Register is subdivided into three word read/write registers and reflected in the corresponding bit a pending interrupt.

A pending interrupt request for a specific TTL I/O line is cleared by writing '1' to the according bit of the Rising Edge Interrupt Status Register.

| Bit | Symbol | Description | Access | Reset Value |
|---|---|---|---|---|
| 15:0 | IP_STA | 16 bit Register<br>Bit 0 represents the interrupt status for I/O Line 1 and bit 15 represents the interrupt status for I/O Input Line 16.<br><br>**Read access**<br>0 : no interrupt request pending<br>1 : interrupt request pending<br><br>**Write access**<br>1 : clear pending interrupt request | R/W | 0x00 |

Table 4-11: Rising Edge Interrupt Status Register Line 1 -16

| Bit | Symbol | Description | Access | Reset Value |
|---|---|---|---|---|
| 15:0 | IP_STA | 16 bit Register<br>Bit 0 represents the interrupt status for I/O Line 17 and bit 15 represents the interrupt status for I/O Input Line 32.<br><br>**Read access**<br>0 : no interrupt request pending<br>1 : interrupt request pending<br><br>**Write access**<br>1 : clear pending interrupt request | R/W | 0x00 |

Table 4-12: Rising Edge Interrupt Status Register Line 17 -32

| Bit | Symbol | Description | Access | Reset Value |
|---|---|---|---|---|
| 15:0 | IP_STA | 16 bit Register<br>Bit 0 represents the interrupt status for I/O Line 33 and bit 15 represents the interrupt status for I/O Input Line 48.<br><br>**Read access**<br>0 : no interrupt request pending<br>1 : interrupt request pending<br><br>**Write access**<br>1 : clear pending interrupt request | R/W | 0x00 |

Table 4-13: Rising Edge Interrupt Status Register Line 33 -48

# 4.6 Rising Edge Interrupt Enable Registers

The Rising Edge Interrupt Enable Register is subdivided into three word read/write registers. To enable an interrupt for positive transitions on TTL input line the corresponding bit must be set to logic level ‘1’. To disable the interrupt source the corresponding bit must be set to logic level ‘0’.

| Bit | Symbol | Description | Access | Reset Value |
|---|---|---|---|---|
| 15:0 | IP_ENA | 16 bit Interrupt Enable Register<br>Bit 0 represents the interrupt enable for I/O Line 1 and bit 15 represents the interrupt enable for I/O Input Line 16.<br><br>0 : Interrupt for I/O line disabled<br>1 : Interrupt for I/O line enabled | R/W | 0x00 |

Table 4-14: Rising Edge Interrupt Enable Register Line 1 -16

| Bit | Symbol | Description | Access | Reset Value |
|---|---|---|---|---|
| 15:0 | IP_ENA | 16 bit Interrupt Enable Register<br>Bit 0 represents the interrupt enable for I/O Line 17 and bit 15 represents the interrupt enable for I/O Input Line 32.<br><br>0 : Interrupt for I/O line disabled<br>1 : Interrupt for I/O line enabled | R/W | 0x00 |

Table 4-15: Rising Edge Interrupt Enable Register Line 17 -32

| Bit | Symbol | Description | Access | Reset Value |
|---|---|---|---|---|
| 15:0 | IP_ENA | 16 bit Interrupt Enable Register<br>Bit 0 represents the interrupt enable for I/O Line 33 and bit 15 represents the interrupt enable for I/O Input Line 48.<br><br>0 : Interrupt for I/O line disabled<br>1 : Interrupt for I/O line enabled | R/W | 0x00 |

Table 4-16: Rising Edge Interrupt Enable Register Line 33 -48

# 4.7 Falling Edge Interrupt Status Registers

The Falling Edge Interrupt Status Register is subdivided into three word read/write registers and reflected in the corresponding bit a pending interrupt.

A pending interrupt request for a specific TTL I/O line is cleared by writing '1' to the according bit of the Falling Edge Interrupt Status Register.

| Bit | Symbol | Description | Access | Reset Value |
|---|---|---|---|---|
| 15:0 | IN_STA | 16 bit Register<br>Bit 0 represents the interrupt status for I/O Line 1 and bit 15 represents the interrupt status for I/O Input Line 16.<br><br>**Read access**<br>0 : no interrupt request pending<br>1 : interrupt request pending<br><br>**Write access**<br>1 : clear pending interrupt request | R/W | 0x00 |

Table 4-17: Falling Edge Interrupt Status Register Line 1 -16

| Bit | Symbol | Description | Access | Reset Value |
|---|---|---|---|---|
| 15:0 | IN_STA | 16 bit Register<br>Bit 0 represents the interrupt status for I/O Line 17 and bit 15 represents the interrupt status for I/O Input Line 32.<br><br>**Read access**<br>0 : no interrupt request pending<br>1 : interrupt request pending<br><br>**Write access**<br>1 : clear pending interrupt request | R/W | 0x00 |

Table 4-18: Falling Edge Interrupt Status Register Line 17 -32

| Bit | Symbol | Description | Access | Reset Value |
|---|---|---|---|---|
| 15:0 | IN_STA | 16 bit Register<br>Bit 0 represents the interrupt status for I/O Line 33 and bit 15 represents the interrupt status for I/O Input Line 48.<br><br>**Read access**<br>0 : no interrupt request pending<br>1 : interrupt request pending<br><br>**Write access**<br>1 : clear pending interrupt request | R/W | 0x00 |

Table 4-199: Falling Edge Interrupt Status Register Line 33 -48

# 4.8 Falling Edge Interrupt Enable Registers

The Falling Edge Interrupt Enable Register is subdivided into three word read/write registers. To enable an interrupt for negative transitions on TTL input line the corresponding bit must be set to logic level ‘1’. To disable the interrupt source the corresponding bit must be set to logic level ‘0’.

| Bit | Symbol | Description | Access | Reset Value |
|---|---|---|---|---|
| 15:0 | IN_ENA | 16 bit Interrupt Enable Register<br>Bit 0 represents the interrupt enable for I/O Line 1 and bit 15 represents the interrupt enable for I/O Input Line 16.<br><br>0 : Interrupt for I/O line disabled<br>1 : Interrupt for I/O line enabled | R/W | 0x00 |

Table 4-20: Falling Edge Interrupt Enable Register Line 1 -16

| Bit | Symbol | Description | Access | Reset Value |
|---|---|---|---|---|
| 15:0 | IN_ENA | 16 bit Interrupt Enable Register<br>Bit 0 represents the interrupt enable for I/O Line 17 and bit 15 represents the interrupt enable for I/O Input Line 32.<br><br>0 : Interrupt for I/O line disabled<br>1 : Interrupt for I/O line enabled | R/W | 0x00 |

Table 4-21: Falling Edge Interrupt Enable Register Line 17 -32

| Bit | Symbol | Description | Access | Reset Value |
|---|---|---|---|---|
| 15:0 | IN_ENA | 16 bit Interrupt Enable Register<br>Bit 0 represents the interrupt enable for I/O Line 33 and bit 15 represents the interrupt enable for I/O Input Line 48.<br><br>0 : Interrupt for I/O line disabled<br>1 : Interrupt for I/O line enabled | R/W | 0x00 |

Table 4-22: Falling Edge Interrupt Enable Register Line 33 -48

# 4.9 Control Register

The Control Register is a byte wide read/write register. The both used bits of the Control Register serve to enable and to switch the polarity of the external clock. I/O interface pin 49 is used as TTL compatible external clock input.

After enabling this external clock all 48 input latches and all 48 output drivers of the TIP675 change there state simultaneous on positive or negative edge of this external clock. Several TIP675 in the system could be synchronized in this way.

| Bit | Symbol | Description | Access | Reset Value |
|---|---|---|---|---|
| 7:2 | | not used | | |
| 1 | EX_CLK_POL | external clock polarity<br>0 : positive edge<br>1 : negative edge | R/W | |
| 0 | EX_CLK_ENA | external clock enable<br>0 : disable<br>1 : enable | R/W | |

Table 4-23: Control Register

**After enable the external clock the value of Line Input Register is invalid until the first external clock edge.**

The maximum input frequency of the external clock is limited to 8 MHz. The symmetry of this external clock does not require 50%, but the minimum pulse length is 10ns.

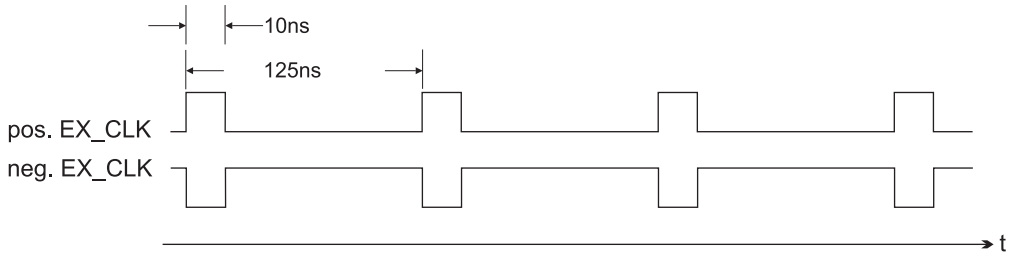



Figure 4-1 : Maximum Frequency of external Clock

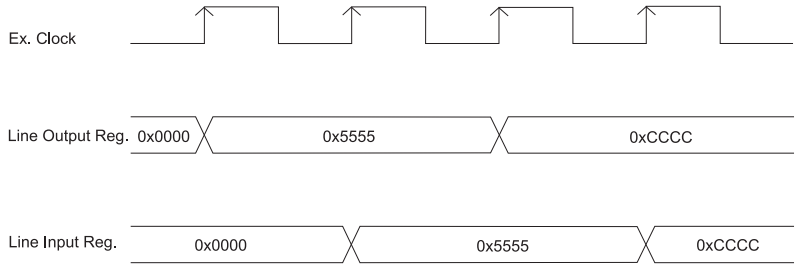
**Info for using the External Clock**

**Input:** After positive or negative external clock edge all input lines are latched and loaded into Line Input Register. Also input interrupts are generated with the external clock edge. This guarantees that the input transitions which are responsible for the interrupt are latched into the Line Input Register.

**Output:** The data of the Line Output Register are switched to the output port with positive or negative external clock edge.

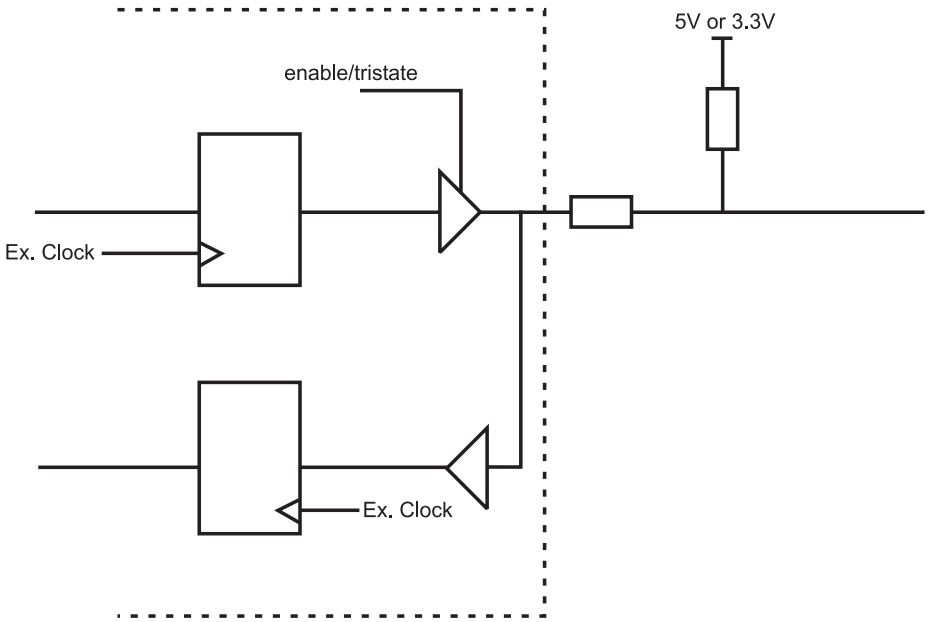
**Input/Output:** If the I/O lines are used as output port and the corresponding Line Input Register is read before a second external clock edge, both registers are different. Only after the second external clock edge both registers, Line Input and Line Output, are equal.

**Example:**




The reason for this is the internal switching time for the signals and the I/O circuit design of the TIP675. If the output register and the input register are triggered by the same external clock signal, both flip-flops load the value at the same time. The output signal needs some nanoseconds to reach the input of the input register. So the previous value at the input register is latched.

The following figure shows a simplified I/O block of the TIP675.




As well by using the internal 8 MHz IP clock these internal switching times are present. But the time between two trigger impulses is short enough to load the actual value into the input registers before a new IP access could be released.

## 4.10 Interrupt Vector Register

The Interrupt Vector Register is a byte wide read/write register.

The value of the Interrupt Vector Register could be read/write during I/O cycle and also be read during an interrupt acknowledge cycle.

| Bit | Symbol | Description | Access | Reset Value |
|---|---|---|---|---|
| 7:0 | IVEC | Used for IP interrupt acknowledge cycle | R/W | |

Table 4-24: Interrupt Vector Register

**All 48 digital I/O lines use the IP interrupt line 0 to signal a pending interrupt.**

# 5 Installation

## 5.1 Pull Up Resistors

Six resistor networks (8 x 4.7k ohms) mounted in sockets are used to pull up the tri-state TTL I/O lines. The resistor networks can be removed or changed in value.

A resistor network is made out of eight individual resistors in one serial package.

Groups of resistors:

N19 : I/O line 1 – 8

N18 : I/O line 25 – 32

N17 : I/O line 9 – 16

N16 : I/O line 33 – 40

N15 : I/O line 17 – 24

N14 : I/O line 41 – 48

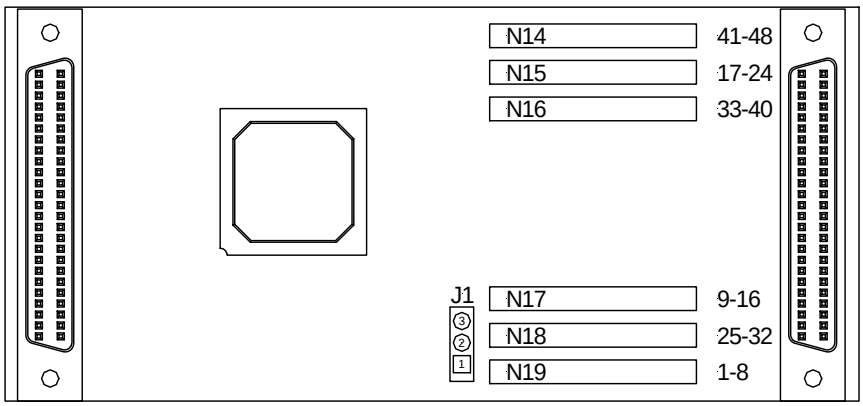



Figure 5-1 : Location of Pull Up Resistors

### 5.1.1 Pining of Pull Up Resistors

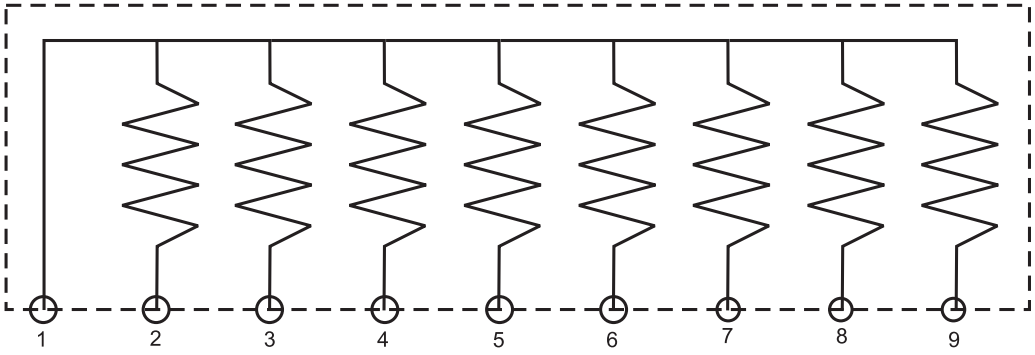



Figure 5-2 : Pining of Pull Up Resistors

## 5.2 Pull Up Voltage

To fit the maximum I/O output voltage to 5V or alternative 3.3V for designs with only 3.3V tolerant devices use the jumper J1. The default is 5V I/O voltage.

Jumper J1 1 – 2 : I/O Voltage 3.3V

Jumper J1 2 – 3 : I/O Voltage 5V (default)

# 5.3 TTL I/O Interface

The 48 TTL I/O lines are realized with an Input / Output register built in the XILINX FPGA and a few external passive devices. A serial resistor reduces spikes during switching process. The 4.7k ohms pull up for the tri-state output function and an electronic protection array for ESD and overvoltage protection.

See the following figure for more information of electrical circuitry.

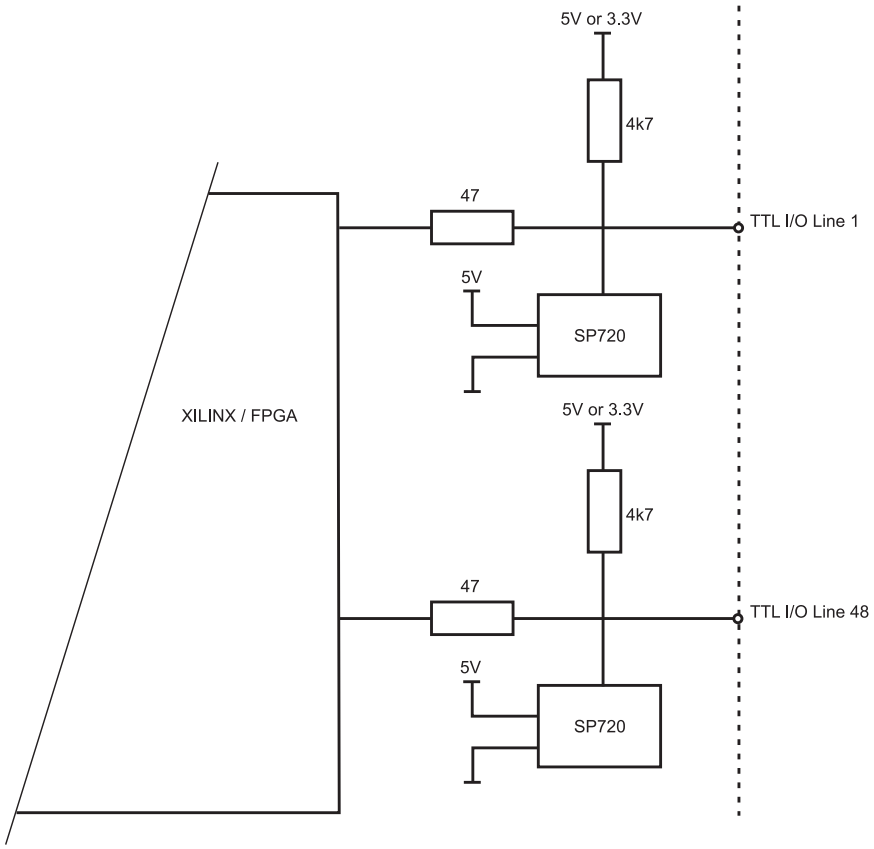



Figure 5-3 : TTL I/O Interface

**Please note that the length and with it the large capacitance of flat cable connected to the TIP675 module should be kept very short to prevent large cross talk.**

**To reduce the cross talk already on the TIP675 all 48 I/O lines are switched not at the same time. The output lines are switched in 8 groups of 6 signals in steps of 15ns. So after about 120ns the switching process is completed.**

# 6 Pin Assignment – I/O Connector

| I/O Pin Number | Function | Signal Name |
|---|---|---|
| 1 | TTL I/O Line 1 | I/O 1 |
| 2 | TTL I/O Line 2 | I/O 2 |
| 3 | TTL I/O Line 3 | I/O 3 |
| 4 | TTL I/O Line 4 | I/O 4 |
| 5 | TTL I/O Line 5 | I/O 5 |
| 6 | TTL I/O Line 6 | I/O 6 |
| 7 | TTL I/O Line 7 | I/O 7 |
| 8 | TTL I/O Line 8 | I/O 8 |
| 9 | TTL I/O Line 9 | I/O 9 |
| 10 | TTL I/O Line 10 | I/O 10 |
| 11 | TTL I/O Line 11 | I/O 11 |
| 12 | TTL I/O Line 12 | I/O 12 |
| 13 | TTL I/O Line 13 | I/O 13 |
| 14 | TTL I/O Line 14 | I/O 14 |
| 15 | TTL I/O Line 15 | I/O 15 |
| 16 | TTL I/O Line 16 | I/O 16 |
| 17 | TTL I/O Line 17 | I/O 17 |
| 18 | TTL I/O Line 18 | I/O 18 |
| 19 | TTL I/O Line 19 | I/O 19 |
| 20 | TTL I/O Line 20 | I/O 20 |
| 21 | TTL I/O Line 21 | I/O 21 |
| 22 | TTL I/O Line 22 | I/O 22 |
| 23 | TTL I/O Line 23 | I/O 23 |
| 24 | TTL I/O Line 24 | I/O 24 |
| 25 | TTL I/O Line 25 | I/O 25 |
| 26 | TTL I/O Line 26 | I/O 26 |
| 27 | TTL I/O Line 27 | I/O 27 |
| 28 | TTL I/O Line 28 | I/O 28 |
| 29 | TTL I/O Line 29 | I/O 29 |
| 30 | TTL I/O Line 30 | I/O 30 |
| 31 | TTL I/O Line 31 | I/O 31 |
| 32 | TTL I/O Line 32 | I/O 32 |
| 33 | TTL I/O Line 33 | I/O 33 |
| 34 | TTL I/O Line 34 | I/O 34 |
| 35 | TTL I/O Line 35 | I/O 35 |
| 36 | TTL I/O Line 36 | I/O 36 |
| 37 | TTL I/O Line 37 | I/O 37 |

| I/O Pin Number | Function | Signal Name |
|---|---|---|
| 38 | TTL I/O Line 38 | I/O 38 |
| 39 | TTL I/O Line 39 | I/O 39 |
| 40 | TTL I/O Line 40 | I/O 40 |
| 41 | TTL I/O Line 41 | I/O 41 |
| 42 | TTL I/O Line 42 | I/O 42 |
| 43 | TTL I/O Line 43 | I/O 43 |
| 44 | TTL I/O Line 44 | I/O 44 |
| 45 | TTL I/O Line 45 | I/O 45 |
| 46 | TTL I/O Line 46 | I/O 46 |
| 47 | TTL I/O Line 47 | I/O 47 |
| 48 | TTL I/O Line 48 | I/O 48 |
| 49 | External Clock | EX_CLK |
| 50 | Signal Ground | GND |

Table 6-1 : Pin Assignment I/O Connector

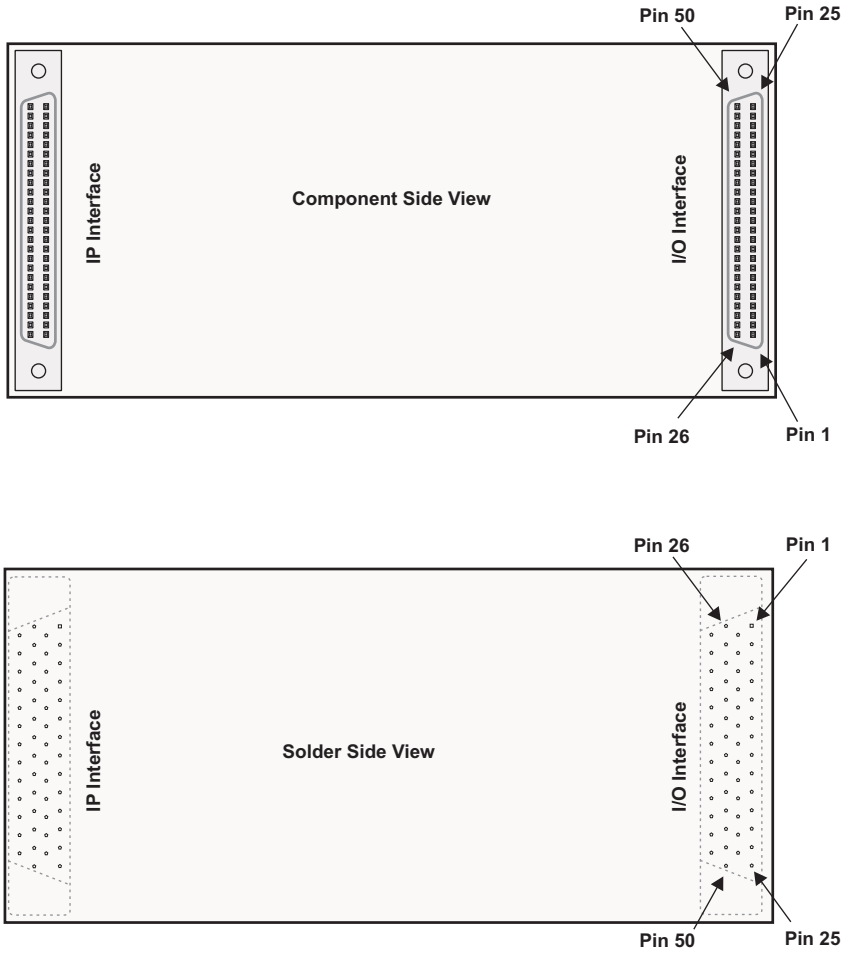



Figure 6-1 : IP Connector Orientation

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