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TEWS TECHNOLOGIES

TIP830

8 Channel Simultaneous Sampling ADC

Version 1.0

User Manual

Issue 1.0.7

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TIP830-10

8 channel 12 bit simultaneous sampling ADC

TIP830-20

8 channel 16 bit simultaneous sampling ADC

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Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

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Issue	Description	Date
1.0	First Issue	May 1994
1.1	General Revision	April 2003
1.2	Extended description of chapter “Pin Assignment”	August 2003
1.3	Additional note for ADC conversion	October 2004
1.4	New address TEWS LLC	September 2006
1.5	PCB Redesign for RoHS compliance and part availability	July 2008
1.6	Added weight to Technical Specification table	October 2008
1.0.7	New Notation for User Manual and Engineering Documentation	January 2011

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1 Product Description

The TIP830 family is IndustryPack® compatible modules with 8 independent channels of high resolution 12 bit or 16 bit analog-to-digital conversion. Each channel consists of a sample and hold 12 bit (TIP830-10) or 16 bit (TIP830-20) A/D converter. The maximum time for sample and convert is 25µs for all channels. The full-scale input range is +/-10V.

A start-of-conversion is initiated by software command or via the trigger I/O pin. All eight channels of the TIP830 sample and convert simultaneously.

By connecting the trigger I/O pins of several modules it is possible to expand the simultaneous sample and convert feature to several TIP830 modules.

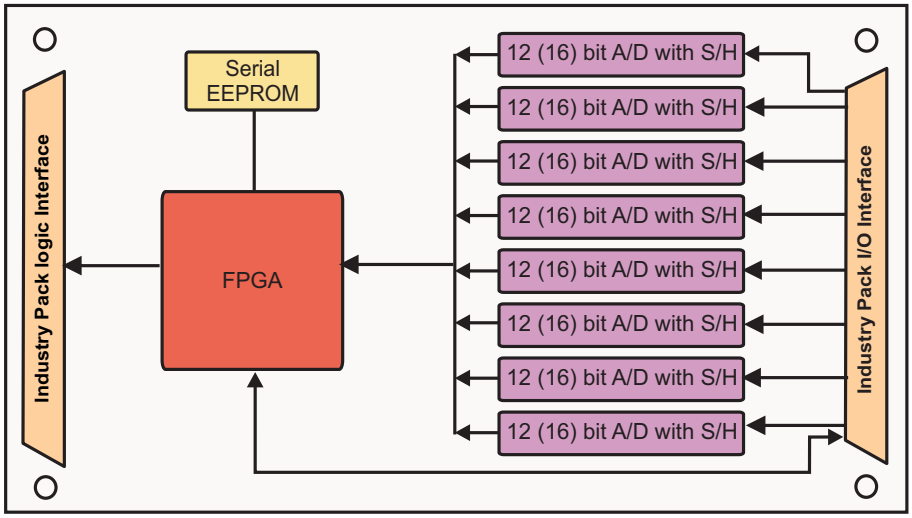


Figure 1-1 : Block Diagram

2 Technical Specification

Logic Interface	Single Size IndustryPack® Logic Interface (8 MHz). **The TIP830 requires 274us after reset, before ID data is ready to be read.**	
Wait States	ADC data read: 1 wait state All other accesses: no wait states	
I/O Interface	50-conductor flat cable	
Analog Input	8 channels, each with independent sample and hold ADC	
Input Voltage Range	+/-10V	
Input Impedance	45 kohms	
Overvoltage	+/-25V with power on, +/-10V with power off	
ADC Resolution	TIP830-10: 12 bit (ADS8506) TIP830-20: 16 bit (ADS8507)	
Integral Linearity Error	TIP830-10: +/-0.9LSB maximum TIP830-20: +/-3LSB maximum	
Bipolar Zero Error	+/-10mV maximum before data correction	
Temperature Drift	+/-0.5ppm/°C	
Conversion Time	25µs maximum for sample and convert, all channels converting simultaneously	
Throughput Rate	40 k samples per second	
Data Correction	Factory calibration data for gain and offset correction stored in serial EEPROM	
External Trigger	TTL level open drain external trigger I/O pin (max 24mA). On-board 4K7 pull-up resistor to +5V.	
Power Requirements	10mA typical @ +5V DC 45mA typical @ +12V DC	
Temperature Range	Operating Storage	-40°C to +85°C -65°C to +150°C
MTBF	TIP830-xx: 581000 h	
Humidity	5 – 95 % non-condensing	
Weight	TIP830-xx: 32g	

Table 2-1 : Technical Specification

3 ID PROM Contents

Address	Function	Contents
0x01	ASCII 'I'	0x49
0x03	ASCII 'P'	0x50
0x05	ASCII 'A'	0x41
0x07	ASCII 'C'	0x43
0x09	Manufacturer ID	0xB3
0x0B	Model Number	0x08 (TIP830-10) 0x07 (TIP830-20)
0x0D	Revision	0x10
0x0F	Reserved	0x00
0x11	Driver-ID Low - Byte	0x00
0x13	Driver-ID High - Byte	0x00
0x15	Number of bytes used	0x1C
0x17	CRC	Board dependent
0x19	Offset ADC channel 1	Board dependent
0x1B	Offset ADC channel 2	Board dependent
0x1D	Offset ADC channel 3	Board dependent
0x1F	Offset ADC channel 4	Board dependent
0x21	Offset ADC channel 5	Board dependent
0x23	Offset ADC channel 6	Board dependent
0x25	Offset ADC channel 7	Board dependent
0x27	Offset ADC channel 8	Board dependent
0x29	Gain ADC channel 1	Board dependent
0x2B	Gain ADC channel 2	Board dependent
0x2D	Gain ADC channel 3	Board dependent
0x2F	Gain ADC channel 4	Board dependent
0x31	Gain ADC channel 5	Board dependent
0x33	Gain ADC channel 6	Board dependent
0x35	Gain ADC channel 7	Board dependent
0x37	Gain ADC channel 8	Board dependent

Table 3-1 : ID PROM Contents

The TIP830 requires 274us after reset before ID data is ready to be read (ID data is loaded from serial EEPROM after reset).

4 IP Addressing

4.1 I/O Addressing

The complete register set of the TIP830 is accessible in the I/O space of the IP.

Address	Symbol	Description	Size (Bit)	Access
0x01	DATAH1	Channel 1 ADC Data Bits 15:8	8	R
0x03	DATAL1	Channel 1 ADC Data Bits 7:0	8	R
0x05	DATAH2	Channel 2 ADC Data Bits 15:8	8	R
0x07	DATAL2	Channel 2 ADC Data Bits 7:0	8	R
0x09	DATAH3	Channel 3 ADC Data Bits 15:8	8	R
0x0B	DATAL3	Channel 3 ADC Data Bits 7:0	8	R
0x0D	DATAH4	Channel 4 ADC Data Bits 15:8	8	R
0x0F	DATAL4	Channel 4 ADC Data Bits 7:0	8	R
0x11	DATAH5	Channel 5 ADC Data Bits 15:8	8	R
0x13	DATAL5	Channel 5 ADC Data Bits 7:0	8	R
0x15	DATAH6	Channel 6 ADC Data Bits 15:8	8	R
0x17	DATAL6	Channel 6 ADC Data Bits 7:0	8	R
0x19	DATAH7	Channel 7 ADC Data Bits 15:8	8	R
0x1B	DATAL7	Channel 7 ADC Data Bits 7:0	8	R
0x1D	DATAH8	Channel 8 ADC Data Bits 15:8	8	R
0x1F	DATAL8	Channel 8 ADC Data Bits 7:0	8	R
0x21	CONCR	Convert Command Register	8	W
0x23	STATR	Status Register	8	R

Table 4-1 : Register Set

4.2 ADC Data Register

Each of the ADCs on the TIP830 has two byte wide data registers. The DATAHx register holds the upper byte (MSB) and DATALx holds the lower byte (LSB) of the converted data. These registers are read only.

For the 12 bit version TIP830-10 the data is returned left shifted by hardware as 16 bit binary two's complement value with data bits 3 to 0 set to '0'.

DATAHx								DATALx							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
12 bit ADC value (2's complement)												0	0	0	0

Table 4-2 : 16 bit ADC Data Alignment for TIP830-10

DATAHx								DATALx							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
16 bit ADC value (2's complement)															

Table 4-3 : 16 bit ADC Data Alignment for TIP830-20

Only byte access is supported for the DATAHx and DATALx registers.

4.3 Control and Status Register

The TIP830 is controlled by the Conversion Command Register CONCR and the Status Register STATR.

4.3.1 Conversion Command Register CONCR

The Conversion Command Register CONCR is used to start a data conversion for all 8 channels simultaneously. Any write to this register will start the conversion.

A write to the Conversion Command Register CONCR also asserts the low active TRIGGER_I/O# signal for 1.5 IP clock cycles.

The CONCR is a write only register. Any read access to this register will return undefined data.

After power up the ADC is in a random state and requires two dummy conversions before operating correctly. This is based on the chip design of the ADC. All drivers from TEWS TECHNOLOGIES already include these two dummy conversions.

4.3.2 Status Register STATR

Bit	Symbol	Description	Access
7:1		Reserved. Undefined for read access.	R
0	Busy	ORed ADC Busy Status of all 8 ADCs 0 : None of the ADCs is busy 1 : At least one of the ADCs is busy converting.	R

Table 4-4 : Status Register STATR

The STATR is a read only register. A write access to this register has no effect.

5 Functional Description

The TIP830 has 8 single-ended ADC channels with 12 bit or 16 bit resolution. All 8 channels are sampled and converted simultaneously. The minimum throughput is 40 k samples per second.

The input voltage range is +/-10V. The 12 bit TIP830-10 has a resolution of 4.88mV (1LSB) and the 16 bit TIP830-20 has a resolution of 305µV (1LSB).

5.1 Trigger I/O

A write access to the Convert Command Register CONCR asserts the low active trigger I/O signal for 1.5 IP clock cycles (approx. 187.5 ns), which in turn starts the simultaneous A/D conversion.

An active low pulse on the trigger I/O signal from an external open drain driver locks a request for an A/D conversion. The A/D conversion is started immediately if there is no active IP cycle at that time. If there is an active IP cycle in progress, the A/D conversion is delayed until the IP cycle is done.

An active low pulse on the trigger I/O signal must be asserted for at least 1.5 IP clock cycles (approx. 187.5 ns).

By connecting the trigger I/O pins, it is possible to expand the simultaneous sample and convert feature to several TIP830 modules. The trigger I/O signal has an on-board pull-up resistor (5V).

5.2 Data Acquisition

The data conversion can be started by writing to the Conversion Command Register CONCR or by a high to low transition from an external source at the trigger I/O pin.

More then one TIP830 can have their trigger I/O pins tied together. In this way the number of simultaneous sampling channels can be increased. The trigger I/O signal is a bidirectional signal. A software conversion command by writing the CONCR at one TIP830 will also trigger all other TIP830 which have their trigger I/O signals connected.

5.3 Data Correction

The calibration data stored in the ID ROM space can be used to correct the offset and gain error of the ADCs by software.

All errors are considered to be linear. For each of the 8 ADCs there are two correction values, one correction value for the offset (or zero) error, and one correction value for the gain (or span) error.

Because the 12 bit data of the TIP830-10 is left aligned to a 16 bit word by hardware, the same scaling and correction algorithms can be used for the TIP830-10 and TIP830-20. The ID ROM space holds all correction values in units of 1LSB (16 bit based). The correction values are treated as a signed byte (-128 to +127).

The basic formula for correction is:

$$Data_{corrected} = Data_{ADC} * (1 - CORR_{gain} / 32768) - CORR_{offset}$$

Floating point arithmetic or 32 bit integer arithmetic with normalized data values is necessary for the data correction.

6 Pin Assignment – I/O Connector

Pin	Signal
Analog Input Connection	
1	ADC Input Channel 1
2	ADC Input Channel 5
3	GND (Channel 1 and 5)
4	ADC Input Channel 2
5	ADC Input Channel 6
6	GND (Channel 2 and 6)
7	ADC Input Channel 3
8	ADC Input Channel 7
9	GND (Channel 3 and 7)
10	ADC Input Channel 4
11	ADC Input Channel 8
12	GND (Channel 4 and 8)
Digital I/O Connection	
23	GND
24	TRIGGER_I/O# (Open Drain TTL) On-board pull-up resistor (5V)
25	GND
Power Output Connection	
45	-12V
46	GND
47	+12V
48	GND
49	+5V
50	GND

Table 6-1 : IP I/O Connector

The power output connections of the IP I/O connector are the unfused IP supply voltages!

Be careful in using these voltages to supply external circuiting! Faulty operation can damage the TIP830.

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