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The Embedded I/O Company

TEWS TECHNOLOGIES

TIP867

8 Channel RS485 Interface

Version 1.0

User Manual

Issue 1.0.5

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TIP867-10R

8 channel RS485 Interface

TIP867-20R

8 channel RS485 Interface plus 8 serial RS485 clock I/O lines

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Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

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Issue	Description	Date
1.0	First Issue	March 1998
1.1	General Revision	August 2003
1.2	New address TEWS LLC	September 2006
1.3	Correction ID-PROM Contents of TIP867-20	September 2008
1.0.4	New notation of User Manual Issue	March 2009
1.0.5	General Revision	August 2014

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1 Product Description

The TIP867 is an IndustryPack® compatible module providing eight channels of high performance serial RS485 interface.

The TIP867-10R provides eight (asynchronous) RS485 channels. The TIP867-20R additionally provides eight RS485 serial clock I/O lines for synchronous high data rates. Features include programmable baud rates up to 2 Mbit/sec, asynchronous or synchronous protocols including NRZ, NRZI, FM, T1, SDLC/HDLC.

Each of the eight serial channels has a 4 byte transmit FIFO and an 8 byte receive FIFO. Programmable FIFO interrupt levels provide flexible interrupt response.

Serial I/O channels 1 to 4 generate interrupts on interrupt request line Intreq0#. Serial I/O channels 5 to 8 generate interrupts on interrupt request line Intreq1#.

The TIP867 uses ESD protected RS485 transceivers (up to +/-15KV according to IEC 1000-4-2).

All transition modules of the TIP866 series are well suited for the TIP867.
The TIP866-TM-10 transition module provides 8 DB9 connectors mounted in a 6U 8TE front panel.
The TIP866-TM-20 transition module offers 8 RJ45 connectors mounted in a 6U 4TE front panel.
The TIP866-TM-30 transition module provides 16 4-pin RJ connectors mounted in a 6U 4TE front panel.

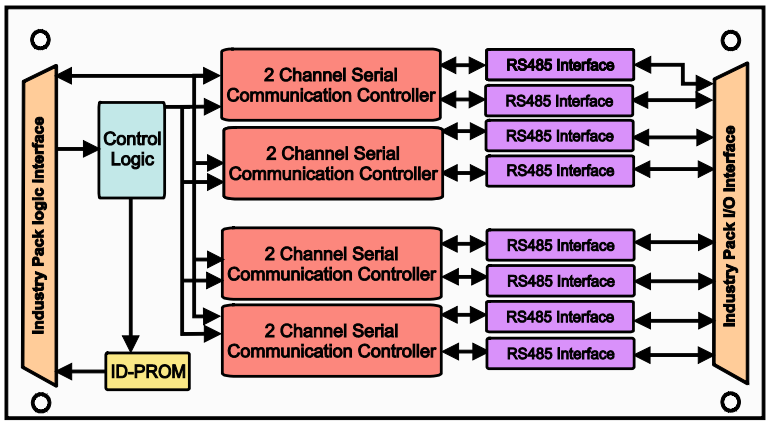


Figure 1-1 : Block Diagram

2 Technical Specification

IP Interface		
Interface	Single Size IndustryPack® Logic Interface compliant to ANSI/VITA 4-1995	
ID ROM Data	Format I	
I/O Space	Used (SCC Register Access)	
Memory Space	Not used	
Interrupts	Intreq0# used (SCC1 B/A, SCC2 B/A) (CH 1 – 4) Intreq1# used (SCC3 B/A, SCC4 B/A) (CH 5 – 8)	
Wait States	ID PROM access: no wait states SCC access: 1 wait state Interrupt vector read: 3 wait states	
DMA	Not supported	
Clock Rate	8 MHz	
Module Type	Type I	
Functional Data		
Serial Controller	Z85230 (dual SCC)	
Number of Channels	8	
Clock Frequency	PCLK 8 MHz, RTxC 7.3728 MHz TRxC external I/O CLK maximum 2 MHz (TIP867-20R only)	
FIFO	8 byte receive FIFO, 4 byte transmit FIFO per channel	
Physical Interface	Half Duplex RS485 Interface	
Transfer Rate	TIP867-10R: up to 500 kbaud TIP867-20R: up to 2 Mbaud using external CLK	
I/O Interface		
ESD Protection	+/-15V Human Body Model	
I/O Signals per Channel	Dx+/-, CLK+/- (TIP867-20R only)	
Interface Connector	50-conductor flat cable	
Physical Data		
Power Requirements	100mA typical @ +5V DC	
Temperature Range	Operating Storage	0 °C to +70 °C -45°C to +125°C
MTBF	702715 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	37 g	

Table 2-1 : Technical Specification

3 ID Prom Contents

Offset	Function	Content
0x01	ASCII 'I'	0x49
0x03	ASCII 'P'	0x50
0x05	ASCII 'A'	0x41
0x07	ASCII 'C'	0x43
0x09	Manufacturer ID	0xB3
0x0B	Model Number	0x24
0x0D	Revision	0x10
0x0F	Reserved	0x00
0x11	Driver-ID Low - Byte	0x00
0x13	Driver-ID High - Byte	0x00
0x15	Number of bytes used	0x0D
0x17	CRC	0xD2 (TIP867-10R) 0x2D (TIP867-20R)
0x19	Version	0x0A (TIP867-10R) 0x14 (TIP867-20R)

Table 3-1 : ID PROM Contents

4 IP Addressing

4.1 I/O Addressing

The Z85230 Serial Communication Controller (SCC) registers are accessed by a set of registers in the TIP867 IP I/O space.

Each Z85230 SCC channel register is accessed by two addresses in the IP's I/O address space. The Z85230 SCC uses an internal set of registers for each channel, which are accessed indirectly.

Offset	Symbol	Description	Size (Bit)
0x01	CHCON0	Port 0 Control Register (SCC1 B Control)	8
0x03	CHDAT0	Port 0 Data Register (SCC1 B Data)	8
0x05	CHCON1	Port 1 Control Register (SCC1 A Control)	8
0x07	CHDAT1	Port 1 Data Register (SCC1 A Data)	8
0x09	CHCON2	Port 2 Control Register (SCC2 B Control)	8
0x0B	CHDAT2	Port 2 Data Register (SCC2 B Data)	8
0x0D	CHCON3	Port 3 Control Register (SCC2 A Control)	8
0x0F	CHDAT3	Port 3 Data Register (SCC2 A Data)	8
0x11	CHCON4	Port 4 Control Register (SCC3 B Control)	8
0x13	CHDAT4	Port 4 Data Register (SCC3 B Data)	8
0x15	CHCON5	Port 5 Control Register (SCC3 A Control)	8
0x17	CHDAT5	Port 5 Data Register (SCC3 A Data)	8
0x19	CHCON6	Port 6 Control Register (SCC4 B Control)	8
0x1B	CHDAT6	Port 6 Data Register (SCC4 B Data)	8
0x1D	CHCON7	Port 7 Control Register (SCC4 A Control)	8
0x1F	CHDAT7	Port 7 Data Register (SCC4 A Data)	8

Table 4-1 : Register Set

The write only Port x Control Register is the WR0 register of the addressed SCC.

5 Programming Hints

5.1 RS485 Transmitter Control

For data signal transceiver direction control, the SCCs RTS# pin is used.

For RS485 applications the auto enable bit (WR3 D5 = ‘1’) must be set.

The RTS# pin enables the RS485 data transmitter immediately and remains active until the transmit buffer is empty.

In manual mode the user must set the RTS bit (WR5 D1= ‘1’) before writing a character to the transmit buffer and clear the RTS bit (WR5 D1 = ‘0’) after writing to the transmit buffer.

5.2 Baud Rates

Baud rates may be derived from a local 7.3728 MHz oscillator frequency, permitting the generation of all standard baud rates (including 19200, 38400 and 57600 baud). Some networks and communication protocols may require a different oscillator frequency. For these applications the oscillator may be replaced or an external clock signal may be used (TIP867-20R only).

5.2.1 Using Internal Baud Rates

A 7.3728 MHz oscillator is connected to the RTxC# pin of all Z85230 SCC channels. This is the standard configuration for supplying the programmable baud rate generator with an input clock. To enable the baud rate generator with the 7.3728 MHz clock, the software must set the bits D[1:0] of the SCC internal WR14 register to ‘01’.

To use the output of the baud rate generator as transmit clock and receive clock, bits D[4:3] and D[6:5] of the SCC internal WR11 register must be set to ‘10’.

5.2.2 Using an External Clock Signal (TIP867-20R only)

The TIP867 can be programmed to receive an external clock signal or transmit an external clock signal. For both modes the SCCs TRxC# pin is used as clock I/O pin (programmable as clock input or clock output).

For proper use of the external clock, both the clock signal transceiver direction and the SCC TRxC# pin I/O direction must be configured properly. The RS485 clock transceiver direction is controlled by the SCCs DTR pin, used as general purpose output.

For using the SCCs DTR pin as a general purpose output, bit D2 in the SCC internal WR14 register must be set to '0'.

After hardware reset both the clock signal transceiver and the TRxC# pin are configured as input for all channels.

5.2.2.1 Receiving an external clock signal

To use the SCCs TRxC# pin as an input for an external clock, first the TRxC# pin direction must be set to input, and then the clock signal receiver must be enabled.

To enable the clock receiver, bit D7 of the Z85230 internal WR5 register must be set to '0'.

To program the SCCs TRxC# pin as clock input, bit D2 of the SCC internal WR11 register must be set to '0'. The external clock is used as transmit clock if the bits D[4:3] of the SCC internal WR11 register are set to '01' and it is used as receive clock if the bits D[6:5] are set to '01'.

5.2.2.2 Transmitting an external clock signal

To use the SCCs TRxC# pin as an output for an external clock, first the clock signal transmitter must be enabled, and then the TRxC# pin I/O direction must be set to output.

To enable the clock transmitter, bit D7 of the SCC internal WR5 register must be set to '1'.

To program the SCCs TRxC# pin as clock output, bit D2 of the SCC internal WR11 register must be set to '1'. The source of the external clock is selected by the state of the bits D[1:0] of the SCC internal WR11 register.

D[1:0]	Clock Source
'00'	7.3728 MHz Oscillator
'01'	Transmit Clock
'10'	Baud Rate Generator Output
'11'	DPPL Output

Table 5-1 : External Clock Sources

6 Pin Assignment – I/O Connector

Pin	Signal	Comment
1	GND	Signal Ground
2	DX-_0	Channel 0 Inverting Data I/O
3	DX+_0	Channel 0 Non-inverting Data I/O
4	CLK-_0	Channel 0 Inverting CLK I/O (TIP867-20R only)
5	CLK+_0	Channel 0 Non-inverting CLK I/O (TIP867-20R only)
6	GND	Signal Ground
7	DX-_1	Channel 1 Inverting Data I/O
8	DX+_1	Channel 1 Non-inverting Data I/O
9	CLK-_1	Channel 1 Inverting CLK I/O (TIP867-20R only)
10	CLK+_1	Channel 1 Non-inverting CLK I/O (TIP867-20R only)
11	GND	Signal Ground
12	DX-_2	Channel 2 Inverting Data I/O
13	DX+_2	Channel 2 Non-inverting Data I/O
14	CLK-_2	Channel 2 Inverting CLK I/O (TIP867-20R only)
15	CLK+_2	Channel 2 Non-inverting CLK I/O (TIP867-20R only)
16	GND	Signal Ground
17	DX-_3	Channel 3 Inverting Data I/O
18	DX+_3	Channel 3 Non-inverting Data I/O
19	CLK-_3	Channel 3 Inverting CLK I/O (TIP867-20R only)
20	CLK+_3	Channel 3 Non-inverting CLK I/O (TIP867-20R only)
21	GND	Signal Ground
22	DX-_4	Channel 4 Inverting Data I/O
23	DX+_4	Channel 4 Non-inverting Data I/O
24	CLK-_4	Channel 4 Inverting CLK I/O (TIP867-20R only)
25	CLK+_4	Channel 4 Non-inverting CLK I/O (TIP867-20R only)

Pin	Signal	Level
26	GND	Signal Ground
27	DX-_5	Channel 5 Inverting Data I/O
28	DX+_5	Channel 5 Non-inverting Data I/O
29	CLK-_5	Channel 5 Inverting CLK I/O (TIP867-20R only)
30	CLK+_5	Channel 5 Non-inverting CLK I/O (TIP867-20R only)
31	GND	Signal Ground
32	DX-_6	Channel 6 Inverting Data I/O
33	DX+_6	Channel 6 Non-inverting Data I/O
34	CLK-_6	Channel 6 Inverting CLK I/O (TIP867-20R only)
35	CLK+_6	Channel 6 Non-inverting CLK I/O (TIP867-20R only)
36	GND	Signal Ground
37	DX-_7	Channel 7 Inverting Data I/O
38	DX+_7	Channel 7 Non-inverting Data I/O
39	CLK-_7	Channel 7 Inverting CLK I/O (TIP867-20R only)
40	CLK+_7	Channel 7 Non-inverting CLK I/O (TIP867-20R only)
41	GND	Signal Ground for External Termination
42	+5V	Power Supply for External Termination
43	NC	Not connected
44	NC	Not connected
45	NC	Not connected
46	NC	Not connected
47	NC	Not connected
48	NC	Not connected
49	NC	Not connected
50	NC	Not connected

Table 6-1 : Pin Assignment I/O Connector

I/O signal level is RS485.
RS485 line termination must be provided externally (e.g. using a transition module).

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