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TEWS TECHNOLOGIES

TPMC670

16/8 Digital Inputs (24V)

16/8 Digital Outputs (24V, 0.5A)

Version 3.0

User Manual

Issue 3.0.0

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TPMC670-10R

16 digital inputs, 16 digital outputs

front panel I/O

TPMC670-11R

8 digital inputs, 8 digital outputs

front panel I/O

TPMC670-20R

16 digital inputs, 16 digital outputs

P14 I/O

TPMC670-21R

8 digital inputs, 8 digital outputs

P14 I/O

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Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‘Active Low’ is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

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1.0	First Issue	January 1999
1.1	Addition Target Chip description	June 1999
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1 Product Description

The TPMC670 is a standard single-width 32 bit PMC with 16/8 24V digital inputs galvanically isolated from the computer system by optocouplers. The inputs are also potential free to each other in groups of four inputs. A high performance input circuit ensures a defined switching point and polarization protection against confusing the pole.

All inputs have a common electronic debounce circuit with a freely programmable debounce time.

All inputs can generate an interrupt. The signal edge handling is programmable to interrupt on rising, falling or both edges of the input signal.

The TPMC670 has 16/8 digital high side switches with galvanic isolation from the computer system by optocouplers. The outputs are also isolated against each other in groups of four outputs. All outputs are protected against short-circuit and thermal overload. The output drivers are capable of driving 0.5A continuous per channel.

A hardware watchdog clears all outputs in case of trigger fail. The TPMC670-1x provides front panel I/O, the TPMC670-2x provides P14 I/O.

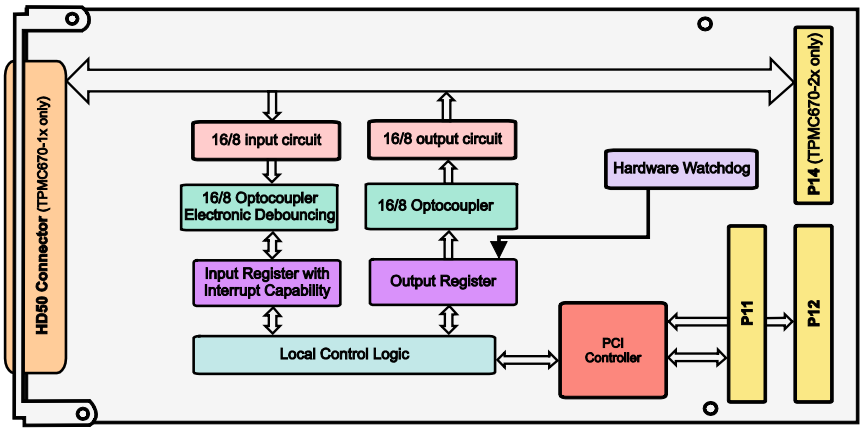


Figure 1-1 : Block Diagram

2 Technical Specification

Mechanical Interface	PCI Mezzanine Card (PMC) Interface, Single Size	
Electrical Interface	PCI Rev. 3.0 compliant 33 MHz / 32 bit PCI 3.3 V and 5 V PCI Signaling Voltage	
On Board Devices		
PCI Target Chip and Local Control Logic	MachXO2 (Lattice)	
I/O Interface		
Number of Inputs	TPMC670-10R/-20R 16 digital Inputs TPMC670-11R/-2R 8 digital Inputs	
Input Isolation	Optocouplers for galvanic isolation, also isolated to each other in groups of four inputs	
Input Voltage	24 V DC typical	
Input Current	4.2 mA typical at 24 V input voltage	
Input Switching Level	12 V typical, 7.5 V minimum, 14 V maximum	
Input Signal Debouncing	Electronic debouncing (7 µs to 440 ms in steps of 7 µs) common for all input channels, can be disabled	
Input Interrupts	16 / 8 input interrupts (Trigger on rising, falling or both edges)	
Number of Outputs	TPMC670-10R/-20R 16 digital Outputs TPMC670-11R/-21R 8 digital Outputs	
Output Isolation	Optocouplers for galvanic isolation, also isolated to each other in groups of four outputs	
External Output Voltage	24 V DC typical, 6 V DC minimum, 48 V DC maximum	
Output Current	0.5 A typical (0.3 A for voltages over 32 V)	
Short Circuit Current	0.8 A typical	
Output Voltage Drop	1.1 V typical at 0.5 A	
Output Protection	Overload, short circuit, GND and Vs open wire protection, thermal shutdown	
I/O Connector	TPMC670-10R/-20R TPMC670-11R/-21R	HD50 connector – SCSI-2 type connector PMC P14 I/O (64 pin Mezzanine connector)
Physical Data		
Power Requirements	25 mA typical @ +5 V DC with all inputs and outputs inactive 90 mA typical @ +5 V DC with all inputs and outputs active	
Temperature Range	Operating Storage	-25 °C to +85 °C -55 °C to +125 °C
MTBF	TPMC670-10R/-20R: 850.000 h TPMC670-11R/-21R: 979.000 h	
Humidity	5 – 95 % non-condensing	
Weight	70 g	

Table 2-1 : Technical Specification

3 Functional Description

3.1 Digital Outputs

3.1.1 Optical Isolation

The TPMC670 has 16 (TPMC670-10/20) or 8 (TPMC670-11/21) digital outputs. The standard signal level for these outputs is 24 V DC. All outputs are isolated by optocouplers from the computer system and are also isolated against each other in groups of four outputs.

GROUP	VS / standard 24V DC	GROUND	OUTPUT
O1	VS_O1	GND_O1	OUT 1 OUT 2 OUT 3 OUT 4
O2	VS_O	GND_O2	OUT 5 OUT 6 OUT 7 OUT 8
O3	VS_O3	GND_O3	OUT 9 OUT 10 OUT 11 OUT 12
O4	VS_O4	GND_O4	OUT 13 OUT 14 OUT 15 OUT 16

Table 3-1 : Isolated Digital Outputs

3.1.2 Output Polarity

Each output can be individually switched to the according power supply VS_Ox (high side switch).

3.1.3 Overload Protection

The output drivers used on the TPMC670 are smart drivers TDE1707. The maximum continuous output current is 0.5 A. The output circuits are protected against overload, short circuit and over temperature. In case of such a failure the corresponding output is switched off until the error condition is removed. Then the output returns automatically to normal operation and the state programmed in the Data Output Register.

For details about the protection of the TDE1707 please refer to the data sheet, available at http://www.st.com.

3.1.4 Output Watchdog

Writing ‘1’ into bit 1 of the Global Control Register and the following first write access to the Data Output Register enables the hardware watchdog function. The status of the watchdog is indicated at the bit 3 of Global Control Register.

Any software access (read or write) to the Data Output Register of the TPMC670 will retrigger the watchdog. The maximum time between two accesses is set to 120 ms, if the time expires without a software access all outputs go into the ‘OFF’ state. At the same time the watchdog status will change from ‘0’ to ‘1’ and lock the Data Output Register. This prevents a write access to the Data Output Register.

Writing ‘1’ to the watchdog status (Bit 3 Control Register) clears this bit and also unlocks the Output Register. After unlocking the Data Output Register the outputs stay in the ‘OFF’ state till the next write access to this register.

The watchdog is disabled after power-on or reset.

3.2 Digital Inputs

3.2.1 Optical Isolation

The TPMC670 has 16 (TPMC670-10R/20R) or 8 (TPMC670-11R/21R) digital inputs. The standard signal level for these inputs is 24 V DC. The switching level of the inputs is between 7.5 V and 14 V. All inputs are isolated by optocouplers from the computer system and are also isolated against each other in groups of four inputs.

GROUP	GROUND	INPUT
I1	GND_I1	IN 1 IN 2 IN 3 IN 4
I2	GND_I2	IN 5 IN 6 IN 7 IN 8
I3	GND_I3	IN 9 IN 10 IN 11 IN 12
I4	GND_I4	IN 13 IN 14 IN 15 IN 16

Table 3-2 : Isolated Digital Inputs

3.2.2 Debounce Function

A programmable debounce function common for all inputs is implemented on the TPMC670. There is only one debounce time adjustable for all 16 (TPMC670-10R/20R) or 8 (TPMC670-11R/21R) digital inputs.

If the debounce function is enabled, the input pin must be static for the programmed debounce time before the rising or falling edge is recognized as valid. Thus, only after a correct identification the Data Input Register is updated and an interrupt is generated.

The debounce function is disabled after power-on and reset. The debounce time is set to value '0' after power-on and reset.

3.2.3 Interrupt Logic

Interrupt generation can be individually programmed for each channel and input transition. To enable the interrupt after a reset, the Global Interrupt Enable bit in the Control Register must be set to the value '1'. Also the respective bit for rising or falling edge in the Rising Edge / Falling Edge Interrupt Enable Registers must be set.

The Global Interrupt Enable and also all individually interrupt enable bits are disabled after power-on and reset.

4 Address Map

4.1 PCI Configuration Space

PCI CFG Register Address	Write '0' to all unused (Reserved) bits								Initial Values (Hex Values)
	31	24	23	16	15	8	7	0	
0x00	Device ID				Vendor ID				9050 10B5
0x04	Status				Command				0280 0000
0x08	Class Code						Revision ID		118000 00
0x0C	not supported		Header Type		PCI Latency Timer		Cache Line Size		00 00 00 00
0x10	Base Address Register 0 (BAR0)								FFFFFF80
0x14	Base Address Register 1 (BAR1)								FFFFFF81
0x18	Base Address Register 2 (BAR2)								FFFFFFF1
0x1C	not supported								00000000
0x20	not supported								00000000
0x24	not supported								00000000
0x28	CardBus CIS Pointer								00000000
0x2C	Subsystem ID 0x029E (TPMC670)				Subsystem Vendor ID 0x1498 (TEWS Technologies)				029E 1498
0x30	not supported								00000000
0x34	Reserved						New Cap. Ptr.		000000 40
0x38	Reserved								00000000
0x3C	Max_Lat		Min_Gnt		Interrupt Pin		Interrupt Line		00 00 01 00
0x40-0xFF	Reserved								

Table 4-1 : PCI Configuration Space Header

4.2 Base Address Register Configuration

The TPMC670 maps its internal registers into an address spaces within the PCI I/O space.

For backward compatibility a subset of PCI9030 registers have been implemented. This subset contains all registers that are used by the standard TEWS module driver. They can be accessed both in memory and I/O space.

Base Address Register (BAR)	PCI Space Mapping	Size (Byte)	Port Width (Bit)	Endian Mode	Description
0	MEM	128	32	LIT	Configuration Register Space
1	IO	128	32	LIT	
2	IO	16	16	BIG	Local Register Space

Table 4-2 : Base Address Register Configuration

4.3 Configuration Register Space Address Map

Offset to PCI Base Address 0/1	Register Name	Size (Bit)
0x00 - 0x27		
0x28	Local Address Space 0 Bus Region Descriptor (LAS0BRD)	32
0x2C - 0x48		
0x4C	Interrupt Control/Status (INTCSR)	32
0x50	Serial EEPROM and Initialization Control (CNTRL)	32
0x54	General Purpose I/O Control (GPIOC)	32
0x58 - 0x7B		
0x7C	Configuration Space Revision Register (CREVREG)	32

Table 4-3 : Configuration Register Space Address Map

4.4 Local Register Space Address Map

Offset to PCI Base Address 2	Register Name	Size (Bit)
0x00	Data Output Register	16
0x02	Data Input Register	16
0x04	Control / Status Register	16
0x06	Rising Edge Interrupt Enable Register	16
0x08	Falling Edge Interrupt Enable Register	16
0x0A	Rising Edge Interrupt Status Register	16
0x0C	Falling Edge Interrupt Status Register	16
0x0E	Debounce Time Register	16

Table 4-4 : Local Register Space Address Map

5 Register Description

5.1 Configuration Register Space

5.1.1 Local Address Space 0 Bus Region Descriptor (LAS0BRD)

Bit	Symbol	Description	Access	Reset Value
31-25	-	Reserved	R	0
24	ASBYTE_ORDER	Address Space Byte Ordering 1 : activate Big Endian 0 : activate Little Endian	R/W	1
23-0	-	Reserved	R	0

Table 5-1 : Local Address Space 0 Bus Region Descriptor

5.1.1 Interrupt Control/Status (INTCSR)

Bit	Symbol	Description	Access	Reset Value
31-8	-	Reserved	R	0
7	SW_INT	Software Interrupt 1 : generates PCI Interrupt (INTA# output asserted) if PCI Interrupt Enable bit is set (bit [6]=1) 0 : clears PCI Interrupt	R/W	0
6	PCI_INT_EN	PCI Interrupt Enable 1 : enables PCI interrupt 0 : disables PCI interrupt	R/W	1
5-3	-	Reserved	R	0
2	LINT_STAT	Local Interrupt (LINTi1) Status 1 : indicates interrupt active 0 : indicates Interrupt not active	R	0
1	LINT_POL	Local Interrupt (LINTi1) Polarity 1 : adjusts active high polarity 0 : adjusts active low polarity	R/W	0
0	LINT_EN	Local Interrupt (LINTi1) Enable 1 : enables Local Control Logic interrupts 0 : disables Local Control Logic interrupts	R/W	1

Table 5-2 : Interrupt Control/Status

5.1.2 Serial EEPROM and Initialization Control (CNTRL)

Bit	Symbol	Description	Access	Reset Value
31	-	Reserved	R	0
30	SWRST	Software Reset 1 : resets the Functional Register Space. Reset stays active until it is cleared 0 : clears the Functional Register Space reset	R/W	0
29	-	Reserved	R	0
28	EEPRSNT	Serial EEPROM Present 1 : indicates serial EEPROM is present 0 : indicates no serial EEPROM is present	R	1
27	EEDO	Serial EEPROM Data Out Bit This bit is the data output of the serial EEPROM	R	-
26	EEDI	Serial EEPROM Data In Bit This bit is the data input of the serial EEPROM	R/W	0
25	EECS	Serial EEPROM Chip Select 1 : asserts serial EEPROM chip select 0 : de-asserts serial EEPROM chip select	R/W	0
24	EESK	Serial EEPROM Clock Toggling this bit generates a serial EEPROM clock	R/W	0
23-8	-	Reserved	R	0

Table 5-3 : Serial EEPROM and Initialization Control

5.1.2 General Purpose I/O Control (GPIOC)

Bit	Symbol	Description	Access	Reset Value
31-15	-	Reserved	R	0
14-12	-	Reserved	R	001
11	GPIO3_DATA	GPIO3 Data Output Function: Stimulates corresponding pin Input Function: Provides state of corresponding pin	R/W	0
10	GPIO3_DDR	GPIO3 Data Direction 1 : activates output function 0 : activates input function	R/W	1
9	-	Reserved	R	0
8	GPIO2_DATA	GPIO2 Data Output Function: Stimulates corresponding pin Input Function: Provides state of corresponding pin	R/W	0
7	GPIO2_DDR	GPIO2 Data Direction 1 : activates output function 0 : activates input function	R/W	1
6	-	Reserved	R	0
5	GPIO1_DATA	GPIO1 Data Output Function: Stimulates corresponding pin Input Function: Provides state of corresponding pin	R/W	0
4	GPIO1_DDR	GPIO1 Data Direction 1 : activates output function 0 : activates input function	R/W	1
3	-	Reserved	R	0
2	GPIO0_DATA	GPIO0 Data Output Function: Stimulates corresponding pin Input Function: Provides state of corresponding pin	R/W	0
1	GPIO0_DDR	GPIO0 Data Direction 1 : activates output function 0 : activates input function	R/W	1
0	-	Reserved	R	0

Table 5-4 : General Purpose I/O Control

5.1.1 Configuration Space Revision Register (CREVREG)

Bit	Symbol	Description	Access	Reset Value
31-0	CREVREG	Firmware Version Register for Configuration Space	R	n/a

Table 5-5 : Configuration Space Revision Register

5.1 Local Register Space

5.1.1 Data Output Register

The Data Output Register is a word wide read/write register that is used to set or clear the different outputs of the TPMC670.

Bit	Symbol	Description	Access	Reset Value
15	OUTPUT16	To set an output line active, write '1' to the corresponding bit. For the inactive state write '0' to the corresponding bit. 0 : inactive 1 : active Bit 0 represents output line 1 and bit 15 represents output line 16. After power-on or reset the Data Output Register is cleared to '0', all outputs are inactive.	R/W	0x0000
14	OUTPUT15			
13	OUTPUT14			
12	OUTPUT13			
11	OUTPUT12			
10	OUTPUT11			
9	OUTPUT10			
8	OUTPUT9			
7	OUTPUT8			
6	OUTPUT7			
5	OUTPUT6			
4	OUTPUT5			
3	OUTPUT4			
2	OUTPUT3			
1	OUTPUT2			
0	OUTPUT1			

Table 5-6 : Data Output Register

5.1.2 Data Input Register

The Data Input Register is a word wide read only register that reflects the actual status of the inputs.

Bit	Symbol	Description	Access	Reset Value
15	INPUT16	0 : Input line is logic low 1 : Input line is logic high Bit 0 represents Input Line 1 and bit 15 represents the Input Line 16.	R	-
14	INPUT15			
13	INPUT14			
12	INPUT13			
11	INPUT12			
10	INPUT11			
9	INPUT10			
8	INPUT9			
7	INPUT8			
6	INPUT7			
5	INPUT6			
4	INPUT5			
3	INPUT4			
2	INPUT3			
1	INPUT2			
0	INPUT1			

Table 5-7 : Data Input Register

5.1.3 Control / Status Register

The Control / Status Register is a read/write register.

Bit	Symbol	Description	Access	Reset Value
15 : 4	-	Not used and undefined during reads	-	-
3	WD_STA	Watchdog Status Flag 1 = indicates that the watchdog had recognized a failure and had disabled all output channels. Also the Output Register is locked. Writing '1' to this bit unlocks the Output Register. 0 = signals normal operation	R/W	0
2	DB_ENA	Debounce Enable 1 = enables the debounce function for all 16 inputs 0 = disables debounce function	R/W	0
1	WD_ENA	Watchdog Enable 1 = enables watchdog for all 16 outputs 0 = disables watchdog function	R/W	0
0	INT_ENA	Global Interrupt Enable 1 = globally enables interrupt for all 16 inputs 0 = globally disables interrupts The input channels generate interrupts at pin INTA# of the PCI bus.	R/W	0

Table 5-8 : Control / Status Register

The watchdog status is only active if the watchdog is enabled.

5.1.4 Rising Edge Interrupt Enable Register

The Rising Edge Interrupt Enable Register is a word wide read/write register.

Bit	Symbol	Description	Access	Reset Value
15	INT_ENA_H16	0 : Interrupt for input line disabled 1 : Interrupt for input line enabled Bit 0 of the Rising Edge Interrupt Enable Register enables the interrupt of input line 1 for the rising edge. Bit 15 enables interrupt of input line 16 for rising edge. All other bits are equivalent.	R/W	0x0000
14	INT_ENA_H15			
13	INT_ENA_H14			
12	INT_ENA_H13			
11	INT_ENA_H12			
10	INT_ENA_H11			
9	INT_ENA_H10			
8	INT_ENA_H9			
7	INT_ENA_H8			
6	INT_ENA_H7			
5	INT_ENA_H6			
4	INT_ENA_H5			
3	INT_ENA_H4			
2	INT_ENA_H3			
1	INT_ENA_H2			
0	INT_ENA_H1			

Table 5-9 : Rising Edge Interrupt Enable Register

5.1.5 Falling Edge Interrupt Enable Register

The Falling Edge Interrupt Enable Register is a word wide read/write register.

Bit	Symbol	Description	Access	Reset Value
15	INT_ENA_L16	0 : Interrupt for input line disabled 1 : Interrupt for input line enabled Bit 0 of the Falling Edge Interrupt Enable Register enables the interrupt of input line 1 for the falling edge. Bit 15 enables interrupt of input line 16 for falling edge. All other bits are equivalent.	R/W	0x0000
14	INT_ENA_L15			
13	INT_ENA_L14			
12	INT_ENA_L13			
11	INT_ENA_L12			
10	INT_ENA_L11			
9	INT_ENA_L10			
8	INT_ENA_L9			
7	INT_ENA_L8			
6	INT_ENA_L7			
5	INT_ENA_L6			
4	INT_ENA_L5			
3	INT_ENA_L4			
2	INT_ENA_L3			
1	INT_ENA_L2			
0	INT_ENA_L1			

Table 5-10: Falling Edge Interrupt Enable Register

5.1.6 Rising Edge Interrupt Status Register

The Rising Edge Interrupt Status Register is a word wide read/write register.

Bit	Symbol	Description	Access	Reset Value
15	INT_STA_H16	Read access: 0 = no interrupt request pending 1 = interrupt request pending Write access: 0 = no effect 1 = clear pending interrupt request Bit 0 of this register reflects the interrupt request state of input line 1 for the rising edge, bit 15 reflects the interrupt request state of input line 16 for the rising edge. An interrupt request for a specific input line is cleared by writing '1' to the according bit of the Rising Edge Interrupt Status Register.	R/W	0x0000
14	INT_STA_H15			
13	INT_STA_H14			
12	INT_STA_H13			
11	INT_STA_H12			
10	INT_STA_H11			
9	INT_STA_H10			
8	INT_STA_H9			
7	INT_STA_H8			
6	INT_STA_H7			
5	INT_STA_H6			
4	INT_STA_H5			
3	INT_STA_H4			
2	INT_STA_H3			
1	INT_STA_H2			
0	INT_STA_H1			

Table 5-11: Rising Edge Interrupt Status Register

5.1.7 Falling Edge Interrupt Status Register

The Falling Edge Interrupt Status Register is a word wide read/write register.

Bit	Symbol	Description	Access	Reset Value
15	INT_STA_L16	Read access: 0 = no interrupt request pending 1 = interrupt request pending Write access: 0 = no effect 1 = clear pending interrupt request Bit 0 of this register reflects the interrupt request state of input line 1 for the falling edge, bit 15 reflects the interrupt request state of input line 16 for the falling edge. An interrupt request for a specific input line is cleared by writing '1' to the according bit of the Falling Edge Interrupt Status Register.	R/W	0x0000
14	INT_STA_L15			
13	INT_STA_L14			
12	INT_STA_L13			
11	INT_STA_L12			
10	INT_STA_L11			
9	INT_STA_L10			
8	INT_STA_L9			
7	INT_STA_L8			
6	INT_STA_L7			
5	INT_STA_L6			
4	INT_STA_L5			
3	INT_STA_L4			
2	INT_STA_L3			
1	INT_STA_L2			
0	INT_STA_L1			

Table 5-12: Falling Edge Interrupt Status Register

5.1.8 Debounce Time Register

The Debounce Time Register is a word wide read/write register.

Bit	Symbol	Description	Access	Reset Value
15	DB_TIME	The debounce time could be programmed by writing a hexadecimal value in the register. One hexadecimal step correspondence to a debounce time of about 7 µs. min debounce time: 7 µs max debounce time: 440 ms debounce step: ca. 7 µs The value 0 in this register sets the debounce time to a minimum of 7µs. This is the default state after power-on or reset. Any debounce time in the range of 7 µs to 440 ms can be programmed in steps of ca. 7 µs. The debounce time is common for all 16 inputs.	R/W	0x0000
14				
13				
12				
11				
10				
9				
8				
7				
6				
5				
4				
3				
2				
1				
0				

Table 5-13: Debounce Time Register

To use the programmable debounce time, the Debounce Enable Bit of the Control / Status Register must be set to '1'.

If the Debounce Enable Bit of the Control / Status Register is set to '0', no debounce function is active for all inputs.

The following formulas can be used to determine the preload value.

$$t_{db} = (Z+1) \cdot \frac{64}{PCICLK} \cdot 3.5$$

$$Z = \frac{t_{db}}{64 \cdot 3.5} \cdot PCICLK - 1$$

$$t_{max} = (Z+1) \cdot \frac{64}{PCICLK} \cdot 4$$

$$t_{min} = (Z+1) \cdot \frac{64}{PCICLK} \cdot 3$$

t_{db}	-	typical debounce time [s]
Z	-	preload value
PCICLK	-	33.33 MHz
t_{max}	-	max. debounce time [s]
t_{min}	-	min. debounce time [s]

Figure 5-1: Formulas to determine preload value

Debounce Time Examples:

typ. Debounce Time [ms]	inaccuracy [ms]	Counter decimal	Counter hex.
0.007	± 0.001	0	0x0000
0.014	± 0.002	1	0x0001
0.021	± 0.003	2	0x0002
0.027	± 0.004	3	0x0003
0.034	± 0.005	4	0x0004
0.041	± 0.006	5	0x0005
0.050	± 0.007	6	0x0006
0.060	± 0.008	7	0x0007
0.070	± 0.010	9	0x0009
0.080	± 0.011	10	0x000A
0.090	± 0.012	12	0x000C
0.100	± 0.013	13	0x000D
0.200	± 0.028	28	0x001C
0.300	± 0.042	43	0x002B
0.400	± 0.057	58	0x003A
0.500	± 0.071	73	0x0049
0.600	± 0.085	88	0x0058
0.700	± 0.100	103	0x0067
0.800	± 0.114	118	0x0076
0.900	± 0.128	132	0x0084
1.000	± 0.142	147	0x0093
2.000	± 0.285	296	0x0128
3.000	± 0.428	445	0x01BD
4.000	± 0.571	594	0x0252
5.000	± 0.714	743	0x02E7
6.000	± 0.856	891	0x037B
7.000	± 0.999	1040	0x0410
8.000	± 1.142	1189	0x04A5
9.000	± 1.285	1338	0x053A
10.000	± 1.428	1487	0x05CF
20.000	± 2.857	2975	0x0B9F
50.000	± 7.142	7439	0x1D0F
100.000	± 14.285	14879	0x3A1F
200.000	± 28.571	29760	0x7440
250.000	± 35.714	37201	0x9151
300.000	± 42.856	44641	0xAE61
350.000	± 50.000	52082	0xCB72
400.000	± 57.142	59522	0xE882
440.402	± 62.915	65535	0xFFFF

Table 5-14: Debounce Time / Examples

6 Configuration Hints

6.1 Big / Little Endian

- PCI – Bus (Little Endian)

Byte 0	AD[7..0]
Byte 1	AD[15..8]
Byte 2	AD[23..16]
Byte 3	AD[31..24]

- Every Local Address Space (0...3) and the Expansion ROM Space can programmed to operate in Big or Little Endian Mode.

Big Endian		**Little Endian**	
32 Bit		**32 Bit**	
Byte 0	D[31..24]	Byte 0	D[7..0]
Byte 1	D[23..16]	Byte 1	D[15..8]
Byte 2	D[15..8]	Byte 2	D[23..16]
Byte 3	D[7..0]	Byte 3	D[31..24]
16 Bit upper lane		**16 Bit**	
Byte 0	D[31..24]	Byte 0	D[7..0]
Byte 1	D[23..16]	Byte 1	D[15..8]
16 Bit lower lane			
Byte 0	D[15..8]		
Byte 1	D[7..0]		
8 Bit upper lane		**8 Bit**	
Byte 0	D[31..24]	Byte 0	D[7..0]
8 Bit lower lane			
Byte 0	D[7..0]		

Table 6-1 : Local Bus Little/Big Endian

6.2 Local Software Reset

A local reset is used to reset the on board local logic.

The local reset is active during PCI reset or if the PCI Adapter Software Reset bit is set in the local configuration register CNTRL (offset 0x50).

CNTRL[30] PCI Adapter Software Reset:

Value of 1 resets the on board local logic. It remains in this reset condition until the PCI Host clears this bit. The contents of the PCI Configuration Registers are not reset. The PCI Interface is not reset.

6.3 Configuration EEPROM

For backward compatibility the serial EEPROM contains the configuration data of the previous version's PCI controller.

Address	Offset							
	0x00	0x02	0x04	0x06	0x08	0x0A	0x0C	0x0E
0x00	0x9050	0x10B5	0x0280	0x0000	0x1180	0x0000	0x029E	0x1498
0x10	0x0000	0x0040	0x0000	0x0100	0x4801	0x4801	0x0000	0x0000
0x20	0x0000	0x4C06	0x0000	0x0003	0x0FFF	0xFFF1	0x0000	0x0000
0x30	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0001
0x40	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
0x50	0x0171	0x78A0	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
0x60	0x0000	0x0000	0x0000	0x0009	0x0000	0x0000	0x0000	0x0000
0x70	0x0000	0x0000	0x0030	0x0041	0x0078	0x0000	0x0249	0x2492
0x80	0x0000	0x0000	0x0000	0x0000	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0x90	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xA0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xB0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xC0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xD0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xE0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xF0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF

Table 6-2 : Configuration EEPROM TPMC670-xx

7 Installation TPMC670

7.1 Input Wiring

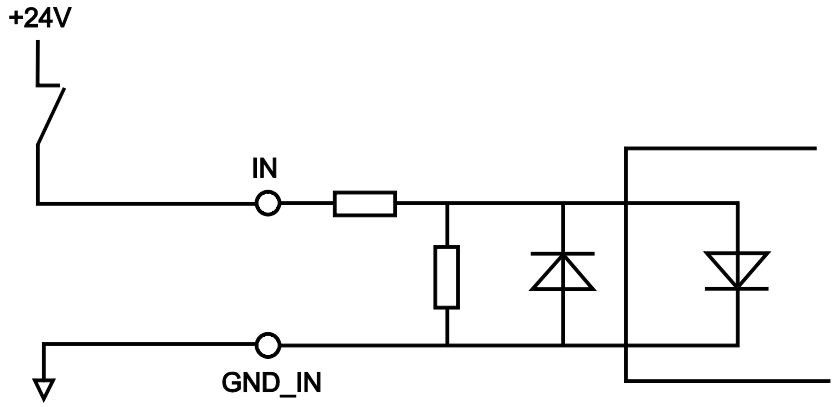


Figure 7-1 : Input Wiring

7.2 Output Wiring

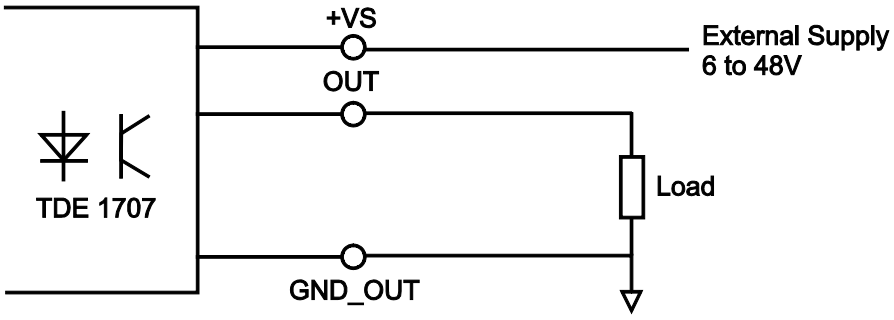


Figure 7-2 : Output Wiring

8 Pin Assignment – I/O Connector

8.1 Front Panel I/O

Pin	Signal		Pin	Signal	
1	VS_O1	External Supply OUT1 .. OUT4	26	GND_O2	Ground OUT 5 .. OUT 8
2	VS_O1	External Supply OUT1 .. OUT4	27	GND_O3	Ground OUT 9 .. OUT 12
3	VS_O2	External Supply OUT5 .. OUT8	28	GND_O4	Ground OUT 13 .. OUT 16
4	VS_O2	External Supply OUT5 .. OUT8	29	n.c.	not used
5	VS_O3	External Supply OUT9 .. OUT12	30	n.c.	not used
6	VS_O3	External Supply OUT9 .. OUT12	31	IN 1	Input Line 1
7	VS_O4	External Supply OUT13 .. OUT16	32	IN 2	Input Line 2
8	VS_O4	External Supply OUT13 .. OUT16	33	IN 3	Input Line 3
9	OUT 1	Output Line 1	34	IN 4	Input Line 4
10	OUT 2	Output Line 2	35	IN 5	Input Line 5
11	OUT 3	Output Line 3	36	IN 6	Input Line 6
12	OUT 4	Output Line 4	37	IN 7	Input Line 7
13	OUT 5	Output Line 5	38	IN 8	Input Line 8
14	OUT 6	Output Line 6	39	IN 9	Input Line 9
15	OUT 7	Output Line 7	40	IN 10	Input Line 10
16	OUT 8	Output Line 8	41	IN 11	Input Line 11
17	OUT 9	Output Line 9	42	IN 12	Input Line 12
18	OUT 10	Output Line 10	43	IN 13	Input Line 13
19	OUT 11	Output Line 11	44	IN 14	Input Line 14
20	OUT 12	Output Line 12	45	IN 15	Input Line 15
21	OUT 13	Output Line 13	46	IN 16	Input Line 16
22	OUT 14	Output Line 14	47	GND_I1	Ground IN 1 .. IN 4
23	OUT 15	Output Line 15	48	GND_I2	Ground IN 5 .. IN 8
24	OUT 16	Output Line 16	49	GND_I3	Ground IN 9 .. IN 12
25	GND_O1	Ground OUT 1 .. OUT 4	50	GND_I4	Ground IN 13 .. IN 16

Table 8-1 : Pin Assignment I/O HD50 Connector

Please check the maximum current of the used connection cable.

Some standard cables (AWG28 50pin) are limited to 0.75 A per lead.

8.2 Mezzanine Card Connector P14

Pin	Signal	Description
1	VS_O1	External Supply OUT1 .. OUT4
3	VS_O2	External Supply OUT5 .. OUT8
5	VS_O3	External Supply OUT9 .. OUT12
7	VS_O4	External Supply OUT13 .. OUT15
9	OUT 1	Output Line 1
11	OUT 3	Output Line 3
13	OUT 5	Output Line 5
15	OUT 7	Output Line 7
17	OUT 9	Output Line 9
19	OUT 11	Output Line 11
21	OUT 13	Output Line 13
23	OUT 15	Output Line 15
25	GND_O1	Ground OUT 1 .. OUT 4
27	GND_O3	Ground OUT 9 .. OUT 12
29	n.c.	not used
31	IN 1	Input Line 1
33	IN 3	Input Line 3
35	IN 5	Input Line 5
37	IN 7	Input Line 7
39	IN 9	Input Line 9
41	IN 11	Input Line 11
43	IN 13	Input Line 13
45	IN 15	Input Line 15
47	GND_I1	Ground IN 1 .. IN 4
49	GND_I3	Ground IN 9 .. IN 12
51	n.c.	not used
53	n.c.	not used
55	n.c.	not used
57	n.c.	not used
59	n.c.	not used
61	n.c.	not used
63	n.c.	not used

Pin	Signal	Description
2	VS_O1	External Supply OUT1 .. OUT4
4	VS_O2	External Supply OUT5 .. OUT8
6	VS_O3	External Supply OUT9 .. OUT12
8	VS_O4	External Supply OUT13 .. OUT15
10	OUT 2	Output Line 2
12	OUT 4	Output Line 4
14	OUT 6	Output Line 6
16	OUT 8	Output Line 8
18	OUT 10	Output Line 10
20	OUT 12	Output Line 12
22	OUT 14	Output Line 14
24	OUT 16	Output Line 16
26	GND_O2	Ground OUT 5 .. OUT 8
28	GND_O4	Ground OUT 13 .. OUT 16
30	n.c.	not used
32	IN 2	Input Line 2
34	IN 4	Input Line 4
36	IN 6	Input Line 6
38	IN 8	Input Line 8
40	IN 10	Input Line 10
42	IN 12	Input Line 12
44	IN 14	Input Line 14
46	IN 16	Input Line 16
48	GND_I2	Ground IN 5 .. IN 8
50	GND_I4	Ground IN 13 .. IN 16
52	n.c.	not used
54	n.c.	not used
56	n.c.	not used
58	n.c.	not used
60	n.c.	not used
62	n.c.	not used
64	n.c.	not used

Table 8-2 : Mezzanine Card Connector P14

Please verify that the tracks from the P14 connector to the Px connector of the PMC carrier board are designed for a current of typical 0.5 A min per output.

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