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TEWS TECHNOLOGIES

TIP570

Optically Isolated

16 Channel 12-Bit ADC

8 Channel 12-Bit DAC

Version 1.2

User Manual

Issue 1.2.1

May 2011

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TIP570-10

Optically Isolated 16 channels of 12-Bit ADC (input voltage range ±10V, programmable gain: 1, 2, 5, 10)

Optically Isolated 8 channels of 12-Bit DAC (output voltage range ±10V)

TIP570-11

Optically Isolated 16 channels of 12-Bit ADC (input voltage range ±10V, programmable gain: 1, 2, 4, 8)

Optically Isolated 8 channels of 12-Bit DAC (output voltage range ±10V)

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Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

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Issue	Description	Date
1.0	First Issue	January 2001
1.1	General Revision	April 2003
1.2	Added Programming and Installation Notes	October 2004
1.3	News Address TEWS LLC	September 2006
1.4	Added TIP570-11 Combined chapters “Programming Notes” and “Programming Hints”	March 2007
1.5	Added weight information to Technical Specifications Table	October 2008
1.1.6	New notation for User Manual and Engineering Documentation	April 2009
1.2.0	New Board Revision	February 2010
1.2.1	Corrected Pin Assignment Table	May 2011

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1 Product Description

The TIP570 is an IndustryPack® compatible module with an optically isolated 16 channel multiplexed 12-bit ADC and an optically isolated 8 channel 12-bit DAC. The ADC input path can be software configured to operate as 16 input channels in single-ended mode or as 8 input channels in differential mode.

The ADC input multiplexer is overvoltage protected for up to 70Vpp. A programmable gain amplifier supports gains of 1, 2, 5, 10 (TIP570-10) or gains of 1, 2, 4, 8 (TIP570-11). The full-scale input voltage range is +/–10V (gain = 1). The data acquisition and conversion time is mode-dependent: up to 10µs typical without channel or gain change, up to 12.5µs typical with channel or gain change.

The 8 channel DAC full-scale output voltage is +/–10V. The output amplifier is capable of sinking and sourcing 2mA for each DAC channel (1000pF load). The output voltage settles to 12 bits in 5µs typical.

Each TIP570 is factory calibrated. The calibration data is stored in the EEPROM unique to each IP.

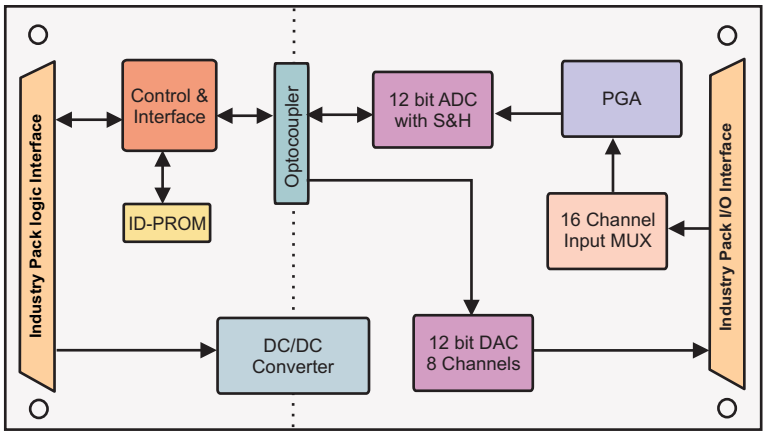


Figure 1-1 : Block Diagram

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2 Technical Specification

IP Interface		
Interface	Single Size IndustryPack® Logic Interface compliant to ANSI/VITA 4-1995 with an 8MHz Clock	
ID ROM Data	Format I	
I/O Space	Used with 0 wait states	
Memory Space	not used	
Interrupts	INTREQ0 used / INTREQ1 not used	
DMA	Not supported	
Module Type	Type I	
On Board Devices		
A/D Converter	ADS8508 (Texas Instruments)	
D/A Converter	DAC7615 (Texas Instruments)	
Analog-to-Digital Conversion		
Resolution	12 bit	
Input Voltage Range	±10V	
Analog Inputs	16 single-ended or 8 differential input channels	
Programmable Input Gain Amplifier	TIP570-10: 1, 2, 5, 10 TIP570-11: 1, 2, 4, 8	
Digital-to-Analog Conversion		
Resolution	12 bit	
Output Voltage Range	±10V	
Output Settling Time	5µs typical, 10µs maximum to 0.012%	
Output Load per Channel	max. 2mA, 1000pF	
I/O Interface		
Interface Connector	50-conductor flat cable	
Isolation	All D/A channels are optically isolated from the IP Interface	
Power Requirements	550mA typical @ +5V DC ±12V DC: not used	
Physical Data		
Temperature Range	Operating Storage	-40°C to +85°C -40°C to +85°C
MTBF	369000h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	46 g	

Table 2-1 : Technical Specification

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3 ID PROM Contents

The TIP570 ID PROM consists of two 64 byte pages. The active page is selected in the EEPROM Control Register. After reset, the first 64 byte page is selected and readable in the IP ID PROM Space. Both pages are also readable in the IP Memory Space.

The first 64 byte page stores the ID PROM, Type I data.

The second 64 byte page stores the ADC and DAC calibration data values.

3.1 First 64 byte page – ID PROM, Type I

Address	Function	Contents
0x01	ASCII 'I'	**0x49**
0x03	ASCII 'P'	**0x50**
0x05	ASCII 'A'	**0x41**
0x07	ASCII 'C'	**0x43**
0x09	Manufacturer ID	**0xB3**
0x0B	Model Number	**0x2C**
0x0D	Revision	**0x10**
0x0F	Reserved	**0x00**
0x11	Driver-ID Low - Byte	**0x00**
0x13	Driver-ID High - Byte	**0x00**
0x15	Number of bytes used	**0x0D**
0x17	CRC	**TIP570-10: 0x08** **TIP570-11: 0x29**
0x19	Version	**TIP570-10: 0x0A** **TIP570-11: 0x0B**
0x1A … 0x3F	Undefined	**0xFF**

Table 3-1 : ID PROM Contents – First 64 byte page

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3.2 Second 64 byte page – Calibration Data

Address	Function	Contents
ADC Correction Data		
0x01	Offset Error for Gain = 1	**Board dependent**
0x03	Offset Error for Gain = 2	**Board dependent**
0x05	Offset Error for Gain = 4 or 5	**Board dependent**
0x07	Offset Error for Gain = 8 or 10	**Board dependent**
0x09	Gain Error for Gain = 1	**Board dependent**
0x0B	Gain Error for Gain = 1	**Board dependent**
0x0D	Gain Error for Gain = 4 or 5	**Board dependent**
0x0F	Gain Error for Gain = 8 or 10	**Board dependent**
DAC Correction Data		
0x11	DAC 1 Offset Error	**Board dependent**
0x13	DAC 2 Offset Error	**Board dependent**
0x15	DAC 3 Offset Error	**Board dependent**
0x17	DAC 4 Offset Error	**Board dependent**
0x19	DAC 5 Offset Error	**Board dependent**
0x1B	DAC 6 Offset Error	**Board dependent**
0x1D	DAC 7 Offset Error	**Board dependent**
0x1F	DAC 8 Offset Error	**Board dependent**
0x21	DAC 1 Gain Error	**Board dependent**
0x23	DAC 2 Gain Error	**Board dependent**
0x25	DAC 3 Gain Error	**Board dependent**
0x27	DAC 4 Gain Error	**Board dependent**
0x29	DAC 5 Gain Error	**Board dependent**
0x2B	DAC 6 Gain Error	**Board dependent**
0x2D	DAC 7 Gain Error	**Board dependent**
0x2F	DAC 7 Gain Error	**Board dependent**
0x31 … 0x3F	Undefined	**0xFF**

Table 3-2 : ID PROM Contents – Second 64 byte page

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4 IP Addressing

4.1 I/O Addressing

The complete register set of the TIP570 is accessible in the I/O space of the IP Module.

Address	Symbol	Description	Size (Bit)	Access
0x00	ADC_CTRL	ADC Control Register	16	R/W
0x02	ADC_DATA	ADC Data Register	16	R
0x04	ADC_STAT	ADC Status Register	16	R
0x06	ADC_CONV	ADC Convert Register	16	W
0x09	INTVEC	Interrupt Vector Register	8	R/W
0x0B	EEP_CTRL	EEPROM Control Register	8	R/W
0x10	DAC_CTRL	DAC Control Register	16	R/W
0x12	DAC_DATA	DAC Data Register	16	R/W
0x14	DAC_STAT	DAC Status Register	16	R
0x16	DAC_CONV	DAC Convert Register	16	R/W

Table 4-1 : TIP570 Register Set

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4.2 ADC Control Register (Address: 0x00)

The ADC Control Register (ADC_CTRL) is used to select an input channel, an input gain and input modes for the next A/D conversion.

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>15:10</td><td>-</td><td>Not used, always read as ‘0’.</td><td>R/W</td><td>-</td></tr>
<tr><td>9</td><td>INT</td><td>ADC Interrupt Enable:
0 = Interrupts disabled
1 = Interrupts enabled
If Interrupts are enabled, interrupt requests will be asserted on INTREQ0 after an A/D conversion is done and the converted data is stored inside the ADC Data Register.</td><td>R/W</td><td>0</td></tr>
<tr><td>8</td><td>PIPE</td><td>Pipeline Mode Control:
0 = Pipeline Mode Off
Data of conversion N is shifted into the ADC Data Register after the conversion N is done.
1 = Pipeline Mode On
Data of conversion N−1 is shifted into the ADC Data Register during the conversion N.</td><td>R/W</td><td>0</td></tr>
<tr><td>7</td><td>AUTO</td><td>Automatic Settling Time Mode Control:
0 = Automatic Mode Off
In this mode, the SET_BUSY bit in the ADC Status Register has to be read as ‘0’ (settling time done) before starting an A/D conversion manually by writing to the ADC Convert Register.
It is allowed to write new data to the ADC Control Register immediately after starting the A/D conversion.
1 = Automatic Mode On
In this mode, the A/D conversion is automatically started after the required settling time is done.

In both modes, the ADC Data register only contains valid data when the ADC_BUSY Bit in the ADC Status Register is read as ‘0’. Otherwise, the serial transfer from the ADC is still in progress.</td><td>R/W</td><td>0</td></tr>
<tr><td>6:5</td><td>G1 G0</td><td>Input Gain Selection:
<table>
<tr><th>Gain</th><th>G1</th><th>G0</th><th>Input Voltage Range</th></tr>
<tr><td>1</td><td>0</td><td>0</td><td>±10V</td></tr>
<tr><td>2</td><td>0</td><td>1</td><td>±5V</td></tr>
<tr><td>4 or 5</td><td>1</td><td>0</td><td>±2.5V or ±2V</td></tr>
<tr><td>8 or 10</td><td>1</td><td>1</td><td>±1.25V or ±1V</td></tr>
</table></td><td>R/W</td><td>00</td></tr>
<tr><td>4</td><td>DIFF</td><td>Input Mode Control:
0 = Single-Ended Mode
1 = Differential Mode
See chapter “Pin Assignment” for usable input channels.</td><td>R/W</td><td>0</td></tr>
</table>

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<table>
<tr>
<td>3:0</td>
<td>CS</td>
<td>Channel Selection:
<table>
<tr><th>CS[3:0]</th><th>Single-ended Mode</th><th>Differential Mode</th></tr>
<tr><td>0000</td><td>ADC Channel 1</td><td>ADC Channel 1</td></tr>
<tr><td>0001</td><td>ADC Channel 2</td><td>ADC Channel 2</td></tr>
<tr><td>0010</td><td>ADC Channel 3</td><td>ADC Channel 3</td></tr>
<tr><td>0011</td><td>ADC Channel 4</td><td>ADC Channel 4</td></tr>
<tr><td>0100</td><td>ADC Channel 5</td><td>ADC Channel 5</td></tr>
<tr><td>0101</td><td>ADC Channel 6</td><td>ADC Channel 6</td></tr>
<tr><td>0110</td><td>ADC Channel 7</td><td>ADC Channel 7</td></tr>
<tr><td>0111</td><td>ADC Channel 8</td><td>ADC Channel 8</td></tr>
<tr><td>1000</td><td>ADC Channel 9</td><td>-</td></tr>
<tr><td>1001</td><td>ADC Channel 10</td><td>-</td></tr>
<tr><td>1010</td><td>ADC Channel 11</td><td>-</td></tr>
<tr><td>1011</td><td>ADC Channel 12</td><td>-</td></tr>
<tr><td>1100</td><td>ADC Channel 13</td><td>-</td></tr>
<tr><td>1101</td><td>ADC Channel 14</td><td>-</td></tr>
<tr><td>1110</td><td>ADC Channel 15</td><td>-</td></tr>
<tr><td>1111</td><td>ADC Channel 16</td><td>-</td></tr>
</table>
See chapter “Pin Assignment” for usable input channels.</td>
<td>R/W</td>
<td>0000</td>
</tr>
</table>

Table 4-2 : ADC Control Register

In general, after changing the ADC input channel or gain it takes some settling time until the ADC input signal path is properly set up. This settling time must be expired before an ADC conversion should be started (status can be checked in the ADC Status Register).

4.3 ADC Data Register (Address: 0x02)

The ADC Data Register (ADC_DATA) is used to store the converted data value from the ADC. The 12-bit value from the ADC is shifted to the upper 12 bits (15:4) by hardware of the ADC Data Register, so it can be processed as a 16-bit two’s complement integer value directly.

Bit	Symbol	Description	Access	Reset Value
15:4	ADC_DATA	12-bit ADC value	R	0x000
3:0	-	Not used, always read as ‘0’.	R	-

Table 4-3 : ADC Data Register

The content of the ADC Data Register is not valid as long as the ADC_BUSY Bit is set in the ADC Status Register.

See chapter “Functional Description” for ADC Data Coding.

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4.4 ADC Status Register (Address: 0x04)

The ADC Status Register (ADC_STAT) provides status flags for the ADC communication.

Bit	Symbol	Description	Access	Reset Value
15:2	-	Not used, always read as '0'.	R	-
1	ADC_BUSY	ADC Busy Flag: This bit is hardware-set to '1' by writing to the ADC Convert Register when Automatic Mode is Off or by writing to the ADC Control Register with Automatic Mode On. This bit is hardware-cleared to '0' when the ADC conversion is done and the ADC Data Register contains valid data. 0 = No ADC conversion in progress. ADC Data Register contains valid data. 1 = ADC conversion in progress. There is no valid data in the ADC Data Register.	R	0
0	SET_BUSY	Settling Time Busy Flag: This bit is hardware-set to '1' by writing to the ADC Control Register. This bit is hardware-cleared to '0' when the ADC input path settling time is done. 0 = ADC settling time over 1 = ADC settling time not over In Automatic Settling Time Mode, the TIP570 takes care of this bit automatically. In None Automatic Settling Time Mode, the user must wait for the SET_BUSY bit to be clear before starting an A/D conversion.	R	0

Table 4-4 : ADC Status Register

4.5 ADC Convert Register (Address: 0x06)

The ADC Convert Register (ADC_CONV) is used to start an A/D conversion manually in None Automatic Settling Time Mode. Prior to starting an A/D conversion, both the SET_BUSY Bit and the ADC_BUSY Bit in the ADC Status Register have to be read as '0'.

The conversion is started with a write access to the ADC Convert Register, no matter the data value.

It is allowed to write new channel/gain settings into the ADC Control Register immediately after starting a manual A/D conversion.

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4.6 Interrupt Vector Register (Address: 0x09)

The Interrupt Vector Register (INTVEC) is a byte wide read/write register. An interrupt acknowledge cycle clears the interrupt request and puts the Interrupt Vector onto the data bus.

If interrupts are enabled in the ADC Control Register, interrupts are generated whenever a conversion of the ADC is done; i.e. when the ADC_BUSY flag in the ADC Status Register becomes inactive (set to '0').

Bit	Symbol	Description	Access	Reset Value
7:0	INTVEC	Interrupt Vector loaded by software	R/W	0x00

Table 4-5 : Interrupt Vector Register

4.7 EEPROM Control Register (Address: 0x0B)

The IP ID and Memory Spaces consist of two 64 byte pages. The active one gets selected in this register.

Bit	Symbol	Description	Access	Reset Value
7:2	-	Not used, always read as '0'.	R	-
1	PPS	EEPROM Page Select: 0 = First 64 byte page is selected (ID PROM, Type I) 1 = Second 64 byte page is selected (Calibration Data)	R/W	0
0	PWE	EEPROM Write Enable Control: 0 = Write Accesses to the EEPROM are disabled 1 = Write Accesses to the EEPROM are enabled	R/W	0

Table 4-6 : EEPROM Control Register

Bit 0 (enabling write access to the EEPROM) is for factory calibration only! This bit has to remain '0' during normal operation; otherwise all calibration data could be lost!

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4.8 DAC Control Register (Address: 0x10)

The DAC Control Register (DAC_CTRL) is used to reset all analog outputs to 0V.

Bit	Symbol	Description	Access	Reset Value
15:1	-	Not used, always read as '0'.	R	0
0	DAC_RST	DAC Analog Output Reset: 0 = DAC outputs are in normal operation 1 = DAC outputs are set to 0V.	R/W	0

Table 4-7 : DAC Control Register

The DAC analog outputs are also set to 0V for the time the IP_RESET# signal is asserted.

See chapter "Functional Description" for a complete DAC reset procedure.

4.9 DAC Data Register (Address: 0x12)

The DAC Data Register (DAC_DATA) holds the 12-bit DAC Data to be converted. Each DAC conversion that is started uses the data stored in this register. Only the upper 12 bits (15:4) are used for the DAC conversion.

Bit	Symbol	Description	Access	Reset Value
15:4	DAC_DATA	12-bit DAC Data in two's complement format	R/W	0
3:0	-	Not used, always read as '0'.	R/W	0

Table 4-8 : DAC Data Register

See chapter "Functional Description" for DAC Data Coding.

4.10 DAC Status Register (Address: 0x14)

The DAC Status Register (DAC_STAT) provides status flags for the DAC communication.

Bit	Symbol	Description	Access	Reset Value
15:1	-	Not used, always read as '0'.	R/W	0
3:0	DAC_BUSY	DAC Busy Flag: This bit is hardware-set to '1' by writing to the DAC Convert Register. This bit is hardware-cleared when the DAC conversion is done. 0 = A new DAC conversion can be started by writing to the DAC Convert Register 1 = DAC conversion in progress	R/W	0

Table 4-9 : DAC Status Register

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4.11 DAC Convert Register (Address: 0x16)

The DAC Convert Register (DAC_CONV) is used to start DAC conversions. The write access that sets the channel and conversion mode also starts the conversion. Therefore, the DAC_BUSY Bit in the DAC Status Register must be read as '0' before starting a conversion.

<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Access</th><th>Reset Value</th></tr>
<tr><td>15:4</td><td>-</td><td>Not used, always read as '0'.</td><td>R/W</td><td>0</td></tr>
<tr><td>4</td><td>MODE</td><td>DAC Operating Mode:
0 = DAC Transparent Mode
1 = DAC Latched Mode
In Transparent Mode, a conversion immediately updates the analog output for the selected channel.
In Latched Mode, a conversion will not update the analog output for the selected channel but only update the channels input data register. A special write command to the DAC Convert Register will update all DAC outputs simultaneously with the data stored in their respective input data registers.</td><td>R/W</td><td>0</td></tr>
<tr><td>3:0</td><td>CS[3:0]</td><td>DAC Channel Selection:
<table>
<tr><th>Mode</th><th>CS[3:0]</th><th>Function</th></tr>
<tr><td colspan="3">Transparent Mode</td></tr>
<tr><td>0</td><td>0000</td><td>No Function</td></tr>
<tr><td>0</td><td>0001</td><td>Load DAC Output 1</td></tr>
<tr><td>0</td><td>0010</td><td>Load DAC Output 2</td></tr>
<tr><td>0</td><td>0011</td><td>Load DAC Output 3</td></tr>
<tr><td>0</td><td>0100</td><td>Load DAC Output 4</td></tr>
<tr><td>0</td><td>0101</td><td>Load DAC Output 5</td></tr>
<tr><td>0</td><td>0110</td><td>Load DAC Output 6</td></tr>
<tr><td>0</td><td>0111</td><td>Load DAC Output 7</td></tr>
<tr><td>0</td><td>1000</td><td>Load DAC Output 8</td></tr>
<tr><td>0</td><td>others</td><td>No Function</td></tr>
<tr><td colspan="3">Latched Mode</td></tr>
<tr><td>1</td><td>0000</td><td>Load All DAC Outputs</td></tr>
<tr><td>1</td><td>0001</td><td>Load DAC Register 1</td></tr>
<tr><td>1</td><td>0010</td><td>Load DAC Register 2</td></tr>
<tr><td>1</td><td>0011</td><td>Load DAC Register 3</td></tr>
<tr><td>1</td><td>0100</td><td>Load DAC Register 4</td></tr>
<tr><td>1</td><td>0101</td><td>Load DAC Register 5</td></tr>
<tr><td>1</td><td>0110</td><td>Load DAC Register 6</td></tr>
<tr><td>1</td><td>0111</td><td>Load DAC Register 7</td></tr>
<tr><td>1</td><td>1000</td><td>Load DAC Register 8</td></tr>
<tr><td>1</td><td>others</td><td>Reserved</td></tr>
</table>
</td><td>R/W</td><td>0000</td></tr>
</table>

Table 4-10: DAC Convert Register

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5 Functional Description

5.1 Data Correction

There are two errors affecting the accuracy of the ADC and the DAC that can be corrected using the factory calibrated calibration data space.

First, there is the so called “offset error”. For the ADC, this is the converted data value with its inputs connected to GND in single-ended mode or with shorted inputs in differential mode. For the DAC, this is the data value that is required to produce a zero voltage output signal. The offset error is corrected by subtracting the offset calibration data from the data values.

Second, there is the so called “gain error”. The gain error is the difference between the ideal gain and the actual gain of the ADC and DAC. It is corrected by multiplying the data values with a correction factor.

The correction values are obtained during factory calibration and are stored in an on board EEPROM as two’s complement byte-wide values in the range from -128 to +127. To achieve a higher accuracy, they are scaled to ¼LSB.

5.1.1 ADC Data Correction

The basic formula for correcting ADC input values is:

$$\mathbf{Data = ReadValue * (1 - GAIN_{corr} / 8192) - OFFSET_{corr} / 4}$$

Data is the corrected digital value. *ReadValue* is the digital value read from the ADC. $GAIN_{corr}$ and $OFFSET_{corr}$ are the correction factors from the on board EEPROM. $GAIN_{corr}$ and $OFFSET_{corr}$ are stored separately for each of the gain values.

Floating point arithmetic or scaled integer arithmetic is necessary to avoid rounding errors while computing the above formulas.

5.1.2 DAC Data Correction

The basic formula for correcting DAC output values is:

$$\mathbf{Data = Value * (1 - GAIN_{corr} / 8192) - OFFSET_{corr} / 4}$$

Data is the corrected digital value that should be programmed to the data register. *Value* is the ideal digital value for the desired output voltage. $GAIN_{corr}$ and $OFFSET_{corr}$ are the correction factors from the on board EEPROM. $GAIN_{corr}$ and $OFFSET_{corr}$ are stored separately for each of the possible D/A channels.

Floating point arithmetic or scaled integer arithmetic is necessary to avoid rounding errors while computing the above formulas.

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5.2 Data Coding

5.2.1 ADC Data Coding

Analog Input Voltage	Description	ADC Data Register Value
+9.9951V	+FSR	0x7FF0
+0.00488V	Midscale +1LSB	0x0001
0V	Midscale	0x0000
-0.00488V	Midscale -1LSB	0xFFF0
-10V	-FSR	0x8000

Table 5-1 : ADC Data Coding

5.2.2 DAC Data Coding

Data Value	Analog Output Voltage	
Voltage Range: -10V … +10V (Bipolar)		
0x7FF0	+FSR	+9.9951V
0x0001	Midscale +1LSB	+0.00488V
0x0000	Midscale	0V
0xFFF0	Midscale -1LSB	-0.00488V
0x8000	-FSR	-10V

Table 5-2 : DAC Data Coding

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5.3 Initialization after Power-Up

5.3.1 ADC Initialization

After power-up, the on board ADC device is in a random state and requires two dummy conversions before operating correctly. This is based on the chip design of the ADC device.

Software should ignore the data of the first two conversions after power-up.

All drivers from TEWS TECHNOLOGIES already include these two dummy conversions.

5.3.2 DAC Initialization

The TIP570 uses two four-channel serial DAC devices to build up the eight DAC output channels. The reset signals of these devices only affect the internal data input registers and the data output registers of each channel but not the devices' general input shift register.

Therefore, the following DAC reset procedure has to be used once after every power on, reset and also every time a software reset is required. If this reset procedure is not used, programming one DAC output channel could result in undefined output voltages on other DAC output channels due to corrupted data in the devices' input shift registers.

DAC Reset Procedure:

1. Set DAC devices into reset state
    - Write 0x0001 into DAC_CTRL Register
2. Clear DAC Data Register
    - Write 0x0000 into DAC_DATA Register
3. Clear Input Shift Register of the first four-channel DAC device
    - Write 0x0001 into DAC_CONV Register
    - Wait for DAC_BUSY Bit in the DAC_STAT Register to become inactive
4. Clear Input Shift Register of the second four-channel DAC device
    - Write 0x0005 into DAC_CONV Register
    - Wait for DAC_BUSY Bit in the DAC_STAT Register to become inactive
5. Set DAC devices to normal operation
    - Write 0x0000 into DAC_CTRL Register

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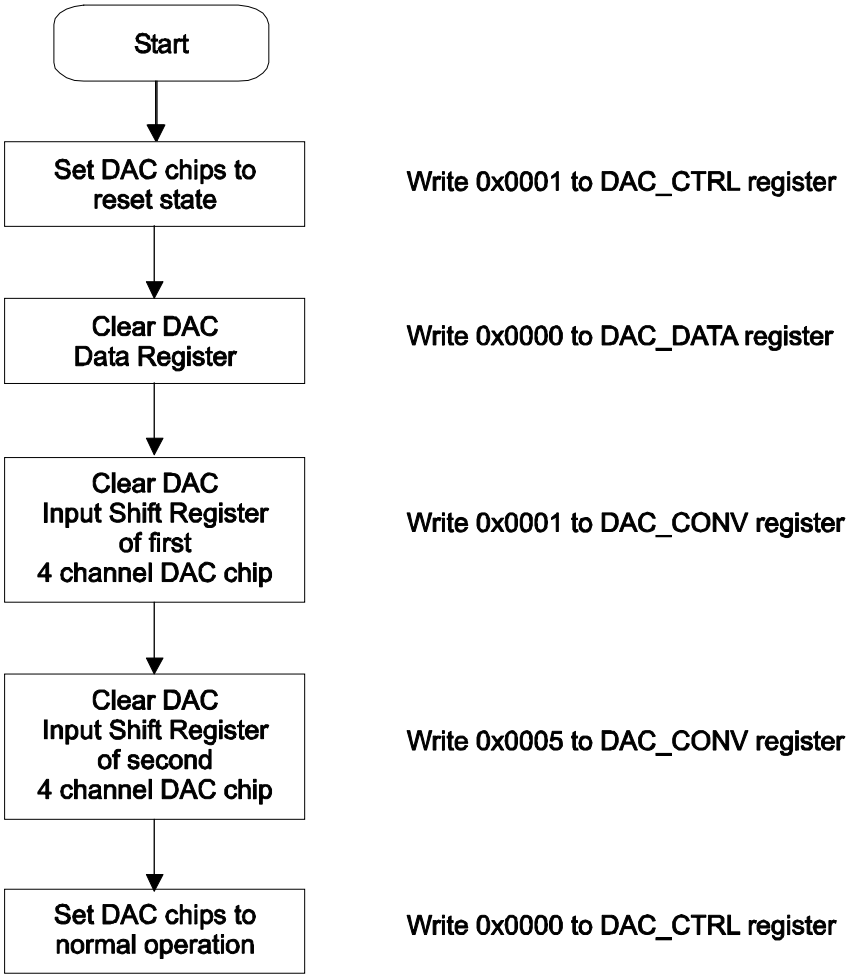


Figure 5-1 : DAC Reset Procedure

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5.4 Operating Modes

5.4.1 ADC Operating Modes

The TIP570 supports four different operating modes for the ADC device. These modes are set up in the ADC Control Register, specifically in Bit [8:7].

ADC Control Register Bit		Mode Description
8 (PIPE)	7 (AUTO)	
0	0	Automatic Mode OFF Pipeline Mode OFF A write access to the ADC Convert Register starts conversion N. The result of conversion N is shifted into the ADC Data Register.
0	1	Automatic Mode ON Pipeline Mode OFF A write access to the ADC Control Register starts conversion N after the settling time expires. The result of conversion N is shifted into the ADC Data Register.
1	0	Automatic Mode OFF Pipeline Mode ON A write access to the ADC Convert Register starts conversion N. The result of conversion N-1 is shifted into the ADC Data Register.
1	1	Automatic Mode ON Pipeline Mode ON A write access to the ADC Control Register starts conversion N after the settling time expires. The result of conversion N-1 is shifted into the ADC Data Register.

With the Automatic Mode set to OFF, it is necessary to check the SET_BUSY Bit in the ADC Status Register to be sure that the ADC analog input path settling time has expired before starting a conversion manually.

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5.4.1.1 Automatic OFF – Pipeline OFF

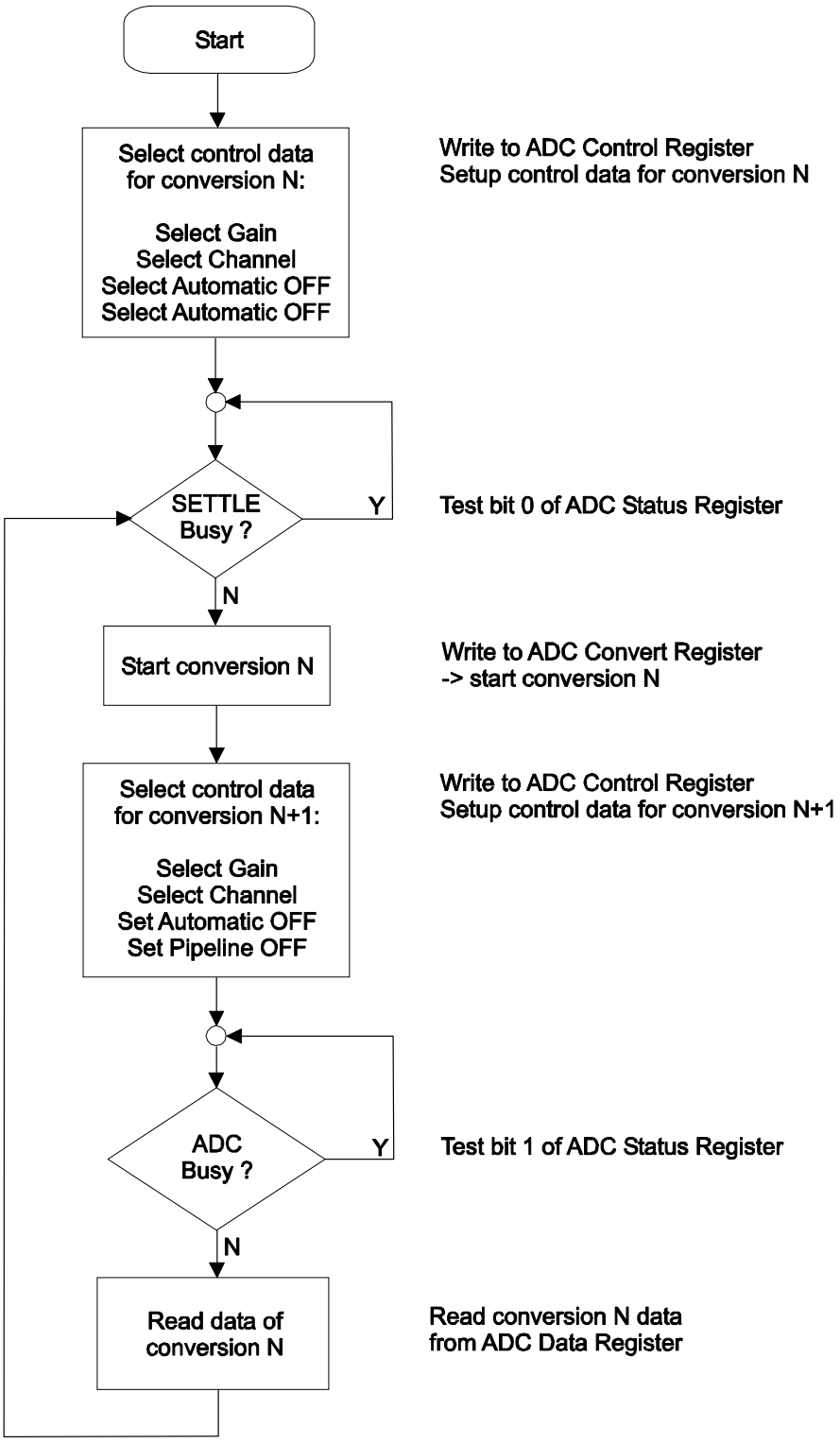


Figure 5-2 : Flowchart ADC Conversion (Automatic OFF – Pipeline OFF)

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5.4.1.2 Automatic OFF – Pipeline ON

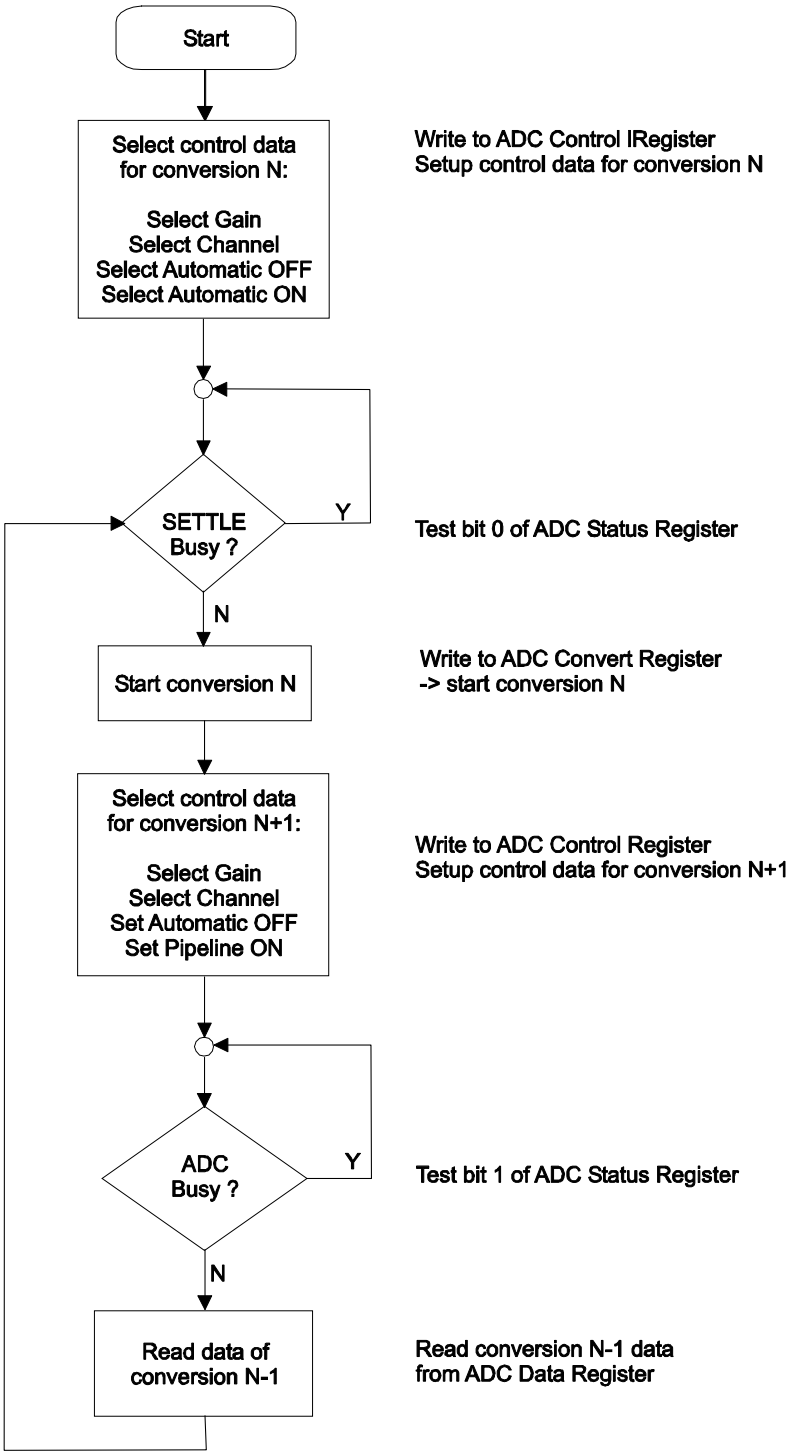


Figure 5-3 : Flowchart ADC Conversion (Automatic OFF – Pipeline ON)

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5.4.1.3 Automatic ON – Pipeline OFF

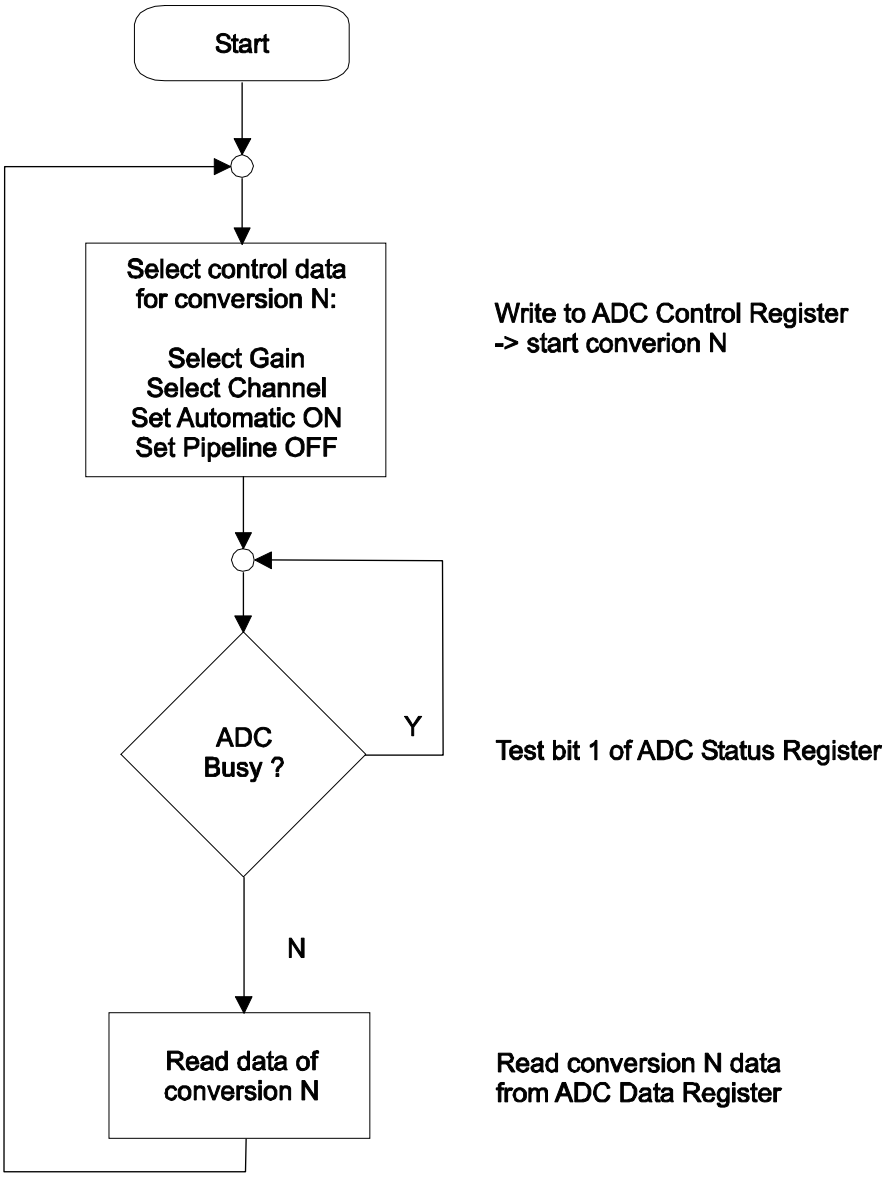


Figure 5-4 : Flowchart ADC Conversion (Automatic ON – Pipeline OFF)

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5.4.1.4 Automatic ON – Pipeline ON

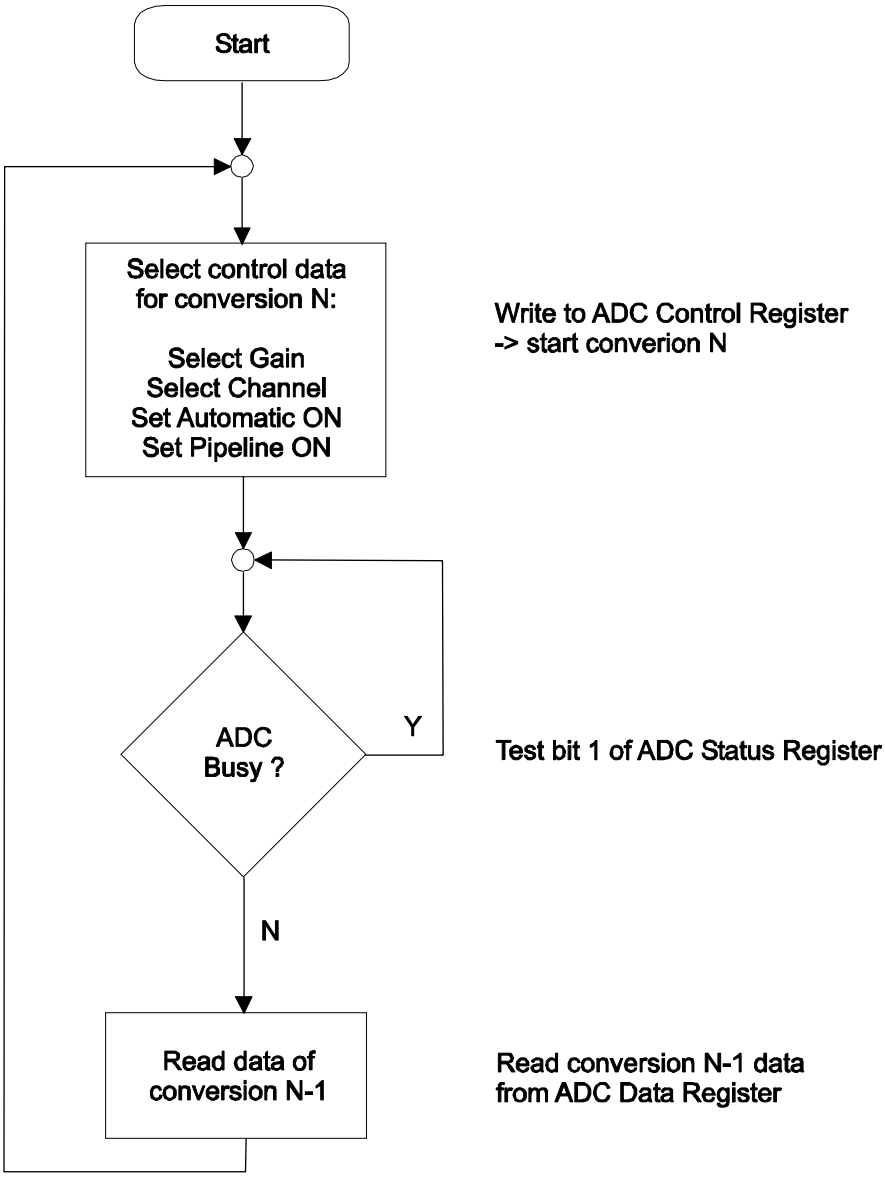


Figure 5-5 : Flowchart ADC Conversion (Automatic ON – Pipeline ON)

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5.4.2 DAC Operating Modes

5.4.2.1 Transparent Mode

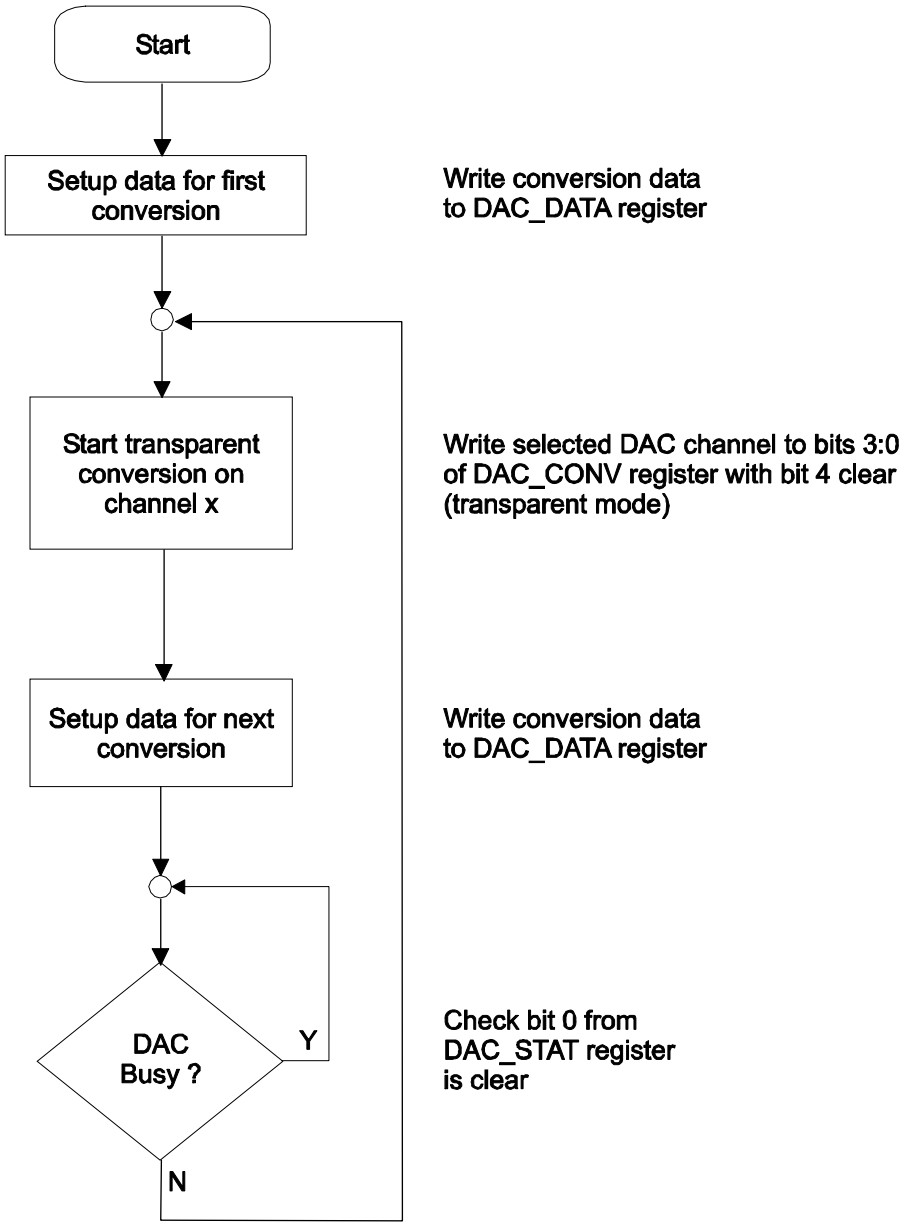


Figure 5-6 : Flowchart DAC Conversion (Transparent Mode)

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5.4.2.2 Latched Mode

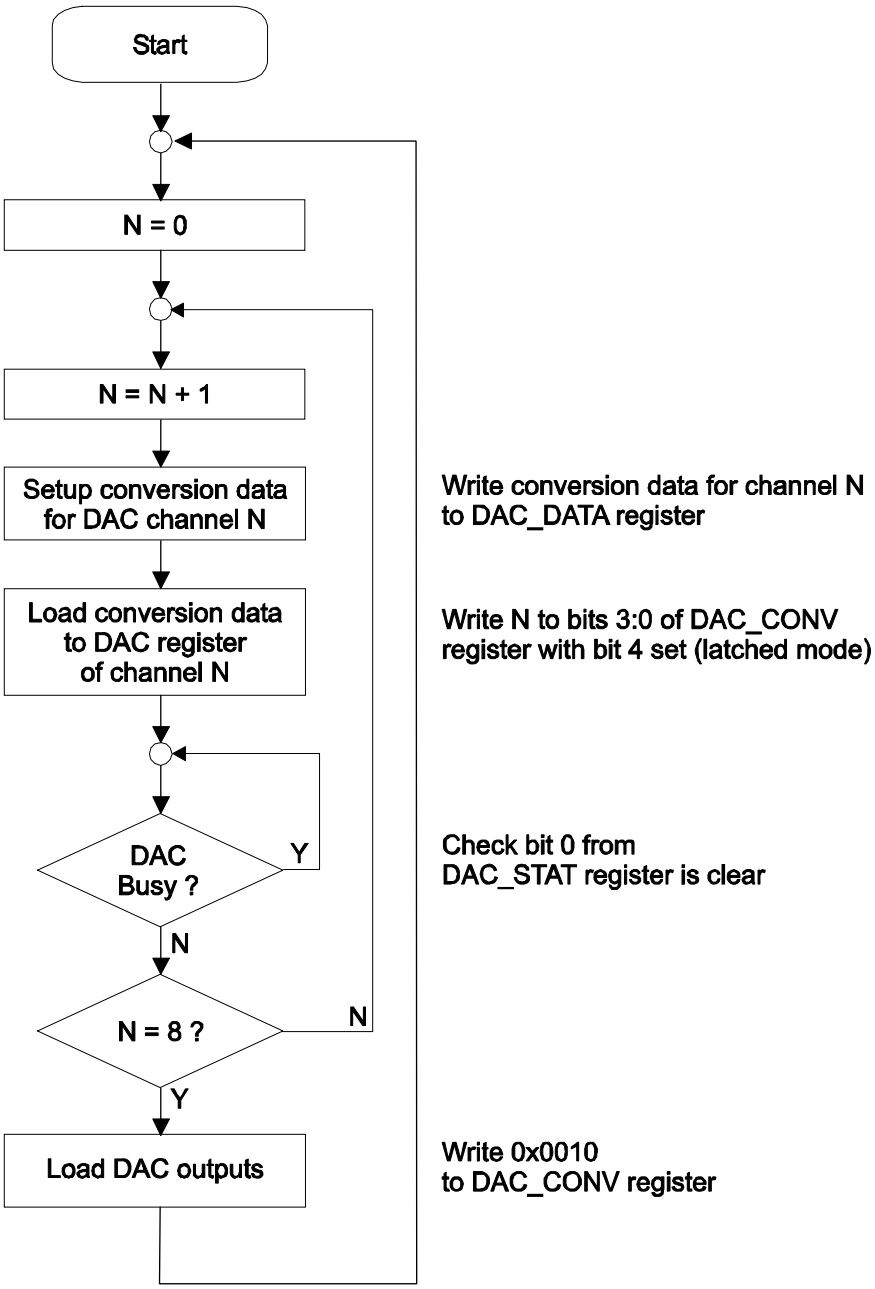


Figure 5-7 : Flowchart DAC Conversion (Latched Mode)

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6 Installation Notes

6.1 Analog Inputs

Make sure that all unused analog input pins are tied to the AGND signal level (or any other valid signal level within the analog input voltage range). This is required even when the unused channels are turned off by software.

If unused analog inputs are left floating, they could badly degrade performance of the active channels.

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7 Pin Assignment – I/O Connector

ADC Signals		
Pin	**Single-ended Mode**	**Differential Mode**
1	ADC Input 1	ADC Input 1+
2	ADC Input 9	ADC Input 1 -
3	AGND	
4	ADC Input 10	ADC Input 2 -
5	ADC Input 2	ADC Input 2+
6	AGND	
7	ADC Input 3	ADC Input 3+
8	ADC Input 11	ADC Input 3 -
9	AGND	
10	ADC Input 12	ADC Input 4 -
11	ADC Input 4	ADC Input 4+
12	AGND	
13	ADC Input 5	ADC Input 5+
14	ADC Input 13	ADC Input 5 -
15	AGND	
16	ADC Input 14	ADC Input 6 -
17	ADC Input 6	ADC Input 6+
18	AGND	
19	ADC Input 7	ADC Input 7+
20	ADC Input 15	ADC Input 7 -
21	AGND	
22	ADC Input 16	ADC Input 8 -
23	ADC Input 8	ADC Input 8+
24	AGND	
25	-	

DAC Signals	
Pin	**Signal**
26	-
27	DAC Output 1
28	AGND
29	DAC Output 2
30	AGND
31	DAC Output 3
32	AGND
33	DAC Output 4
34	AGND
35	DAC Output 5
36	AGND
37	DAC Output 6
38	AGND
39	DAC Output 7
40	AGND
41	DAC Output 8
42	AGND
43	-
44	-
45	-
46	-
47	-
48	-
49	-
50	-

Table 7-1 : Pin Assignment I/O Connector

See chapter “Installation Notes” for unused analog inputs.

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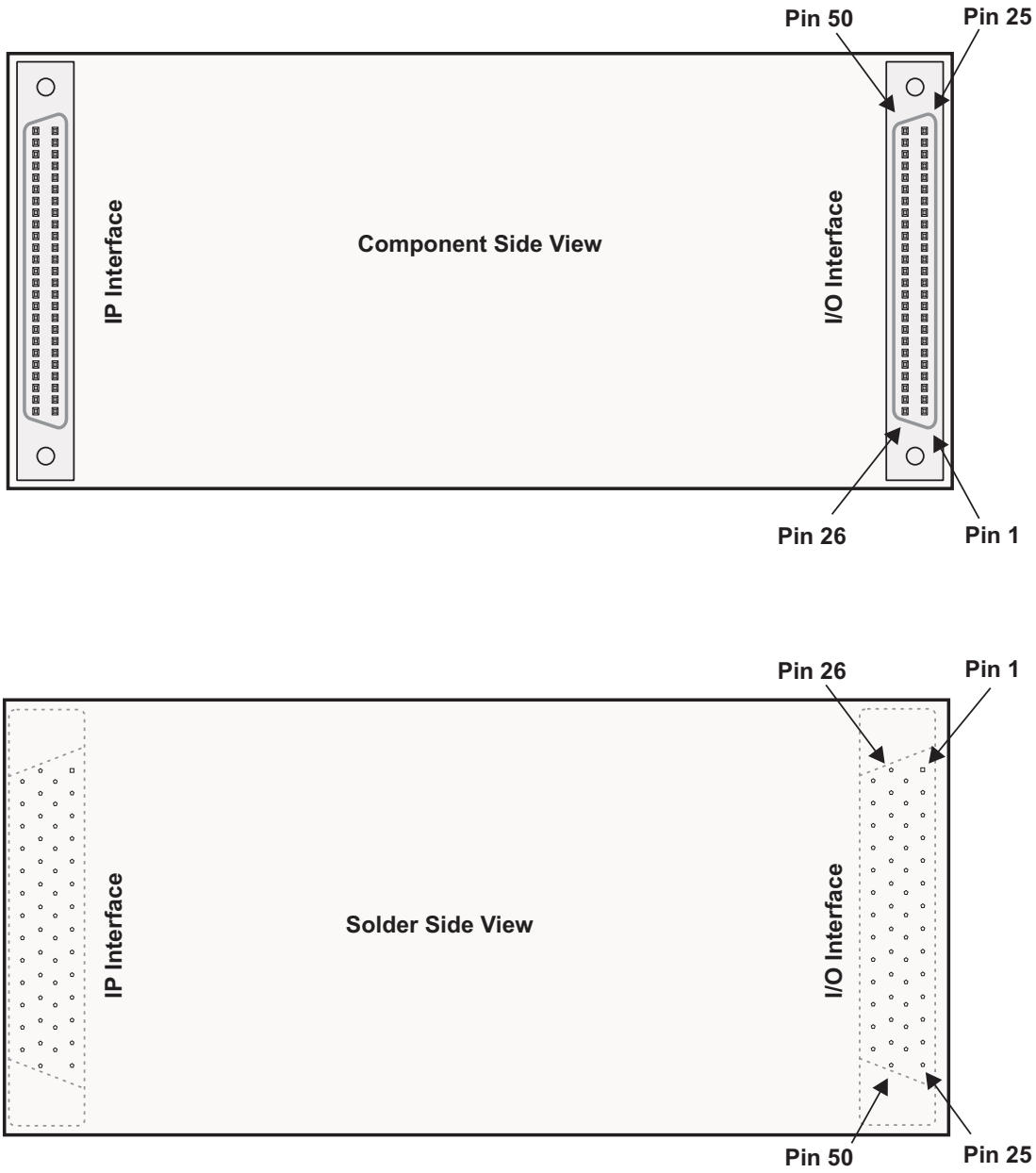


Figure 7-1 : IP Connector Orientation

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