TIP830

8 Channel Simultaneous Sampling ADC
Version 1.0 Revision B

User Manual

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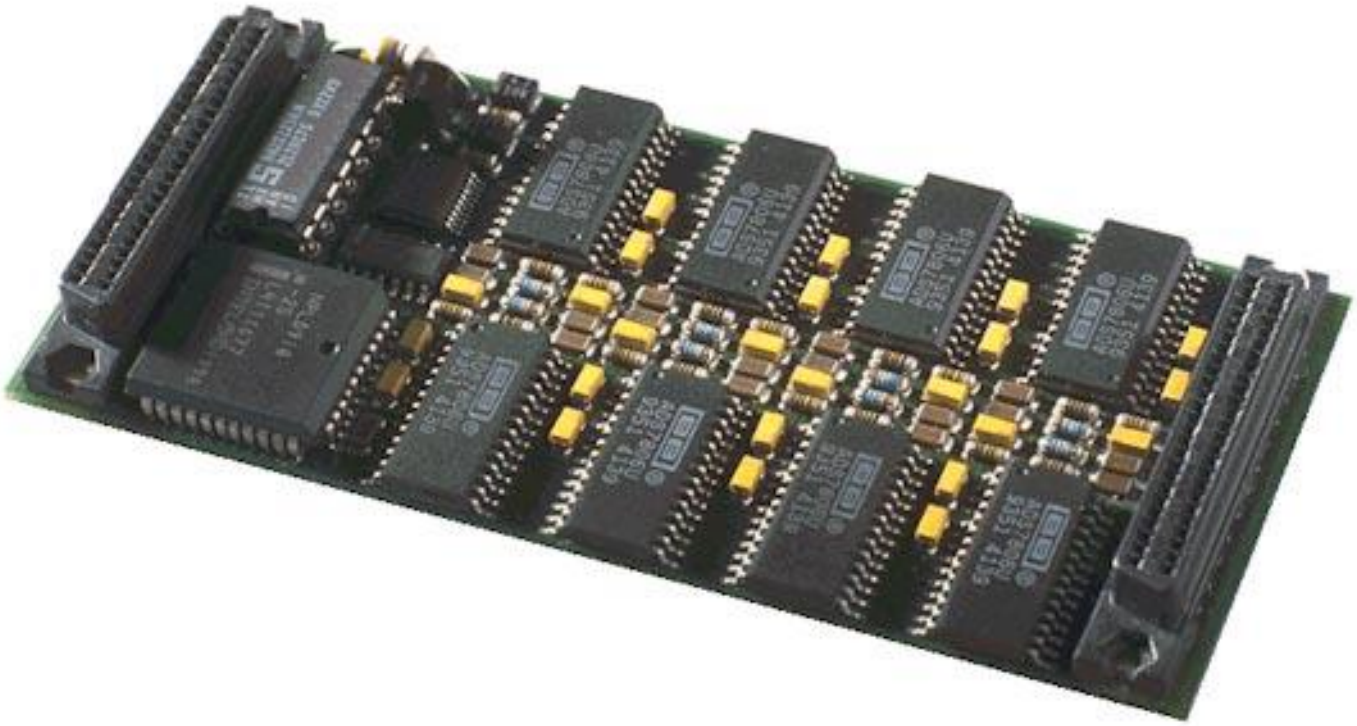

TIP830-10

8 channel 12 bit simultaneous sampling ADC

TIP830-20

8 channel 16 bit simultaneous sampling ADC

This manual covers both products

TEWS DATEN*TECHNIK* GmbH has made any effort to ensure that this manual is accurate and complete. However TEWS DATEN*TECHNIK* GmbH reserves the right to change the product described in this document at any time without notice.

This product has been designed to operate with IndustryPack® compatible carriers. Connection to incompatible hardware is likely to cause serious damage.

TEWS DATEN*TECHNIK* GmbH is not liable for any damage arising out of the application or use of the device described herein.

1. Product Description

The TIP830 family are IndustryPack® compatible moduls providing eight independent channels of high resolution 12-bit (TIP830-10) or 16-bit (TIP830-20) analog-to-digital conversion. Each single channel consists of a sample and hold and a 12-bit or 16-bit A/D converter.

The maximum time for sample and convert is 25 µs for all channels. Full scale input range is ±10 V.

A start-of-conversion is initiated by software command or via the trigger I/O pin. All eight channels of the TIP830 sample and convert simultaneous.

By connecting the trigger I/O pins of several modules it is possible to extend the simultaneous sample and convert feature to several TIP830 modules.

For First-Time-Buyers the engineering kit TIP830-EK is recommended. The engineering kit includes TIP830-DOC, schematics, data sheets, a 50 pin terminal block and a 50 pin flat cable.

The subroutine package (TIP830-SW-x1) provides a high level language C call interface to the hardware.

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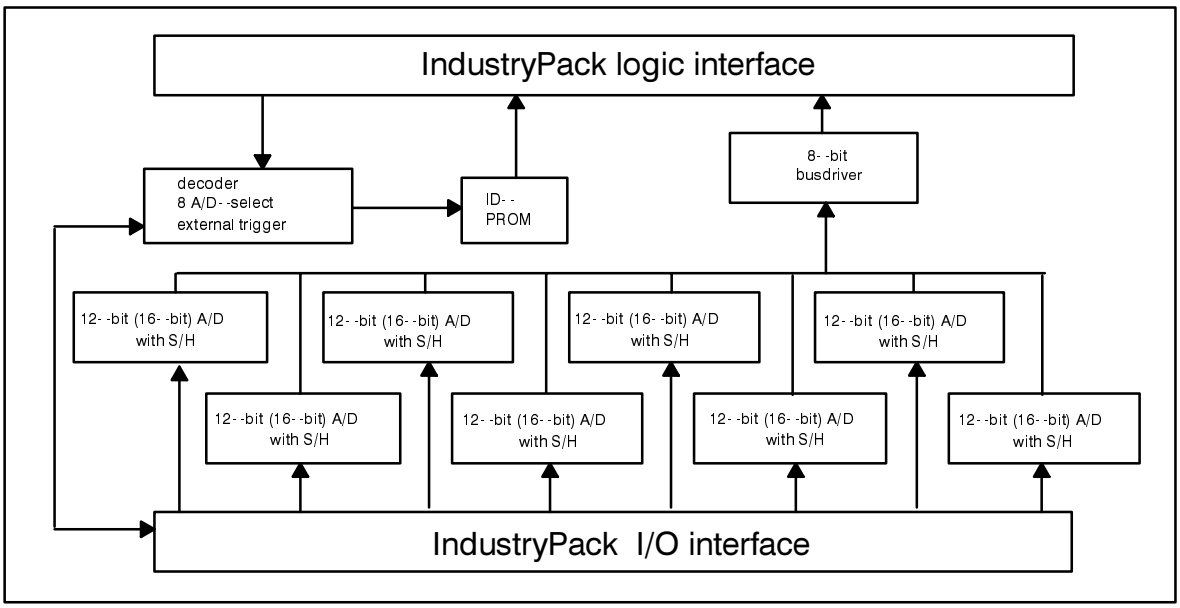

Figure 1: TIP830 Block Diagram

2. Technical Specification

Logic Interface	IndustryPack® Logic Interface
I/O Interface	50-conductor flat cable
Size	single wide IP
Analog Input	8 channels each with independent sample and hold and ADC
Input Voltage Range	±10V
Input Impedance	45 kΩ
Over Voltage	±25V with power on ±10V with power off
ADC Resolution	12 bit (ADS7806) for TIP830-10 16 bit (ADS7807) for TIP830-20
Integral Linearity Error	maximum ±0.9 LSB for TIP830-10 maximum ±3 LSB for TIP830-20
Bipolar Zero Error	maximum ±10mV before data correction
Temperature Drift	±0.5 ppm/°C
Conversion Time	max 25µsec for sample and convert all channels converting simultaneously
Throughput Rate	40k samples per second
Data Correction	factory calibration data for gain and offset correction in ID-PROM
External Trigger	TTL level open collector external trigger I/O pin
Wait States	one wait state for ADC data read no wait states for all other access
Power Reqirements	130mA @ +5V typical 18mA @ +12V typical
Size	single wide IP
Temperature Range	Operating 0°C to 85°C Storage -45°C to 125°C
Humidity	5 - 95% non-condensing

3. ID Prom Contents

ADDRESS	FUNCTION	
$ 01	ASCII 'I'	$ 49
$ 03	ASCII 'P'	$ 50
$ 05	ASCII 'A'	$ 41
$ 07	ASCII 'C'	$ 43
$ 09	Manufacturer ID	$ B3
$ 0B	Model Number	$ 08 for TIP830-10 $ 07 for TIP830-20
$ 0D	Revision	$ 10
$ 0F	RESERVED	$ 00
$ 11	Driver-ID low-byte	$ 00
$ 13	Driver-ID high-byte	$ 00
$ 15	number of bytes used	$ 1C
$ 17	C R C	$ board dependend
$ 19	Offset ADC channel 1	$ board dependend
$ 1B	Offset ADC channel 2	$ board dependend
$ 1D	Offset ADC channel 3	$ board dependend
$ 1F	Offset ADC channel 4	$ board dependend
$ 21	Offset ADC channel 5	$ board dependend
$ 23	Offset ADC channel 6	$ board dependend
$ 25	Offset ADC channel 7	$ board dependend
$ 27	Offset ADC channel 8	$ board dependend
$ 29	Gain ADC channel 1	$ board dependend
$ 2B	Gain ADC channel 2	$ board dependend
$ 2D	Gain ADC channel 3	$ board dependend
$ 2F	Gain ADC channel 4	$ board dependend
$ 31	Gain ADC channel 5	$ board dependend
$ 33	Gain ADC channel 6	$ board dependend
$ 35	Gain ADC channel 7	$ board dependend
$ 37	Gain ADC channel 8	$ board dependend

Figure 2: ID PROM contents

4. VMEbus Addressing

The TIP830 is accessed in the I/O space through the following set of registers:

ADDRESS	NAME	FUNCTION	SIZE
$ 01	DATAH1	Data Bits D08 - D15 channel 1	byte
$ 03	DATAL1	Data Bits D00 - D07 channel 1	byte
$ 05	DATAH2	Data Bits D08 - D15 channel 2	byte
$ 07	DATAL2	Data Bits D00 - D07 channel 2	byte
$ 09	DATAH3	Data Bits D08 - D15 channel 3	byte
$ 0B	DATAL3	Data Bits D00 - D07 channel 3	byte
$ 0D	DATAH4	Data Bits D08 - D15 channel 4	byte
$ 0F	DATAL4	Data Bits D00 - D07 channel 4	byte
$ 11	DATAH5	Data Bits D08 - D15 channel 5	byte
$ 13	DATAL5	Data Bits D00 - D07 channel 5	byte
$ 15	DATAH6	Data Bits D08 - D15 channel 6	byte
$ 17	DATAL6	Data Bits D00 - D07 channel 6	byte
$ 19	DATAH7	Data Bits D08 - D15 channel 7	byte
$ 1B	DATAL7	Data Bits D00 - D07 channel 7	byte
$ 1D	DATAH8	Data Bits D08 - D15 channel 8	byte
$ 1F	DATAL8	Data Bits D00 - D07 channel 8	byte
$ 21	CONCR	Convert Command Register	byte
$ 23	STATR	Status Register	byte

Figure 3: TIP830 Register Map

4.1. ADC Data Register

Each of the ADCs on the TIP830 has two byte wide data register. The DATAHx register holds the upper byte (MSB) of the converted data and DATALx holds the lower byte (LSB). These registers are read only.

For the 12 bit version TIP830-10 the data is returned left shifted by hardware as 16 bit binary two's complement value with data bits D0 to D3 set to zero.

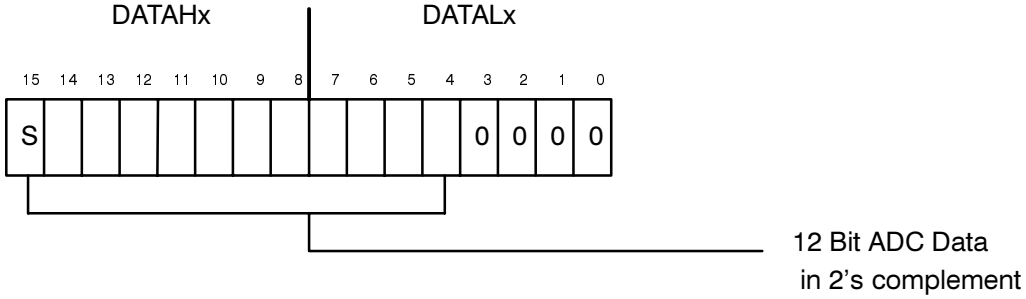

Figure 4: ADC Data Register Alignment for TIP830-10

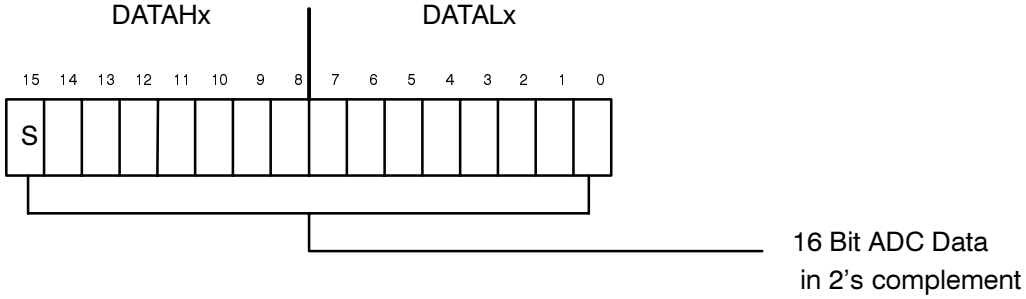

Figure 5: ADC Data Register Alignment for TIP830-20

Note

Only byte access is supported for these registers.

4.2. Control and Status Register

The TIP830 is controlled by the conversion command register CONCR and the status register STATR.

4.2.1. CONCR Conversion Command Register

The Conversion Command Register CONCR is used to start a data conversion at all 8 channels simultaneously. Any write to this register will start the conversion.

Note

The CONCR is a write only register. Any read access to this register will return a random number.

4.2.2. STATR Status Register

The Status Register STATR of the TIP830 is a read only register. Bit 0 of this register holds the ored busy status of all eight ADC's. This bit is '1' as long at least one of the ADCs is busy converting.

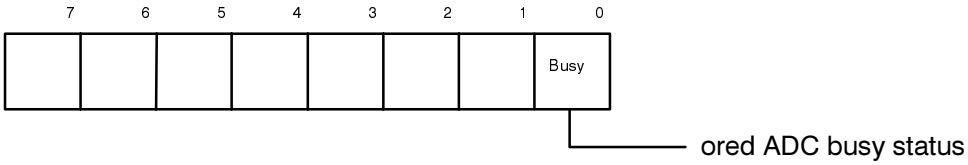

Figure 6: STATR Status Register

Note

The STATR is a read only register. Any write access to this register will have no effect.

5. Functional Description

The TIP830 has eight single ended ADC channels with 12 bit or 16 bit resolution. All eight channels are sampled and converted simultaneously. The minimum throughput is 40k samples per second.

The input voltage range is ±10V. The 12 bit TIP830-10 has a resolution of 4.88mV (1 LSB) and the 16 bit TIP830-20 has a resotution of 305µV (1 LSB).

5.1. Data Aquisition

The data conversion can be started by writing to the Conversion Command Register CONCR or by an high to low transition from an external source at the trigger I/O pin.

More then one TIP830s can have their trigger I/O pins tied together. In this way the number of simultaneous sampling channels can be increased. The trigger I/O signal is a bidirectional signal. A software conversion command by writing the CONCR at one TIP830 will also trigger all other TIP830 which have their trigger I/O signals connected.

5.2. Data Correction

This section of the manual describes how to use the calibration data stored in the ID-PROM to correct the offset and gain error of the ADC's by software.

All errors are considered to be linear. For each of the eight ADC's two correction number are used. One corrects for the offset (or zero) error, and the second corrects for gain (or span) error.

Because the 12 bit data of the TIP830-10 is left aligned into a 16 bit word by hardware, the same scaling and correction algorithms can be used for the TIP830-10 and TIP830-20. The ID-PROM holds all correction numbers in units of 1 LSB of a 16 bit data word. The correction numbers are treated as a signed byte (-128 to +127).

The basic formula for correction is:

$$Data_{corrected} = Data_{ADC} * (1 - PROM_{gain} / 32768) - PROM_{offset}$$

Note

Floating point arithmetic or 32 bit integer arithmetic with normalized data values is nessicary for the gain error correction.

6. IP I/O connector

Pin-Number	Function
01	ADC Input channel 1
02	ADC Input channel 5
03	AGND (channel 1 and 5)
04	ADC Input channel 2
05	ADC Input channel 6
06	AGND (channel 2 and 6)
07	ADC Input channel 3
08	ADC Input channel 7
09	AGND (channel 3 and 7)
10	ADC Input channel 4
11	ADC Input channel 8
12	AGND (channel 4 and 8)
23	GND
24	Trigger I/O (open collector TTL)
25	GND
45	- 12V
46	GND
47	+ 12V
48	GND
49	+ 5V
50	GND

Figure 7: TIP830 IP I/O connector