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TEWS TECHNOLOGIES

TPMC880

Ethernet Interface

Version 1.0

User Manual

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TPMC880-10

10/100Base-T and 10Base2 Ethernet Interface

TPMC880-11

10/100Base-T Ethernet Interface

TPMC880-12

10Base2 Ethernet Interface

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Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

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Table of Contents

1 PRODUCT DESCRIPTION 6
2 TECHNICAL SPECIFICATION 7
3 ETHERNET CONTROLLER INTEL 21143 8
3.1 PCI Configuration Registers 8
3.2 Control and Status Registers (CSRs) 9
4 FUNCTIONAL DESCRIPTION 10
5 MODULE INITIALIZATION 11
5.1 General Purpose Port Settings 11
5.2 Configuration EEPROM 12
6 PHYSICAL INTERFACE 14
6.1 LXT970A Fast Ethernet Transceiver 14
6.2 DP8392A Coax Transceiver 16
7 FRONT PANEL DESCRIPTION 17
7.1 Status LEDs 17
7.2 Pin Assignment – I/O Connector 18
7.2.1 RJ45 I/O Connector 18
7.2.2 BNC Connector 18

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Table of Figures

FIGURE 1-1 : BLOCK DIAGRAM....6
FIGURE 2-1 : TECHNICAL SPECIFICATION....7
FIGURE 3-1 : 21143 PCI CONFIGURATION REGISTERS....8
FIGURE 3-2 : 21143 CONTROL AND STATUS REGISTERS....9
FIGURE 5-1 : PROM CONTENT TPMC880-10....12
FIGURE 5-2 : PROM CONTENT TPMC880-11....12
FIGURE 5-3 : PROM CONTENT TPMC880-12....12
FIGURE 6-1 : LXT970A REGISTERS....15
FIGURE 7-1 : FRONT PANEL CONNECTORS AND LEDS (TPMC880-10)....17
FIGURE 7-2 : RJ45 I/O CONNECTOR....18
FIGURE 7-3 : BNC CONNECTOR....18

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1 Product Description

The TPMC880 is a PCI Mezzanine Card (PMC) compatible module providing a single channel Ethernet Interface.

Three TPMC880 board options are available:

- TPMC880-11: 10/100Base-T Ethernet interface via TP cable / RJ45 connector
- TPMC880-12: 10Base2 Ethernet ("Cheapernet") interface via coax cable / BNC connector
- TPMC880-10: 10/100Base-T and 10Base2 Ethernet interface on one board.

The TPMC880 uses the Intel™ 21143-TD Ethernet controller which supports 10 and 100Mb/s transmission rates for half and full duplex operation via its MII/SYM port and also provides an AUI port for use with external coax transceivers.

For the TPMC880-10/-11 board options the 21143 MII/SYM port connects to a LXT970A Fast Ethernet transceiver device with 10Base-T / 100Base-TX capability. The 10/100Base-T twisted-pair port is galvanically isolated from the LXT970A and the 21143 by an isolation module.

The TPMC880-10/-11 board options are capable of performing auto-negotiation, allowing both link partners to select the best possible link mode.

For the TPMC880-10/-12 board options the 21143 AUI port connects to a DP8392A coax transceiver device for 10Base2. To guarantee overvoltage protection of up to 500Vrms for the 10Base2 BNC interface on the TPMC880-10/-12, the BNC transmission path and the supply voltage is fed over a DC/DC converter and an isolation module to the coax transceiver, which is directly connected to the coax cable.

All TPMC880 board options have front panel mounted LEDs to indicate network status.

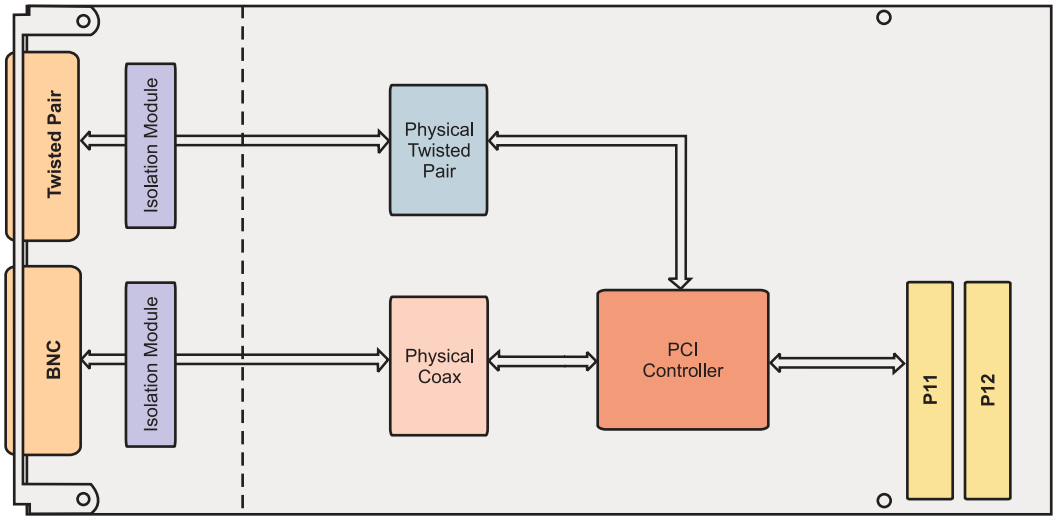


Figure 1-1 : Block Diagram

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2 Technical Specification

PMC Interface		
Mechanical Interface	PCI Mezzanine Card (PMC) Interface Single Size	
Electrical Interface	PCI Rev. 2.1 compliant 33MHz / 32bit PCI 3.3V and 5V PCI Signaling Voltage	
On Board Devices		
Ethernet Controller	21143-TD (Intel)	
100Base-T Transceiver	TPMC880-10/-11 : LXT970-ATC (Intel)	
10Base2 Transceiver	TPMC880-10/-12 : DP8392A (National)	
Board Data		
Physical Interface	TPMC880-10 : 10Base-T / 100Base-TX + 10Base2 TPMC880-11 : 10Base-T / 100Base-TX TPMC880-12 : 10Base2	
I/O Interface	TPMC880-10 : RJ45 (Twisted-Pair) and BNC (Coax) connector TPMC880-11 : RJ45 connector (Twisted-Pair 100 ohms) TPMC880-12 : BNC connector (RG58A/U, Coax 50 ohms)	
Isolation Voltage	TPMC880-10/-12 : 550Vpp TPMC880-11 : 1400Vpp	
Physical Data		
Power Requirements	150mA typical @ +3.3V DC (all TPMC880 options) 600mA typical @ +5V DC (TPMC880-10) 225mA typical @ +5V DC (TPMC880-11) 375mA typical @ +5V DC (TPMC880-12)	
Temperature Range	Operating Storage	0 °C to +70 °C -55°C to +125°C
MTBF	TPMC880-10 : 88661 h TPMC880-11 : 159453 h TPMC880-12 : 161499 h	
Humidity	5 – 95 % non-condensing	
Weight	TPMC880-10 : 78 g TPMC880-11 : 63 g TPMC880-12 : 71 g	

Figure 2-1 : Technical Specification

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3 Ethernet Controller Intel 21143

3.1 PCI Configuration Registers

The 21143 PCI configuration registers are accessible in the PCI configuration space of the PMC slot on which the TPMC880 resides.

Identifier	Offset	Function				PCI writeable
CFID	0x00	Device ID (0x0019)		Vendor ID (0x1011)		N
CFCS	0x04	Status		Command		Y
CFRV	0x08	Class Code			Revision ID	N
CFLT	0x0C	Reserved		Latency Timer	Cache line Size	Y[7:0]
CBIO	0x10	PCI Base Address for I/O Mapped Configuration Registers				Y
CBMA	0x14	PCI Base Address for Memory Mapped Configuration Registers				Y
-	0x18	Reserved				
-	0x1C	Reserved				
-	0x20	Reserved				
-	0x24	Reserved				
CCIS	0x28	Cardbus CIS Pointer				N
CSID	0x2C	Subsystem ID (TPMC880-10 : 0x000A) (TPMC880-11 : 0x000B) (TPMC880-12 : 0x000C)		Subsystem Vendor ID (0x1498)		N
CBER	0x30	PCI Base Address for Local Expansion ROM				Y
CCAP	0x34	Reserved		Reserved	Capabilities Pointer	N
-	0x38	Reserved				N
CFIT	0x3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	Y
CFDD	0x40	Configuration Device and Driver Area Register				Y
CWUA0	0x44	Wake-up LAN Address A-D				Y
CWUA1	0x48	Reserved		Wake-up LAN Address F	Wake-up LAN Address F	Y
SOP0	0x4C	SecureOn Password D	SecureOn Password C	SecureOn Password B	SecureOn Password A	Y
SOP1	0x50	Reserved		SecureOn Password F	SecureOn Password E	Y
CWUC	0x54	Remote Wake-up LAN Command		Remote Wake-up LAN Command		Y
-	0x58-0xD8	Reserved				
CCID	0xDC	Power Management Capabilities		Next Item Pointer	Capabilities Identification	N
CPMC	0xE0	Reserved		Power Management Control and Status		Y

Figure 3-1 : 21143 PCI Configuration Registers

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All wake-up LAN and power management functions are not used on the TPMC880.

For a detailed register description please refer to the 21143 user manual which is part of the TPMC880-ED Engineering Documentation.

3.2 Control and Status Registers (CSRs)

The 21143 Control and Status Registers are accessible in PCI memory or I/O space. The PCI base address for the 21143 Control and Status Registers is defined in offset 0x10 or 0x14 in the 21143 PCI configuration space.

For a detailed register description please refer to the 21143 user manual which is part of the TPMC880-ED Engineering Documentation.

Identifier	Offset	Function
CSR 0	0x00	Bus Mode Register
CSR 1	0x08	Transmit Poll Demand Register
CSR 1 PM	0x08	Wake-up frame filter Register (not used on TPMC880)
CSR 2	0x10	Receive Poll Demand Register
CSR 2 PM	0x10	Wake-up Control and Status (not used on TPMC880)
CSR 3	0x18	Descriptor List Base Address Register
CSR 4	0x20	Descriptor List Base Address Register
CSR 5	0x28	Status Register
CSR6	0x30	Operation Mode Register
CSR 7	0x38	Interrupt Enable Register
CSR 8	0x40	Missed Frames and Overflow Counter Register
CSR 9	0x48	Boot/Serial ROM/MII Management Register
CSR 10	0x50	Boot ROM Programming Address Register
CSR 11	0x58	General Purpose Timer and Interrupt Mitigation Control Register
CSR 12	0x60	SIA Status Register
CSR 13	0x68	SIA Connectivity Register
CSR 14	0x70	SIA Transmit and Receive Register
CSR 15	0x78	SIA and General Purpose Port Register

Figure 3-2 : 21143 Control and Status Registers

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4 Functional Description

The 21143 Ethernet Controller provides a MII/SYM port for 10/100Base-T applications and an AUI port for 10Base2 applications.

On the TPMC880-10/-11 the 21143 MII/SYM port directly connects to the MII interface of a LXT970A Fast Ethernet transceiver. On the TPMC880-10/-12 the 21143 AUI port directly connects to a DP8392A coaxial transceiver.

The software driver configures the Ethernet Controller 21143 soon after power up. Some initial 21143 register settings are loaded automatically from the on board serial EEPROM. Other hardware dependent information (supported network media, supported link speeds, power down features etc.) are read by the software driver from the serial EEPROM for the 21143 configuration. The software driver must also provide memory space for transmit and receive buffers, which will be written or read by the 21143.

The 21143 Ethernet Controller receives/sends data from/to host memory via the PCI bus and sends/receives the converted (framed) data to/from the physical transceiver device, which does the coding for the transmission medium (Twisted-Pair/Coax). The 21143 Ethernet Controller acts as a bus master during DMA cycles to the host memory. After gaining access to the PCI bus the controller is reading transmit data from the buffers in host memory which will be accessed through a list of chained pointers. The first pointer from the list is stored in the CSR4 and must be initialized by the software driver. Also CSR3 must be loaded with the first pointer for the receive buffer list after power up or reset. If there are no free buffers available in host memory, the 21143 Ethernet Controller can generate an interrupt on the PCI bus and will discard any received frames until free buffers are available in host memory. During normal receive operation any data longer than 46 bytes will be transferred from the LAN to the receive buffer. As long as there is enough space in the internal transmit FIFO of the 21143 Ethernet Controller, data from the transmit buffer will be accepted. The driver has to instruct the 21143 Ethernet Controller via the Transmit/ Receive Poll Register (CSR 1, CSR 2) if new data are available in a buffer. The TPMC880 can generate interrupts, if a complete frame is received or transmitted from/to the LAN.

It is possible to set the TPMC880 to a low power consumption mode by setting bit 30 or 31 in the 21143 CFDD Register when the receive/transmit process has stopped.

The LXT970A Fast Ethernet transceiver operation mode can be configured by 21143 Status and Control Registers. The DP8392A coax transceiver can not be configured by software.

The TPMC880 supports the following LAN modes:

TPMC880-10:

- Twisted-Pair with 100Mb/s, full duplex / half duplex operation
- Twisted-Pair with 10Mb/s, full duplex / half duplex operation
- Coax cable with 10Mb/s, half duplex operation

TPMC880-11:

- Twisted-Pair with 100Mb/s, full duplex / half duplex operation
- Twisted-Pair with 10Mb/s, full duplex / half duplex operation

TPMC880-12:

- Coax cable with 10Mb/s, half duplex operation

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5 Module Initialization

5.1 General Purpose Port Settings

On the TPMC880-10/-11 the General Purpose Port of the 21143 Ethernet Controller can be configured by the software driver for the following features:

- General Purpose Port 0: Input, MII interrupt from LXT970A
- General Purpose Port 1: Output, power down LXT970A, high active
- General Purpose Port 2: Output, reset LXT970A, low active
- General Purpose Port 3: Not used

The General Purpose Port 0 can be used by the software driver to determine a LXT970A interrupt if a change of link parameters (transmission rate, full/half duplex, and link failure) has occurred during normal operation. GEP0 interrupts must be enabled in the General Purpose Register CSR15 (offset 0x78) of the 21143 Ethernet Controller and in the LXT970A Interrupt Enable Register (offset 0x11) to use this feature.

The General Purpose Port 1 can be used by the software driver to switch the LXT970A to a low power consumption mode when a '1' is driven on General Purpose Port 1.

The General Purpose Port 2 can be used by the software driver to issue software reset to the LXT970A when a '0' is driven on General Purpose Port 2.

General Purpose Port 3 is not connected on the TPMC880-10/11.

The default General Purpose Configuration data is stored in the serial EEPROM and must be downloaded by the software driver. Further information regarding the EEPROM content can be found in the "Serial ROM Format Guide" which is part of the TPMC880-ED Engineering Documentation.

On the TPMC880-12 the General Purpose Port of the 21143 Ethernet Controller is not used.

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5.2 Configuration EEPROM

During power up some initial 21143 register information are loaded from the on board serial EEPROM (Subsystem ID, Sub vendor ID etc). The EEPROM data also determine the supported media, transfer capabilities, reset sequences for the LXT970A PHY device etc. This information must be read by the software driver to configure the 21143 Ethernet Controller for the desired link connection (Twisted-Pair/BNC, transmission speed, half/full duplex, FIFO threshold etc).

Address	Content							
0x00	0x9814	0x0A00	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
0x10	0xFE00	0x0401	IEEE_2	IEEE_1	IEEE_0	0x001E	0x0000	0x0088
0x20	0x0486	0x0201	0x0E0D	0x0607	0x9703	0x0002	0x0E0D	0x0405
0x30	0x030E	0x0D00	0x0504	0x0500	0x78E0	0x0100	0x5000	0x1801
0x40	0x8805	0x030E	0x0D00	0x0504	0x0589	0x0601	0x030E	0x0D06
0x50	0x0504	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
0x60	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
0x70	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	CRC_0	CRC_1

Figure 5-1 : PROM Content TPMC880-10

Address	Content							
0x00	0x9814	0x0B00	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
0x10	0x1B00	0x0401	IEEE_2	IEEE_1	IEEE_0	0x001E	0x0000	0x0088
0x20	0x0395	0x0300	0x0104	0x0503	0x0E0D	0x0504	0x0500	0x78E0
0x30	0x0100	0x5000	0x1801	0x8805	0x30E0	0x0D00	0x0504	0x0589
0x40	0x0601	0x030E	0x0D06	0x0504	0x0500	0x0000	0x0000	0x0000
0x50	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
0x60	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
0x70	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	CRC_0	CRC_1

Figure 5-2 : PROM Content TPMC880-11

Address	Content							
0x00	0x9814	0x0C00	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
0x10	0xAE00	0x0401	IEEE_2	IEEE_1	IEEE_0	0x001E	0x0000	0x0001
0x20	0x0386	0x0201	0x0E0D	0x0607	0x8405	0x0100	0x0085	0x0601
0x30	0x0100	0x0000	0x0504	0x0000	0x0000	0x0000	0x0000	0x0000
0x40	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
0x50	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
0x60	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
0x70	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	CRC_0	CRC_1

Figure 5-3 : PROM Content TPMC880-12

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IEEE_2: Ethernet address upper word

IEEE_1: Ethernet address middle word

IEEE_0: Ethernet address lower word

CRC_1: SROM CRC higher word

CRC_0: SROM CRC lower word

The serial EEPROM can be accessed through the CSR9 (offset 0x48) of the 21143 Ethernet Controller. Further information regarding the EEPROM access and content can be found in the 21143 Manual and the “Serial ROM Format Guide” which are part of the TPMC880-ED Engineering Documentation.

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6 Physical Interface

6.1 LXT970A Fast Ethernet Transceiver

The LXT970A is a 10Base-T/100Base-TX Ethernet transceiver used for the TPMC880-10/-11 10/100Base-T interface. The LXT970A line signals are fed through a 1:1 transformer module to the RJ45 front panel connector.

The LXT970A provides 12 on-chip Status and Control Registers, accessible by the 21143 Ethernet Controller.

Data transmission between the 21143 and the LXT970A is handled via the Media Indepdent Interface (MII).

The MII-signals used are:

- Transmit data (TXD 0...3)
- Receive data (RXD 0...3)
- Transmit clock (TX_CLK)
- Receive clock (RX_CLK)
- Transmit enable (TX_EN)
- Receive data valid (RX_DV)
- Rx_Error (RX_ER)
- Tx_Error (TX_ER)
- Carrier sense (CRS)
- Collision detect (COL)

LXT970A device configuration and register access is handled by the MII management interface. This serial synchronous interface supports read and write access to the LXT970A internal registers.

The MII management interface supports the following signals:

- Clock (MDC)
- Bidirectional data line (MDIO)
- MDIO interrupt output (MDINT)

After power up, the LXT970A will automatically perform an auto-negotiation algorithm with its link partner to determine the link parameters.

The following transmission rates and modes are supported by the LXT970A:

- 100Mb/s full duplex
- 100Mb/s half duplex
- 10Mb/s full duplex
- 10Mb/s half duplex

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The LXT970A will set bit 9 in the Chip Status Register (offset 0x14) if auto-negotiation is finished. The software driver can then read the Chip Status Register, bits 11 and 12 to detect link speed and duplex mode. To initialize the 21143 Ethernet Controller, this information must be written to the Operation Mode Register CSR6 (offset 0x30) of the 21143 Ethernet Controller.

The LXT970A supports monitoring status via LEDs on the TPMC880 front panel.

The LEDs signal the following events :

- 100Mb/s on/off (speed status)
- Link status (connection status)
- Transmit activity
- Receive activity

The LXT970A can issue a low activ interrupt to the 21143 Ethernet Controller on its MII port via the MDINT pin, if interrupts are enabled in the Interrupt Enable Register (offset 0x11) of the LXT970A and in the General Purpose Control Register CSR15 (offset 0x78) of the 21143. This interrupt can be used to indicate that the link parameters have been changed or that the link has failed during normal operation. This feature may be used by software drivers for auto-sensing a change of link parameters during operation (without resetting the module). To determine the interrupt source the software driver has to read the Status Register (offset 01) of the LXT970A .

The LXT970A can be configured by software driver through the Control Register (offset 0x00).

Following figure shows the LXT970A registers.

Operation	Address Offset	Function
R/W	0x0	Control Register
R	0x1	Status Register
R	0x2	PHY Identification Register 1
R	0x3	PHY Identification Register 2
R/W	0x4	Auto-Negotiation Advertisement Register
R	0x5	Auto-Negotiation Link Partner Ability Register
R	0x6	Auto-Negotiation Expansion Register
R/W	0x10h	Mirror Register
R/W	0x11h	Interrupt Enable Register
R	0x12h	Interrupt Status Register
R/W	0x13h	Configuration Register
R	0x14h	Chip Status Register

Figure 6-1 : LXT970A Registers

All LXT970A registers can be accessed through CSR 9 of the 21143 Ethernet Controller by sequentially writing data bits to bit 17 or sequentially reading data bits from bit 19 (serial synchronous data transmission). Bit 16 must be toggled for generating the clock signal for each LXT970A register access. Bit 18 defines the operation mode. For read access bit 18 should be set to ‘1’, for write access bit 18 should be set to ‘0’. During read operations the incoming data on bit 19 is sampled on the rising edge of the clock signal provided with bit 16.

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The registers are accessible via the MII management interface port of the 21143 Ethernet Controller. To access a LXT970A register, it is necessary to provide a serial data stream in a frame structure on the MDIO pin. The frame implements a 32 bit preamble (all “1”), a frame delimiter (“01”), an opcode (“10”: read register, “01”: write register), a 5 bit device address (hardwired to “00000”), and a 5 bit register address offset (0x0 ... 0x14). During write operations 16 bit data can be passed to the LXT970A after a turnaround cycle (2 MDC clock cycles).

For a detailed description please refer to the LXT970A datasheet which is part of the TPMC880-ED Engineering Documentation.

6.2 DP8392A Coax Transceiver

The DP8392A is a coaxial transceiver and is connected to the AUI port of the 21143 Ethernet Controller. The 21143 AUI port provides 10Mb/s serial Manchester encoded data and the following three differential signal pairs:

- Transmit data (TX+ / TX-)
- Receive data (RX+ / RX-)
- Collision detected (CD+ / CD-)

The 21143 AUI port signals are fed through a 1:1 transformer module to provide overvoltage protection. For the same reason the supply voltage for the DP8392A is generated from a DC/DC converter. The DP8392A connects directly to the RG58A/U coax cable via the standard BNC-T connector.

Note that the coax cable segment length shouldn’t be greater than 185 m, to guarantee that the DP8392A is not receiving or sending poor quality signals.

Make sure that the BNC cable is properly terminated with a 50 ohms resistor on each end of the cable segment.

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7 Front Panel Description

7.1 Status LEDs

The front panel status LEDs indicate the following states:

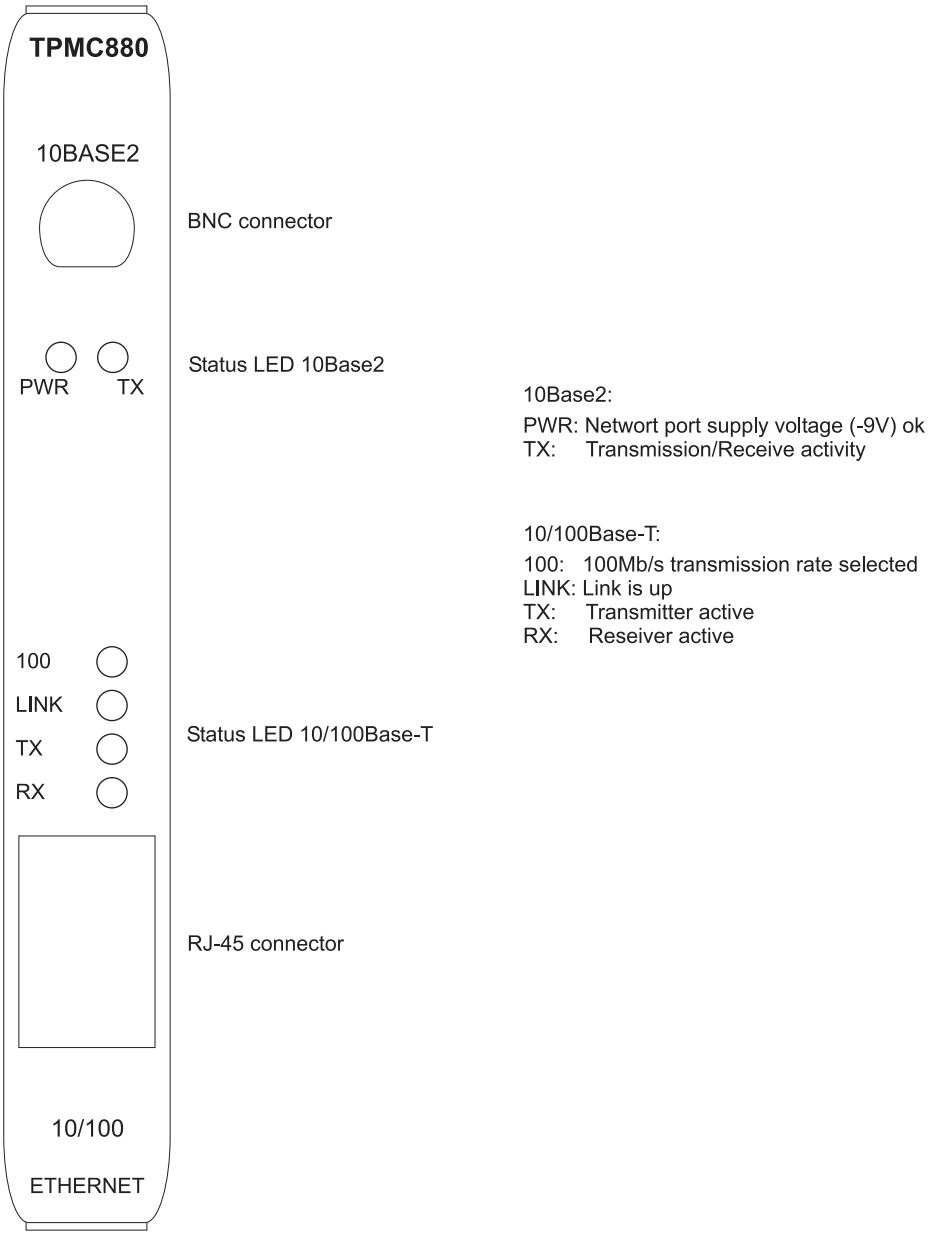


Figure 7-1 : Front panel connectors and LEDs (TPMC880-10)

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7.2 Pin Assignment – I/O Connector

7.2.1 RJ45 I/O Connector

Pin	Function
1	Transmit data +
2	Transmit data -
3	Receive data +
4	Not used
5	Not used
6	Receive data -
7	Not used
8	Not used

Figure 7-2 : RJ45 I/O Connector

The RJ45 shield connects to the TPMC880 front panel.

7.2.2 BNC Connector

The BNC connector center pin is directly connected to the data input and output pin of the DP8392A coax transceiver device. The BNC connector shield is connected to the collision detect pin of the DP8392A and to the separated ground potential of the BNC port. Conforming to IEEE802.3 the BNC connector shield provides a high voltage discharge path to front panel potential.

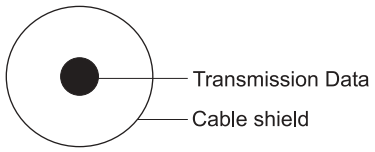


Figure 7-3 : BNC connector

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