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TEWS TECHNOLOGIES

TPMC901

6/4/2 Channel Extended CAN Bus

PMC Module

Version 1.0

User Manual

Issue 1.3

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TPMC901-10

6 channel extended CAN bus PMC module

TPMC901-11

4 channel extended CAN bus PMC module

TPMC901-12

2 channel extended CAN bus PMC module

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Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

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1 Product Description

The TPMC901 is a PCI Mezzanine Card (PMC) compatible module. The TPMC901-10 provides six complete CAN bus interfaces using six Intel 82527 CAN controllers. Additionally to the standard data and remote frame, all channels support the extended data and remote frame according to the CAN specification 2.0 part A and B (standard 11 bit identifier and extended 29 bit identifier). All channels have the capability to transmit, receive and perform message filtering on extended and standard messages.

Each channel supports CAN High Speed according to ISO11898 as the physical interface. The bus line termination is selectable by a jumper separate for each bus line pair. The data transfer rates of up to 1 Mbps are supported for a bus line length of 40 m. The TPMC901-11 supports only four CAN bus channels and the TPMC901-12 has two CAN bus channels.

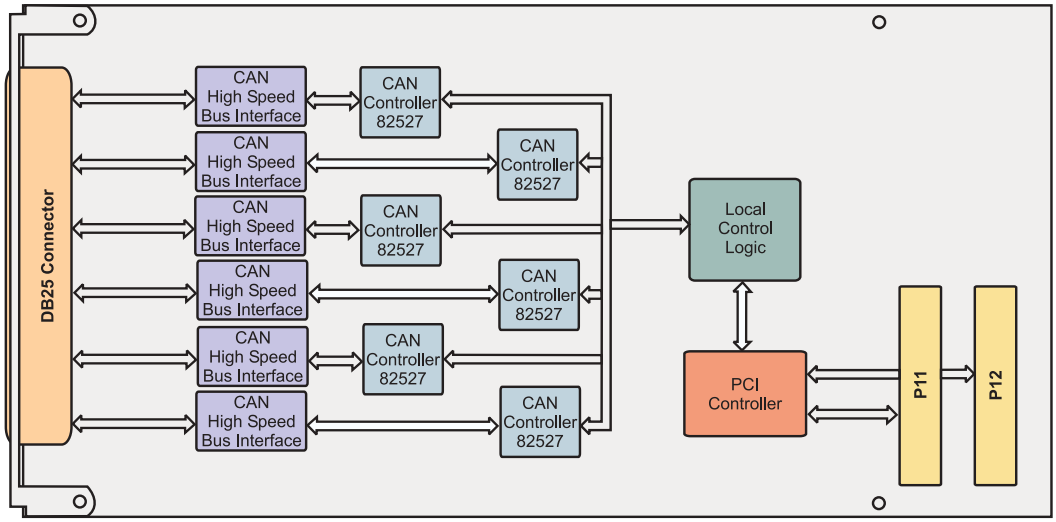


Figure 1-1 : Block Diagram

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2 Technical Specification

PMC Interface		
Mechanical Interface	PCI Mezzanine Card (PMC) Interface Single Size	
PCI Signaling Voltage	5V	
PCI Target Chip	PCI9050-1 (PLX Technology)	
CAN Controller	Intel 82527	
Physical Interface	CAN High Speed (according to ISO 11898)	
Bus Line Termination	On board 120 ohms, selectable by jumper for each channel	
Transfer Rate	1Mbit/s maximum (bus line length up to 40m)	
I/O Interface		
Number of Channels	TPMC901-10: 6 channels TPMC901-11: 4 channels TPMC901-12: 2 channels	
I/O Connector	1 DB25 male connector (all modules)	
Physical Data		
Power Requirements	TPMC901-10: 685mA typical @ +5V DC TPMC901-11: 505mA typical @ +5V DC TPMC901-12: 325mA typical @ +5V DC	
Temperature Range	Operating Storage	0 °C to +70 °C -55°C to +125°C
MTBF	TPMC901-10: 378144 h TPMC901-11: 446368 h TPMC901-12: 544630 h	
Humidity	5 – 95 % non-condensing	
Weight	85 g	

Figure 2-1 : Technical Specification

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3 TPMC901 Local Space Addressing

3.1 PCI9050 Local Space Configuration

The local on board addressable regions are accessed from the PCI side by using the PCI9050 local spaces.

PCI9050 Local Space	PCI9050 PCI Base Address (Offset in PCI Configuration Space)	PCI Space Mapping	Size (Byte)	Port Width (Bit)	Endian Mode	Description
0	0 (0x10)	MEM	128	32	LITTLE	Local Configuration Registers
1	1(0x14)	I/O	128	32	LITTLE	Local Configuration Registers
2	2 (0x18)	MEM	s.b.	8	LITTLE	Local Address Space 0
3	3 (0x1C)	I/O	4	8	LITTLE	Local Address Space 1
4	4 (0x20)	-	-	-	-	Local Address Space 2
5	5 (0x24)	-	-	-	-	Local Address Space 3
6	6 (0x30)	-	-	-	-	Local Expansion ROM Space

Figure 3-1 : PCI9050 Local Space Configuration

Size of Local Address Space 0:	TPMC901-10	2048	byte
	TPMC901-11	1024	byte
	TPMC901-12	512	byte

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3.2 Local Address Space 0

The complete register sets of the CAN controllers of the TPMC901-xx are accessible in the memory space of the PMC module.

Address range: PCI Base Address 2 for Local Address Space 0 + (0x0000 to 0x05FF)

The TPMC901-10 uses all six channels (CANCH0 to CANCH5). The TPMC901-11 uses only the channels CANCH0 to CANCH3 and the TPMC901-12 uses only the channels CANCH0 and CANCH1.

CAN controller channel 0 CANCH0:	PCI Base Address 2 + (0x0000 to 0x00FF)
CAN controller channel 1 CANCH1:	PCI Base Address 2 + (0x0100 to 0x01FF)
CAN controller channel 2 CANCH2:	PCI Base Address 2 + (0x0200 to 0x02FF)
CAN controller channel 3 CANCH3:	PCI Base Address 2 + (0x0300 to 0x03FF)
CAN controller channel 4 CANCH4:	PCI Base Address 2 + (0x0400 to 0x04FF)
CAN controller channel 5 CANCH5:	PCI Base Address 2 + (0x0500 to 0x05FF)

For more information about the register sets of the CAN controller refer to the data sheet of the 82527 Serial Communication Controller which is part of the TPMC901-ED Engineering Documentation.

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3.2.1 CAN Controller Address Map

Following figure shows the Address Offset of CAN Controller Register for the TPMC901-xx.

Register Offset	Function
0x00	Control Register
0x01	Status Register
0x02	CPU Interface Register
0x03	Reserved
0x04 – 0x05	High Speed Read Register
0x06 – 0x07	Global Mask – Standard
0x08 – 0x0B	Global Mask – Extended
0x0C – 0x0F	Message 15 Mask
0x10 – 0x1E	Message 1
0x1F	CLKOUT Register
0x20 – 0x2E	Message 2
0x2F	Bus Configuration Register
0x30 – 0x3E	Message 3
0x3F	Bit Timing Register 0
0x40 – 0x4E	Message 4
0x4F	Bit Timing Register 1
0x50 – 0x5E	Message 5
0x5F	Interrupt Register
0x60 – 0x6E	Message 6
0x6F	Reserved
0x70 – 0x7E	Message 7
0x7F	Reserved
0x80 – 0x8E	Message 8
0x8F	Reserved
0x90 – 0x9E	Message 9
0x9F	P1CONF
0xA0 – 0xAE	Message A
0xAF	P2CONF
0xB0 – 0xBE	Message B
0xBF	P1IN
0xC0 – 0xCE	Message C
0xCF	P2IN
0xD0 – 0xDE	Message D
0xDF	P1OUT
0xE0 – 0xEE	Message E
0xEF	P2OUT
0xF0 – 0xFE	Message F
0xFF	Serial Reset Address

Figure 3-2 : CAN Controller Address Map TPMC901-xx

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3.3 Local Address Space 1

The interrupt status register of the TPMC901 is accessible in the I/O space of the PMC module. **Address range:** PCI Base Address 3 for Local Address Space 1 + 0x0000.

3.3.1 Interrupt Status Register

All CAN controllers generate interrupts at pin INTA# of the PCI bus. The interrupt status can be read at the Interrupt Status Register STATREG. It is accessible through the PCI Base Address 3 for Local Address Space 1 + 0x0000.

The Interrupt Status Register is a byte wide read register.

Bit	Symbol	Description	Access	Reset Value
7:6		Always read as '1'	R	
5	CAN5	Interrupt Status of all six channels 0 = indicates interrupt is pending on corresponding channel TPM901-10: uses bits 0 to bit 5 TPMC901-11: uses only bit 0 to bit 3 (the bit 4 to bit 7 are always '1') TPMC901-12: uses the bit 0 and bit 1 (the remaining bits are always '1')	R	
4	CAN4			
3	CAN3			
2	CAN2			
1	CAN1			
0	CAN0			

Figure 3-3 : Interrupt Status Register STATREG

If the PCI Interrupt Enable of the PCI target chip is disabled (INTCSR bit 6 is set to '0') the Interrupt Status Register STATREG can be used as a polling register for interrupts of the CAN controllers.

For disabling the PCI interrupts change only bit 6 of the Interrupt Control/Status Register INTCSR. Do not change any other bit of this register.

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4 PCI 9050 Target Chip

4.1 PCI Configuration (CFG) Registers

4.1.1 PCI Header of the TPMC901

PCI CFG Register Address	Write '0' to all unused (Reserved) bits				PCI write able	Read after Reset (Hex Value)	Read after initialization write access (Hex Value)
	31 24	23 16	15 8	7 0			
0x00	Device ID (Target Chip PCI 9050-1)		Vendor ID (PLX – Technology)		N	9050 10B5	9050 10B5
0x04	Status		**Command**		Y	0280 0000	0280 0000
0x08	Class Code			Revision ID	N	028000 XX	028000 XX
0x0C	BIST	Header Type	PCI Latency Timer	Cache line Size	Y[7:0]	00 00 00 00	00 00 00 00
0x10	**PCI Base Address 0 for Memory Mapped Configuration Registers**				Y	00000000	FFFFFF80
0x14	**PCI Base Address 1 for I/O Mapped Configuration Registers**				Y	00000001	FFFFFF81
0x18	**PCI Base Address 2 for Local Address Space 0**				Y	00000000	FFFFF800
0x1C	**PCI Base Address 3 for Local Address Space 1**				Y	00000000	FFFFFFFD
0x20	PCI Base Address 4 for Local Address Space 2				Y	00000000	00000000
0x24	PCI Base Address 5 for Local Address Space 3				Y	00000000	00000000
0x28	Cardbus CIS Pointer				N	00000000	00000000
0x2C	Subsystem ID (TPMC901)		Subsystem Vendor ID (TEWS TECHNOLOGIES GmbH)		N	0385 1498	0385 1498
0x30	PCI Base Address for Local Expansion ROM				Y	00000000	00000000
0x34	Reserved				N	00000000	00000000
0x38	Reserved				N	00000000	00000000
0x3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	Y[7:0]	00 00 01 00	00 00 01 00

Figure 4-1 : PCI Configuration Register Map

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4.1.2 PCI Base Address Initialization

PCI Base Address Initialization is scope of the PCI host software.

PCI9050 PCI Base Address Initialization:

1. Write 0xFFFF_FFFF to the PCI9050 PCI Base Address Register.
2. Read back the PCI9050 PCI Base Address Register.
3. For PCI Base Address Registers 0:5, check bit 0 for PCI Address Space.

   Bit 0 = '0' requires PCI Memory Space mapping

   Bit 0 = '1' requires PCI I/O Space mapping

   For the PCI Expansion ROM Base Address Register, check bit 0 for usage.

   Bit 0 = ‘0’: Expansion ROM not used

   Bit 0 = ‘1’: Expansion ROM used
4. For PCI I/O Space mapping, starting at bit location 2, the first bit set determines the size of the required PCI I/O Space size.

   For PCI Memory Space mapping, starting at bit location 4, the first bit set to '1' determines the size of the required PCI Memory Space size.

   For PCI Expansion ROM mapping, starting at bit location 11, the first bit set to '1' determines the required PCI Expansion ROM size.

   For example, if bit 5 of a PCI Base Address Register is detected as the first bit set to ‘1’, the PCI9050 is requesting a 32 byte space (address bits 4:0 are not part of base address decoding).
5. Determine the base address and write the base address to the PCI9050 PCI Base Address Register. For PCI Memory Space mapping the mapped address region must comply with the definition of bits 3:1 of the PCI9050 PCI Base Address Register.

After programming the PCI9050 PCI Base Address Registers, the software must enable the PCI9050 for PCI I/O and/or PCI Memory Space access in the PCI9050 PCI Command Register (Offset 0x04). To enable PCI I/O Space access to the PCI9050, set bit 0 to '1'. To enable PCI Memory Space access to the PCI9050, set bit 1 to '1'.

For further information please refer to the PCI9050-1 manual which is also part of the TPMC901-ED Engineering Documentation.

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4.2 Local Configuration Register (LCR)

After reset, the PCI9050 Local Configuration Registers are loaded from the on board serial configuration EEPROM.

The PCI base address for the PCI9050 Local Configuration Registers is PCI9050 PCI Base Address 0 (PCI Memory Space) (Offset 0x10 in the PCI9050 PCI Configuration Register Space) or PCI9050 PCI Base Address 1 (PCI I/O Space) (Offset 0x14 in the PCI9050 PCI Configuration Register Space).

Do not change hardware dependent bit settings in the PCI9050 Local Configuration Registers.

Offset from PCI Base Address	Register	Value	Description
0x00	Local Address Space 0 Range	0x0FFFF800	Memory Space 6x CAN Controller
0x04	Local Address Space 1 Range	0x0FFFFFFD	Interrupt Status Register
0x08	Local Address Space 2 Range	0x00000000	Not used
0x0C	Local Address Space 3 Range	0x00000000	Not used
0x10	Local Exp. ROM Range	0x00000000	Not used
0x14	Local Re-map Register Space 0	0x00000001	Enabled, local 0x0000
0x18	Local Re-map Register Space 1	0x00000801	Enabled, local 0x0800
0x1C	Local Re-map Register Space 2	0x00000000	Not used
0x20	Local Re-map Register Space 3	0x00000000	Not used
0x24	Local Re-map Register ROM	0x00000000	Not used
0x28	Local Address Space 0 Descriptor	0x80307802	Local Timing, 6x CAN Controller
0x2C	Local Address Space 1 Descriptor	0x00000080	Local Timing, Interrupt Status Register
0x30	Local Address Space 2 Descriptor	0x00000000	Not used
0x34	Local Address Space 3 Descriptor	0x00000000	Not used
0x38	Local Exp. ROM Descriptor	0x00000000	Not used
0x3C	Chip Select 0 Base Address	0x00000401	Chip select 6x CAN
0x40	Chip Select 1 Base Address	0x00000803	Chip select Interrupt Status Register
0x44	Chip Select 2 Base Address	0x00000000	Not used
0x48	Chip Select 3 Base Address	0x00000000	Not used
0x4C	Interrupt Control/Status	0x00000043	Interrupt Configuration
0x50	Miscellaneous Control Register	0x00780000	Retry Delay = max.

Figure 4-2 : PCI9050 Local Configuration Register

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4.3 Configuration EEPROM

After power-on or PCI reset, the PCI9050 loads initial configuration register data from the on board configuration EEPROM.

The configuration EEPROM contains the following configuration data:

- Address 0x00 to 0xOF : PCI9050 PCI Configuration Register Values
- Address 0x10 to 0x64 : PCI9050 Local Configuration Register Values
- Address 0x65 to 0x7E : Not used
- Address 0x7F : TPMC variant

See the PCI9050 Manual for more information.

Address	Offset							
	0x00	0x02	0x04	0x06	0x08	0x0A	0x0C	0x0E
0x00	0x9050	0x1498	0x0280	0x0000	0x0385	0x1498	0x0000	0x0100
0x10	0x0FFF	s.b.	0x0FFF	0xFFFD	0x0000	0x0000	0x0000	0x0000
0x20	0x0000	0x0000	0x0000	0x0001	0x0000	0x0801	0x0000	0x0000
0x30	0x0000	0x0000	0x0000	0x0000	0x8030	0x7802	0x0000	0x0080
0x40	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	s.b.
0x50	0x0000	0x0803	0x0000	0x0000	0x0000	0x0000	0x0000	0x0043
0x60	0x0078	0x0000	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0x70	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	s.b.

Figure 4-3 : Configuration EEPROM TPMC901-xx

LSW of Range for PCI to Local Address Space 0 (Offset 0x12):	TPMC901-10	0xF800
	TPMC901-11	0xFD00
	TPMC901-12	0xFE00
LSW of Chip Select (CS0) (Offset 0x4E):	TPMC901-10	0x0401
	TPMC901-11	0x0201
	TPMC901-12	0x0101
Subsystem-ID Value (Offset 0x7E):	TPMC901-10	0x000A
	TPMC901-11	0x000B
	TPMC901-12	0x000C

For changing these configuration values and more details about the EEPROM please refer to the PLX9050-1 data sheet which is part of the TPMC901-ED Engineering Documentation.

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5 Configuration Hints

5.1 PCI Interrupt Control/Status

All CAN controllers generate interrupts at pin INTA# of the PCI bus. The interrupt status can be read at the Interrupt Status Register STATREG.

The interrupts can be disabled by setting bit 6 to '0' in the PCI Interrupt Control/Status Register INTCSR.

Bit	Symbol	Description	Access	Reset Value
31:8		unused	R	0
7		Software Interrupt	R/W	0
6		PCI Interrupt Enable	R/W	1
5		Local Interrupt 2 Status	R	0
4		Local Interrupt 2 Polarity	R/W	0
3		Local Interrupt 2 Enable	R/W	1
2		Local Interrupt 1 Status	R	0
1		Local Interrupt 1 Polarity	R/W	0
0		Local Interrupt 1 Enable	R/W	1

Figure 5-1 : Interrupt Control/Status Register INTCSR (Address 0x4C)

5.2 CAN Controller Hardware Initialization

Before reading or writing to any of the CAN controller of the TPMC901, the user must initialize the clock registers of each CAN controller chip. It is necessary to do this in a specific order: Starting with CAN controller channel 0, then channel 1, channel 2, channel 3, channel 4 and, finally channel 5.

The following figure lists the hardware initialization required for each CAN controller of the TPMC901.

It is absolutely necessary to initialize the CAN controller of the TPMC901 in the following order: Ch0, Ch1, Ch2, Ch3, Ch4, and Ch5.

Register	Channel_ Base + Address	DATA	Decryption
Control Register	0x00	0x40	Change Configuration Enable
CPU Interface Register	0x02	0x01	Clock divider = 1
CLKOUT Register	0x1F	0x20	CLOUT = 8MHz

Figure 5-2 : Required Hardware Initialization

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5.3 Local Software Reset

The PCI9050 Local Reset Output LRESETo# is used to reset the on board local logic.

The PCI9050 local reset is active during PCI reset or if the PCI Adapter Software Reset bit is set in the PCI9050 local configuration register CNTRL (offset 0x50).

CNTRL[30] PCI Adapter Software Reset:

Value of '1' resets the PCI9050 and issues a reset to the Local Bus (LRESETo# asserted). The PCI9050 remains in this reset condition until the PCI Host clears this bit. The contents of the PCI9050 PCI and Local Configuration Registers are not reset. The PCI9050 PCI Interface is not reset.

5.4 Big / Little Endian

- PCI – Bus (Little Endian)

Byte 0	AD[7..0]
Byte 1	AD[15..8]
Byte 2	AD[23..16]
Byte 3	AD[31..24]

- Every Local Address Space (0...3) and the Expansion ROM Space can programmed to operate in Big or Little Endian Mode.

Big Endian		**Little Endian**	
32 Bit		**32 Bit**	
Byte 0	D[31..24]	Byte 0	D[7..0]
Byte 1	D[23..16]	Byte 1	D[15..8]
Byte 2	D[15..8]	Byte 2	D[23..16]
Byte 3	D[7..0]	Byte 3	D[31..24]
16 Bit upper lane		**16 Bit**	
Byte 0	D[31..24]	Byte 0	D[7..0]
Byte 1	D[23..16]	Byte 1	D[15..8]
16 Bit lower lane			
Byte 0	D[15..8]		
Byte 1	D[7..0]		
8 Bit upper lane		**8 Bit**	
Byte 0	D[31..24]	Byte 0	D[7..0]
8 Bit lower lane			
Byte 0	D[7..0]		

Figure 5-3 : Local Bus Little/Big Endian

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Standard use of the TPMC901:

Local Address Space 0	8 bit bus in Little Endian Mode
Local Address Space 1	not used
Local Address Space 2	not used
Local Address Space 3	not used
Expansion ROM Space	not used

To change the Endian Mode use the Local Configuration Registers for the corresponding Space. Bit 24 of the according register sets the mode. A value of 1 indicates Big Endian and a value of 0 indicates Little Endian.

For further information please refer to the PCI9050 manual which is also part of the TPMC901-ED Engineering Documentation.

Use the PCI Base Address 0 + Offset or PCI Base Address 1 + Offset:

Short cut Offset	Name	
LAS0BRD	0x28	Local Address Space 0 Bus Region Description Register
LAS1BRD	0x2C	Local Address Space 0 Bus Region Description Register
LAS2BRD	0x30	Local Address Space 0 Bus Region Description Register
LAS3BRD	0x34	Local Address Space 0 Bus Region Description Register
EROMBRD	0x38	Expansion ROM Bus Region Description Register

You could also use the PCI - Base Address 1 I/O Mapped Configuration Registers.

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6 Installation TPMC901

6.1 CAN Bus Termination

Each end of a CAN bus must be terminated by a 120ohms resistor between the CAN bus lines CAN high and CAN low.

This termination could be activated by installing jumper on the jumper field ‘J3’:

Jumper J3 (1-2) installed:	Bus line termination for CAN bus channel 0 active
Jumper J3 (3-4) installed:	Bus line termination for CAN bus channel 1 active
Jumper J3 (5-6) installed:	Bus line termination for CAN bus channel 2 active
Jumper J3 (7-8) installed:	Bus line termination for CAN bus channel 3 active
Jumper J3 (9-10) installed:	Bus line termination for CAN bus channel 4 active
Jumper J3 (11-12) installed:	Bus line termination for CAN bus channel 5 active

Factory setting for J3 is bus line termination active for all channels.

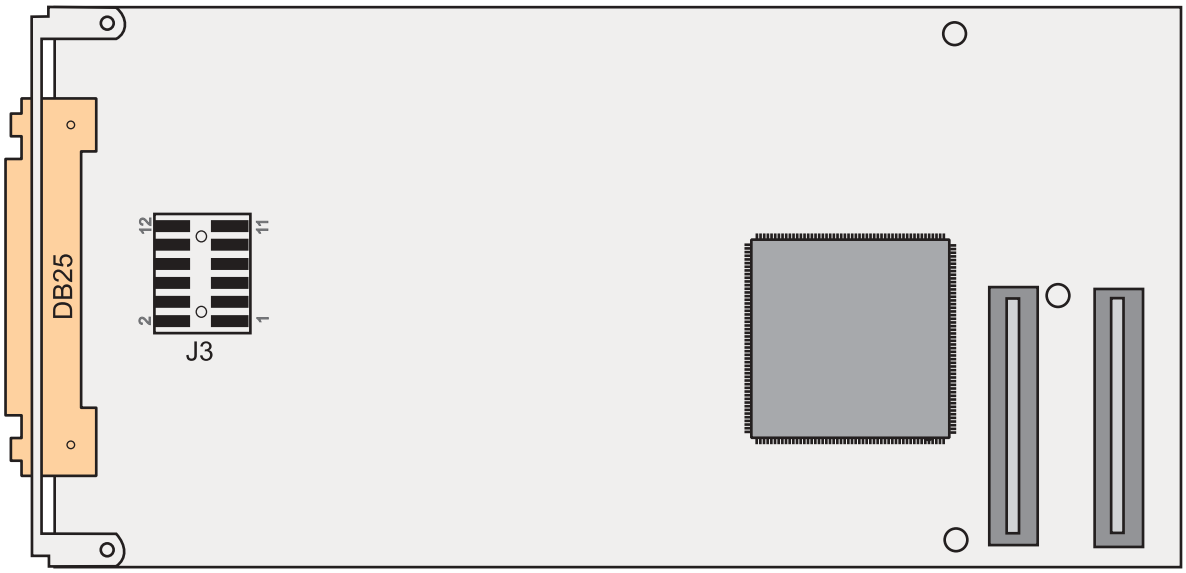


Figure 6-1 : Jumper Location

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7 Pin Assignment

7.1 Front Panel I/O

Pin	Function		
	TPMC901-10	TPMC901-11	TPMC901-12
01	GND	GND	GND
14	CAN Low Channel 0	CAN Low Channel 0	CAN Low Channel 0
02	CAN High Channel 0	CAN High Channel 0	CAN High Channel 0
15	GND	GND	GND
03	GND	GND	GND
16	CAN Low Channel 1	CAN Low Channel 1	CAN Low Channel 1
04	CAN High Channel 1	CAN High Channel 1	CAN High Channel 1
17	GND	GND	GND
05	GND	GND	NC
18	CAN Low Channel 2	CAN Low Channel 2	NC
06	CAN High Channel 2	CAN High Channel 2	NC
19	GND	GND	NC
07	GND	GND	NC
20	CAN Low Channel 3	CAN Low Channel 3	NC
08	CAN High Channel 3	CAN High Channel 3	NC
21	GND	GND	NC
09	GND	NC	NC
22	CAN Low Channel 4	NC	NC
10	CAN High Channel 4	NC	NC
23	GND	NC	NC
11	GND	NC	NC
24	CAN Low Channel 5	NC	NC
12	CAN High Channel 5	NC	NC
25	GND	NC	NC
13	NC	NC	NC

Figure 7-1 : DB25 Male Connector

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