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TEWS TECHNOLOGIES

TVME8240

Single Board Computer

with IndustryPack® Interface

Version 1.2

User Manual

Issue 1.2.9

December 2009

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TVME8240

Single Board Computer with IndustryPack Interface

Available Board Options :

TMVE8240-11

MPC8240 250 MHz, 64 MB SDRAM,
1 + 8 MB FLASH, Fast Ethernet,
Front Panel I/O

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Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

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1 Introduction

The TVME8240 is a VME single slot Single Board Computer (SBC) using the Motorola MPC8240 Embedded PowerPC Processor.

The board provides four single IndustryPack (IP) slots supporting single and double-sized IP modules running at 8 MHz or 32 MHz and front I/O ribbon cable connectors.

1.1 Features

Processor	MPC8240 Embedded PowerPC Processor (Timer, DMA, I2C, Interrupt Controller)
FLASH Memory	1 Mbyte 8 bit wide socket Boot FLASH 8 Mbyte 64 bit wide on board Memory FLASH
System Memory	64 Mbyte 64 bit wide Synchronous DRAM
LAN Interface	21143 10/100Base-TX Ethernet Controller 21143 MII Port & LXT970 Fast Ethernet Transceiver for RJ45 10/100Base-TX 21143 AUI Port for VME P2 10Base-T
IndustryPack Interface	Four single-sized / Two double-sized Industry Pack modules (16 bit) supported 8 MHz / 32 MHz selectable for each slot Front I/O ribbon cable connectors
PCI Expansion Capability	PMC-Span support
NVRAM & RTC	8 Kbyte (M48T59 device)
Asynchronous Serial Interface	One fix RS232 Port (DB9, VME P2) One RS232/RS422 Adapter Port (DB9, VME P2) (RS232 Default)
Miscellaneous	RESET switch ABORT switch Front panel status indicators
Form Factor	Standard 6U VME

Table 1-1 : Features TVME8240

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1.2 Block Diagram

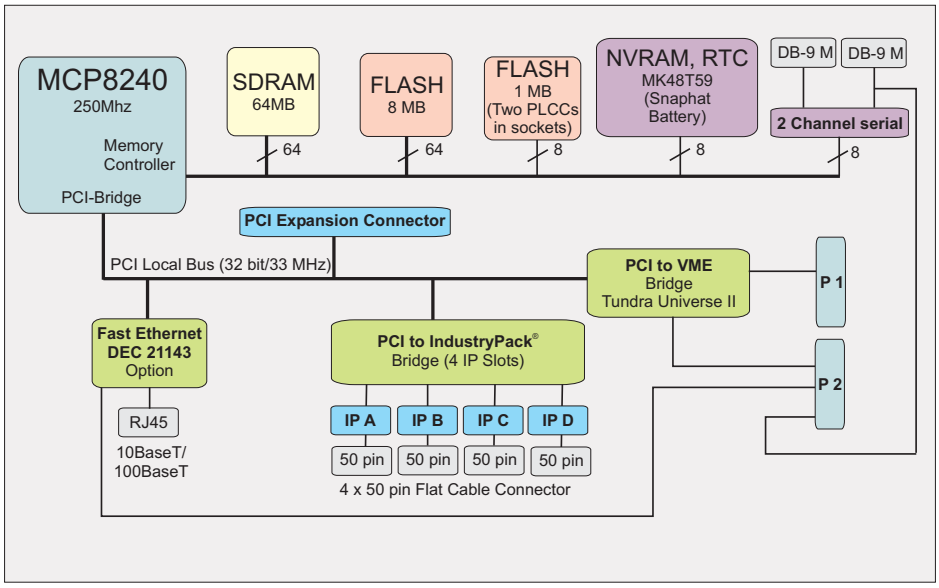


Figure 1-1 : Block Diagram TVME8240 Front I/O

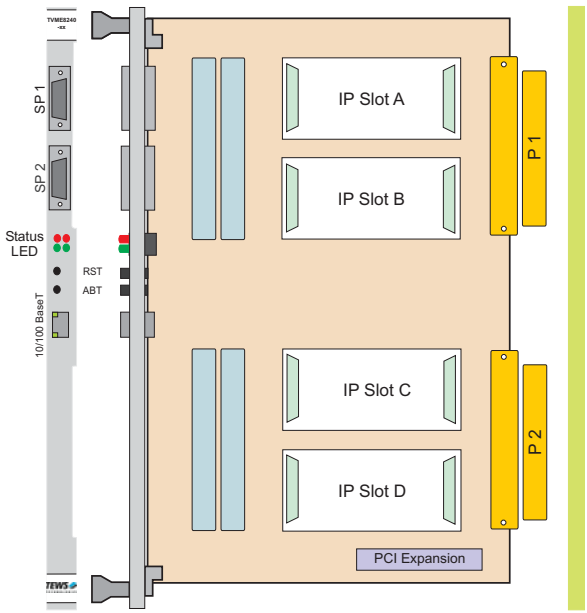


Figure 1-2 : Block Diagram TVM8240 Board Layout Front I/O

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2 Description

2.1 Processor

The TVME8240 uses the Motorola MPC8240 Embedded PowerPC processor.

2.2 Local Memory Bus

The TVME8240 uses the MPC8240 integrated memory controller for accessing the local memory devices.

The TVME8240 provides the following devices on the local memory bus:

- Board mounted Memory FLASH (8 Mbyte, 64 bit wide)
- Socket Boot FLASH (1Mbyte, 8 bit wide)
- SDRAM memory (64 Mbyte, 64 bit wide)
- NVRAM (8 Kbyte, 8 bit wide) / Real-Time Clock / Watchdog (M48T59 compatible)
- 16550 compatible Dual UART (8 bit wide)
- Utility Registers (8 bit wide)

2.2.1 FLASH Memory

The TVME8240 provides two banks of FLASH memory:

- Bank 0 consists of two 32-pin PLCC sockets each populated with a 512 K x 8 bit FLASH device for a total of 1 Mbyte 8 bit wide Boot FLASH.
- Bank 1 consists of four 1 M x 16 bit on board FLASH devices providing a total of 8 Mbyte 64 bit wide Memory FLASH.

2.2.2 SDRAM Memory

The TVME8240 provides four 8 M x 16 bit SDRAM devices, building up 64 Mbyte 64 bit wide SDRAM memory.

2.2.3 NVRAM / Real-Time Clock

The TVME8240 uses an ST M48T59 compatible device to provide 8 KB of non-volatile static RAM and real-time clock.

The M48T59 device consists of two parts:

- A 28-pin 330mil SO device which contains the RTC, 8 Kbyte SRAM and sockets for the Snaphat battery.
- A Snaphat battery that is placed on top of the device.

Please refer to the M48T59 manual for details.

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2.2.4 16550 compatible Dual UART

The TVME8240 uses the Exar XR16C2550 16550 compatible Dual UART with a 1.8432 MHz clock-oscillator providing two asynchronous serial ports.

Please refer to the XR16C2550 manual for details.

2.2.5 Utility Registers

The TVME8240 provides some additional registers for board control and status functions.

Please refer to the address map section of this manual for details.

2.3 PCI Bus

The TVME8240 implements a 32 bit, 33 MHz PCI bus.

The TVME8240 implements the following devices on the PCI bus:

- MPC8240 (PowerPC CPU, Local Memory Controller, Local PCI Bridge, PCI Arbiter, System Clock Generation, Interrupt Controller)
- Universe-II (VME PCI Bridge)
- 21143 (10/100Base-TX Ethernet LAN Controller)
- PCI9030 (PCI Local Target Chip)
- Optional PCI Devices on PCI Expansion Connector (e.g. TEWS TECHNOLOGIES' TVME230 IP-Span or Motorola PMC-Span)

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2.3.1 PCI Arbiter Assignment

The TVME8240 uses the MPC8240 integrated PCI arbiter for arbitration of PCI devices.

The MPC8240 integrated PCI arbiter provides PCI arbitration for the MPC8240 itself and up to five external PCI Masters.

The TVME8240 uses the following PCI arbiter assignment for the various PCI devices.

PCI Arbiter GNT/REQ Line	PCI Device
0	Universe-II (VME PCI Bridge)
1	21143 (LAN Controller)
2	SYM53C875 (SCSI Controller)
3	PCI Expansion (e.g. PMC-span)
4	N/A

Table 2-1 : PCI Arbiter Assignment

2.3.2 PCI IDSEL Assignment

The MPC8240 CPU provides capability for generating PCI configuration cycles.

The TVME8240 uses the following IDSEL assignment for the various on board PCI devices.

Device Number	Address Line	PCI Device
0d13 = 0b0_1101	AD13	Universe-II (VME PCI Bridge)
0d14 = 0b0_1110	AD14	21143 (LAN Controller)
0d15 = 0b0_1111	AD15	SYM53C875 (SCSI Controller)
0d16 = 0b1_0000	AD16	PCI9030 (PCI Target Chip)

Table 2-2 : PCI IDSEL Assignment

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2.4 VME Bus Interface

The TVME8240 uses the Universe-II VME PCI Bridge (Tundra) to build the VME interface.

The Universe-II VME PCI Bridge provides a 32 bit address / 32 bit data VME interface.

Please refer to the Universe-II manuals for details.

2.5 LAN Interface

The TVME8240 uses the 21143 10/100Base-TX Ethernet LAN Controller (Intel) with the LXT970 Fast Ethernet Transceiver (Intel) on its MII interface to build the Ethernet interface.

A 10/100Base-TX Ethernet interface is available on an 8P RJ45 connector on the front panel.

A 10Base-T AUI interface is available at the VME P2 connector.

Please refer to the 21143 and LXT970 manuals for details.

2.6 IP Bus Interface

The TVME8240 uses a XC2S100 FPGA (Xilinx) for the IndustryPack interface logic.

The TVME8240 uses the PCI9030 PCI Target Chip (PLX Technologies) to access the IndustryPack FPGA from the PCI bus.

Four single-sized IP slots (A–D) are provided. Double-sized IP modules (16 bit) can be used on combined IP slots A/B or C/D. The clock rate for each IP slot is programmable to be 8 MHz or 32 MHz.

Please refer to the IP interface section for details.

2.7 PCI Expansion Interface

The TVME8240 provides a 114-pin PCI expansion connector for using existing VME PCI Expansion Boards (e.g. TEWS TECHNOLOGIES' TVME230 IP-Span or Motorola PMC-Span).

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2.8 Asynchronous Serial Interface

The TVME8240 provides two asynchronous serial interface ports used by the on board Dual UART.

Port A is a fix RS232 port.

Port B can be configured for RS232 or RS422 by an adapter card.

Both serial ports are available on DB9 male connectors on the front panel or on the VME P2 connector.

2.9 Interrupt Controller

The TVME8240 uses the MPC8240 integrated Embedded Programmable Interrupt Controller (EPIC) in the serial mode.

The following interrupt sources are available:

Serial Interrupt No.	Edge / Level	Polarity	Interrupt Source
0	Level	Low	VME Bus Error
1	Edge	Low	ABORT Switch
2	Level	Low	21143
3	Level	Low	SYM53C875
4	Level	Low	PCI9030
5	Level	Low	Universe-II LINT0
6	Level	Low	Universe-II LINT1
7	Level	Low	Universe-II LINT2
8	Level	Low	Universe-II LINT3
9	Level	Low	PCI Expansion INTA
10	Level	Low	PCI Expansion INTB
11	Level	Low	PCI Expansion INTC
12	Level	Low	PCI Expansion INTD
13	Level	Low	Real-Time Clock
14	Level	Low	UART Channel A
15	Level	Low	UART Channel B

Table 2-3 : EPIC Serial Interrupt Assignment

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2.10 Status Indicators

The TVME8240 provides four status indicators visible on the front panel.

Function	Label	Color	Description
VME Bus System Controller	SYS	Green	Indicates if the TVME8240 is the VME Bus System Controller
Board Activity	ACT	Green	Indicates Memory Bus or PCI Bus activity
Board Failure	FAIL	Red	User controlled
Active Fuse	FUSE	Red	Indicates triggered fuses for IP Interface / LAN power supply

Table 2-4 : Status Indicators

All status indicators are ON during a board reset.

2.11 Reset Switch

The TVME8240 provides a momentary RESET switch accessible on the front panel.

The RESET switch can be used to generate a board hardware reset.

2.12 Abort Switch

The TVME8240 provides a momentary ABORT switch accessible on the front panel.

The ABORT switch can be used to generate a CPU interrupt.

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3 Address Maps

The TVME8240 uses the MPC8240 address map B in host mode.

The following address maps reflect MPC8240 configuration register settings done by board initialization software.

3.1 Address Map - Processor View

Processor Address		Size (Byte)	Description
Start	End		
0x0000_0000	TOP_DRAM	DRAM_SIZE	SDRAM Memory (64 bit wide) 64 Mbyte : TOP_DRAM = 0x03FF_FFFF
TOP_DRAM + 1	0x3FFF_FFFF	1 G – DRAM_SIZE	Reserved
0x4000_0000	0x7FFF_FFFF	1 G	Reserved
0x8000_0000	0xFCEF_FFFF	2 G – 49 M	PCI MEM Space
0xFCF0_0000	0xFCFF_FFFF	1 M	MPC8240 EUMB
0xFD00_0000	0xFDFF_FFFF	16 M	PCI MEM Space (0-based)
0xFE00_0000	0xFE00_FFFF	64 K	PCI I/O Space (0-based)
0xFE01_0000	0xFE7F_FFFF	8 M – 64 K	Reserved
0xFE80_0000	0xFEBF_FFFF	4 M	PCI I/O Space (0-based)
0xFEC0_0000	0xFEDF_FFFF	2 M	Configuration Address Register
0xFEE0_0000	0xFEEF_FFFF	1 M	Configuration Data Register
0xFEF0_0000	0xFEFF_FFFF	1 M	PCI Interrupt Acknowledge
0xFF00_0000	0xFF7F_FFFF	8 M	Memory FLASH (64 bit wide)
0xFF80_0000	0xFFDF_FFFF	6 M	Reserved
0xFFE0_0000	0xFFEF_FFFF	1 M	Peripheral Devices (8 bit wide)
0xFFF0_0000	0xFFFF_FFFF	1 M	Boot FLASH (8 bit wide)

Table 3-1 : Address Map – Processor View

Device	Read	Write
SDRAM	All	All
Memory FLASH	All	64 bit Only
Peripheral Devices	8 bit Only	8 bit Only
Boot FLASH	All	8 bit Only

Table 3-2 : Supported Transfer Sizes

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Processor Address		Translated PCI Address		PCI Space
Start	End	Start	End	
0x8000_0000	0xFCEF_FFFF	0x8000_0000	0xFCEF_FFFF	MEM
0xFD00_0000	0xFDFF_FFFF	0x0000_0000	0x00FF_FFFF	MEM
0xFE00_0000	0xFE00_FFFF	0x0000_0000	0x0000_FFFF	I/O
0xFE80_0000	0xFEBF_FFFF	0x0000_0080	0x00BF_FFFF	I/O

Table 3-3 : PCI Address Translation

3.2 Address Map – PCI Memory Master View

PCI Memory Address		Size (Byte)	Description
Start	End		
0x0000_0000	TOP_DRAM	DRAM_SIZE	SDRAM Memory (64 bit wide) 64 Mbyte : TOP_DRAM = 0x03FF_FFFF
TOP_DRAM + 1	0x3FFF_FFFF	1 G – DRAM_SIZE	Reserved
0x4000_0000	0x7FFF_FFFF	1 G	Reserved
0x8000_0000	0xFCEF_FFFF	2 G – 49 M	PCI Memory Space
0xFCF0_0000	0xFCF0_0FFF	4 K	PCI accessible MPC8240 EUMB
0xFCF0_1000	0xFCFF_FFFF	1 M – 4 K	Reserved
0xFD00_0000	0xFDFF_FFFF	16 M	SDRAM Memory (0-Based)
0xFE00_0000	0xFEFF_FFFF	16 M	Reserved
0xFF00_0000	0xFF7F_FFFF	8 M	Memory FLASH (64 bit wide)
0xFF80_0000	0xFFDF_FFFF	6 M	Reserved
0xFFE0_0000	0xFFEF_FFFF	1 M	Peripheral Devices (8 bit wide)
0xFFF0_0000	0xFFFF_FFFF	1 M	Boot FLASH (8 bit wide)

Table 3-4 : Address Map – PCI Memory Master View

On the TVME8240 the MPC8240 responds as a target to PCI Memory cycles for accessing SDRAM, PCI accessible MPC8240 EUMB, Memory FLASH, Peripheral Devices and Boot FLASH.

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3.3 Address Map – PCI I/O Master View

PCI I/O Address		Size (Byte)	Description
Start	End		
0x0000_0000	0x0000_FFFF	64 K	PCI I/O Space
0x0001_0000	0x007F_FFFF	8 M – 64 K	Reserved
0x0080_0000	0x00BF_FFFF	4 M	PCI I/O Space
0x00C0_0000	0xFFFF_FFFF	4 G – 12 M	Reserved

Table 3-5 : Address Map – PCI I/O Master View

The MPC8240 does not responding as a target to PCI I/O cycles.

3.4 Address Map – Peripheral Devices Detail

Address		Size (Byte)	Description
Start	End		
0xFFE0_0000	0xFFE0_1FFF	8 K	NVRAM / RTC
0xFFE0_2000	0xFFE3_FFFF	256 K – 8 K	Reserved
0xFFE4_0000	0xFFE4_0003	4	UTILITY REG
0xFFE4_0004	0xFFE7_FFFF	256 K – 4	Reserved
0xFFE8_0000	0xFFE8_0007	8	UART CH A
0xFFE8_0008	0xFFE8_000F	8	UART CH B
0xFFE8_0010	0xFFEF_FFFF	512 K -16	Reserved

Table 3-6 : Address Map – Peripheral Devices Detail

For read or write accesses to the Peripheral Devices only 8 bit (byte) transfer sizes are allowed.

For the NVRAM / RTC register map please refer to the M48T59 device documentation.

For the UART register map please refer to the XR16C2550 documentation.

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3.5 Address Map – Utility Register Detail

Address	Size (Byte)	Register Name
0xFFE4_0000	1	CONTROL
0xFFE4_0001	1	STATUS
0xFFE4_0002	1	Reserved
0xFFE4_0003	1	LED

Table 3-7 : Address Map – Utility Register Detail

3.5.1 Control Register (0xFFE4_0000)

Bit	Name	Access	Reset	Function
0 (MSB)	BOARD_RST	R/W	0	0: Normal Board Operation 1: Assert Board Reset
1	I2C_EEP_WE	R/W	0	0: I2C EEPROM Writes Disabled 1: I2C EEPROM Writes Enabled
2	MEM_FLASH_WE	R/W	0	0: Memory FLASH Writes Disabled 1: Memory FLASH Writes Enabled
3	BOOT_FLASH_WE	R/W	0	0: Boot FLASH Writes Disabled 1: Boot FLASH Writes Enabled
4	Reserved	-	-	Write as '0' Undefined for Reads
5	VME_BERR_INT_EN	R/W	0	0: VME Bus Error Interrupt Disabled 1: VME Bus Error Interrupt Enabled
6	Reserved	-	-	Write as '0' Undefined for Reads
7 (LSB)	Reserved	-	-	Write as '0' Undefined for Reads

Table 3-8 : Control Register

A board reset is also performed at power-up.

A board reset will perform a general board hardware reset, re-configuration of the IP FPGA, PCI reset and CPU reset.

If the TVME8240 is the VME bus system controller, a board reset will also trigger a VME bus system reset.

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3.5.2 Status Register (0xFFE4_0001)

Bit	Name	Access	Reset	Function
0 (MSB)	BOOT_JMP	R	-	0: Boot Jumper Open 1: Boot Jumper Closed
1	PCI_EXP_PRSNT	R	-	0: PCI Expansion Board Not Present 1: PCI Expansion Board Present
2	SER_B_MODE	R	-	0: RS422 Adapter 1: RS232 Adapter or No Adapter
3	ABORT_SW	R	-	0: Abort Switch Not Active 1: Abort Switch Active
4	Reserved	-	-	Undefined for Reads
5	FPGA_DONE	R	-	0: IP FPGA Configuration Not Done 1: IP FPGA Configuration Done
6	VME_BERR	R/C	-	Reads: 0: No VME Bus Error Event 1: VME Bus Error Event occurred Writes: Write as '1' to clear VME Bus Error Status and/or to clear VME Bus Error Interrupt Status. This status bit is capable of generating an interrupt if enabled in the Control Register.
7 (LSB)	Reserved	-	-	Undefined for Reads

Table 3-9 : Status Register

Board initialization software should verify successful IP FPGA configuration.

3.5.3 LED Register (0xFFE4_0003)

Bit	Name	Access	Reset	Function
0 (MSB)	FAIL_LED	R/W	0	0: Set Fail LED OFF 1: Set Fail LED ON
1	Reserved	-	-	Write as '0' Undefined for Reads
2	Reserved	-	-	Write as '0' Undefined for Reads
3	Reserved	-	-	Write as '0' Undefined for Reads
4	Reserved	-	-	Write as '0' Undefined for Reads.
5	Reserved	-	-	Write as '0'

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				Undefined for Reads
6	Reserved	-	-	Write as '0' Undefined for Reads.
7 (LSB)	Reserved	-	-	Write as '0'. Undefined for Reads

Table 3-10: LED Register

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4 MPC8240

The TVME8240 uses the MPC8240 in host mode with address map B.

The MPC8240 processor and peripheral logic are configured to operate in big endian mode.

4.1 MPC8240 Configuration Register

Setting up the MPC8240 Configuration Registers is scope of the board initialization software.

4.1.1 Configuration Register Access

The MPC8240 Configuration Registers are accessed in two steps:

1. A 32 bit register address 0x8000_00nn is written to the CONFIG_ADDR port at 0xFEC0_0000, where nn is the (word-aligned) register offset.

2. Data is accessed at the CONFIG_DATA port at 0xFEE0_000m, where m is the offset within the word-aligned address (depending on transfer size).

Data can be accessed multiple times at the CONFIG_DATA port until the CONFIG_ADDR port value is changed.

All of the MPC8240 Configuration Registers are intrinsically little endian. Therefore all of the following Configuration Register settings are shown in little endian order.

Since on the TVME8240 the MPC8240 processor and peripheral logic operates in big endian mode, software must either use byte reversed load / store instructions or byte-swap the values for the CONFIG_ADDR and CONFIG_DATA port access.

E.g. for reading the Device ID Register (offset 0x02) one should write 0x0000_0080 (0x00 is the word-aligned offset for 0x02) to 0xFEC0_0000 and read the half-word 0x0300 at 0xFEE0_0002.

E.g. for setting the Output Driver Control Register (offset 0x73) one should write 0x7000_0080 (0x70 is the word-aligned offset for 0x73) to 0xFEC0_0000 and write the byte 0xC0 to 0xFEE0_0003.

E.g. for setting the EUMBBAR Register (offset 0x78) to 0xFCF0_0000 one should write 0x78000080 to 0xFEC0_0000 and write the word 0x0000F0FC to 0xFEE0_0000.

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4.1.2 Configuration Register Settings

Register Offset	Register Description	Size (Byte)	Access Type	Setting
0x00	Vendor ID	2	R	0x1057 (Motorola)
0x02	Device ID	2	R	0x0003 (MPC8240)
0x04	PCI Command Register	2	R/W	0x0006
0x06	PCI Status Register	2	R/C	Status
0x08	Revision ID	1	R	Reset_Value
0x09	Standard Programming Interface	1	R	0x00 (Host)
0x0A	Subclass	1	R	0x00
0x0B	Class Code	1	R	0x06 (Host)
0x0C	Cache Line Size	1	R/W	Reset_Value
0x0D	Latency Timer	1	R/W	Reset_Value
0x0E	Header Type	1	R	0x00
0x0F	BIST Control	1	R	0x00
0x10	Local Memory Base Address Register (LMBAR)	4	R/W	Reset_Value
0x14	Peripheral Control Status Register Base Address (PCSRBAR)	4	R/W	0xFCF0_0000
0x30	Expansion ROM Base Address	4	R	0x0000_0000
0x3C	Interrupt Line	1	R/W	Reset_Value
0x3D	Interrupt Pin	1	R	0x01
0x3E	MAX GNT	1	R	0x00
0x3F	MAX LAT	1	R	0x00
0x40	Bus Number	1	R/W	0x00
0x41	Subordinate Bus Number	1	R/W	0x00
0x46	PCI Arbiter Control Register	2	R/W	0x8000
0x70	Power Management Configuration Register 1	2	R/W	0x0000
0x72	Power Management Configuration Register 2	1	R/W	0x40
0x73	Output Driver Control Register	1	R/W	0xC0
0x74	Clock Driver Control Register	2	R/W	0x0000
0x78	Embedded Utilities Memory Block Base Address (EUMBBAR)	4	R/W	0xFCF0_0000
0x80, 0x84	Memory Starting Address Registers	4	R/W	0x4040_4000, 0x4040_4040
0x88, 0x8C	Extended Memory Starting Address Registers	4	R/W	0x0000_0000, 0x0000_0000

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Register Offset	Register Description	Size (Byte)	Access Type	Setting
0x90, 0x94	Memory Ending Address Registers	4	R/W	0x4F4F_4F3F, 0x4F4F_4F4F
0x98, 0x9C	Extended Memory Ending Address Registers	4	R/W	0x0000_0000, 0x0000_0000
0xA0	Memory Bank Enable Register	1	R/W	0x01
0xA3	Page Mode Register	1	R/W	0x00
0xA8	Processor Interface Configuration Register 1	4	R/W	0xFF14_1298
0xAC	Processor Interface Configuration Register 2	4	R/W	0x0000_0600
0xB8	ECC Single Bit Error Counter Register	1	R/W	0x00
0xB9	ECC Single Bit Error Trigger Register	1	R/W	0x00
0xC0	Error Enabling Register 1	1	R/W	Reset_Value
0xC1	Error Detection Register 1	1	R/C	Status
0xC3	Processor Internal Bus Error Status Register	1	R/C	Status
0xC4	Error Enabling Register 2	1	R/W	Reset_Value
0xC5	Error Detection Register 2	1	R/C	Status
0xC7	PCI Bus Error Status Register	1	R/C	Status
0xC8	Processor/PCI Error Address Register	4	R	Reset_Value
0xE0	Address Map B Options Register (AMBOR)	1	R/W	0xC0
0xF0	Memory Control Configuration Register 1 (MCCR1)	4	R/W	0x03E8_0000
0xF4	Memory Control Configuration Register 2 (MCCR2)	4	R/W	0x0A40_0F8C
0xF8	Memory Control Configuration Register 3 (MCCR3)	4	R/W	0x0620_0000
0xFC	Memory Control Configuration Register 4 (MCCR4)	4	R/W	0x2500_2220

Table 4-1 : MPC8240 Configuration Register Settings

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Board initialization software notes:

The MEMGO bit in the MCCR1 register (offset 0xF0) must not be set until all other memory configuration parameters have been appropriately configured.

The DLL_RESET bit in the AMBOR register (offset 0xE0) must be explicitly set and then cleared by software during initialization.

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4.2 MPC8240 EPIC Register

The TVME8240 uses the MPC8240 EPIC in serial mode as the board interrupt controller.

4.2.1 EPIC Register Access

The EPIC Registers are part of the MPC8240 Embedded Utility Memory Block (EUMB).

The EUMB base address is set in the EUMBBAR Register.

For the TVME8240 memory map the EUMB base address is set to 0xFCF0_0000.

4.2.2 EPIC Register Settings

4.2.2.1 Global Configuration Register (GCR)

Offset from EUMBBAR: 0x4_1020

The mode bit in the GCR must be set for EPIC mixed mode operation.

4.2.2.2 EPIC Interrupt Configuration Register (EICR)

Offset from EUMBBAR: 0x4_1030

The EICR clock ratio field should be set to 0x2 for optimized interrupt performance.

The EICR SIE bit must be set to enable Serial Interrupt Mode.

4.2.2.3 Serial Interrupt Vector / Priority Registers (SVPR)

The polarity and sense bits in the SVPRs must be configured accordingly to the EPIC Serial Interrupt Assignment table.

Please refer to chapter “Interrupt Controller” for the EPIC serial interrupt assignment.

4.2.2.4 EPIC Register Programming

The EPIC Programming Guidelines from the MPC8240 manual should be followed.

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4.3 I2C

The TVME8240 provides an on board I2C EEPROM for board specific data.

4.3.1 I2C EEPROM

EEPROM Offset	Description	Content
0x00	Check sum	see note below
0x01	Number Of Valid Bytes Following	e.g. 0x06
0x02	Board Type (High Byte)	0x2030 for TVME8240
0x03	Board Type (Low Byte)	
0x04	Board Option (High Byte)	e.g. 0x000B for TVME8240-11
0x05	Board Option (Low Byte)	
0x06	Board Version (Major)	V <major>.<minor> e.g. 0x0100 = V1.0
0x07	Board Version (Minor)	
0x08 ... 0x0F	Factory Reserved	
0x10 ... 0xFF	Reserved	

Table 4-2 : I2C EEPROM Content

The address of the on board I2C EEPROM is 0b000.

Writes to the on board I2C EEPROM must be enabled in the Utility Control Register.

The check sum is the 2's-complement of the lower byte of the sum of all used locations of the I2C EEPROM, except the check sum byte.

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5 FLASH Programming

5.1 8 bit Wide Socket Boot FLASH

The TVME8240 provides 1 MB of 8 bit wide socket Boot FLASH using two 512 K x 8 bit 32-pin PLCC FLASH devices.

The Boot FLASH address range is 0xFFF0_0000 to 0xFFFF_FFFF.

Boot FLASH Socket XU1 is for the lower 512 K address range of the Boot FLASH (0xFFF0_0000 to 0xFFF7_FFFF).

Boot FLASH Socket XU2 is for the upper 512 K address range of the Boot FLASH (0xFFF8_0000 to 0xFFFF_FFFF).

The Boot FLASH data bus port width is 8 bit.

For writes to the Boot FLASH only byte (8 bit) transfer sizes are allowed.

Writes to the Boot FLASH must be enabled in the Utility Control Register.

The 8 bit wide socket Boot FLASH must always be installed and provide the board initialization code at the system reset vector.

Command Sequence	Cycles	1st Cycle		2nd Cycle		3rd Cycle		4th Cycle		5th Cycle		6th Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read	1	RA	RD										
Reset	1	Base+ 0x000	0xF0										
Auto Select	4	Base+ 0x555	0xAA	Base+ 0x2AA	0x55	Base+ 0x555	0x90	Base+ 0x000	MID				
								Base+ 0x001	DID				
Write	4	Base+ 0x555	0xAA	Base+ 0x2AA	0x55	Base+ 0x555	0xA0	WA	WD				
Chip Erase	6	Base+ 0x555	0xAA	Base+ 0x2AA	0x55	Base+ 0x555	0x80	Base+ 0x555	0xAA	Base+ 0x2AA	0x55	Base+ 0x555	0x10
Sector Erase	6	Base+ 0x555	0xAA	Base+ 0x2AA	0x55	Base+ 0x555	0x80	Base+ 0x555	0xAA	Base+ 0x2AA	0x55	SAx	0x30

Table 5-1 : Boot FLASH Command Cycles

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All the Boot FLASH command cycles are write cycles except the 1st cycle of the Read command and the 4th cycle of the Auto Select command which are read cycles.

The base address for the lower 512 K Boot FLASH device is 0xFFF0_0000.

The base address for the upper 512 K Boot FLASH device is 0xFFF8_0000.

For Write commands the program should poll for RD = WD from RA = WA after the 4th cycle.

For Erase commands the program should poll for RD = 0xFF from the Boot FLASH device base address for Chip Erase or SAx for Sector Erase after the 6th cycle.

Symbols:

DID = Device ID, MID = Manufacturer ID, RA = Read Address, RD = Read Data,

SA = Sector Address, WA = Write Address, WD = Write Data

Manufacturer	Device	Manufacture ID	Device ID
AMD	29F040B	0x01	0xA4
ST	29F040B	0x20	0xE2

Table 5-2 : Boot FLASH Auto Select Codes

Sector	Sector Size (Byte)	Sector Address Range
SA0	64 K	0xFFF0_0000 - 0xFFF0_FFFF
SA1	64 K	0xFFF1_0000 - 0xFFF1_FFFF
SA2	64 K	0xFFF2_0000 - 0xFFF2_FFFF
SA3	64 K	0xFFF3_0000 - 0xFFF3_FFFF
SA4	64 K	0xFFF4_0000 - 0xFFF4_FFFF
SA5	64 K	0xFFF5_0000 - 0xFFF5_FFFF
SA6	64 K	0xFFF6_0000 - 0xFFF6_FFFF
SA7	64 K	0xFFF7_0000 - 0xFFF7_FFFF
SA8	64 K	0xFFF8_0000 - 0xFFF8_FFFF
SA9	64 K	0xFFF9_0000 - 0xFFF9_FFFF
SA10	64 K	0xFFFA_0000 - 0xFFFA_FFFF
SA11	64 K	0xFFFB_0000 - 0xFFFB_FFFF
SA12	64 K	0xFFFC_0000 - 0xFFFC_FFFF
SA13	64 K	0xFFFD_0000 - 0xFFFD_FFFF
SA14	64 K	0xFFFE_0000 - 0xFFFE_FFFF
SA15	64 K	0xFFFF_0000 - 0xFFFF_FFFF

Table 5-3 : Boot FLASH Sector Map

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5.2 64 bit Wide On Board Memory FLASH

The TVME8240 provides 8 Mbyte of 64 bit wide board mounted Memory FLASH using four 1 M x16 bit FLASH devices.

The Memory FLASH address range is 0xFF00_0000 to 0xFF7F_FFFF.

The Memory FLASH data bus port width is 64 bit.

For writes to the Memory FLASH only double-word (64 bit) transfer sizes are allowed.

Writes to the Memory FLASH must be enabled in the Utility Control Register.

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Command Sequence	Cycles	1st Cycle		2nd Cycle		3rd Cycle		4th Cycle		5th Cycle		6th Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read	1	RA	RD										
Reset	1	Base + 0x0_0000	0x00F000F0 00F000F0										
Auto Select	4	Base + 0x2_AAA8	0x00AA00AA 00AA00AA	Base + 0x1_5550	0x00550055 00550055	Base + 0x2_AAA8	0x00900090 00900090	Base + 0x0_0000	MID				
								Base + 0x0_0008	DID				
Write	4	Base + 0x2_AAA8	0x00AA00AA 00AA00A	Base + 0x1_5550	0x00550055 00550055	Base + 0x2_AAA8	0x00A000A0 00A000A0	WA	WD				
Chip Erase	6	Base + 0x2_AAA8	0x00AA00AA 00AA00A	Base + 0x1_5550	0x00550055 00550055	Base + 0x2_AAA8	0x00800080 00800080	Base + 0x2_AAA8	0x00AA00AA 00AA00A	Base + 0x1_5550	0x00550055 00550055	Base + 0x2_AAA8	0x00100010 00100010
Sector Erase	6	Base + 0x2_AAA8	0x00AA00AA 00AA00A	Base + 0x1_5550	0x00550055 00550055	Base + 0x2_AAA8	0x00800080 00800080	Base + 0x2_AAA8	0x00AA00AA 00AA00A	Base + 0x1_5550	0x00550055 00550055	SAx	0x00300030 00300030

Table 5-4 : Memory FLASH Command Cycles

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All the Memory FLASH command cycles are write cycles except the 1st cycle of the Read command and the 4th cycle of the Auto Select command which are read cycles.

The Memory FLASH base address is 0xFF00_0000.

For Write commands the program should poll for RD = WD from RA = WA after the 4th cycle.

For Erase commands the program should poll for RD = 0xFFFFFFFFFFFFFFFF from the Memory FLASH base address for Chip Erase or SAx for Sector Erase after the 6th cycle.

Symbols:

DID = Device ID, MID = Manufacturer ID, RA = Read Address, RD = Read Data,

SA = Sector Address, WA = Write Address, WD = Write Data

Manufacturer	Device	Manufacturer ID	Device ID
SST	39VF160	0x00BF00BF00BF00BF	0x2782278227822782
SST	39VF1601	0x00BF00BF00BF00BF	0x234B234B234B234B
SST	39VF1602	0x00BF00BF00BF00BF	0x234A234A234A234A

Table 5-5 : Memory FLASH Auto Select Codes

Sector	Sector Size (Byte)	Sector Address Range
SST 39xF160 (Uniform)		
SA0	16 K	0xFF00_0000 - 0xFF00_3FFF
SA1	16 K	0xFF00_4000 - 0xFF00_7FFF
SA2	16 K	0xFF00_8000 - 0xFF00_BFFF
SA3	16 K	0xFF00_C000 - 0xFF00_FFFF
SA4	16 K	0xFF01_0000 - 0xFF01_3FFF
…	…	…
SA511	16 K	0xFF7F_C000 - 0xFF7F_FFFF

Table 5-6 : Memory FLASH Sector Map

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6 VME Bus Interface

The Tundra Universe-II VME PCI bridge is used as the TVME8240 VME PCI bridge.

The Universe-II is accessible on both the VME bus and the TVME8240 PCI bus.

Please refer to the Universe-II manual for a detailed description of the Universe-II VME PCI bridge.

6.1 Universe-II PCI Header

The Universe-II PCI device number is 13.

Register Offset	PCI Configuration Register				Setting
	31 ... 24	23 ... 16	15 ... 8	7 ... 0	
0x00	Device ID (Universe)		Vendor ID (Tundra)		0x0000_10E3
0x04	Status		Command		0x0200_0007
0x08	Class Code			Revision ID	0x0680_0001
0x0C	Reserved	Header	Latency	Cache Line	0x0000_0000
0x10	PCI Base Address 0 (Configuration Register I/O Mapped)				0xFFFF_F001[1] (4 Kbyte)
0x14	PCI Base Address 1 (Configuration Register Memory Mapped)				0xFFFF_F000[1] (4 Kbyte)
0x18	PCI Unimplemented				0x0000_0000
0x1C	PCI Unimplemented				0x0000_0000
0x20	PCI Unimplemented				0x0000_0000
0x24	PCI Unimplemented				0x0000_0000
0x28	PCI Reserved				0x0000_0000
0x2C	PCI Reserved				0x0000_0000
0x30	PCI Unimplemented				0x0000_0000
0x34	PCI Reserved				0x0000_0000
0x38	PCI Reserved				0x0000_0000
0x3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	0x0003_0100

[1] Read back value after writing all 1's.

Table 6-1 : Universe-II PCI Header

6.2 Universe-II Power-Up Options

The TVME8240 uses the default Universe-II power-up option configuration.

See the Universe-II user manual for details.

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6.3 Universe-II Reset Signals

The Universe-II PWRRST# input is controlled by a power-up reset logic.

The Universe-II RST# input is connected to the PCI reset signal.

The Universe-II LRST# output is used to assert a general board reset in case of a VME bus system reset.

The Universe-II VMERST# input is used to assert a VME bus system reset in case of a general board reset.

The Universe-II VRSYSRST# and VXSYSRST# signals are mapped to the VME bus SYSRST# signal.

If the Universe-II is the VME bus system controller, a general board reset will also assert a VME bus system reset.

If the Universe-II is not the VME bus system controller, a VME bus system reset will also assert a general board reset.

6.4 Universe-II Interrupts

The Universe-II LINT#[4:7] interrupt pins are not used.

The Universe-II LINT#[0:3] interrupt pins are used as outputs and are mapped to the serial interrupts no. [5:8] of the MPC8240 EPIC.

6.4.1 VME Bus Error Interrupt

The TVME8240 provides a dedicated interrupt source for VME bus error events asserted by the Universe-II.

The Universe-II does only provide a limited option for mapping a VME bus error event to the Universe-II LINT# interrupt pins. To overcome this limitation the TVME8240 logic directly monitors the Universe-II VX_BERR output that is used for asserting VME bus errors.

The TVME8240 VME bus error interrupt is handled via the Utility Registers in the Peripheral Devices address space. Please see the Address Map section for details.

6.5 Universe-II VME Bus Modes

On the TVME8240 the Universe-II supports VME bus A32/24/16 master and slave address modes and D32/16/8 master and slave data transfer modes.

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7 LAN Interface

The Intel 21143 Ethernet controller is used for the TVME8240 Ethernet interface.

The 21143 is accessible on the TVME8240 PCI bus.

The 21143 INT# interrupt output is mapped to the serial interrupt no. 2 of the MPC8240 EPIC.

The 21143 is reset by a PCI reset.

Please refer to the 21143 manual for a detailed description of the 21143 Ethernet Controller.

7.1 21143 PCI Header

The 21143 PCI device number is 14.

Register Offset	PCI Configuration Register				Setting
	31 … 24	23 … 16	15 … 8	7 … 0	
0x00	Device ID (21143)		Vendor ID (Intel)		0x0019_1011
0x04	Status		Command		0x0280_0007
0x08	Class Code			Revision ID	0x0200_0041
0x0C	Reserved	Header	Latency	Cache Line	0x0000_0000
0x10	PCI Base Address 0 (Configuration Register I/O Mapped)				0xFFFF_FF81[1] (128Byte)
0x14	PCI Base Address 1 (Configuration Register Memory Mapped)				0xFFFF_FC00[1] (1 Kbyte)
0x18	Reserved				0x0000_0000
0x1C	Reserved				0x0000_0000
0x20	Reserved				0x0000_0000
0x24	Reserved				0x0000_0000
0x28	Card bus CIS Pointer				0x0000_0000
0x2C	Subsystem ID (TVME8240)		Subsystem Vendor ID (TEWS TECHNOLOGIES)		0x2030_1498
0x30	PCI Expansion ROM Base Address				0x0000_0000
0x34	Reserved			Cap. Pointer	0x0000_0000
0x38	Reserved				0x0000_0000
0x3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	0x2814_0100

(1) Read back Value after writing all 1's.

Table 7-1 : 21143 PCI Header

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7.2 21143 Configuration EEPROM

Some parts of the 21143 configuration EEPROM are used directly by the 21143 upon reset.

Some parts of the 21143 configuration EEPROM are used by software drivers.

Description				EEPROM Offset
Value				
15	8	7	0	
Sub-System Vendor ID				0x00
0x1498				
Sub-System ID				0x02
0x2030				
Card bus CIS Pointer High				0x04
0x0000				
Card bus CIS Pointer Low				0x6
0x0000				
ID_Reserved1				0x8
0x0000				
ID_Reserved1				0xA
0x0000				
ID_Reserved1				0xC
0x0000				
MiscHwOptions		ID_Reserved1		0xF
0x00		0x00		
Func0HwOptions		ID_BLOCK_CRC		0x10
0x00		Tbd		
Controller_Count		SROM Format Ver.		0x12
0x01		0x04		
IEEE Network Address (6 Byte)				0x14
0x0100				
IEEE Network Address (6 Byte)				0x16
0x_uv_06				
IEEE Network Address (6 Byte)				0x18
0x_yz_wx				
		Controller_0 Dev#		0x1A
		0x00		
Controller_0 Info Leaf Offset				0x1B
0x0020				
		Reserved		0x1D
		0x00		
Reserved				0x1E
0x0000				
Selected Connection Type				0x20
0x0800				
		Block Count		0x22
		0x02		

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Description		
Value		
	Block Length	0x23
	0x86	
	Block Type	0x24
	0x02	
	Media Code	0x25
	0x01	
GPR Seq. Word #1		0x26
0x0801		
GPR Seq. Word #1		0x28
0x0001		
	Block Length	0x2A
	0x93	
	Block Type	0x2B
	0x03	
	PHY#	0x2C
	0x00	
	GPR Seq. Length	0x2D
	0x00	
	RST Seq. Length	0x2E
	0x03	
RST Sequence 1st Word		0x2F
0x0801		
RST Sequence 2nd Word		0x31
0x0000		
RST Sequence 3rd Word		0x33
0x0001		
Media Capabilities		0x35
0x7800		
Nway Advertisement		0x37
0x01E0		
FDX Bit Map		0x39
0x5000		
TTM Bit Map		0x3B
0x1800		
	PHY Ins. Ind.	0x3D
	0x00	
	Reserved	0x3E - 0x7B
	0x00	
Manufacturer_Reserved		7C
0x0000		
SROM_CRC		7E
Tbd		

Table 7-2 : 21143 Configuration EEPROM Settings

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EEPROM Address	0x00	0x02	0x04	0x06	0x08	0x0A	0x0C	0x0E
0x00	0x1498	0x2030	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
0x10	IDCRC	0x0104	0x0100	0xuv06	0xyzwx	0x2000	0x0000	0x0000
0x20	0x0800	0x8602	0x0102	0x0801	0x0001	0x0393	0x0000	0x0103
0x30	0x0008	0x0100	0x0000	0xE078	0x0001	0x0050	0x0018	0x0000
0x40	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
0x50	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
0x60	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
0x70	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	ROMCRC

ICCRC: 0x00_ID-Block-CRC, ROMCRC: SROM CRC, MAC Addr.: 00_01_06_uv_wx_yz

Table 7-3 : 21143 Configuration EEPROM Content

7.3 21143 Ports

The 21143 MII port connects to an Intel LXT970 Fast Ethernet transceiver to build the Fast Ethernet interface available at the RJ45 connector on the front plate.

The 21143 AUI port connects to the VME P2 connector.

The 21143 10Base-T TP port is not used.

7.4 21143 GEP Pin Usage

The 21143 GEP[0] pin is used as an output that connects to the LXT970 Fast Ethernet transceiver reset input.

A low on the GEP[0] output holds the LXT970 in reset. The LXT970 is also reset by a PCI reset.

The 21143 GEP[3:1] pins are used as inputs.

Interrupts for GEP[1:0] inputs must be disabled.

7.5 Media Capabilities

10/100Base-TX Ethernet interface on the RJ45 front panel connector.

AUI port for a 10Base-T or 10Base2 Ethernet interface on the VME P2 Connector.

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8 IP Bus Interface

The TVME8240 IP interface is accessible in the PCI Memory space.

The PCI9030 PCI Target Chip from PLX Technology is used as the PCI target device for accessing the IP interface.

A FPGA is used on the PCI9030 local bus to build the IP interface and provide IP Interface Control Registers.

8.1 PCI9030 PCI Target Chip

The PCI9030 provides four local spaces 0:3 that are used for the TVME8240 IP interface.

Basic PCI9030 register configuration is loaded from a serial EEPROM after power-up or board reset.

Programming of the PCI9030 PCI and local configuration registers is scope of the board initialization software.

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8.1.1 PCI9030 PCI Header

The PCI9030 PCI device number is 16.

Register Offset	PCI Configuration Register				Setting
	31 … 24	23 … 16	15 … 8	7 … 0	
0x00	Device ID (PCI9030)		Vendor ID (PLX Technology)		0x9030_10B5
0x04	Status		Command		0x0280_0003
0x08	Class Code			Revision ID	0x0680_0000
0x0C	Not Supported	Header	Not Supported	Cache Line	0x0000_0000
0x10	PCI Base Address 0 (PCIBAR0) (PCI9030 Local Configuration Register Memory Mapped)				0xFFFF_FF80 (128 Byte)
0x14	PCI Base Address 1 (PCIBAR1) (PCI9030 Local Configuration Register I/O Mapped)				0xFFFF_FF81[1] (128 Byte)
0x18	PCI Base Address 2 (PCIBAR2) (Local Space 0)				0xFFFF_FF00[1] (256 Byte)
0x1C	PCI Base Address 3 (PCIBAR3) (Local Space 1)				0xFFFF_FC00[1] (1 Kbyte)
0x20	PCI Base Address 4 (PCIBAR4) (Local Space 2)				0xFE00_0000[1] (32 Mbyte)
0x24	PCI Base Address 5 (PCIBAR5) (Local Space 3)				0xFF00_0000[1] (16 Mbyte)
0x28	Not Supported				0x0000_0000
0x2C	Subsystem ID (TVME8240)		Subsystem Vendor ID (TEWS TECHNOLOGIES)		0x2030_1498
0x30	PCI Expansion ROM Base Address				0x0000_0000
0x34	Reserved			Cap. Pointer	0x0000_0040
0x38	Reserved				0x0000_0000
0x3C	Not Supported	Not Supported	Interrupt Pin	Interrupt Line	0x0000_0100
0x40	PM Capabilities		PM NxtCap	PM CapID	0x4801_4801
0x44	PM Data	PM CSR EXT	PM CSR		0x0000_0000
0x48	Reserved	HS CSR	HS NxtCap	HS CapID	0x0000_4C06
0x4C	VPD Address		VPD NxtCap	VPD CapID	0x0000_0003
0x50	VPD Data				0x0000_0000

[1] Read back Value after writing all 1's.

Table 8-1 : PCI9030 PCI Header

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8.1.2 Local Configuration Register

The PCI base address for the PCI9030 Local Configuration Registers can be obtained from the PCIBAR0 (PCI Memory mapped) register at offset 0x10 or from the PCIBAR1 (PCI I/O mapped) register at offset 0x14 in the PCI9030 PCI configuration register space.

Register Offset	Local Configuration Register	Name	Setting
0x00	Local Space 0 Range	LAS0RR	0x0FFF_FF00
0x04	Local Space 1 Range	LAS1RR	0x0FFF_FC00
0x08	Local Space 2 Range	LAS2RR	0x0E00_0000
0x0C	Local Space 3 Range	LAS3RR	0x0F00_0000
0x10	Expansion ROM Range	EROMRR	0x0000_0000
0x14	Local Space 0 Remap	LAS0BA	0x0800_0001
0x18	Local Space 1 Remap	LAS1BA	0x0400_0001
0x1C	Local Space 2 Remap	LAS2BA	0x0000_0001
0x20	Local Space 3 Remap	LAS3BA	0x0200_0001
0x24	Expansion ROM Remap	EROMBA	0x0000_0000
0x28	Local Space 0 Descriptor	LAS0BRD	0xD541_60A0
0x2C	Local Space 1 Descriptor	LAS1BRD	0x1541_20A2
0x30	Local Space 2 Descriptor	LAS2BRD	0x1541_20A2
0x34	Local Space 3 Descriptor	LAS3BRD	0x1501_20A2
0x38	Expansion ROM Descriptor	EROMBRD	0x0000_0000
0x3C	Local Chip Select 0	CS0BASE	0x0800_0081
0x40	Local Chip Select 1	CS1BASE	0x0400_0201
0x44	Local Chip Select 2	CS2BASE	0x0100_0001
0x48	Local Chip Select 3	CS3BASE	0x0280_0001
0x4C	Serial EEPROM / Interrupt Control & Status	PROT_AREA / INTCSR	0x0030_0049
0x50	Miscellaneous	CNTRL	0x007A_4000
0x54	General Purpose I/O	GPIOC	0x0224_9252

Table 8-2 : PCI9030 Local Configuration Register

Shown values are register values after serial EEPROM configuration.

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8.1.3 PCI9030 Configuration EEPROM

Basic PCI9030 register configuration is loaded from an on board serial EEPROM at power-up or board reset.

EEPROM Offset	Register Offset	Register Description	Register Bits Affected	Value
0x00	PCI 0x02	Device ID	PCIIDR[31:16]	0x9030
0x02	PCI 0x00	Vendor ID	PCIIDR[15:0]	0x10B5
0x04	PCI 0x06	PCI Status	PCISR[15:0]	0x0280
0x06	PCI 0x04	PCI Command	Reserved	0x0000
0x08	PCI 0x0A	Class Code	PCICCR[15:0]	0x0680
0x0A	PCI 0x08	Class Code / Revision	PCICR[7:0] / PCIREV[7:0]	0x0000
0x0C	PCI 0x2E	Subsystem ID	PCISID[15:0]	0x2030
0x0E	PCI 0x2C	Subsystem Vendor ID	PCISVID[15:0]	0x1498
0x10	PCI 0x36	MSB New Capability Pointer	Reserved	0x0000
0x12	PCI 0x34	LSB New Capability Pointer	CAP_PTR[7:0]	0x0040
0x14	PCI 0x3E	Max_Lat, Max_Gnt	Reserved	0x0000
0x16	PCI 0x3C	Interrupt Pin	PCIIPR[7:0] / Reserved	0x0100
0x18	PCI 0x42	MSW Power Management Capabilities	PMC[14:11, 5, 3:0]	0x4801
0x1A	PCI 0x40	LSW Power Management Capabilities	PM_NEXT[7:0] / PMCAPID[7:0]	0x4801
0x1C	PCI 0x46	MSW Power Management Data / PMCSR Bridge Support Ext.	Reserved	0x0000
0x1E	PCI 0x44	LSW Power Management Control / Status	PMCSR[14:8]	0x0000
0x20	PCI 0x4A	MSW Hot Swap Control / Status	Reserved	0x0000
0x22	PCI 0x48	LSW Hot Swap Next Capability Pointer / Hot Swap Control	HS_NEXT[7:0] / HS_CNTL[7:0]	0x4C06
0x24	PCI 0x4E	PCI Vital Product Data Address	Reserved	0x0000
0x26	PCI 0x4C	PCI Vital Product Data Next Capability Pointer / PCI Vital Product Data Control	PVPD_NEXT[]7:0] / PVPD_CNTL[7:0]	0x0003
0x28	Local 0x02	MSW Local Space 0 Range	LAS0RR[31:16]	0x0FFF
0x2A	Local 0x00	LSW Local Space 0 Range	LAS0RR[15:0]	0xFF00
0x2C	Local 0x06	MSW Local Space 1 Range	LAS1RR[31:16]	0x0FFF
0x2E	Local 0x04	LSW Local Space 1 Range	LAS1RR[15:0]	0xFC00
0x30	Local 0x0A	MSW Local Space 2 Range	LAS2RR[31:16]	0x0E00
0x32	Local 0x08	LSW Local Space 2 Range	LAS2RR[15:0]	0x0000
0x34	Local 0x0E	MSW Local Space 3 Range	LAS3RR[31:16]	0x0F00
0x36	Local 0x0C	LSW Local Space 3 Range	LAS3RR[15:0]	0x0000
0x38	Local 0x12	MSW Local Exp. ROM Range	EROMRR[31:16]	0x0000
0x3A	Local 0x10	LSW Local Exp. ROM Range	EROMRR[15:0]	0x0000
0x3C	Local 0x16	MSW Local Space 0 Remap	LAS0BA[31:16]	0x0800
0x3E	Local 0x14	LSW Local Space 0 Remap	LAS0BA[15:0]	0x0001
0x40	Local 0x1A	MSW Local Space 1 Remap	LAS1BA[31:16]	0x0400

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EEPROM Offset	Register Offset	Register Description	Register Bits Affected	Value
0x42	Local 0x18	LSW Local Space 1 Remap	LAS1BA[31:16]	0x0001
0x44	Local 0x1E	MSW Local Space 2 Remap	LAS2BA[31:16]	0x0000
0x46	Local 0x1C	LSW Local Space 2 Remap	LAS2BA[31:16]	0x0001
0x48	Local 0x22	MSW Local Space 3 Remap	LAS3BA[31:16]	0x0200
0x4A	Local 0x20	LSW Local Space 3 Remap	LAS3BA[31:16]	0x0001
0x4C	Local 0x26	MSW Local Exp. ROM Remap	EROMBA[31:16]	0x0000
0x4E	Local 0x24	LSW Local Exp. ROM Remap	EROMBA[15:0]	0x0000
0x50	Local 0x2A	MSW Local Space 0 Descriptor	LAS0BRD[31:0]	0xD541
0x52	Local 0x28	LSW Local Space 0 Descriptor	LAS0BRD[15:0]	0x60A0
0x54	Local 0x2E	MSW Local Space 1 Descriptor	LAS1BRD[31:0]	0x1541
0x56	Local 0x2C	LSW Local Space 1 Descriptor	LAS1BRD[15:0]	0x20A2
0x58	Local 0x32	MSW Local Space 2 Descriptor	LAS2BRD[31:0]	0x1541
0x5A	Local 0x30	LSW Local Space 2 Descriptor	LAS2BRD[15:0]	0x20A2
0x5C	Local 0x36	MSW Local Space 3 Descriptor	LAS3BRD[31:0]	0x1501
0x5E	Local 0x34	LSW Local Space 3 Descriptor	LAS3BRD[15:0]	0x20A2
0x60	Local 0x3A	MSW Local Exp. ROM Descriptor	EROMBRD[31:16]	0x0000
0x62	Local 0x38	LSW Local Exp. ROM Descriptor	EROMBRD[15:0]	0x0000
0x64	Local 0x3E	MSW Local Chip Select 0	CS0BASE[31:16]	0x0800
0x66	Local 0x3C	LSW Local Chip Select 0	CS0BASE[15:0]	0x0081
0x68	Local 0x42	MSW Local Chip Select 1	CS1BASE[31:16]	0x0400
0x6A	Local 0x40	LSW Local Chip Select 1	CS1BASE[15:0]	0x0201
0x6C	Local 0x46	MSW Local Chip Select 2	CS2BASE[31:16]	0x0100
0x6E	Local 0x44	LSW Local Chip Select 2	CS2BASE[15:0]	0x0001
0x70	Local 0x4A	MSW Local Chip Select 3	CS3BASE[31:16]	0x0280
0x72	Local 0x48	LSW Local Chip Select 3	CS3BASE[15:0]	0x0001
0x74	Local 0x4E	Serial EEPROM Write Protect	PROT_AREA[7:0]	0x0030
0x76	Local 0x4C	LSW Interrupt Control / Status	INTCSR[15:0]	0x0049
0x78	Local 0x52	MSW Miscellaneous	CNTRL[31:16]	0x007A
0x7A	Local 0x50	LSW Miscellaneous	CNTRL[15:0]	0x4000
0x7C	Local 0x56	MSW General Purpose I/O Control	GPIOC[31:16]	0x0224
0x7E	Local 0x54	LSW General Purpose I/O Control	GPIOC[15:0]	0x9252
0x80	Local 0x72	MSW Power Management Data Select		0x0000
0x82	Local 0x70	LSW Power Management Data Select		0x0000
0x84	Local 0x76	MSW Power Management Data Scale		0x0000
0x86	Local 0x74	LSW Power Management Data Scale		0x0000

Table 8-3 : PCI9030 Configuration EEPROM Settings

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EEPROM Address	0x00	0x02	0x04	0x06	0x08	0x0A	0x0C	0x0E
0x00	0x9030	0x10B5	0x0280	0x0000	0x0680	0x0000	0x2030	0x1498
0x10	0x0000	0x0040	0x0000	0x0100	0x4801	0x4801	0x0000	0x0000
0x20	0x0000	0x4C06	0x0000	0x0003	0x0FFF	0xFF00	0x0FFF	0xFC00
0x30	0x0E00	0x0000	0x0F00	0x0000	0x0000	0x0000	0x0800	0x0001
0x40	0x0400	0x0001	0x0000	0x0001	0x0200	0x0001	0x0000	0x0000
0x50	0xD541	0x60A0	0x1541	0x20A2	0x1541	0x20A2	0x1501	0x20A2
0x60	0x0000	0x0000	0x0800	0x0081	0x0400	0x0201	0x0100	0x0001
0x70	0x0280	0x0001	0x0030	0x0049	0x007A	0x4000	0x0224	0x9252
0x80	0x0000	0x0000	0x0000	0x0000	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0x90	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xA0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xB0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xC0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xD0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xE0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xF0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF

Table 8-4 : PCI9030 Configuration EEPROM Content

8.2 IP Interface

The IP FPGA provides the interface between the PCI9030 local bus and the IP slots.

The IP FPGA also provides the IP Interface Control Registers.

The IP FPGA is configured at power-up or board reset by an on board serial PROM.

Board Initialization software should verify successful FPGA configuration in the Utility Status Register.

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8.2.1 PCI9030 Local Space Assignment

The PCI9030 local spaces must be used to access the IP interface. The PCI base address for each local space can be obtained from the PCI9030 PCI configuration register space.

PCI9030 Local Space	Size (Byte)	Port Width (Bit)	Endian Mode	PCI Space	IP Interface Space
0	256	16	Big	Mem	IP Interface Register
1	1 K	16	Big	Mem	IP A-D ID, INT, IO Space
2	32 M	16	Big	Mem	IP A-D MEM Space (16 bit)
3	16 M	8	Big	Mem	IP A-D MEM Space (8 bit)

Table 8-5 : PCI9030 Local Space Assignment

8.2.2 Local Space 0 Address Map

The PCI9030 local space 0 is used for the IP interface registers.

The PCI base address for local space 0 is PCIBAR2 at offset 0x18 in the PCI9030 PCI configuration register space.

Offset (Base = PCI Base Address 2)	Size (Byte)	Register
0x00	2	REVISION ID
0x02	2	IP A CONTROL
0x04	2	IP B CONTROL
0x06	2	IP C CONTROL
0x08	2	IP D CONTROL
0x0A	2	RESET
0x0C	2	STATUS
0x0E	2	Reserved
0x10 - 0xFF	240	Reserved

Table 8-6 : Local Space 0 Address Map (IP Interface Register)

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8.2.3 IP Interface Register

8.2.3.1 Revision ID Register

The Revision ID Register shows the revision of the on board IP FPGA logic.

Bit	Name	Description
15 (MSB)	-	Read : Undefined Write : No Effect
14		
13		
12		
11		
10		
9		
8		
7	REV_ID	Read: FPGA Logic Revision ID Write : No Effect
6		
5		
4		
3		
2		
1		
0 (LSB)		

Table 8-7 : Revision ID Register

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8.2.3.2 IP X Control Registers

The IP X Control Registers can be used to control IP interrupts, recover time and clock rate.

There is one IP X Control Register for each IP Slot (A-D).

Bit	Name	Description
15 (MSB)	-	Read : Undefined Write : No Effect. Should be written with 0's
14		
13		
12		
11		
10		
9		
8		
7	INT1_EN	0 : IP Interrupt 1 Disabled 1 : IP Interrupt 1 Enabled
6	INT0_EN	0 : IP Interrupt 0 Disabled 1 : IP Interrupt 0 Enabled
5	INT1_SENSE	0 : IP Interrupt 1 Level Sensitive 1 : IP Interrupt 1 Edge Sensitive
4	INT0_SENSE	0 : IP Interrupt 0 Level Sensitive 1 : IP Interrupt 0 Edge Sensitive
3	ERR_INT_EN	0 : IP Error Interrupt Disabled 1 : IP Error Interrupt Enabled
2	TIME_INT_EN	0 : IP Timeout Interrupt Disabled 1 : IP Timeout Interrupt Enabled
1	RECOVER	0 : IP Recover Time Disabled 1 : IP Recover Time Enabled
0 (LSB)	CLKRATE	0 : IP Clock Rate 8 MHz 1 : IP Clock Rate 32 MHz

Table 8-8 : IP X Control Register

After power-up or board reset all bits in the IP X Control Registers are cleared.

If IP recover time is enabled for an IP slot, an IP cycle for this slot will not begin until the IP recover time is expired. The IP recover time is app. 1µs.

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8.2.3.3 Reset Register

The Reset Register can be used to assert the IP RESET# signal and to detect when the IP RESET# signal is negated.

Bit	Name	Description
15 (MSB)	-	Read : Undefined Write : No Effect. Should be written with 0's
14		
13		
12		
11		
10		
9		
8		
7		
6		
5		
4		
3		
2		
1		
0 (LSB)	IP_RESET	Read : 0 : IP RESET# Signal is De-asserted 1 : IP RESET# Signal is Asserted Write : 0 : No Effect 1 : Assert IP RESET# Signal (Automatic Negation)

Table 8-9 : Reset Register

The IP RESET# signal is also asserted at power-up or board reset.

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8.2.3.4 Status Register

The Status Register can be used to read IP timeout, error and interrupt status.

The IP timeout time is app. 8µs.

An IP timeout occurs if the IP module fails to generate the IP ACK# signal within the IP timeout time. An IP timeout is not reported to the PCI9030 or the PCI Master, but in the Status Register. For timeout reads all F's are returned.

Bit	Name	Description
15 (MSB)	TIME_D	Read : 0 : No Timeout on IP_D 1 : IP_D Timeout has occurred Write : 0 : No Effect 1 : Clear IP_D Timeout Status
14	TIME_C	Read : 0 : No Timeout on IP_C 1 : IP_C Timeout has occurred Write : 0 : No Effect 1 : Clear IP_C Timeout Status
13	TIME_B	Read : 0 : No Timeout on IP_B 1 : IP_B Timeout has occurred Write : 0 : No Effect 1 : Clear IP_B Timeout Status
12	TIME_A	Read : 0 : No Timeout on IP_A 1 : IP_A Timeout has occurred Write : 0 : No Effect 1 : Clear IP_A Timeout Status
11	ERR_D	Read : 0 : No Error on IP_D 1 : IP_D ERROR# Signal Asserted Write : No Effect
10	ERR_C	Read : 0 : No Error on IP_C 1 : IP_C ERROR# Signal Asserted Write : No Effect
9	ERR_B	Read : 0 : No Error on IP_B 1 : IP_B ERROR# Signal Asserted Write : No Effect

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Bit	Name	Description
8	ERR_A	Read : 0 : No Error on IP_A 1 : IP_A ERROR# Signal Asserted Write : No Effect
7	INT1_D	Read : 0 : No Interrupt 1 Request on IP_D 1 : Active IP_D Interrupt 1 Request Write : 0 : No Effect 1 : Clear Edge Sensitive IP_D Interrupt 1 Status
6	INT0_D	Read : 0 : No Interrupt 0 Request on IP_D 1 : Active IP_D Interrupt 0 Request Write : 0 : No Effect 1 : Clear Edge Sensitive IP_D Interrupt 0 Status
5	INT1_C	Read : 0 : No Interrupt 1 Request on IP_C 1 : Active IP_C Interrupt 1 Request Write : 0 : No Effect 1 : Clear Edge Sensitive IP_C Interrupt 1 Status
4	INT0_C	Read : 0 : No Interrupt 0 Request on IP_C 1 : Active IP_C Interrupt 0 Request Write : 0 : No Effect 1 : Clear Edge Sensitive IP_C Interrupt 0 Status
3	INT1_B	Read : 0 : No IP_B Interrupt 1 Request 1 : Active IP_B Interrupt 1 Request Write : 0 : No Effect 1 : Clear Edge Sensitive IP_B Interrupt 1 Status
2	INT0_B	Read : 0 : No Interrupt 0 Request on IP_B 1 : Active IP_B Interrupt 0 Request Write : 0 : No Effect 1 : Clear Edge Sensitive IP_B Interrupt 0 Status
1	INT1_A	Read : 0 : No Interrupt 1 Request on IP_A 1 : Active IP_A Interrupt 1 Request Write : 0 : No Effect 1 : Clear Edge Sensitive IP_A Interrupt 1 Status

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Bit	Name	Description
0 (LSB)	INT0_A	Read : 0 : No Interrupt 0 Request on IP_A 1 : Active IP_A Interrupt 0 Request Write : 0 : No Effect 1 : Clear Edge Sensitive IP_A Interrupt 0 Status

Table 8-10 : Status Register

8.2.4 Local Space 1 Address Map

The PCI9030 local space 1 is used for the IP A-D ID, INT and I/O space.

The PCI base address for local space 1 is PCIBAR3 at offset 0x1C in the PCI9030 PCI configuration register space.

Offset (Base = PCI Base Address 3)		Size (Byte)	Description
Start	End		
0x0000_0000	0x0000_007F	128	IP A I/O Space
0x0000_0080	0x0000_00BF	64	IP A ID Space
0x0000_00C0	0x0000_00FF	64	IP A INT Space
0x0000_0100	0x0000_017F	128	IP B I/O Space
0x0000_0180	0x0000_01BF	64	IP B ID Space
0x0000_01C0	0x0000_01FF	64	IP B INT Space
0x0000_0200	0x0000_027F	128	IP C I/O Space
0x0000_0280	0x0000_02BF	64	IP C ID Space
0x0000_02C0	0x0000_02FF	64	IP C INT Space
0x0000_0300	0x0000_037F	128	IP D I/O Space
0x0000_0380	0x0000_03BF	64	IP D ID Space
0x0000_03C0	0x0000_03FF	64	IP D INT Space

Table 8-11 : Local Space 1 Address Map (IP A-D ID, INT, I/O Space)

The TVME8240 will perform write cycles to the IP ID space.

Any access to the IP INT space will assert the IP INTSEL# signal on the selected IP slot. The TVME8240 will perform write cycles to the IP INT space.

The user should perform IP INT space read cycles on the desired IP slot to generate an IP INTSEL# cycle and read the interrupt vector. For this read cycle the address must reflect if the IP INTSEL# cycle is for IP INT0# or for IP INT1#.

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8.2.5 Local Space 2 Address Map

The PCI9030 local space 2 is used for the IP A-D Memory space (16 bit port).

The PCI base address for local space 2 is PCIBAR4 at offset 0x20 in the PCI9030 PCI configuration register space.

Offset (Base = PCI Base Address 4)		Size (Byte)	Description
Start	End		
0x0000_0000	0x007F_FFFF	8 M	IP A MEM Space (16 bit)
0x0080_0000	0x00FF_FFFF	8 M	IP B MEM Space (16 bit)
0x0100_0000	0x017F_FFFF	8 M	IP C MEM Space (16 bit)
0x0180_0000	0x01FF_FFFF	8 M	IP D MEM Space (16 bit)

Table 8-12 : Local Space 2 Address Map (IP A-D Memory Space 16 bit)

8.2.6 Local Space 3 Address Map

The PCI9030 local space 3 is used for the IP A-D Memory space (8 bit port).

The PCI base address for local space 3 is PCIBAR5 at offset 0x24 in the PCI9030 PCI configuration register space.

Offset (Base = PCI Base Address 5)		Size (Byte)	Description
Start	End		
0x0000_0000	0x003F_FFFF	4 M	IP A MEM Space (8 bit)
0x0040_0000	0x007F_FFFF	4 M	IP B MEM Space (8 bit)
0x0080_0000	0x00BF_FFFF	4 M	IP C MEM Space (8 bit)
0x00C0_0000	0x00FF_FFFF	4 M	IP D MEM Space (8 bit)

Table 8-13 : Local Space 3 Address Map (IP A-D Memory Space 8 bit)

The 8 bit IP Memory space should be used for memory space linear byte addressing of IP modules that use IP data lines D7:0 only.

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8.3 IP Interrupts

The IP FPGA maps all IP interface interrupts sources (Timeout, Error, INT0, INT1) to the PCI9030 local interrupt input 1 (LINT1#).

The PCI9030 PCI Target Chip maps its local interrupt inputs to its PCI interrupt output (INTA#).

The PCI9030 PCI interrupt output is mapped to the serial interrupt no. 4 of the MPC8240 EPIC.

The PCI9030 local interrupt 2 (LINT2#) is not used.

Upon detecting EPIC Serial Interrupt No. 4 read the IP Status Register to determine the IP interrupt source.

Timeout interrupts and edge sensitive IP interrupts must be cleared in the IP Status Register.

Error interrupts should be disabled after being noticed once.

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9 Board I/O

9.1 Board I/O Overview

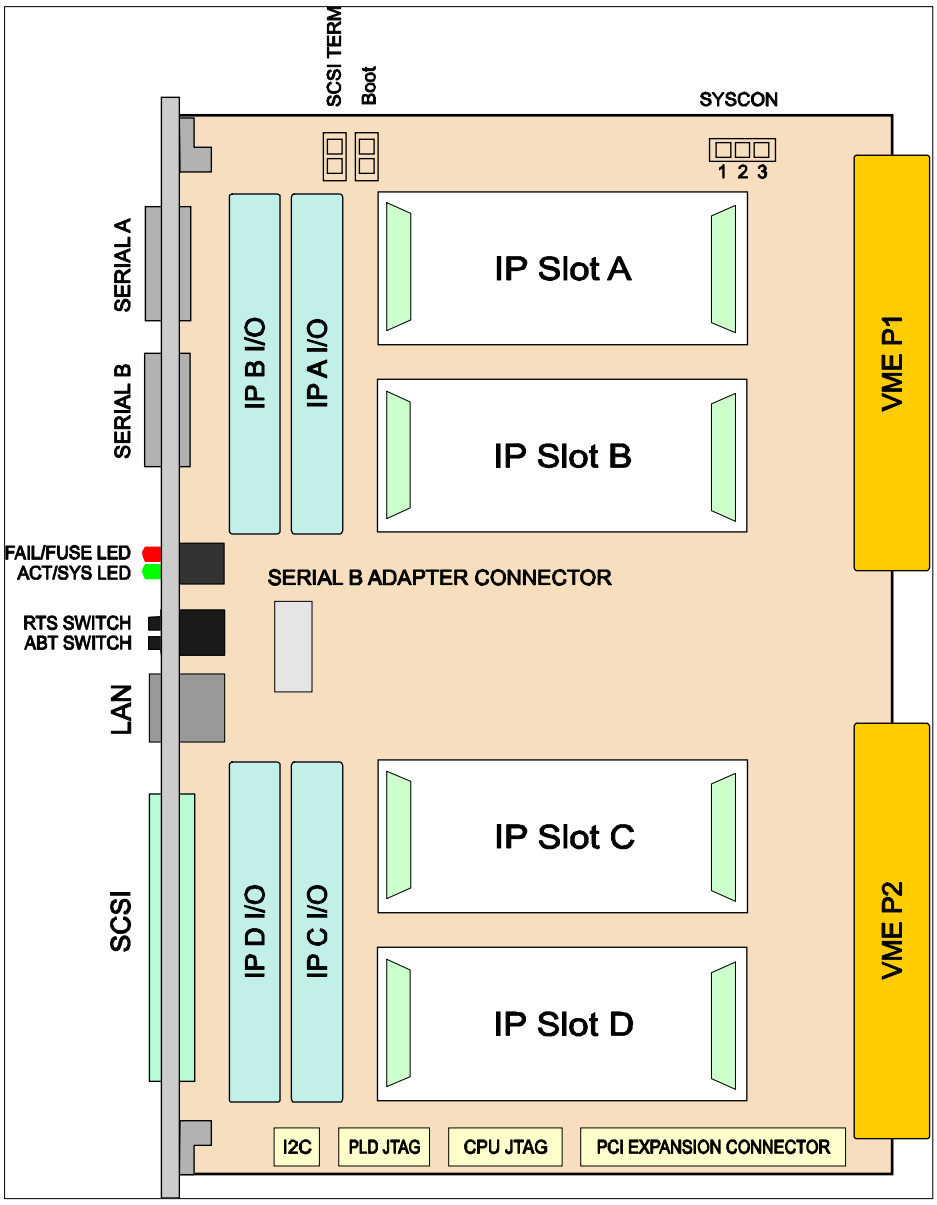


Figure 9-1 : Board I/O Overview

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9.2 Jumper

9.2.1 Boot Jumper

Boot Jumper	
Jumper Installed	Execute Memory FLASH Program after board initialization
No Jumper Installed	Execute PMON Bug Program after board initialization

Table 9-1 : Boot Jumper

The boot jumper status can be read in the Utility Status Register.

After board initialization the boot jumper determines the address of the next program instruction.

The 8 bit wide socket Boot FLASH must always be installed and provide the board initialization code at the system reset vector.

If used, the first instruction in the Memory FLASH must reside at address 0xFF00_0100.

9.2.2 VME System Controller Jumper

VME SYSTEM CONTROLLER JUMPER	
Jumper 1-2 Installed	Not VME System Controller
Jumper 2-3 Installed	VME System Controller Auto Configuration
No Jumper Installed	VME System Controller

Table 9-2 : VME System Controller Jumper

The VME system controller jumper controls the Universe-II BGIN3# input signal, which the Universe-II samples at the end of VME SYSRST# to determine VME System Controller mode.

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9.3 LEDs

During board reset all LEDs are ON.

9.3.1 FAIL LED

The FAIL LED (Red) can be set by software control via the Utility LED Register to indicate a failure condition.

9.3.2 FUSE LED

The FUSE LED (Red) is set by hardware control if any of the on board resettable fuses triggers.

There is one resettable fuse for each of the following power supplies:

- IP Slot A/B +5V
- IP Slot C/D +5V
- IP Slot A/B/C/D +12V
- IP Slot A/B/C/D -12V
- VME P2 LAN +12V

9.3.3 ACT LED

The ACT (Activity) LED (Green) is set by hardware control if there is any activity on the Local Memory bus or PCI bus.

9.3.4 SYS LED

The SYS (System Controller) LED (Green) is set by hardware control if the Universe (VME-PCI Bridge) is the VME bus System Controller.

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9.4 Switches

9.4.1 RST Switch

The RST (RESET) switch can be used to generate a board reset.

A board reset is also performed at power-up.

A board reset can also be asserted by software programming the Utility Control Register.

A board reset will perform a general board hardware reset, re-configuration of the IP FPGA, PCI reset and CPU reset.

If the TVME8240 is the VME bus system controller, a board reset will also trigger a VME bus system reset.

9.4.2 ABT Switch

The ABT (ABORT) switch can be used to generate a CPU interrupt.

The Abort Switch is mapped to serial interrupt no. 1 of the MPC8240 EPIC. Serial interrupt no. 1 must be configured as edge sensitive.

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9.5 Connectors

9.5.1 VME Interface Connectors

9.5.1.1 VME P1 Connector

Pin	Row A	Row B	Row C
1	VME_D0	VME_BBSY#	VME_D8
2	VME_D1	VME_BCLR#	VME_D9
3	VME_D2	VME_ACFAIL#	VME_D10
4	VME_D3	VME_BGIN0#	VME_D11
5	VME_D4	VME_BGOUT0#	VME_D12
6	VME_D5	VME_BGIN1#	VME_D13
7	VME_D6	VME_BGOUT1#	VME_D14
8	VME_D7	VME_BGIN2#	VME_D15
9	GND	VME_BGOUT2#	GND
10	VME_SYSCLK	VME_BGIN3#	VME_SYSFAIL#
11	GND	VME_BGOUT3#	VME_BERR#
12	VME_DS1#	VME_BR0#	VME_SYSRST#
13	VME_DS0#	VME_BR1#	VME_LWORD#
14	VME_WRITE#	VME_BR2#	VME_AM5
15	GND	VME_BR3#	VME_A23
16	VME_DTACK#	VME_AM0	VME_A22
17	GND	VME_AM1	VME_A21
18	VME_AS#	VME_AM2	VME_A20
19	GND	VME_AM3	VME_A19
20	VME_IACK#	GND	VME_A18
21	VME_IACKIN#	NC	VME_A17
22	VME_IACKOUT#	NC	VME_A16
23	VME_AM4	GND	VME_A15
24	VME_A7	VME_IRQ7#	VME_A14
25	VME_A6	VME_IRQ6#	VME_A13
26	VME_A5	VME_IRQ5#	VME_A12
27	VME_A4	VME_IRQ4#	VME_A11
28	VME_A3	VME_IRQ3#	VME_A10
29	VME_A2	VME_IRQ2#	VME_A9
30	VME_A1	VME_IRQ1#	VME_A8
31	-12V	NC	+12V
32	+5V	+5V	+5V

Table 9-3 : VME P1 Connector

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9.5.1.2 VME P2 Connector

Pin	Row A	Row B	Row C
1	SCSI_D0#	+5V	AUI_CD-
2	SCSI_D1#	GND	AUI_CD+
3	SCSI_D2#	NC	AUI_TD-
4	SCSI_D3#	VME_A24	AUI_TD+
5	SCSI_D4#	VME_A25	AUI_RD-
6	SCSI_D5#	VME_A26	AUI_RD+
7	SCSI_D6#	VME_A27	+12VLAN
8	SCSI_D7#	VME_A28	NC
9	SCSI_PAR0	VME_A29	NC
10	SCSI_ATN#	VME_A30	NC
11	SCSI_BSY#	VME_A31	NC
12	SCSI_ACK#	GND	NC
13	SCSI_RST#	+5V	NC
14	SCSI_MSG#	VME_D16	NC
15	SCSI_SEL#	VME_D17	NC
16	SCSI_CD#	VME_D18	NC
17	SCSI_REQ#	VME_D19	NC
18	SCSI_IO#	VME_D20	SER_RXDB+ (i)
19	SER_TXDB+ (o)	VME_D21	NC
20	NC	VME_D22	SER_CTSB+ (i)
21	NC	VME_D23	NC
22	NC	GND	NC
23	NC	VME_D24	NC
24	NC	VME_D25	NC
25	SER_RXDB(-) (i)	VME_D26	NC
26	SER_TXDB(-) (o)	VME_D27	SER_RTSB+ (o)
27	SER_CTSB(-) (i)	VME_D28	SER_TXDA (o)
28	NC	VME_D29	SER_RXDA (i)
29	SER_RTSB(-) (o)	VME_D30	SER_RTSA (o)
30	NC	VME_D31	SER_CTSA (i)
31	NC	GND	SER_DTRA (o)
32	NC	+5V	SER_DCDA (i)

Table 9-4 : VME P2 Connector

The serial port signals (SER_x) are shown in the TVME8240 pin function. E.g. for serial port A the external TXD line must be connected to pin C28 (SER_RXDA), NOT to pin C27 (SER_TXDA).

For serial port B: The SER_xB+ pins are used as the RS422+ signal lines when the RS422 adapter is used. The SER_xB(-) pins are used as the RS232 signal lines when the RS232 adapter is used and are used as the RS422- signal lines when the RS422 adapter is used.

For each serial port only one connection scheme is allowed at a time, either via the VME P2 connector or via the front plate DB9 connector.

Please see the SCSI Interface section for using 16bit SCSI Targets on the VME P2 connector.

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9.5.2 IP Interface Connectors

9.5.2.1 IP P1 Connector

Pin	Signal	Pin	Signal
1	GND	2	CLK
3	RESET#	4	D0
5	D1	6	D2
7	D3	8	D4
9	D5	10	D6
11	D7	12	D8
13	D9	14	D10
15	D11	16	D12
17	D13	18	D14
19	D15	20	BS0#
21	BS1#	22	-12V
23	+12V	24	+5V
25	GND	26	GND
27	+5V	28	WRITE#
29	IDSEL#	30	NC
31	MEMSEL#	32	NC
33	INTSEL#	34	DMAACK#
35	IOSEL#	36	RSV0
37	A1	38	DMAEND#
39	A2	40	ERROR#
41	A3	42	INTREQ0#
43	A4	44	INTREQ1#
45	A5	46	STROBE#
47	A6	48	ACK#
49	RSV1	50	GND

Table 9-5 : IP P1 Connector

The following signals have an on board pull-up resistor (4K7, 3.3V):

RESET#, WRITE#, IDSEL#, IOSEL#, INTSEL#, MEMSEL#, DMAACK#. DMAEND#, ERROR#, INTREQ0#, INTREQ1#, RSV0, RSV1, STROBE#, ACK#.

DMA is not supported on the IP interface.

9.5.2.2 IP P2 Connector

For each IP slot the IP P2 connector signals (IP module I/O lines) are routed directly to the appropriate pins of the 50P IP I/O ribbon cable connector.

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9.5.3 PCI Expansion Connector

Pin	Signal		Pin	Signal
1	+3.3V		2	+3.3V
3	CLK		4	INTA#
5	GND		6	INTB#
7	PONRST#		8	INTC#
9	HRST#		10	INTD#
11	TDO		12	TDI
13	TMS		14	TCK
15	TRST#		16	PRSNT#
17	GNT#	GND	18	REQ#
19	+12V		20	-12V
21	PERR#		22	SERR#
23	LOCK#		24	SDONE
25	DEVSEL#		26	SBO#
27	GND		28	GND
29	TRDY#		30	IRDY#
31	STOP#		32	FRAME#
33	GND		34	GND
35	ACK64#		36	NC
37	REQ64#		38	NC
39	PAR		40	RST#
41	C/BE1#		42	C/BE0#
43	C/BE3#		44	C/BE2#
45	AD1		46	AD0
47	AD3		48	AD2
49	AD5		50	AD4
51	AD7		52	AD6
53	AD9		54	AD8
55	AD11		56	AD10
57	AD13	+5V	58	AD12
59	AD15		60	AD14
61	AD17		62	AD16
63	AD19		64	AD18
65	AD21		66	AD20
67	AD23		68	AD22
69	AD25		70	AD24
71	AD27		72	AD26
73	AD29		74	AD28
75	AD31		76	AD30
77	PAR64		78	NC
79	C/BE5#		80	C/BE4#
81	C/BE7#		82	C/BE6#

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Pin	Signal		Pin	Signal
83	AD33		84	AD32
85	AD35		86	AD34
87	AD37		88	AD36
89	AD39		90	AD38
91	AD41		92	AD40
93	AD43		94	AD42
95	AD45	GND	96	AD44
97	AD47		98	AD46
99	AD49		100	AD48
101	AD51		102	AD50
103	AD53		104	AD52
105	AD55		106	AD54
107	AD57		108	AD56
109	AD59		110	AD58
111	AD61		112	AD60
113	AD63		114	AD62

Table 9-6 : PCI Expansion Connector

The PCI Expansion Connector type is AMP 2-767004-4.

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9.5.4 Serial Interface Connectors

9.5.4.1 Serial Port A

Pin	Signal
1	DCD (input)
2	RXD (input)
3	TXD (output)
4	DTR (output)
5	GND
6	DSR (input)
7	RTS (output)
8	CTS (input)
9	RI (input)

Table 9-7 : Serial Port A DB9 male Connector

9.5.4.2 Serial Port B

RS232 Adapter (TVME8240-A1-10)

The RS232 adapter card (TVME824-A1-10) will be delivered with every TVME8240 board.

Pin	Signal
1	Reserved
2	RXD (input)
3	TXD (output)
4	Reserved
5	GND
6	Reserved
7	RTS (output)
8	CTS (input)
9	Reserved

Table 9-8 : Serial Port B DB9 male Connector (RS232)

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RS422 Adapter (TVME8240-A1-11)

The RS422 adapter card (TVME8240-A1-11) can be ordered separately.

Pin	RS422
1	RXD+ (input)
2	RXD- (input)
3	TXD- (output)
4	TXD+ (output)
5	GND
6	RTS+ (output)
7	RTS- (output)
8	CTS- (input)
9	CTS+ (input)

Table 9-9 : Serial Port B DB9 male Connector (RS422)

The serial port signals are shown in the TVME8240 pin function. E.g. for serial port A the external TXD line must be connected to pin 2 (RXD input) of the serial port A connector, not to pin 3 (TXD output).

The serial interface signals are also available on the VME P2 connector.

For each serial port only one connection scheme is allowed at a time, either via the VME P2 connector or via the DB9 connector at the front plate.

Serial port A mode is RS232 always. Serial port B mode is configurable by an adapter card. Factory default is RS232 adapter card. A RS422 adapter card can be ordered.

9.5.5 LAN Interface Connector

Pin	Signal
1	TD+
2	TD-
3	RD+
4	NC
5	NC
6	RD-
7	NC
8	NC

Table 9-10 : LAN Connector 8P RJ45

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10 Installation and Use Notes

10.1 NVRAM Real-Time Clock Control

The TVME8240 provides a M48T59 NVRAM / RTC device with a snaphat battery plugged on top. The snaphat battery provides power for the SRAM cells when the main power supply is off.

The TVME8240 is shipped with the snaphat battery installed on top of the M48T59 NVRAM device. The Real-Time Clock function of the M48T59 device is **turned-off by default**, to save battery energy.

If the M48T59 Real-Time Clock function has been turned-off (factory default), it must be enabled again, before using any other board resources (e.g. Ethernet).

The PMON "date" command can be used to enable the Real-Time Clock function.

Setup / Start the Real-Time Clock function:

```
PMON> date 200408101445.00
Tue Aug 10 14:45:00 2004
PMON> reboot
```

Stop the Real-Time Clock function :

(This is recommended for TVME8240 board storage) :

```
PMON> date -x
Clock is stopped...
PMON>
```


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11 Technical Information

11.1 Processor

- Motorola MPC8240 Integrated Host PPC (250 MHz Core Frequency)
- Embedded Version MPC603e (G2) Processor Core
- Floating Point Unit
- DMA Controller
- 16 Kbyte I-Cache, 16 kbyte D-Cache
- Four cascadable 31 bit timer

11.2 Memory

- 64 Mbyte 64 bit wide SDRAM (83 MHz)
- 8 Mbyte 64 bit wide Flash Memory

11.3 Other Devices

- 8 Kbyte NVRAM (M48T59) with exchangeable battery
- 1 Mbyte 8 bit wide Boot-Flash (two PLCC sockets)

11.4 VME Interface

- Tundra Universe-II
- A16-A32 Master/Slave Address Modes; D08-D64 Master/Slave Data Transfer Modes
- RR/PRI VME bus Arbiter
- IRQ 1-7 (any of seven IRQs)
- System Controller Jumper (Yes, No, Auto Detect)
- Four Location Monitors
- DMA Controller
- VME Bus Error Interrupt

11.5 Ethernet Interface

- Intel 21143TD Controller
- PCI DMA support
- 10Base-T, 100Base-TX Interface on RJ-45 front panel connector
- 10Base-T / 10Base2 AUI Port on VME P2 connector

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11.6 Asynchronous Serial Interface

- Dual 16C550 compatible UART (1.8432 MHz clock-source)
- Port 1 : RS232 configuration, Port 2 : RS232 Adapter (default), RS422 Adapter (option)
- Max baud rate 115kbps
- Two DB9 front panel connectors

11.7 PCI Expansion Connector

- 32 bit 33 MHz PCI Interface (114-pin connector)
- 5V PCI Signaling Voltage (PCI Expansion Board may drive 3.3V or 5V PCI signal levels, PCI Expansion Board must tolerate 5V PCI signal levels)
- Supports Motorola PMC-Span, TEWS' IP-Span (TVME230)

11.8 Power Requirements

The TVME8240 uses the +5V, +12V and -12V power supply pins available on the VME P1 and P2 connectors as the main power supply.

The TVME8240 +3.3V board power supply is generated on board (using the VME +5V power supply).

+ 5V Supply:

On board load: 2.8A typ., 4A max

Additional load (optional I/O):

- PCI Expansion Connector (unfused)
- IP interface (2A fused for IP slots A/B, 2A fused for IP slots C/D. Max. 2A for the total of IP slots A + B, max. 2A for the total of IP slots C + D)

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+ 12V Supply:

On board load: 3mA max. (not required for system function, only used in the 12V fuse status sensing logic.)

Additional load (optional I/O):

- PCI Expansion Connector (unfused)
- VME P2 Connector - LAN Power (1A fused)
- IP interface (Available on all IP slots, fused for a total of 2A, max. 1A per IP Slot)

- 12V Supply:

On board load: 3mA max. (not required for system function, only used in the 12V fuse status sensing logic.)

Additional load (optional I/O):

- PCI Expansion Connector (Unfused)
- IP interface (Available on all IP slots, fused for a total of 2A, max. 1A per IP Slot)

Power Supply Pins on VME Connectors:

The VME P1 and P2 connectors are rated for 2A max. @ 20°C (appr. 1.5A max. @ 70°C) per pin.

For the +5V power supply there are 3-pins on the VME P1 connector and 3-pins on the VME P2 connector.

For the +12V power supply there is 1-pin on the VME P1 connector.

For the -12V power supply there is 1-pin on the VME P1 connector.

This must be considered for the total power supply load (on board load plus additional I/O load).

11.9 IndustryPack Interface

11.9.1 Logic Interface

- Four single size / two double size IP slots
- Spaces available for each IP slot :
  128 byte I/O space, 64 byte ID space, 64 byte INT space, 8 Mbyte MEM space (16 bit), 4 Mbyte MEM space (8 bit linear)
- Data bus width : 16 bit
- Clock rate : 8 MHz / 32 MHz selectable for each IP slot

11.9.2 I/O Interface

- Four 50-pin planar connectors for ribbon cable front I/O
- 1A max continuous dc current per IP I/O line

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11.10 Physical Data

11.10.1 MTBF

(Based on calculation)

TVME8240 Board Option	MTBF Value
-11	205002h

Table 11-1 : MTBF Data

11.10.2 Temperature

Operating Temperature Range: 0°C to 55°C (forced air cooling)

Non-Operating Temperature Range: -40°C to 85°C

11.10.3 Weight

TVME8240-11 : 372.5 g

11.10.4 Humidity

5% to 90% (non-condensing)

11.10.5 Form Factor

- Standard one slot 6U VME
- 3-row (a, b, c) VME P1 & P2 connectors

(PCI expansion board occupies an additional VME slot if installed)

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