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# ADC1xD1xxxCVAL

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# ADC1xD1xxxCVAL

## 1. Introduction

The ADC1xD1x00QML products are low power, high performance 10b and 12b ADCs with sampling rates up to 1.6 GSPS as a dual channel ADC or 3.2 GSPS in a single channel interleaved mode. These products come in a hermetic 376 column ceramic grid array package (376 CCGA) for harsh environments, such as down hole or space.

The ADC1xD1x00 Evaluation Board (ADC1xD1x00CVAL) provides flexible ADC I/O connections for laboratory performance evaluation. As configured, the board is equipped with support shrouds for 100 pin Samtec connectors for interface to a logic analyzer, but capable of being configured for other types of logic analyzer connectors.

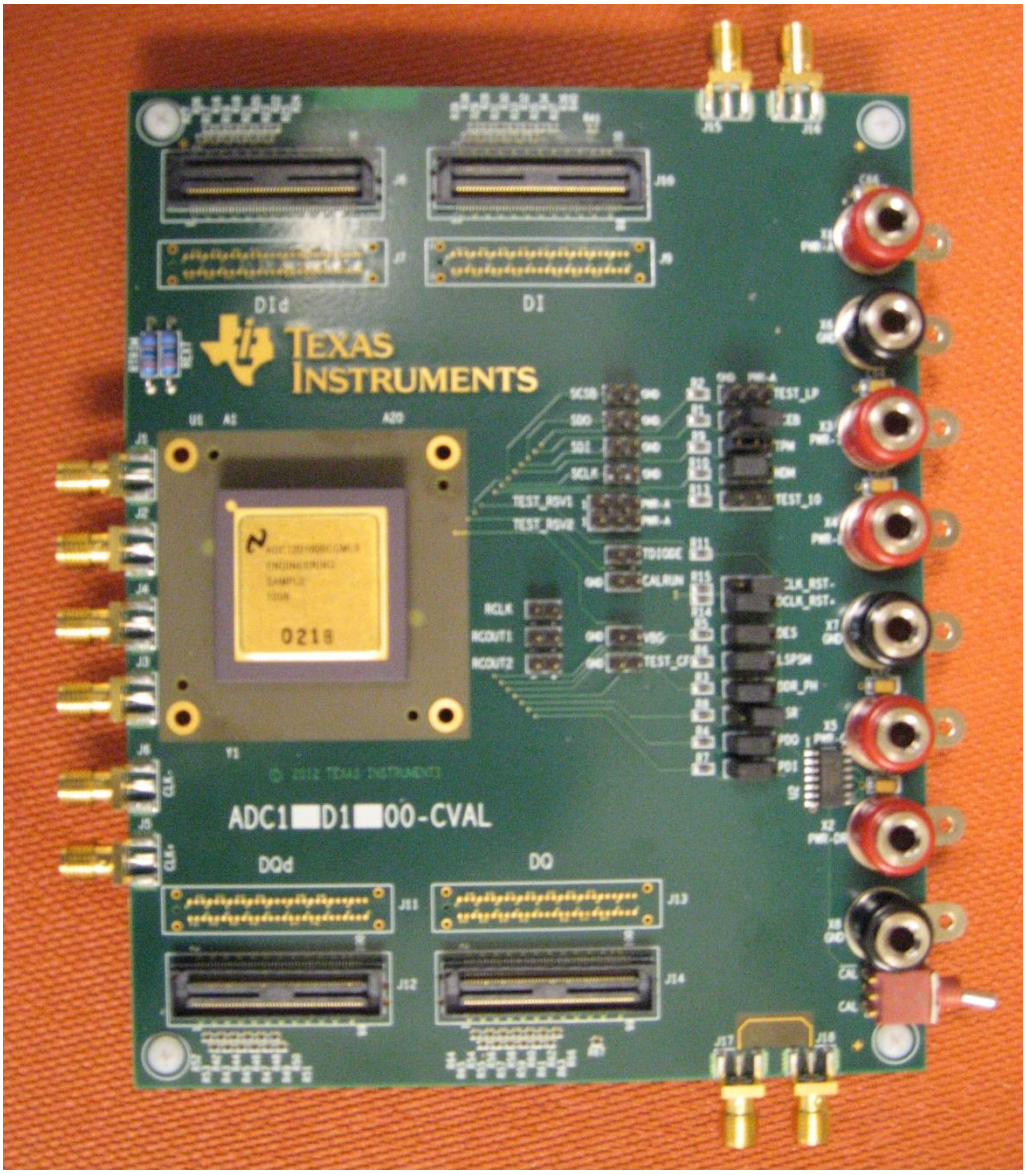



**Figure 1: Picture of Evaluation Board**

Because the 10- and 12-bit Gig ADCs are pin-compatible with one another, this board can be used with the following parts:

- ADC10D1000QML
- ADC12D1600QML

Refer to the individual product datasheets for information on Abs Max and operating conditions. .

## 2. Lab Equipment

The following lab equipment is required to use the ADC1xD1x00 EVAL board:

- Bench supply to drive 1.9V at 3A
- 1 signal generator + bandpass filter + balun to drive sampling clock. Suggested equipment:
  - SMA100A with B22 enhanced low phase-noise option
  - Trilithic 5VF tunable filter
- 1 signal generator to drive the analog input
- High-speed Logic Analyzer to capture the data. Suggested equipment:
  - Agilent 16702B Logic Analysis System
  - Agilent 16760A Timing and State Module
  - Agilent E5379A Differential Probe Adapter
  - Agilent E5386A Half-channel Probe Adapter (for data rates greater than 800MSPS)

Three key requirements for the sampling clock signal generator are low distortion, broad band noise, and phase noise. Even the highest quality signal generator will also produce harmonics, which the ADC performance is very sensitive to. Therefore, a bandpass filter, which can be tuned to the desired sampling clock frequency, will improve the performance of the system. In addition to this, the bandpass filter will reduce broadband noise and increase the system performance.

The logic analyzer should be able to capture differential LVDS signals at high speed, as determined by the sampling clock speed and ADC Demux Mode. In general, the Output Data Rate per Bank can be determined as follows:

| Mode | Output Data Rate per Bank [MSPS] |
|---|---|
| DES 1:1 Non-Demux | Fs/2 |
| DES 1:2 Demux | Fs/4 |
| Non-DES 1:1 Non-Demux | Fs |
| Non-DES 1:2 Demux | Fs/2 |

Table 1. Output Data Rate per Bank by Mode

For example, the ADC12D1600 will generate data at the following rates:

| Mode | Fclk [MHz] | Fs [MSPS] | Output Data Rate per Bank [MSPS] |
|---|---|---|---|
| DES 1:1 Non-Demux | 1600 | 3200 | 1600 |
| DES 1:2 Demux | 1600 | 3200 | 800 |
| Non-DES 1:1 Non-Demux | 1600 | 1600 | 1600 |
| Non-DES 1:2 Demux | 1600 | 1600 | 800 |

Table 2. ADC12D1600 Output Data Rate example

The EVAL board is designed to be used with the Samtec ASP-65067-01 for the logic analyzer probe connection to the Agilent E5379A Differential Probe Adapter. There is also a footprint for the Agilent E5405A Pro Series Soft Touch Connectorless Probe, but this option is not recommended, as the signal integrity is better via the Samtec connector.

### Optional Lab Equipment

If the EVAL board is being used in Extended Control Mode (ECM), then it is also necessary to have a system which can write to the SPI. One option is the Aardvark I2C/SPI Host Adapter and accessories.

- Aardvark I2C/SPI Host Adapter
  http://www.totalphase.com/products/aardvark_i2cspi/
- Level Shifter Board
  http://www.totalphase.com/products/level_shifter/
- 10-pin Split Cable
  http://www.totalphase.com/products/split_cable/

## 3. Driving the Clock and Inputs

### Driving the Sampling Clock

The CLK+/- SMA inputs are connected directly to the ADC; they must be driven AC-coupled and differentially. Therefore, a set of DC blocks is required at the input. To convert a single-ended signal to differential, a National Anaren balun board (400MHz - 3GHz) may conveniently be used.

### Driving the Analog Inputs

The analog inputs may be driven AC-coupled and must be driven differentially. Depending upon the application, an amplifier or balun board may be used to achieve single-ended to differential conversion.

## 4. Jumper Settings

Most of the jumper pins on the EVAL board are also available for customer use, and are more clearly explained in the datasheet; some exceptions are the TEST pins as described below. These pins are related to internal test functions and are not available.

The ADC may be used in either Extended Control Mode (ECM) or Non-ECM, a.k.a “pin-control mode”; this is set by the ECEb pin. In ECM, the ADC modes and settings are written to via the Serial Port Interface. Some control pins remain active in ECM.

| Pin (Board) | Pin (Datasheet) | I/O | Function |
|---|---|---|---|
| TEST_LP | N/A | N/A | Internal test function; do not connect |
| ECEB | ECEb | Input | ECM and Non-ECM: Extended Control Mode Enable bar select |
| TPN | TPM | Input | Non-ECM only: Test Pattern Mode select |
| NDM | NDM | Input | ECM and Non-ECM: Non-Demux Mode select |
| TEST_IO | N/A | N/A | Internal test function; do not connect |
| POR_EN | N/A | N/A | Internal test function; do not connect |
| DCLK_RST+/- | DCLK_RST+/- | Input | Differential DCLK Reset |
| DES | DES | Input | Non-ECM only: DES Mode select |
| LSPSM | LSPSM | Input | Low sampling power saving mode |
| DDR_PH | DDRPh | Input | Non-ECM only: DDR Phase select |
| FSR | FSR | Input | Non-ECM only: Full-Scale Range select |
| PDQ | PDQ | Input | ECM and Non-ECM: Power-Down Q-channel |
| PDI | PDI | Input | ECM and Non-ECM: Power-Down I-channel |
| SCSB | SCSb | Input | SPI: Serial Chip Select bar |
| SDO | SDO | Output | SPI: Serial Data Out |
| SDI | SDI | Input | SPI: Serial Data In |
| SCLK | SCLK | Input | SPI: Serial Clock |
| TEST_RSV1 | N/A | N/A | Internal test function; do not connect |
| TEST_RSV2 | N/A | N/A | Internal test function; do not connect |
| TDIODE | TDIODE+/- | Output | Temperature Sensor Diode terminals |
| CALRUN | CalRun | Output | Calibration Running indication |
| VBG | VBG | I/O | Bandgap Voltage Output / LVDS Common-mode Voltage select |
| TEST_CF | N/A | N/A | Internal test function; do not connect |
| RCLK | RCLK+/- | Input | AutoSync: Reference Clock Input |
| RCOUT1 | RCOut1+/- | Output | AutoSync: Reference Clock Differential Output 1 |
| RCOUT2 | RCOut2+/- | Output | AutoSync: Reference Clock Differential Output 2 |
| | | | |

Table 3. Control pins and function

In Non-ECM, the following control pins are available.

| Pin (Board) | Low | High | Floating |
|---|---|---|---|
| ECEB | ECM | Non-ECM | Not valid |
| TPN | Non-TPM | TPM | Not valid |
| NDM | 1:2 Demux | 1:1 NDM | Not valid |
| DES | Non-DES | DES | Not valid |
| LSPSM | Normal | Low sampling power saving | Not valid |
| DDR_PH | 0˚ Mode | 90˚ Mode | Not valid |
| FSR | See datasheet for details | | Not valid |
| PDQ | Q-channel active | Power Down Q-channel | Not valid |
| PDI | I-channel active | Power Down I-channel | Not valid |
| VBG | N/A | Higher LVDS common-mode voltage | Lower LVDS common-mode voltage |

Table 4. Non-ECM pin control settings

## 5. Board Power On

Refer to the individual product datasheets for information about ABS Max and operating conditions.

### Power supply

For flexibility, each of the different ADC power supply pins has been brought out to a red PWR terminal. It is recommended that all supply pins be powered from a single power supply source. The supply voltage to any of the PWR terminals must not exceed that applied to X-1 PWR (VA). The supply voltage is a nominal 1.9V and should not exceed 2V.

### Power on sequence

The ADC should be powered up in Non-ECM, by putting the ECEB pin high. The ADC does not have a Power on Reset. If the part is started in extended control mode (ECM), by having the ECEB pin low, the registers will come up in an unknown random state, and the part will be in an unknown operating condition. If ECM mode is desired, the board can be placed in ECM by moving the ECEB pin low after power up with the ECEB pin high.

After the board has stabilized the ADC should be calibrated by flipping the red CAL switch from low (CALb) to high (CAL). If the switch remains high, the part cannot be recalibrated in ECM. To enable the part to be recalibrated, in either ECM or with the switch, the CAL switch must be low (CALb). Recalibrate the part when there has been a major change in operating conditions, such as change in Fclk, or temperature.

The CLK+/- SMA inputs are connected directly to the ADC; they must be driven AC-coupled and differentially. Therefore, a set of DC blocks is required at the input. To convert a single-ended signal to differential, a National Anaren balun board (400MHz - 3GHz) may conveniently be used.

## 6. Samtec Connector

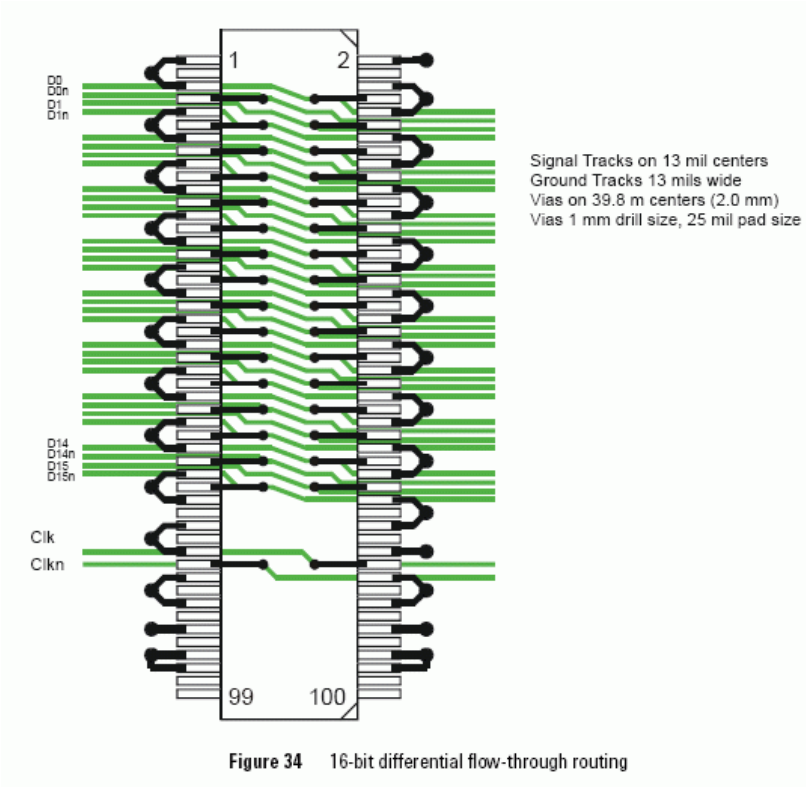



**Figure 2 Flow-through routing for the Samtec connector**

## Footprint dimensions

Use the following 100-pin Samtec connector footprint and support shroud mounting hole dimensions to design your target system board.

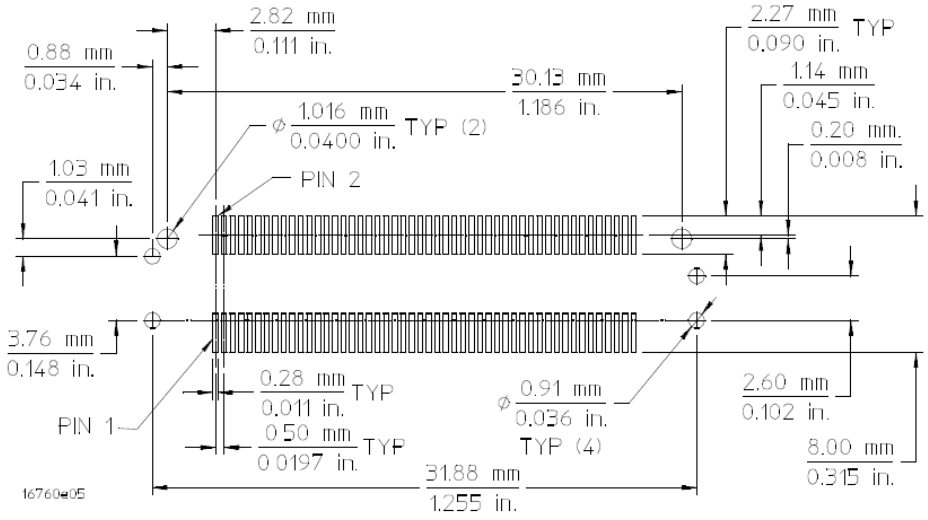



**Figure 8** 100-pin Samtec connector footprint and support shroud mounting hole dimensions

**Figure 3. Samtec connector footprint**

### Ordering Probing Connectors and Shrouds

Connectors and shrouds may be ordered in kits or ordered separately. Select a support shroud appropriate for the thickness of your PC board. The following table lists the Agilent part numbers for each.

**CAUTION** The support shrouds marked with an asterisk in the following table are made of conductive metal. Care should be taken to avoid shorting adjacent boards or components with the shrouds. For this reason it may be advisable not to connect the shrouds to ground.

| For Probe Model # | Agilent Part Number | Consists of | For Target PC Board Thickness |
|---|---|---|---|
| E5378A & E5379A | 16760-68702 | 5 Mating Connectors & 5 Support Shrouds* | up to 1.57 mm (0.062 in.) |
| | 16760-68703 | | up to 3.05 mm (0.120 in.) |

| E5379A Differential Probe | | | |
|---|---|---|---|
| Negative Signals | | Positive Signals | |
| Signal Name | Pin# | Signal Name | Pin# |
| Ground | 1 | Ground | 2 |
| Do Not Connect | 3 | Do Not Connect | 4 |
| Ground | 5 | Ground | 6 |
| D0N | 7 | D0 p | 8 |
| Ground | 9 | Ground | 10 |
| D1 n | 11 | D1 p | 12 |
| Ground | 13 | Ground | 14 |
| D2 n | 15 | D2 p | 16 |
| Ground | 17 | Ground | 18 |
| D3 n | 19 | D3 p | 20 |
| Ground | 21 | Ground | 22 |
| D4 n | 23 | D4 p | 24 |
| Ground | 25 | Ground | 26 |
| D5 n | 27 | D5 p | 28 |
| Ground | 29 | Ground | 30 |
| D6 n | 31 | D6 p | 32 |
| Ground | 33 | Ground | 34 |
| D7 n | 35 | D7 p | 36 |
| Ground | 37 | Ground | 38 |
| D8 n | 39 | D8 p | 40 |
| Ground | 41 | Ground | 42 |
| D9 n | 43 | D9 p | 44 |
| Ground | 45 | Ground | 46 |
| D10 n | 47 | D10 p | 48 |
| Ground | 49 | Ground | 50 |
| D11 n | 51 | D11 p | 52 |
| Ground | 53 | Ground | 54 |
| D12 n | 55 | D12 p | 56 |

| E5379A Differential Probe | | | |
|---|---|---|---|
| Negative Signals | | Positive Signals | |
| Signal Name | Pin# | Signal Name | Pin# |
| Ground | 57 | Ground | 58 |
| D13 n | 59 | D13 p | 60 |
| Ground | 61 | Ground | 62 |
| D14 n | 63 | D14 p | 64 |
| Ground | 65 | Ground | 66 |
| D15 n | 67 | D15 p | 68 |
| Ground | 69 | Ground | 70 |
| NC | 71 | NC | 72 |
| Ground | 73 | Ground | 74 |
| NC | 75 | NC | 76 |
| Ground | 77 | Ground | 78 |
| D16/Clk n | 79 | D16/Clk p | 80 |
| Ground | 81 | Ground | 82 |
| NC | 83 | NC | 84 |
| Ground | 85 | Ground | 86 |
| NC | 87 | Ground | 88 |
| N/C | 89 | N/C | 90 |
| NC | 91 | NC | 92 |
| Ground | 93 | Ground | 94 |
| Ground | 95 | Ground | 96 |
| Do not connect | 97 | Do not connect | 98 |
| Do not connect | 99 | Do not connect | 100 |

**Figure 4. Samtec connector ordering information**

## 7. Using the Aardvark

The Aardvark I2C/SPI Host Adapter is a fast and powerful I2C bus and SPI bus host adapter through USB (see Figure 6). It allows a developer to interface a Linux or Windows PC to a downstream embedded system environment and transfer serial messages using the I2C and SPI protocols.

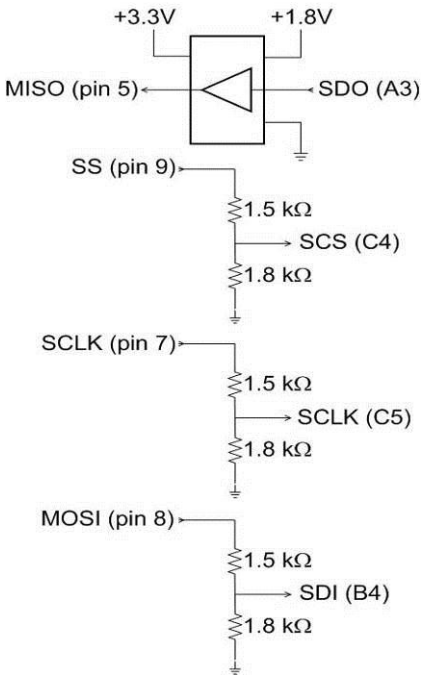
Part Number: TP240141
RoHS Compliant: Yes




**Figure 5. Aardvark I2C/SPI Host Adapter**

For more information please visit the manufacturer website at: **http://www.totalphase.com/products/aardvark_i2cspi/**

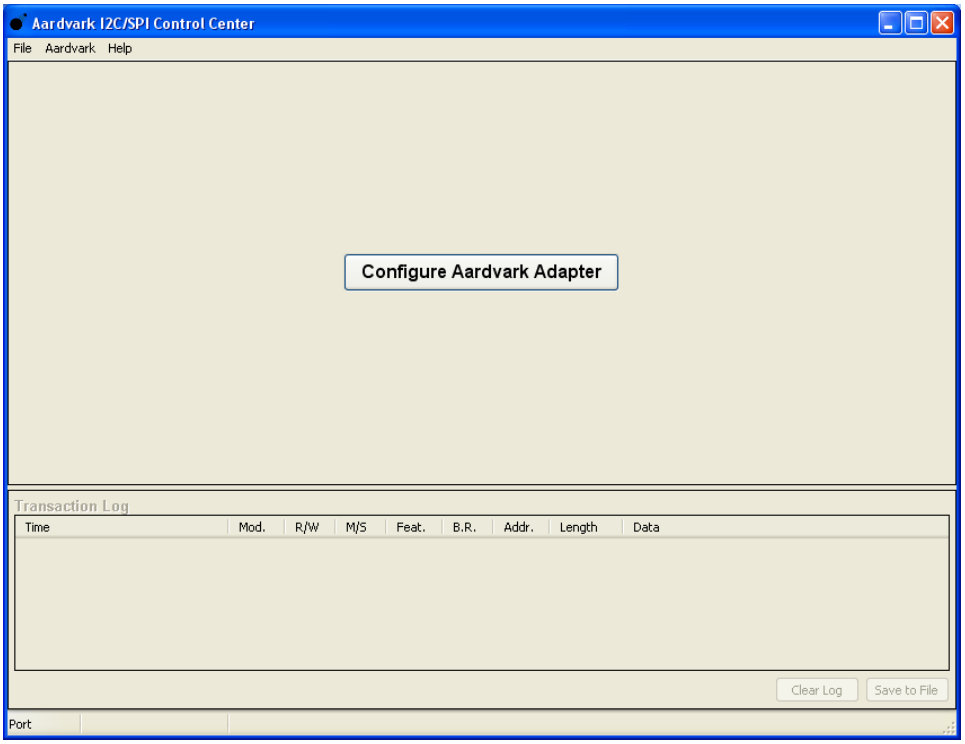
Level translation is required due to the different signaling levels (3.3V for the Aardvark vs. 1.9V for the ADC). A level shifter can be obtained from Total Phase or can be built as shown Figure 6.



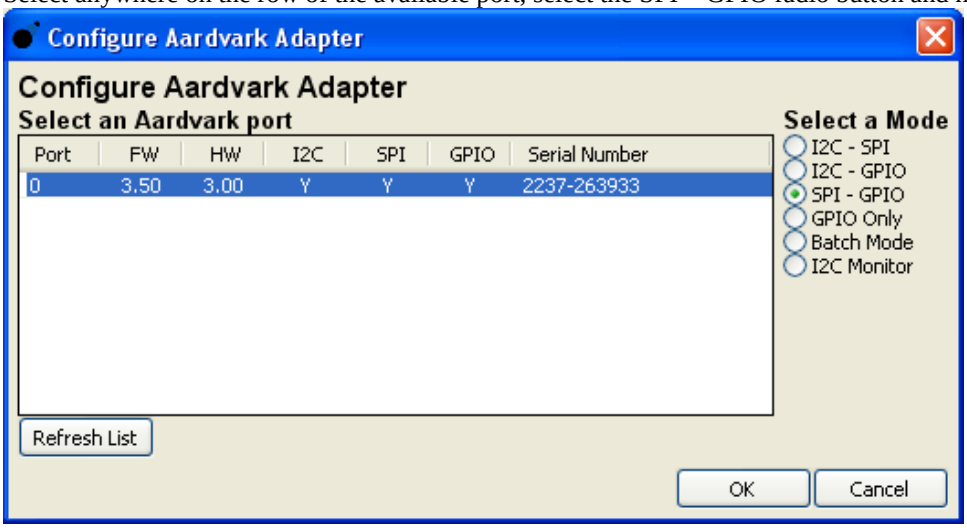

**Aardvark** **ADC**

**Figure 6. Level translator for Aardvark to ADC**

1. Download the Aardvark control GUI software
    a. Go to: http://www.totalphase.com/products/aardvark_i2cspi/ and select the *Downloads* tab.
    b. Download and install the *Control Center Software*.
2. Configure and connect the hardware
    a. Put the ADC into Extended Control Mode (ECM) by setting the ECEB jumper to GND.
    b. The I2C/SPI Level Shifter board should have jumpers at TPWR, MASTER, and 1.8V. (The Gig ADC runs at 1.9V, but 1.8V is appropriately close.)
    c. Connect a USB cable from the PC to the Aardvark
    d. Connect the Aardvark cable to the I2C/SPI Level Shifter board, ADAPTER input
    e. Connect the additionally supplied ribbon cable from the I2C/SPI Level Shifter board, TARGET1 port to the ribbon cable with split outputs
    f. Connect the split output wires to the ADC EVAL board
        i. SS (white) = SCSb
        ii. MOSI (grey) = SDI
        iii. SCLK (purple) = SCLK
        iv. GND (black) = GND
3. Configure the Aardvark software
    a. Select *Configure Aardvark Adapter*



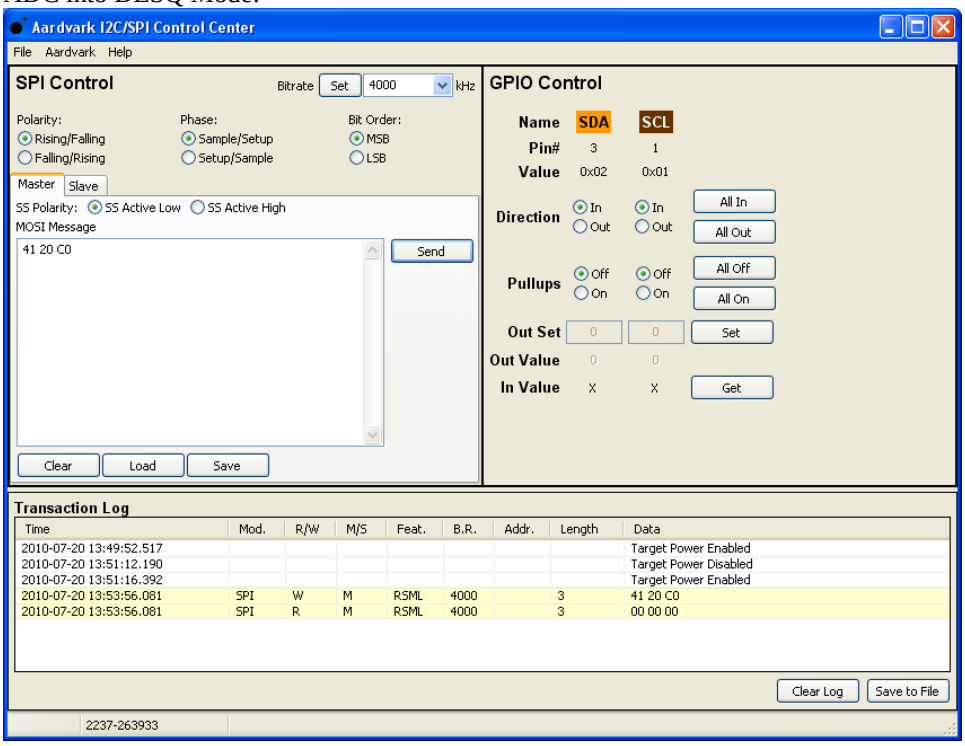
b. Select anywhere on the row of the available port, select the SPI – GPIO radio button and hit OK




c. In the Aardvark I2C/SPI Control Center software, select *Aardvark → Target Power.* On the I2C/SPI Level Shifter board, both LEDs for TARGET (orange) and POWER (green) should light up.

4. Using the software

a. Type the command (hex) in the MOSI Message window and hit the Send button. For example, putting the ADC into DESQ Mode:




5. Tips and tricks

a. During the entire time the ADC is being used in SPI Mode (a.k.a. Extended Control Mode), the jumper on the EVAL board for ECEB stays connected to GND. Moving the ECEB jumper from GND to VA back to GND again is a short-cut to reset the SPI registers back to their default values

b. The Calibration pin is OR'd with the Calibration bit in the SPI internally to the ADC, i.e. the pin remains active when the ADC is in ECM. To calibrate the ADC, it is more convenient to use the Calibration pin (move the jumper from GND to VA and back to GND) than to write the SPI twice.

## 8. Importing data into WaveVision5

The data from the Logic Analyzer has the following (or similar) format:

```
Listing(Listing<1>) - 28 October 2010 (21:54)

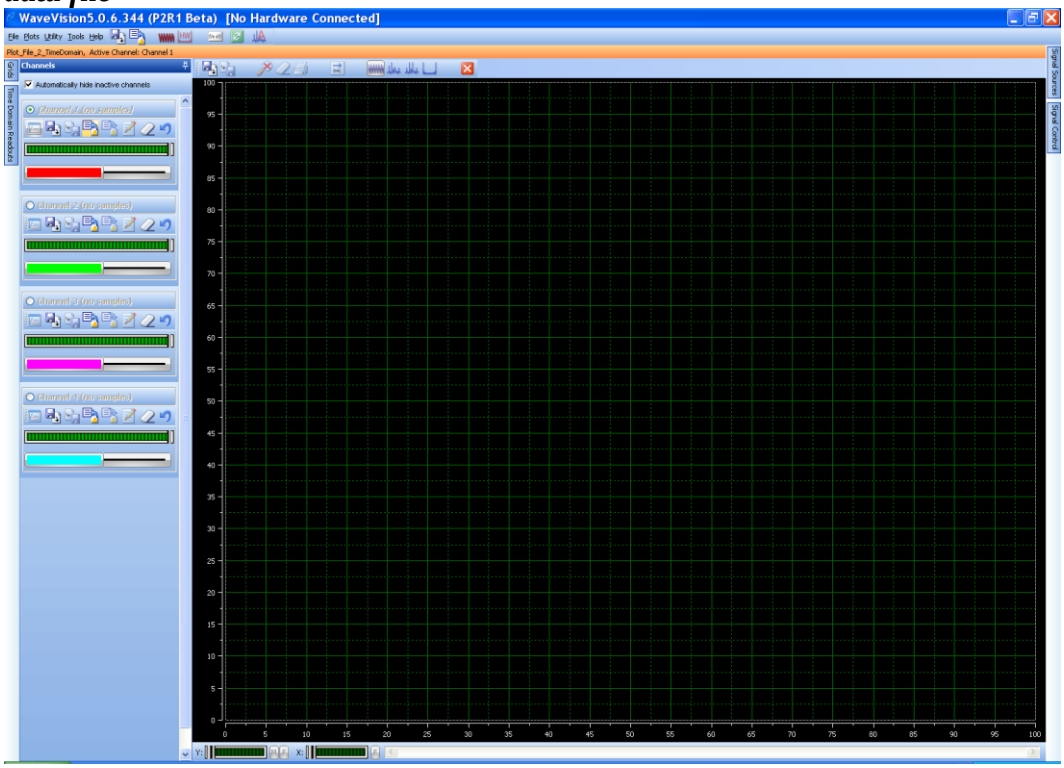
State Number    DId     DI      DQ      DQd     ORI         ORQ
Decimal         Hex     Hex     Hex     Hex     Binary      Binary
_____________   ___     ___     ___     ___     ______      ______

0               2B      24      80      80      0           1
1               D3      DC      80      80      0           1
2               2E      22      80      80      0           1
3               D1      DE      80      80      0           1
4               30      20      80      80      0           1
5               CE      E0      80      80      0           1
6               33      1E      80      80      0           1
7               CC      E3      80      80      0           1
8               35      1C      80      80      0           1
9               C9      E4      80      80      0           1
10              38      1A      80      80      0           1
```

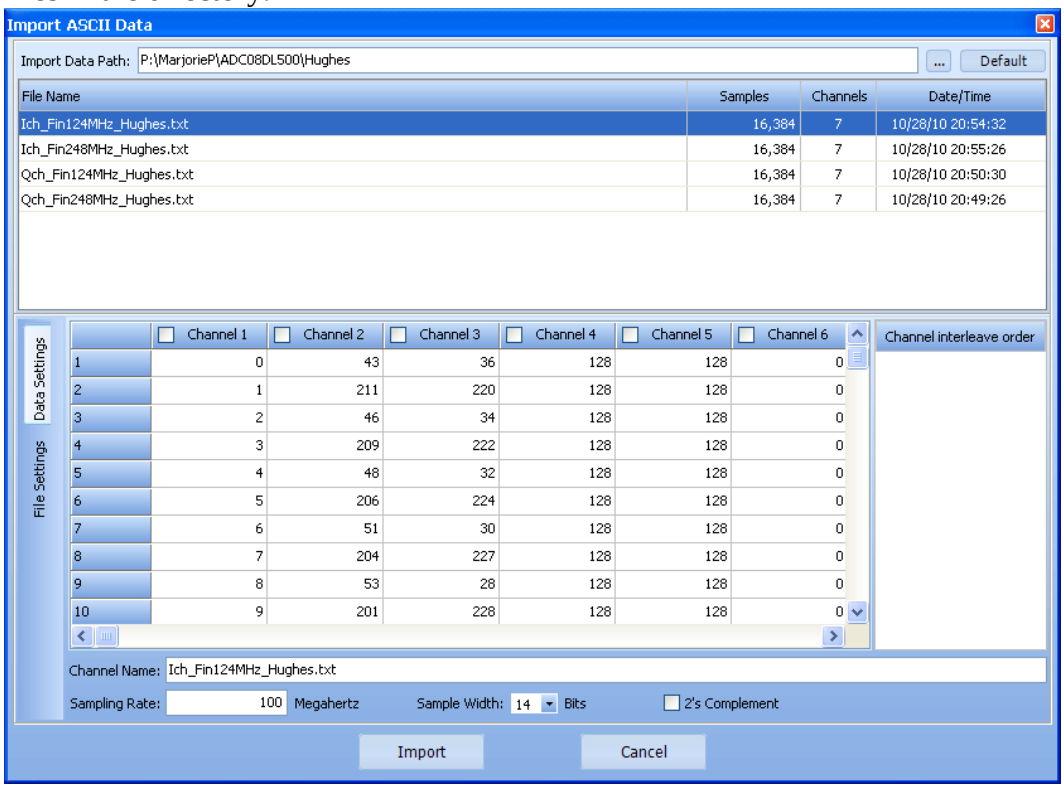
When the data is imported into WaveVision, it is necessary to make selections about how the data was taken, so that it can be correctly reconstructed. Some of these selections are: Demux / Non-Demux Mode, DES / Non-DES Mode, Hexadecimal / Binary / Decimal, Sampling Rate, and Number of Bits. For example, this data was taken on the I-channel in Demux, Non-DES Mode in the Hexadecimal format.

For Non-DES Mode, the data is ordered {DId, DI} or {DQd, DQ}. For DES Mode, the data is ordered {DQd, DId, DQ, DI}.

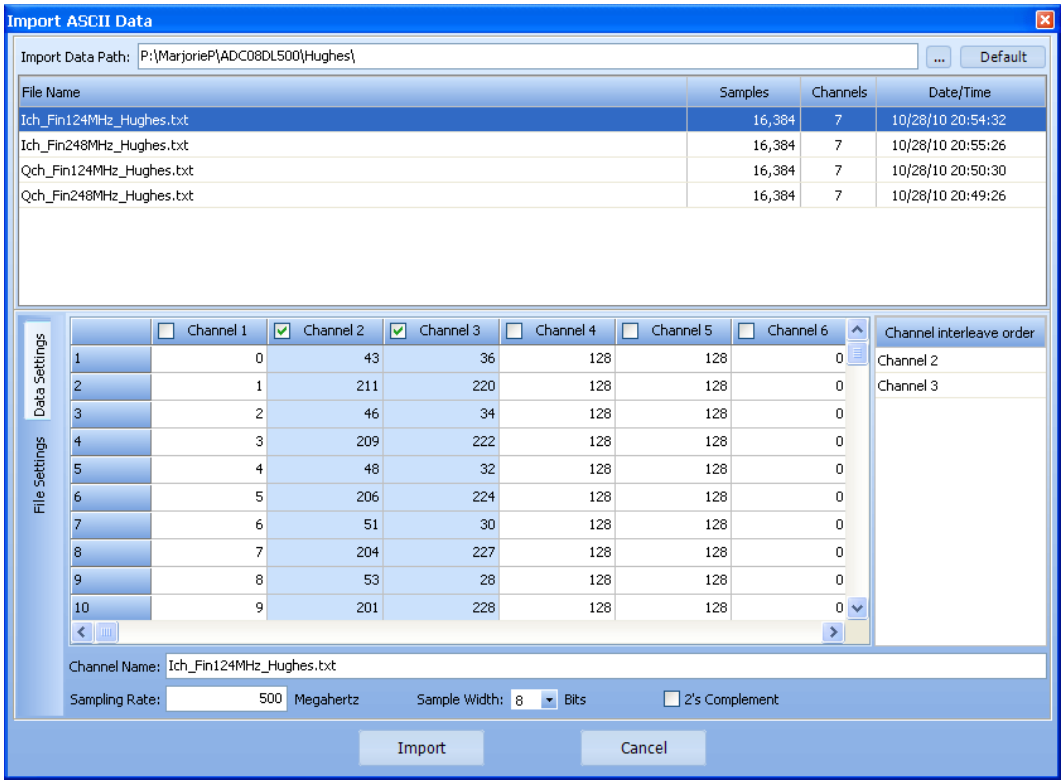
1. To import data, select ***Channels → Import WaveVision 4 data or a single/double column ASCII data file***



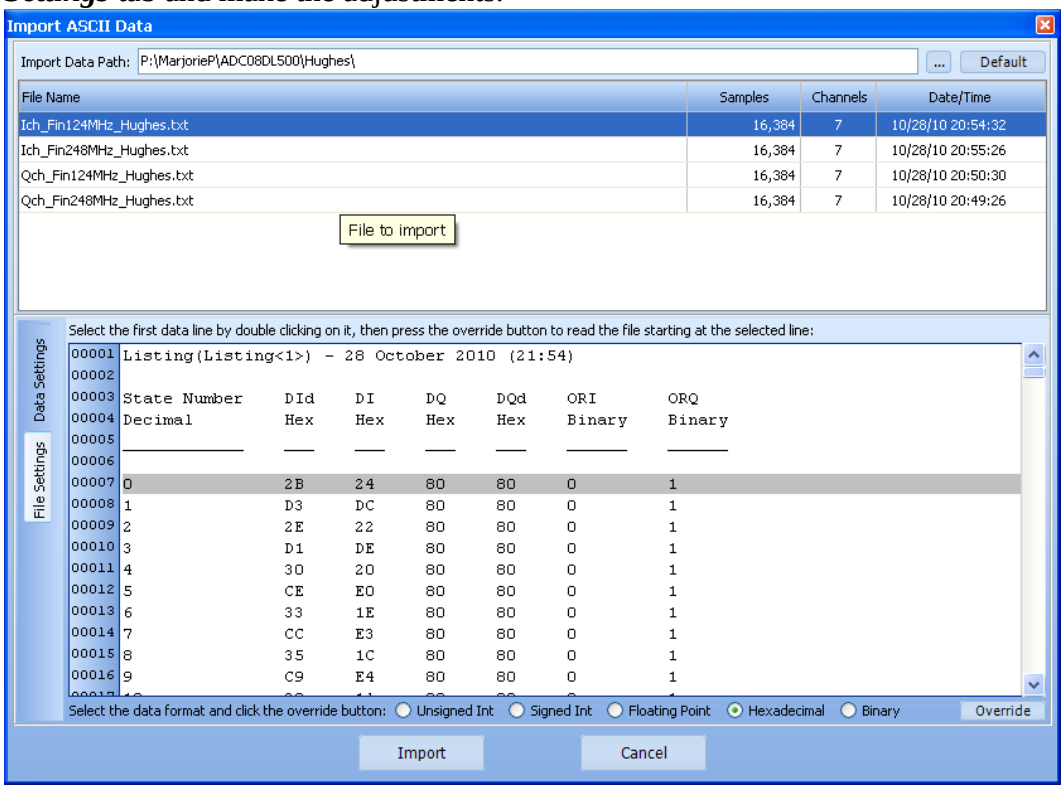

2. Select the Import Data Path. Note that this can take a few moments if there are many or large data files in the directory.



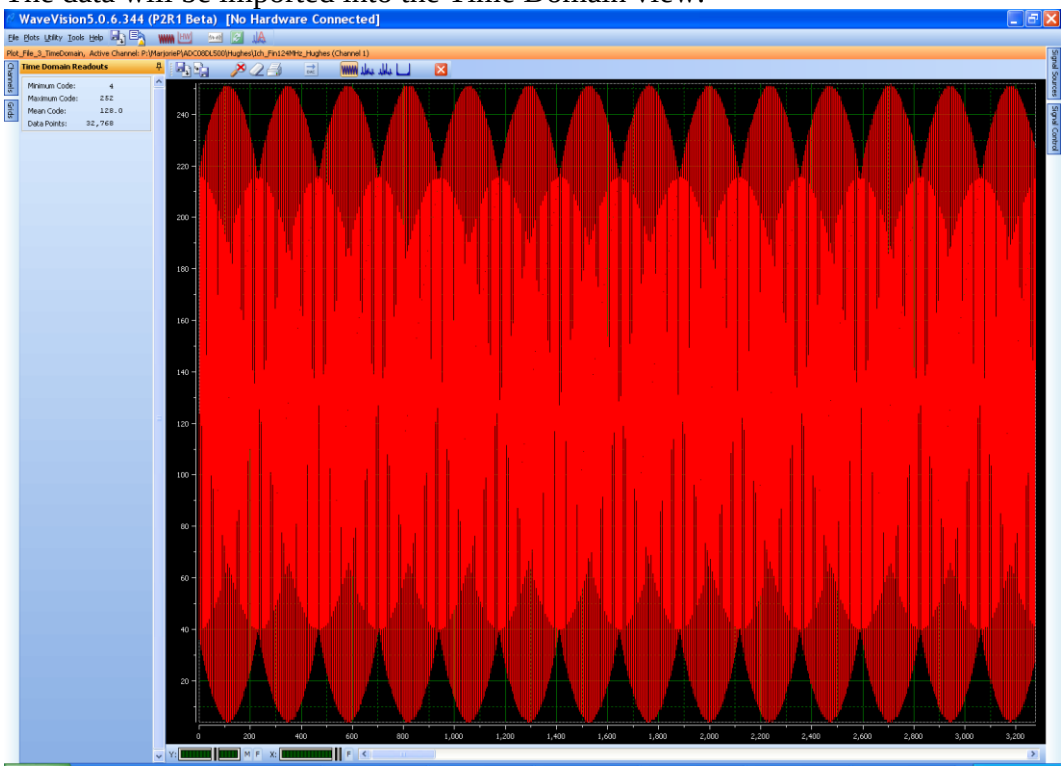
3. Select the Sampling Rate, Sample Width, channels with data (Channel 2, 3 in this example), and the Channel interleave order.



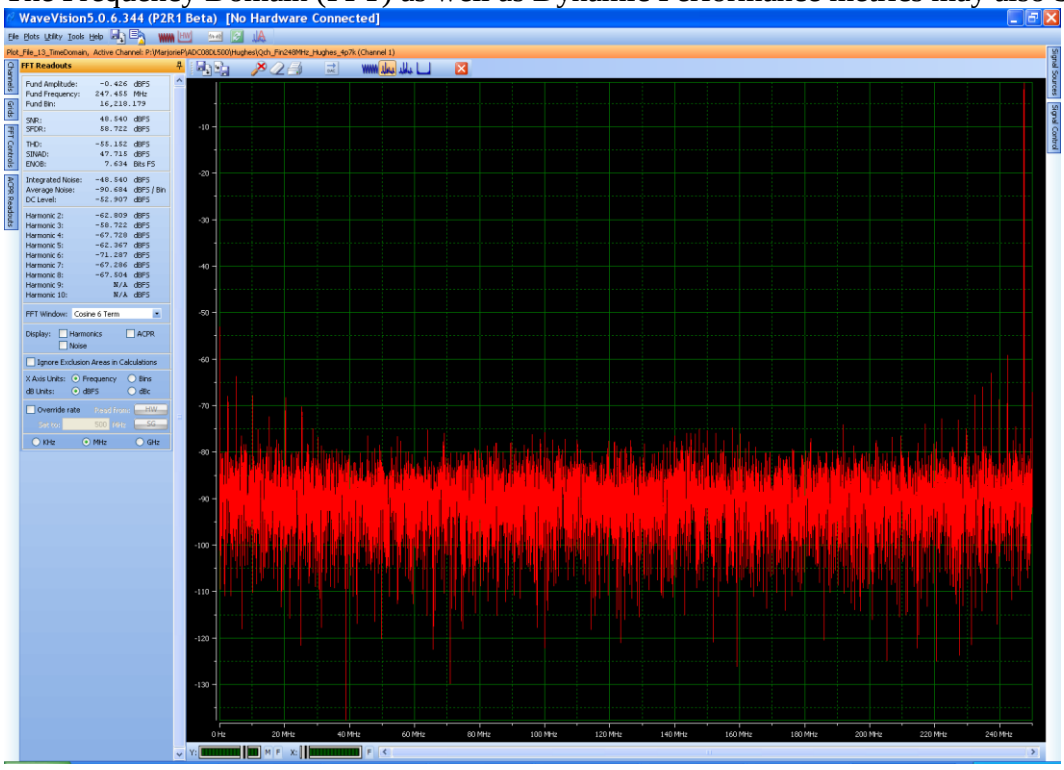

4. To verify the channel headings or override the automatically selected data format, select the ***File Settings*** tab and make the adjustments.



5. The data will be imported into the Time Domain view:




6. The Frequency Domain (FFT) as well as Dynamic Performance metrics may also be selected:



## EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of of 4.0V to +75V; a supply voltage (Vs) range of +4.5V to +75V; and the output voltage range of GND + 0.05V to ( Vs – 0.4V  or 13.6 – whichever is less). Total dissipation of the TI installed sense resistor shall not exceed 0.5W. Turret terminals are rated for 5A max.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than +25°C. The EVM is designed to operate properly with certain components above +25°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

## EVALUATION BOARD/KIT/MODULE (EVM) ADDITIONAL TERMS

Texas Instruments (TI) provides the enclosed Evaluation Board/Kit/Module (EVM) under the following conditions:

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods.

Should this evaluation board/kit not meet the specifications indicated in the User’s Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING LIMITED WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE. EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

Please read the User's Guide and, specifically, the Warnings and Restrictions notice in the User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For additional information on TI's environmental and/or safety programs, please visit www.ti.com/esh or contact TI.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used. TI currently deals with a variety of customers for products, and therefore our arrangement with the user is not exclusive. TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein.

## REGULATORY COMPLIANCE INFORMATION

As noted in the EVM User’s Guide and/or EVM itself, this EVM and/or accompanying hardware may or may not be subject to the Federal Communications Commission (FCC) and Industry Canada (IC) rules.

For EVMs **not** subject to the above rules, this evaluation board/kit/module is intended for use for ENGINEERING DEVELOPMENT, DEMONSTRATION OR EVALUATION PURPOSES ONLY and is not considered by TI to be a finished end product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC or ICES-003 rules, which are designed to provide reasonable protection against radio frequency interference. Operation of the equipment may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

**General Statement for EVMs including a radio**

*User Power/Frequency Use Obligations*: This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

**For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant**

**Caution**
This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

**FCC Interference Statement for Class A EVM devices**
This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

**FCC Interference Statement for Class B EVM devices**
This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

**For EVMs annotated as IC – INDUSTRY CANADA Compliant**
This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

**Concerning EVMs including radio transmitters**
This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

**Concerning EVMs including detachable antennas**
Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

**Concernant les EVMs avec appareils radio**
Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

**Concernant les EVMs avec antennes détachables**
Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

**【Important Notice for Users of this Product in Japan】**

**This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan**

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

1. Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

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【ご使用にあたっての注】

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本製品のご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

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2. 実験局の免許を取得後ご使用いただく。
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**EVALUATION BOARD/KIT/MODULE (EVM)**
**WARNINGS, RESTRICTIONS AND DISCLAIMERS**

**For Feasibility Evaluation Only, in Laboratory/Development Environments.** Unless otherwise indicated, this EVM is not a finished electrical equipment and not intended for consumer use. It is intended solely for use for preliminary feasibility evaluation in laboratory/development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems and subsystems. It should not be used as all or part of a finished end product.

Your Sole Responsibility and Risk. You acknowledge, represent and agree that:

1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the EVM for evaluation, testing and other purposes.
2. You have full and exclusive responsibility to assure the safety and compliance of your products with all such laws and other applicable regulatory requirements, and also to assure the safety of any activities to be conducted by you and/or your employees, affiliates, contractors or designees, using the EVM. Further, you are responsible to assure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.
3. You will employ reasonable safeguards to ensure that your use of the EVM will not result in any property damage, injury or death, even if the EVM should fail to perform as described or expected.
4. You will take care of proper disposal and recycling of the EVM's electronic components and packing materials.

**Certain Instructions**. It is important to operate this EVM within TI's recommended specifications and environmental considerations per the user guidelines. Exceeding the specified EVM ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use these EVMs.

**Agreement to Defend, Indemnify and Hold Harmless.** You agree to defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of or in connection with any use of the EVM that is not in accordance with the terms of the agreement. This obligation shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if the EVM fails to perform as described or expected.

**Safety-Critical or Life-Critical Applications.** If you intend to evaluate the components for possible use in safety critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, such as devices which are classified as FDA Class III or similar classification, then you must specifically notify TI of such intent and enter into a separate Assurance and Indemnity Agreement.


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# ADC12D1XXX Evaluation Board

## SPECIAL NOTES

**These schematics reflect the current state of product development. This design had NOT yet been fully tested at the time these schematics were generated.**

**Since this product is in development, the user of this document is strongly advised to check for the latest revision.**

**National Semiconductor reserves the right to make changes to this product.**

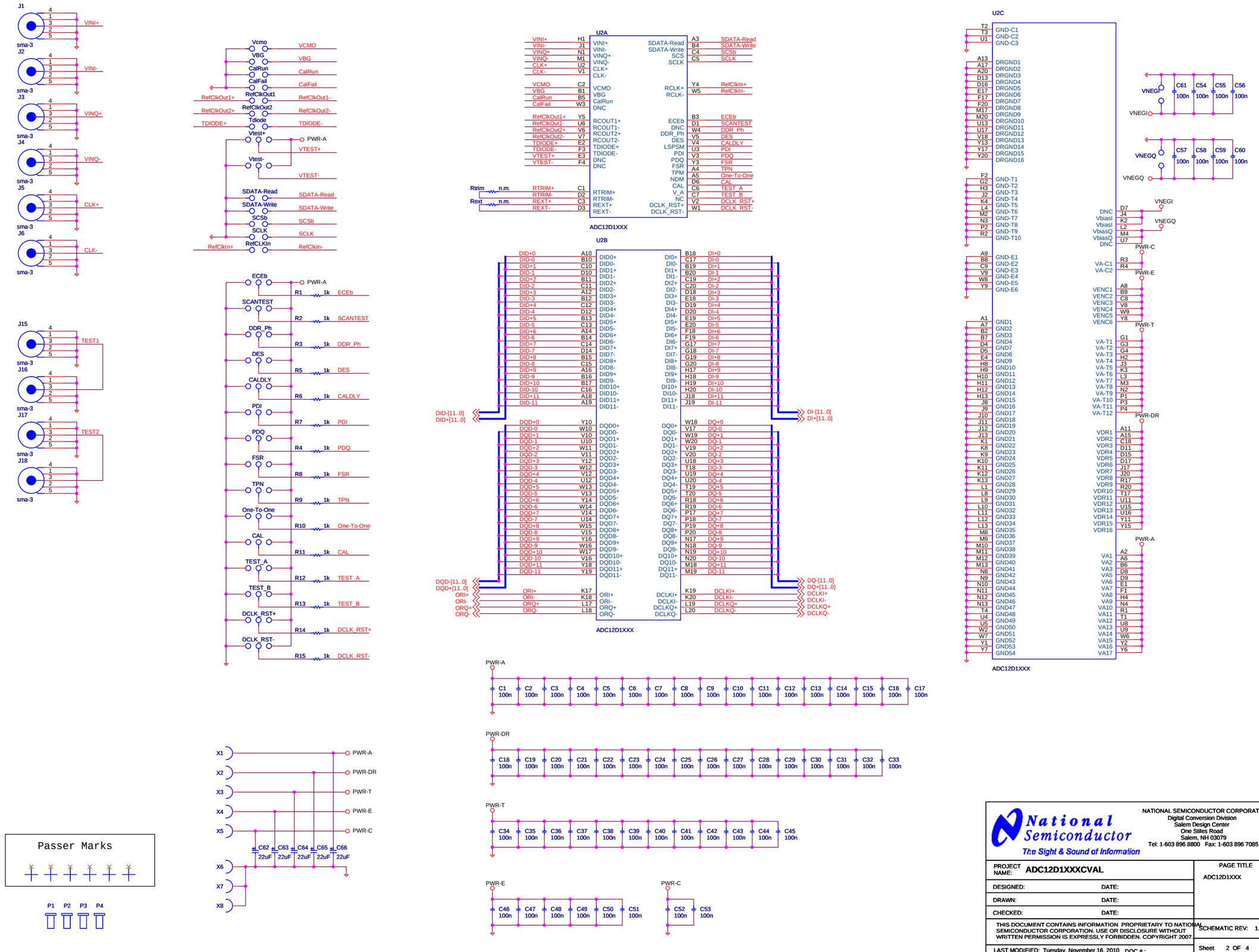
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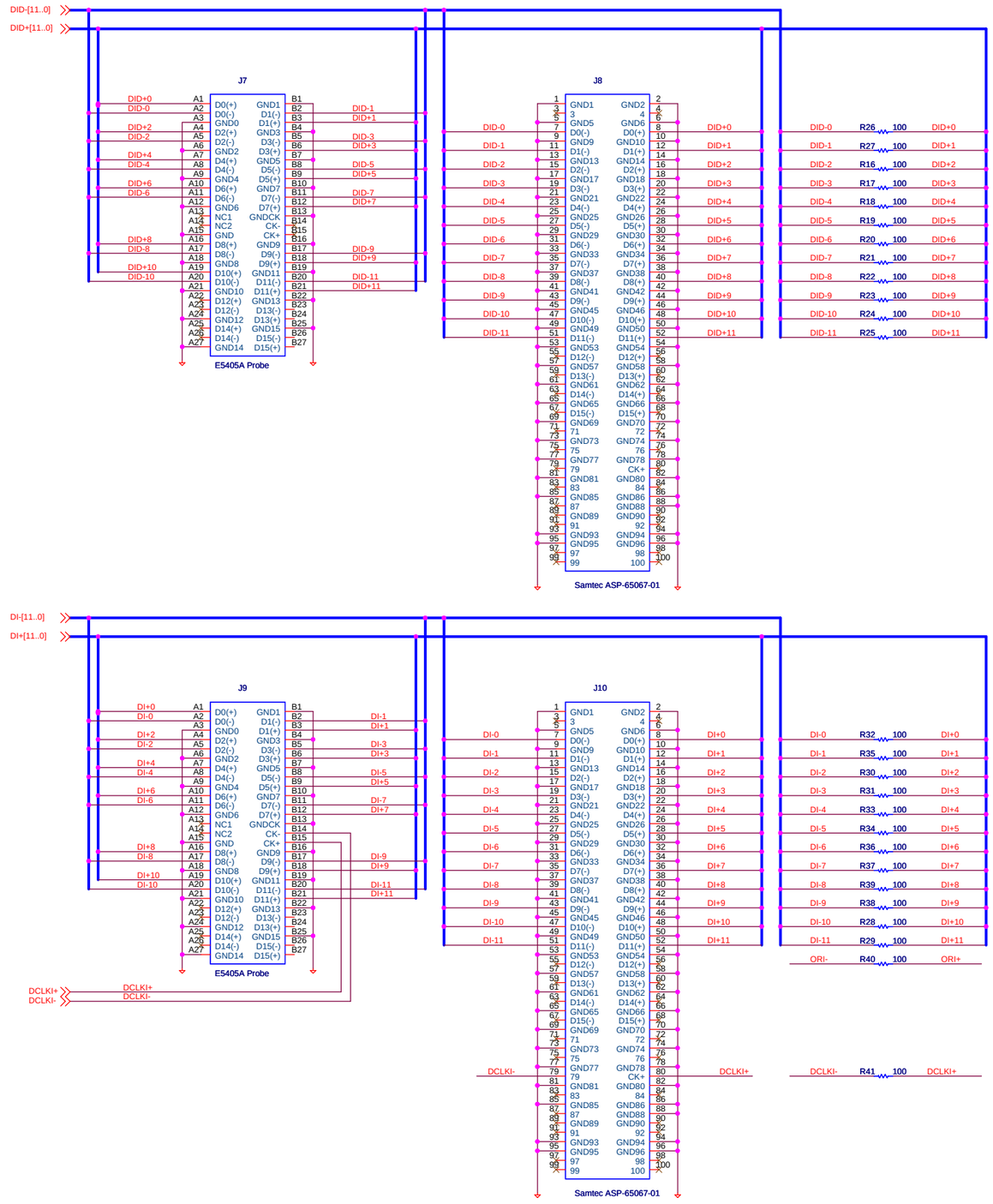
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J1
J2
J3
J4
J5
J6
sma-3
VINI+
VINI-
VINQ+
VINQ-
CLK+
CLK-
J15
J16
J17
J18
TEST1
TEST2
Vcmo
VBG
CalRun
CalFail
RefClkOut1
RefClkOut2
Tdiode
Vtest+
Vtest-
SDATA-Read
SDATA-Write
SCSb
SCLK
RefCLKIn
VCMO
VBG
CalRun
CalFail
RefClkOut1-
RefClkOut2-
TDIODE-
PWR-A
VTEST+
VTEST-
SDATA-Read
SDATA-Write
SCSb
SCLK
RefClkIn-
RefClkOut1+
RefClkOut2+
TDIODE+
ECEb
SCANTEST
DDR_Ph
DES
CALDLY
PDI
PDQ
FSR
TPN
One-To-One
CAL
TEST_A
TEST_B
DCLK_RST+
DCLK_RST-
R1 1k ECEb
R2 1k SCANTEST
R3 1k DDR_Ph
R5 1k DES
R6 1k CALDLY
R7 1k PDI
R4 1k PDQ
R8 1k FSR
R9 1k TPN
R10 1k One-To-One
R11 1k CAL
R12 1k TEST_A
R13 1k TEST_B
R14 1k DCLK_RST+
R15 1k DCLK_RST-
U2A
VINI+ H1
VINI- J1
VINQ+ N1
VINQ- M1
CLK+ U2
CLK- V1
VCMO C2
VBG B1
CalRun B5
CalFail W3
DNC
RefClkOut1+ Y5
RefClkOut1- U6
RefClkOut2+ V6
RefClkOut2- V7
TDIODE+ E2
TDIODE- F3
VTEST+ E3
VTEST- F4
RCOUT1+
RCOUT1-
RCOUT2+
RCOUT2-
TDIODE+
TDIODE-
DNC
DNC
Rtrim n.m. RTRIM+ C1
RTRIM- D2
Rext n.m. REXT+ C3
REXT- D3
RTRIM+
RTRIM-
REXT+
REXT-
SDATA-Read A3
SDATA-Write B4
SCS C4
SCLK C5
RCLK+ Y4
RCLK- W5
ECEb B3
DNC D1
DDR_Ph W4
DES V5
LSPSM V4
PDI U3
PDQ V3
FSR Y3
TPN A4
NDM A5
CAL D6
V_A C6
NC C7
DCLK_RST+ V2
DCLK_RST- W1
SDATA-Read
SDATA-Write
SCSb
SCLK
RefClkIn+
RefClkIn-
ADC12D1XXX
U2B
DID+[11..0]
DID-[11..0]
DID+0 A10
DID-0 B10
DID+1 C10
DID-1 D10
DID+2 B11
DID-2 C11
DID+3 A12
DID-3 B12
DID+4 C12
DID-4 D12
DID+5 B13
DID-5 C13
DID+6 A14
DID-6 B14
DID+7 C14
DID-7 D14
DID+8 B15
DID-8 C15
DID+9 A16
DID-9 B16
DID+10 B17
DID-10 C16
DID+11 A18
DID-11 A19
DID0+
DID0-
DID1+
DID1-
DID2+
DID2-
DID3+
DID3-
DID4+
DID4-
DID5+
DID5-
DID6+
DID6-
DID7+
DID7-
DID8+
DID8-
DID9+
DID9-
DID10+
DID10-
DID11+
DID11-
DI+[11..0]
DI-[11..0]
DI0+ B18 DI+0
DI0- C17 DI-0
DI1+ B19 DI+1
DI1- B20 DI-1
DI2+ C19 DI+2
DI2- C20 DI-2
DI3+ D18 DI+3
DI3- E18 DI-3
DI4+ D19 DI+4
DI4- D20 DI-4
DI5+ E19 DI+5
DI5- E20 DI-5
DI6+ F18 DI+6
DI6- F19 DI-6
DI7+ G17 DI+7
DI7- G18 DI-7
DI8+ G19 DI+8
DI8- G20 DI-8
DI9+ H17 DI+9
DI9- H18 DI-9
DI10+ H19 DI+10
DI10- H20 DI-10
DI11+ J18 DI+11
DI11- J19 DI-11
DQD+[11..0]
DQD-[11..0]
DQD+0 Y10
DQD-0 W10
DQD+1 V10
DQD-1 U10
DQD+2 W11
DQD-2 V11
DQD+3 V12
DQD-3 W12
DQD+4 V12
DQD-4 U12
DQD+5 W13
DQD-5 V13
DQD+6 W14
DQD-6 W14
DQD+7 V14
DQD-7 U14
DQD+8 W15
DQD-8 V15
DQD+9 Y16
DQD-9 W16
DQD+10 W17
DQD-10 V16
DQD+11 Y18
DQD-11 Y19
DQD0+
DQD0-
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DQD1-
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DQD4+
DQD4-
DQD5+
DQD5-
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DQD6-
DQD7+
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DQD9+
DQD9-
DQD10+
DQD10-
DQD11+
DQD11-
DQ+[11..0]
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DQ0- V17 DQ-0
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DQ1- W20 DQ-1
DQ2+ V19 DQ+2
DQ2- V20 DQ-2
DQ3+ U18 DQ+3
DQ3- T18 DQ-3
DQ4+ U19 DQ+4
DQ4- U20 DQ-4
DQ5+ T19 DQ+5
DQ5- T20 DQ-5
DQ6+ R18 DQ+6
DQ6- R19 DQ-6
DQ7+ P17 DQ+7
DQ7- P18 DQ-7
DQ8+ P19 DQ+8
DQ8- P20 DQ-8
DQ9+ N17 DQ+9
DQ9- N18 DQ-9
DQ10+ N19 DQ+10
DQ10- N20 DQ-10
DQ11+ M18 DQ+11
DQ11- M19 DQ-11
ORI+ K17
ORI- K18
ORQ+ L17
ORQ- L18
ORI+
ORI-
ORQ+
ORQ-
DCLKI+ K19 DCLKI+
DCLKI- K20 DCLKI-
DCLKQ+ L19 DCLKQ+
DCLKQ- L20 DCLKQ-
DCLKI+
DCLKI-
DCLKQ+
DCLKQ-
ADC12D1XXX
U2C
GND-C1 T2
GND-C2 T3
GND-C3 U1
DRGND1 A13
DRGND2 A17
DRGND3 A20
DRGND4 D13
DRGND5 D16
DRGND6 E17
DRGND7 F17
DRGND8 F20
DRGND9 M17
DRGND10 M20
DRGND11 U13
DRGND12 U17
DRGND13 V18
DRGND14 Y13
DRGND15 Y17
DRGND16 Y20
GND-T1 F2
GND-T2 G2
GND-T3 H3
GND-T4 J2
GND-T5 K4
GND-T6 L4
GND-T7 M2
GND-T8 N3
GND-T9 P2
GND-T10 R2
GND-E1 A9
GND-E2 B8
GND-E3 C9
GND-E4 V9
GND-E5 W8
GND-E6 Y9
GND1 A1
GND2 A7
GND3 B2
GND4 B7
GND7 D4
GND8 D5
GND9 E4
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GND15 H13
GND16 J8
GND17 J9
GND18 J10
GND19 J11
GND20 J12
GND21 J13
GND22 K1
GND23 K8
GND24 K9
GND25 K10
GND26 K11
GND27 K12
GND28 K13
GND29 L1
GND30 L8
GND31 L9
GND32 L10
GND33 L11
GND34 L12
GND35 L13
GND36 M8
GND37 M9
GND38 M10
GND39 M11
GND40 M12
GND41 M13
GND42 N8
GND43 N9
GND44 N10
GND45 N11
GND46 N12
GND47 N13
GND48 T4
GND49 U4
GND50 U5
GND51 W2
GND52 W7
GND53 Y1
GND54 Y7
VNEGI
VNEGQ
C61 100n
C54 100n
C55 100n
C56 100n
C57 100n
C58 100n
C59 100n
C60 100n
DNC D7
VbiasI J4
VbiasI K2
VbiasQ L2
VbiasQ M4
DNC U7
PWR-C
VA-C1 R3
VA-C2 R4
PWR-E
VENC1 A8
VENC2 B9
VENC3 C8
VENC4 V8
VENC5 W9
VENC6 Y8
PWR-T
VA-T1 G1
VA-T2 G3
VA-T3 G4
VA-T4 H2
VA-T5 J3
VA-T6 K3
VA-T7 L3
VA-T8 M3
VA-T9 N2
VA-T10 P1
VA-T11 P3
VA-T12 P4
PWR-DR
VDR1 A11
VDR2 A15
VDR3 C18
VDR4 D11
VDR5 D15
VDR6 D17
VDR7 J17
VDR8 J20
VDR9 R17
VDR10 R20
VDR11 T17
VDR12 U11
VDR13 U15
VDR14 U16
VDR15 Y11
VDR16 Y15
PWR-A
VA1 A2
VA2 A6
VA3 B6
VA5 D8
VA6 D9
VA7 E1
VA8 F1
VA9 H4
VA10 N4
VA11 R1
VA12 T1
VA13 U8
VA14 U9
VA15 W6
VA16 Y2
VA17 Y6
ADC12D1XXX
PWR-A
C1 100n
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C5 100n
C6 100n
C7 100n
C8 100n
C9 100n
C10 100n
C11 100n
C12 100n
C13 100n
C14 100n
C15 100n
C16 100n
C17 100n
PWR-DR
C18 100n
C19 100n
C20 100n
C21 100n
C22 100n
C23 100n
C24 100n
C25 100n
C26 100n
C27 100n
C28 100n
C29 100n
C30 100n
C31 100n
C32 100n
C33 100n
PWR-T
C34 100n
C35 100n
C36 100n
C37 100n
C38 100n
C39 100n
C40 100n
C41 100n
C42 100n
C43 100n
C44 100n
C45 100n
PWR-E
C46 100n
C47 100n
C48 100n
C49 100n
C50 100n
C51 100n
PWR-C
C52 100n
C53 100n
X1
X2
X3
X4
X5
X6
X7
X8
PWR-A
PWR-DR
PWR-T
PWR-E
PWR-C
C62 22uF
C63 22uF
C64 22uF
C65 22uF
C66 22uF
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P1
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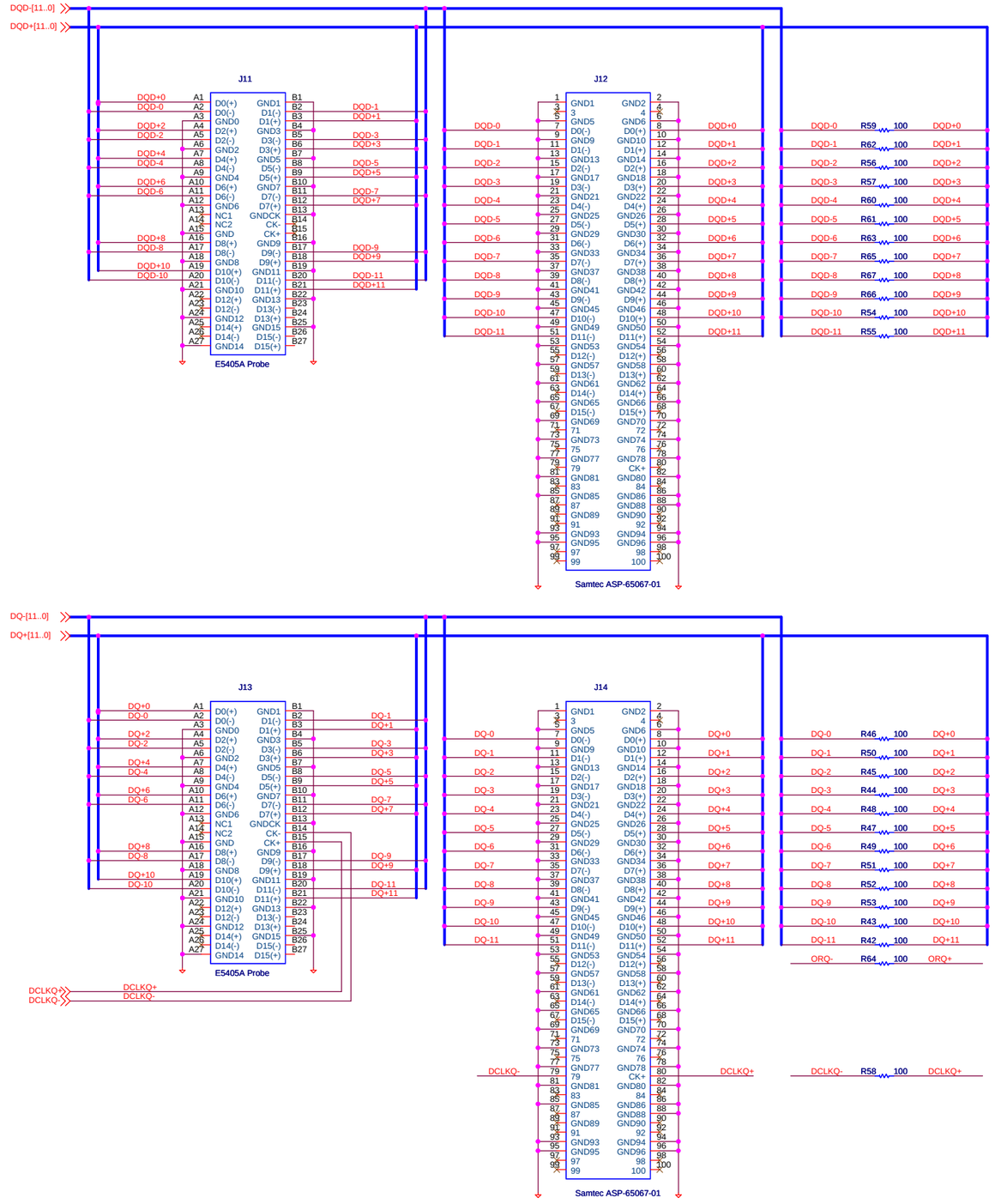


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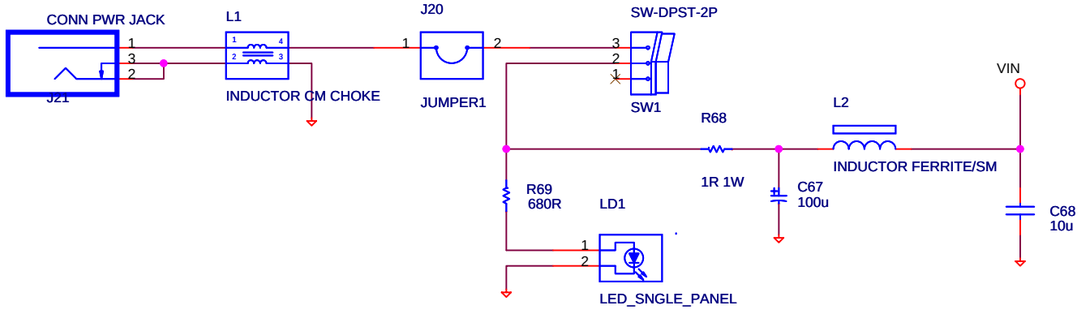
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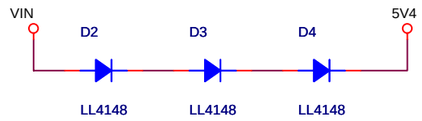


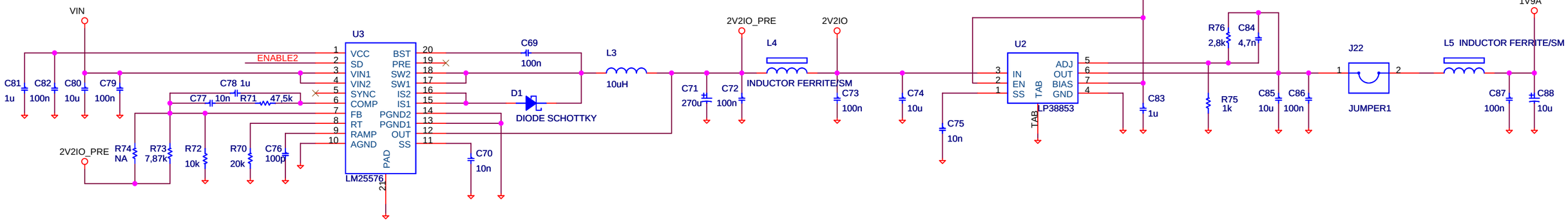

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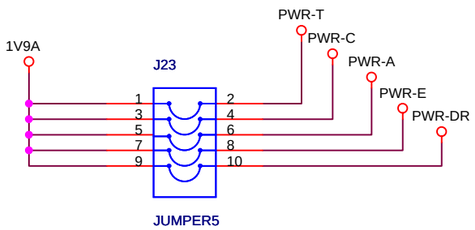
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