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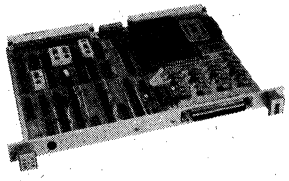
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MPV950D
MPV950S

High Speed, 16-Channel, VMEbus-Compatible ANALOG INPUT SYSTEM

FEATURES

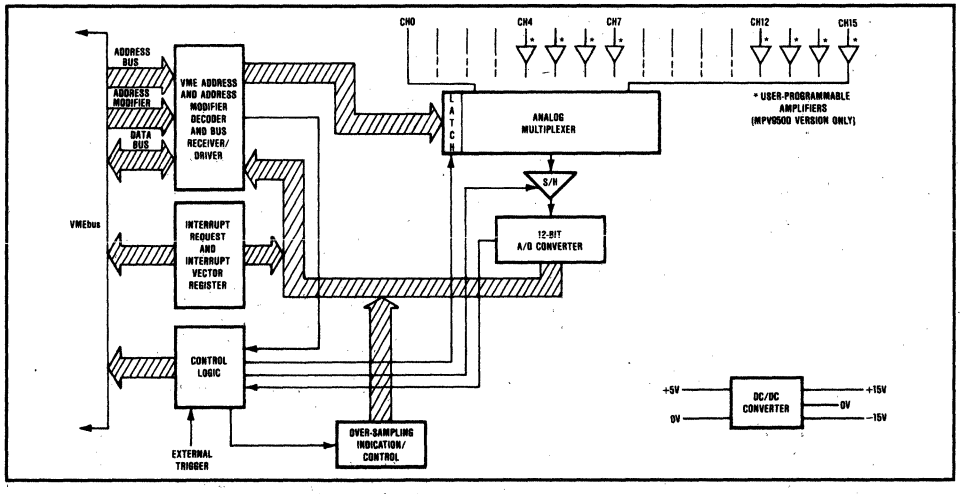
- THROUGHPUT RATES SUITABLE FOR DSP APPLICATIONS
- 3μsec TOTAL THROUGHPUT TIME
- 12-BIT RESOLUTION
- RESISTOR-PROGRAMMABLE-GAIN AMPLIFIER OPTION (MPV950D)
- HIGH AND LOW LEVEL INPUTS (±5V to ±500mV; 0 to +10V or 0 to +1V)
- ADDRESS-SELECTABLE IN WHOLE 16M BYTE MEMORY SPACE

DESCRIPTION

The MPV950 series of analog input/output boards are electrically and mechanically compatible with, and interface directly to, the VMEbus. The analog input section of the MPV950S includes 16 single-ended inputs with gain of 1; the MPV950 includes 8 single-ended inputs with fixed gain of 1 plus 8 inputs with uncommitted amplifiers whose function is user-definable with optional resistor-programmable gains of 1 to 10 (MPV950D), sample/hold amplifier, and 12-bit A/D converter.

An external trigger input is provided and includes an associated front panel indicator which illuminates when the trigger rate exceeds the conversion rate.

MPV950 series boards operate from a single +5V supply with an on-board DC/DC converter providing the remaining power requirements.



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SPECIFICATIONS

ELECTRICAL

Typical at +25°C and rated power supplies unless otherwise specified.

ANALOG INPUT SECTION	
INPUT CHARACTERISTICS	
Number of channels	16
ADC Gain Ranges (jumper-selectable)[1]	0 to +10V, ±5V
Amplifier Gain Ranges, Resistor-Programmable[2] (MPV950D)	1 to 10
Maximum Input Voltage Without Damage	±25V (power off) ±35V (power on)
Input Impedance:	
MPV950S	>10MΩ
MPV950D, unconditioned inputs	>10MΩ
conditioned inputs	dependent upon amplifier configuration
Bias Current (+25°C), max:	
MPV950S	±30nA
MPV950D, unconditioned	±30nA
conditioned	±80nA
Amplifier Input Offset Voltage (MPV950D)	30μV
Amplifier Input Offset Voltage Drift	0.4μV/°C
TRANSFER CHARACTERISTICS	
Resolution	12 bits
Throughput Time, max: 12 bits	3μsec
10 bits	2.2μsec
8 bits	2μsec
ACCURACY	
System Error at +25°C, max[3]	
MPV950S	±0.06% FSR[4]
MPV950D, G = 1	±0.06% FSR
G = 10	±0.06% FSR
System Linearity:	
MPV950S	±0.025%
MPV950D, G = 1	±0.025%
G = 10	±0.025%
ADC Gain Error	Adjustable to zero
ADC Offsett Error	Adjustable to zero
Monotonicity[5]	Guaranteed 0°C to +70°C
STABILITY OVER TEMPERATURE	
System Accuracy Drift	
MPV950S	±50ppm of FSR/°C
MPV950D	±55ppm of FSR/°C
DYNAMIC ACCURACY	
Sample/Hold Aperture Time, max	20nsec
Aperture Time Uncertainty	±100psec
Channel Crosstalk	75dB down at 1kHz for OFF channel to ON channel
POWER REQUIREMENTS	
MPV950S	+5V ±5% at 2.0A max
MPV950D	+5V ±5% at 2.0A max
ENVIRONMENTAL	
Operating Temperature	0°C to +60°C
Storage Temperature	−25°C to +85°C
Relative Humidity	90% noncondensing

NOTES: (1) Factory set for 0 to +10V operation. (2) Factory set for single-ended mode and Gain = 1. (3) Includes linearity errors with gain and offset errors adjustable to zero. (4) FSR means Full Scale Range. (5) No missing codes guaranteed.

MECHANICAL

Compatible with dougle-height VMEbus card-racking systems. Minimum card spacing 20.34mm (0.8") [VMEbus specification-compatible]. One 37-pin 'D' type analog connector on board for analog inputs/outputs. Use Cannon 'D' type connector part number DC37P/1A1N or equivalent.

OPERATING INSTRUCTIONS

INSTALLATION

The MPV950 is shipped from the factory calibrated and ready to use. Installation only requires plugging the card into an empty slot in the VMEbus card cage and wiring the front-panel connector.

PROGRAMMING

The board is programmed as 64 successive memory locations (word locations), switch-selectable in the whole 16M byte address range. The A/D converter output is a 12-bit word, therefore a data word access is required to read the converted data for each channel.

A minimum of instructions are needed to read an input channel. For example, a read instruction addressed to the next channel to be converted will acquire the converted data of the current channel, and upon completion of the data transfer, initiate a conversion at the new channel address just selected (if CPU triggering is selected) or await an external trigger input before conversion at the new address (if external triggering is selected).

All boards are jumpered at the factory with a base address of FFF780H. Each subsequent channel is two memory locations past the start of the last channel; consequently channel 0 is at location FFF780H, channel 1 is at location FFF782H.

The input system operates in the following modes:

Interrupt Mode—A read instruction or an external trigger to the board starts a conversion. An interrupt is generated at the end of the conversion. The interrupt can be connected to any one of seven interrupt request lines but may be disabled by software (Control Register D09=1 enables the board for Interrupt Mode).

Polling Mode—A read instruction or an external trigger to the board starts the conversion. The interrupt is disabled either by software or by setting all switches on the interrupt request lines to the OFF position. The CPU determines the end of conversion by reading the Status Register (Control Register D09=0 disables the interrupt for Polling Mode). When conversion is complete, the CPU reads the data. The read instruction is addressed to the next channel to be converted. The data from the last conversion is thus transferred to the CPU and either conversion is started for the next channel (CPU trigger selected), or an external trigger is awaited (external trigger selected).

During the Interrupt Mode of operation, the MPV950 supplies the interrupt vector on data lines D00-D07 when requested by the CPU. The vector is user-definable as listed in Table I. The MPV950 can also be selected to

interrupt on any one of seven interrupt request lines as shown in Table II. Interrupt capability can be disabled either by software (Control Register D09=0) or by hardware (no switches selected).

TABLE I. Interrupt Vector Selection

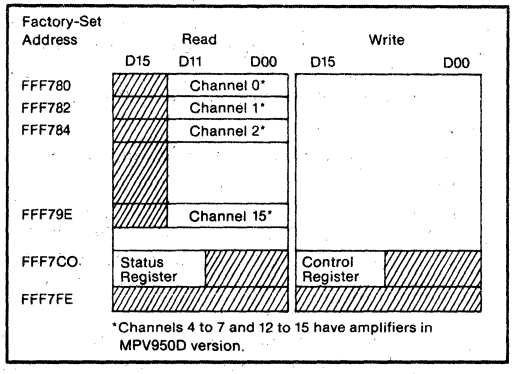
Data Line	Switch Position For "0"	Switch Position For "1"
D00	SW4 psn 1 ON	SW4 psn 1 OFF
D01	2 ON	2 OFF
D02	3 ON	3 OFF
D03	4 ON	4 OFF
D04	5 ON	5 OFF
D05	6 ON	6 OFF
D06	7 ON	7 OFF
D07	8 ON	8 OFF

TABLE II. Interrupt Line Selection

Request Interrupt On Line	Switch Combination (one only)
IRQ1*	SW1 psn 10, 3, 2 ON
IRQ2*	9, 3, 1 ON
IRQ3*	8, 3 ON
IRQ4*	7, 2, 1 ON
IRQ5*	6, 2 ON
IRQ6*	5, 1 ON
IRQ7*	4 ON

SW4 is used to set the interrupt vector while SW1 selects the interrupt line on which the request is to be made (Note that switch SW1 should be set to select interrupt capability on ONE line only).

MEMORY MAP



*Channels 4 to 7 and 12 to 15 have amplifiers in MPV950D version.

STATUS REGISTER

D15	D14	D13	D12	D11	D10	D09	D08
Over Samp	Over Samp	Over Samp	Over Samp	N/A	Conv Comp	Int En	Ext Trig

Over Samp —These bits are normally high. They go low when the external (or internal) trigger rate exceeds the maximum permissible rate.

Conv Comp —This bit is low during conversion. It goes high upon completion of conversion.

Int En —Status of interrupt enable.

Ext Trig —Status of external trigger enable.

CONTROL REGISTER

D15	D14	D13	D12	D11	D10	D09	D08
N/A	N/A	N/A	N/A	N/A	N/A	Int En	Ext Trig

Int En —A 1 enables interrupt, a 0 disables interrupt.

Ext Trig—A 0 enables external triggering, a 1 disables external triggering.

ADDRESS MODIFICATION

The base address of a board can be set to any value by properly setting its address selectors. The base address set at the factory is FFF780H. To change the sense of a bit simply change the position of the switch setting for that bit, (address line A07 is factory-set to a "1")—see Table III.

TABLE III. Address Switch Selection.

Address Line	Factory Set	Switch Position For "0"	Switch Position For "1"
A07	1		
A08	1	SW2 psn 1 ON	SW2 psn 1 OFF
A09	1	2 ON	2 OFF
A10	1	3 ON	3 OFF
A11	0	4 ON	4 OFF
A12	1	5 ON	5 OFF
A13	1	6 ON	6 OFF
A14	1	7 ON	7 OFF
A15	1	8 ON	8 OFF
A16	1	SW3 psn 8 ON	SW3 psn 8 OFF
A17	1	7 ON	7 OFF
A18	1	6 ON	6 OFF
A19	1	5 ON	5 OFF
A20	1	4 ON	4 OFF
A21	1	3 ON	3 OFF
A22	1	2 ON	2 OFF
A23	1	1 ON	1 OFF

ANALOG INPUT RANGE SELECTION

MPV950S

The analog input system can be set for either ±5V or 0 to +10V full scale. It is set for 0 to +10V at the factory (complementary straight binary coding). To set the inputs for the ±5V range, select the jumper links as shown in Table IV (before adding new jumpers, remove those indicated for the present range).

TABLE IV. Input Range Setting Jumpers.

Range	Insert Jumpers
0 to +10V	J6
±5V	J7

The MPV950S is factory-set for complementary straight binary coding. Table V shows the output codes for the analog input section.

TABLE V. Output Codes for Analog Input Section.

COMPLEMENTARY STRAIGHT BINARY

XXXX 1111 1111 1111	(X) FFFH	Negative Full Scale
XXXX 0111 1111 1111	(X) 7FFH	Midscale
XXXX 1000 0000 0000	(X) 000H	Positive Full Scale

Four MSB's are unused and set to 1111.

MPV950D

The analog input system can be set for any range between ±500mV to ±5V or 0 to +1V or 0 to +10V. It is

set for 0 to +10V at the factory (complementary straight binary coding). There are two gain determining elements in this system: the A/D converter and the amplifier associated with a channel. The A/D converter is factory set for a 0 to +10V range and the amplifiers for a gain of 1.

The A/D converter can be set for other ranges by simply changing the jumper links as shown in Table IV. (Before adding new jumpers, remove those indicated for the present range).

The amplifiers can be set to provide any gain value in the range 1 to 10 inclusive. The "uncommitted" amplifier configuration is shown in Figure 1.

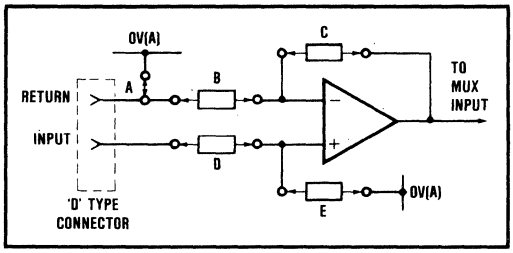


FIGURE 1. "Uncommitted" Amplifier Configuration.

TABLE VI. Circuit Components At Each Channel.

Component	CH7	CH6	CH5	CH4	CH15	CH14	CH13	CH12
A*	J9	J10	J11	J12	J13	J14	J15	J16
B	R33	R37	R41	R45	R49	R53	R57	R61
C*	R34	R38	R42	R46	R50	R54	R58	R62
D*	R35	R39	R43	R47	R51	R55	R59	R63
E	R36	R40	R44	R48	R52	R56	R60	R64

*Factory-fitted link for single-ended input and gain = 1. For other amplifier information, see data sheet on the OPA27 amplifier (PDS-466).

The above arrangement allows the amplifiers to be user connected in many of the standard operational amplifier configurations.

ANALOG INPUT CALIBRATION

If the input range of the A/D converter is to be changed, the following procedure can be used to adjust gain and offset errors. (MPV950 series boards are factory-calibrated on the 0 to +10V range).

Calibration is performed by connecting a voltage source capable of 0.002% accuracy to Channel 0. (This could also be a DC voltage source of less absolute accuracy whose output is monitored by a DVM capable of 0.002% accuracy). Offset and gain adjustments are made while applying the input voltages listed in Table VII.

TABLE VII. Analog Input Calibration Values.

Range	Offset Adjust	Gain Adjust
0 to +10V	1.221mV	+9.9963V
±5V	−4.9988V	+4.9963V

Before making the adjustments, allow the MPV950 to reach thermal equilibrium (about 20 minutes under power). The offset adjustment is made first by using the offset calibration voltage and the following procedure:

1. Set calibration voltage to appropriate value.
2. a. For 0 to +10V range: Adjust the on-board offset potentiometer (RV2) until the output code reads FFFEH.
   b. Adjust the offset potentiometer until the position where the output code makes the transition from FFFEH to FFFFH.
3. a. For ±5V range: Adjust the on-board offset potentiometer (RV2) until the output code reads F7FFH.
   b. Adjust the offset potentiometer until the position where the output code makes the transition from F7FFH to F800H.

To perform the gain adjustment, perform the following procedure:

1. Set input voltage to appropriate value.
2. Adjust the on-board gain potentiometer (RV1) until the output code reads F001H.
3. Adjust the gain potentiometer until the position where the output code makes the transition from F001H to F000H.

Calibration is now complete.

FREQUENCY RESPONSE

The ability of the MPV950 series to respond to an input signal of a given frequency is determined by the rate at which the system can acquire and convert signals and by the frequency response of the input amplifiers (MPV-950D).

For 12-bit operation using all 16 channels simultaneously, maximum recommended input frequency is 10kHz. Care should be taken to ensure that the input signal does not contain frequencies of a significant amplitude beyond this value.

For 10-bit resolution and 16-channel operation, the maximum recommended input frequency is 15kHz.

For 8-bit resolution and 16-channel operation, the maximum recommended input frequency is 16kHz.

If the number of channels used at any one time is reduced, then the input signal frequency can be increased accordingly. For example, for 12-bit operation but using only 8 channels, the maximum input frequency can be increased to 20kHz.

The input signal frequency and number of channels (for 12-bit operation) are related as shown below.

$$\text{Max input signal frequency (kHz)} = A/n$$

where A = 160 for 12-bit operation
= 240 for 10-bit operation
= 256 for 8-bit operation
n = number of channels in use

An external trigger input is provided. Details of the trigger signal are shown in Figure 2. A TTL compatible input signal can be used to trigger the board.

The maximum trigger signal repetition rate must not exceed the rate at which an input can be acquired and converted. For 12-bit operation, the maximum trigger frequency is typically 320kHz (not including CPU latency time); for 10-bit operation it is typically 480kHz, and for 8-bit operation it is typically 512kHz.

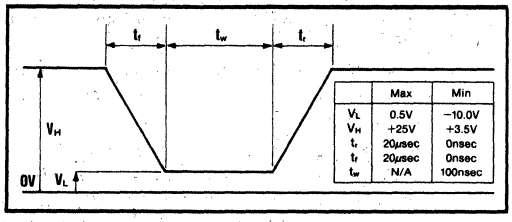


FIGURE 2. External Trigger Signal.

Should the trigger frequency exceed the maximum permissible rate, the front panel LED will illuminate. If this occurs, the trigger frequency should be reduced until the LED is extinguished. Exceeding the maximum trigger rate will also cause data bits D15, D14, D13, D12 (which are normally at a high level), to be driven to a low level, thus indicating the oversampling condition to the CPU.

SHORT CYCLE

If less than 12 bits of resolution is required, the cycle time of the A/D converter can be shortened to give the equivalent of a 10-bit converter with 670nsec conversion time or an 8-bit converter with 500nsec conversion time.

The procedure for obtaining short cycle performance is as follows:

1. Connect a frequency counter or oscilloscope probe to test point TP6.
2. Remove jumpers J1 and J5.
3. Insert jumpers J8, J4, and J3 for 10-bit operation or insert jumpers J8, J4, and J2 for 8-bit operation.
4. Adjust potentiometer RV3 until the pulse width at test point TP6 is 670nsec for 10-bit resolution or 500nsec for 8-bit resolution (see Figure 3).
5. Insert jumper J1.

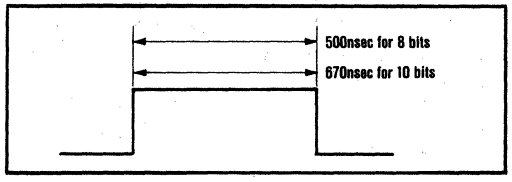


FIGURE 3. Waveform at TP6.

OPERATION SUMMARY

All boards are shipped from the factory ready for immediate use, however they do have a number of user-selectable options. These options, which have already been described, are summarized below.

1. Programming Mode

Units are factory set to the non-interrupt mode and default, on power-up, to the polling mode. Selection of the interrupt mode and interrupt vector is made as outlined earlier. Table I describes the selection of one of seven interrupt vectors.

2. Address/Address Modifier

The units are factory-set for a base address of FFF780H and to respond to short I/O addressing with no address modifier decoding. Table III describes the jumpers which allow the user to configure the units for any address. Address modifier code response can be altered by programming the PROM to suit user requirements (consult factory for details). Address/Address Modifier decoding options are shown in Table VIII.

TABLE VIII. Address and Address Modifier Decoding Options.

J20	J21	AM Codes	Address Decoding
*Insert	Insert	N/A	A01-A15
Insert	Remove	N/A	A01-A23
Remove	Remove	30,39	A01-A23

*Factory-set option.

3. Analog Input Range

Two input systems are available with the units—16 unconditioned inputs (MPV950S), and 8 unconditioned plus 8 conditioned inputs (MPV950D). In both cases the A/D converter may be set to one of two ranges. The amplifiers may be user-set as defined earlier.

4. Triggering

The unit defaults on power-up to the external triggering mode. Selection of internal triggering is as defined earlier (see Control Register).

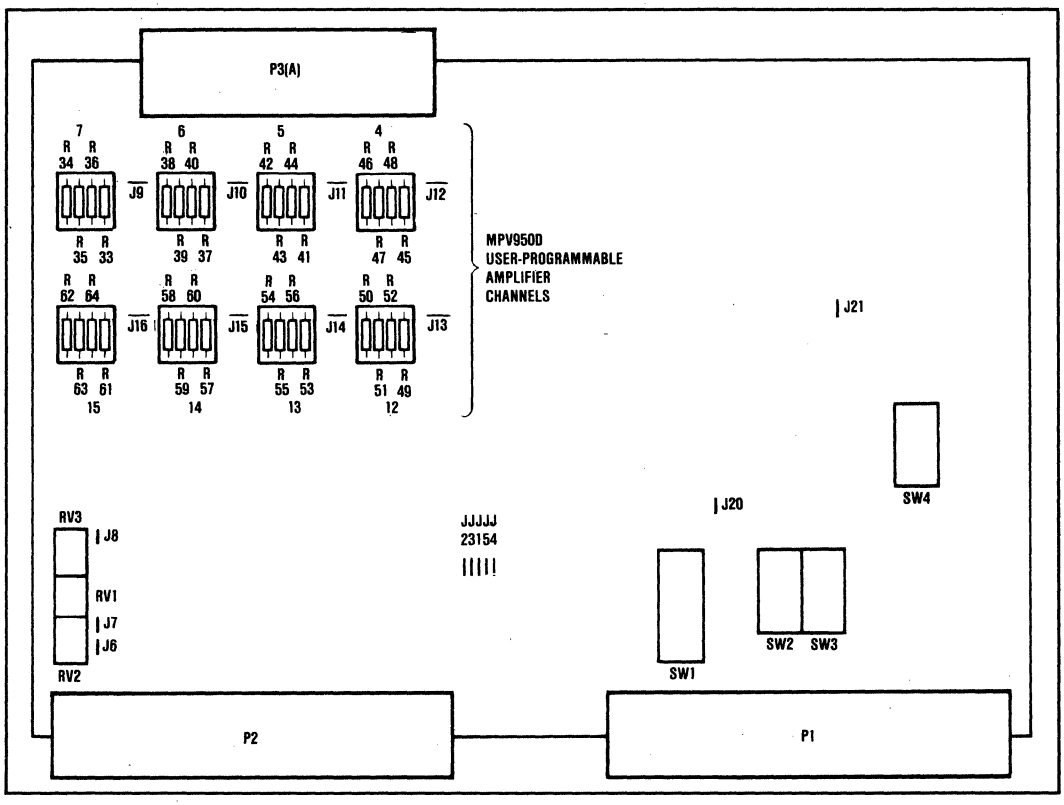


FIGURE 4. MPV950 Series Switch and Jumper Positions.

CONNECTOR PINOUT ("D" TYPE)

Pin No.	Description	Pin No.	Description
1	IN15	20	RET15
2	IN07	21	RET07
3	IN14	22	RET14
4	IN06	23	RET06
5	IN13	24	RET13
6	IN05	25	RET05
7	IN12	26	RET12
8	IN04	27	RET04
9	0V (ANALOG COMMON)	28	0V (ANALOG COMMON)
10	IN11	29	RET11
11	IN03	30	RET03
12	IN10	31	RET10
13	IN02	32	RET02
14	IN09	33	RET09
15	IN01	34	RET01
16	IN08	35	RET08
17	IN00	36	RET00
18	TRIGGER RETURN	37	EXTERNAL TRIGGER
19	TRIGGER RETURN		

NOTE: Unused analog inputs should be connected to 0V (Analog Common)

ORDERING INFORMATION

The following options are available when ordering MPV950 series boards.

Description	Model
16 channels single-ended, analog input	MPV950S
8 channels with user-programmable amplifiers	MPV950D

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