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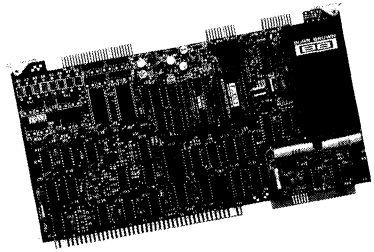
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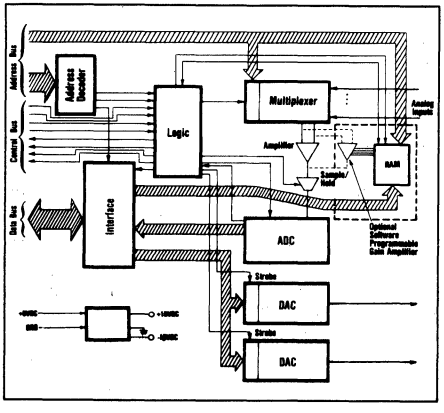
MP8418

MICROCOMPUTER ANALOG I/O SYSTEMS

A 31-CHANNEL ANALOG INPUT, 2-CHANNEL OUTPUT SYSTEM COMPATIBLE WITH INTEL SBC80, INTELLEC® MDS AND NATIONAL BLC-80 MICROCOMPUTERS

FEATURES

- HIGH AND LOW LEVEL INPUTS
- SOFTWARE PROGRAMMABLE GAIN (1 to 1024) AMPLIFIER OPTION
- ANALOG INPUT AND OUTPUT ON ONE BOARD
- EASILY PROGRAMMED
- MEMORY MAPPED
- LOW COST
- BURN-IN



DESCRIPTION

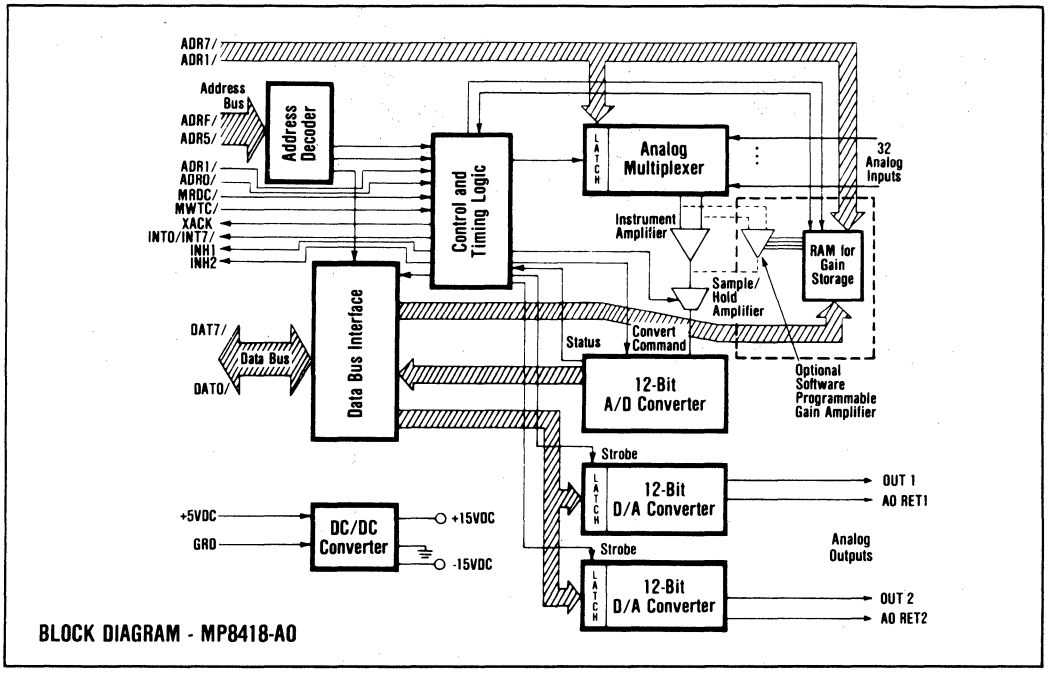
The MP8418 series of analog I/O peripherals are electrically and mechanically compatible with and interface directly to Intel's MULTIBUS® and other microcomputers of similar configuration. These analog systems are treated as memory by the CPU.

The analog input portion of the MP8418 includes: over-voltage protection to 26VDC; provision for up to eight 4mA to 20mA inputs; an analog multiplexer; resistor programmed instrument amplifier or, a software programmable amplifier (gain of 1 to 1024); sample/hold amplifier and; a 12-bit A/D converter. An optional analog output system is included on the same board. It consists of two 12-bit D/A converters with double buffered inputs to minimize glitches, and control logic.

MP8418 is a 15-channel differential (user strapable as 31 channel single-ended) analog input system. With one expander board the system can be expanded to 63 differential channels (strapable as 127 single-ended channels). Another input channel is grounded on the board so that it may be used as ground reference for automatic calibration.

Gains of 1 to 1024 are software selectable for the programmable amplifiers and the gain for each channel (up to 127 channels) may be stored in an on-board RAM if desired. The proper gain for each channel is then selected automatically by the MP8418.

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BLOCK DIAGRAM - MP8418-AO

MECHANICAL SPECIFICATIONS

Compatible with Intellec MDS and SBC-604/614 card spacing.

Minimum card spacing: 15.2mm (0.6").

Microcomputer bus connector required: 86-pin PC edge connector with 0.156" contact centers.

One 50-pin analog edge connector on board for analog inputs.
Mating connector available from Burr-Brown:
2250MC. (Viking #3VH25/1JN5, solder tab);
from 3M: 3415-0001 (Scotchflex).

Two 20-pin analog edge connectors on board for analog outputs and analog input expansion.
Mating connector available from Burr-Brown:
2220MC. (Viking #3VH10/1JN5).

OPERATING INSTRUCTIONS

INSTALLATION

MP8418 is shipped from the factory calibrated and ready to use. Installation requires only plugging the card into any empty slot in the computer and wiring the analog connector.

PROGRAMMING

This peripheral is programmed as a memory location and any memory reference instruction can be used. Both the A/D converter output and D/A converter input are 12-bit words, therefore, two memory locations are needed for each channel. The address block occupied by each MP8418 is user selectable and can be placed anywhere in memory.

Because these peripherals are treated as memory, a minimum of instructions are needed to read an input channel, or to set the input of a D/A converter. For example: when the MP8418 is connected in the HALT mode, the LHLD (load) instruction followed by the proper address can be used to read data from an analog input channel. It will automatically select the desired channel, initiate conversion and when conversion is complete, transfer the A/D converter output to the 8080's H and L registers. The eight least significant bits (LSB's) of the data word are transferred to the CPU first followed by the four most significant bits (MSB's). The four MSB's are in data bus positions 0 - 3. A single SHLD instruction can be used to write data to one analog output channel. The eight LSB's are written first, followed by the four MSB's (in D0-D3). When the four MSB's are written to the board, all twelve bits of the data word are transferred simultaneously to the D/A converter input.

ADC/DAC Bit Placement

	D7	D6	D5	D4	D3	D2	D1	D0
Low Byte	B_3	B_2	B_1	B_0	B_1	B_2	B_1	B_0
High Byte	X	X	X	X	B_{11}	B_{10}	B_9	B_8

On MP8418's, with the software programmable gain amplifier, an on-board random access memory (RAM) may be used to store the gain for each channel. In this

mode, (Control Register D4 = 1), the proper gain is automatically selected from the RAM when a channel is converted. If the RAM is not used (Control Register D4 = 0), the amplifier gain must be written to an on-board register (Control Register D0-D3).

All these systems are jumpered at the factory with a base address of $F700_{16}$. Each subsequent channel is two memory locations past the start of the last channel, consequently channel one is at location $F702_{16}$, channel two is at location $F704_{16}$, etc.

The input system operates in several modes:

INTERRUPT MODE: A read instruction to the board (ADR0 = 0) starts the conversion. An interrupt is generated at the end of the conversion. The interrupt can be connected to any of eight vector locations and may also be disabled by software. Control Register D6 = 1 enables interrupt for interrupt mode.

POLLING MODE: A read to the board starts the conversion. The interrupt is disabled by software and the CPU may then read the status word to determine when conversion is complete. Control Register D6 = 0 disables interrupt for polling mode.

HALT MODE: a read instruction to the board starts the conversion. The MP8418 halts the CPU until conversion is complete, at which point the data is transferred to the CPU. Only one instruction is needed to start conversion and to transfer data to the CPU (an LHLD or POP referenced to the channel's LSB's can be used).

CONTINUOUS MODE: A read instruction to the board starts the conversion. The CPU is not halted, but reads the status of the MP8418 to determine when conversion is complete (Control Register D6 = 0) - or the CPU waits for an interrupt (Control Register D6 = 1). When conversion is complete, the CPU reads the data. The read instruction is addressed to the next channel to be converted. The data from the last conversion is thus transferred to the CPU and conversion is started for the next channel.

EXTERNAL TRIGGER: This mode allows a conversion to be started independent of the CPU. A read instruction is required to set the proper channel. Once the board has been set, a low to high transition of the EXTERNAL TRIGGER input (P5, pin 20) will start conversion. End of conversion can be detected by polling or interrupt technique. Data is obtained by any read command. The external trigger will start conversion independent of other board functions. The busy input (P5, pin 19) goes high at the start of conversion and goes low when the MSB of the converted data is read by CPU.

ELECTRICAL SPECIFICATIONS

Typical at 25°C and rated power supplies unless otherwise noted.

ANALOG INPUT SECTION	MP8418
INPUT CHARACTERISTICS	
Number of Channels	31 single-ended/15 differential
ADC Gain Ranges (Jumper Selectable)[1]	0 to 5V, 0 to 10V, ±2.5V, ±5V, ±10V
Amplifier Gain Ranges	
Resistor Programmable[2]/Software Programmable	1 to 1000/1 to 1024
Maximum Input Voltage Without Damage[3]	±26 volts
Input Impedance	100MΩ, 10pF OFF Channel
	100MΩ, 100pF ON Channel
Bias Current (25°C)	±20nA
Bias Current (0 to 70°C)	±50nA
Differential Bias Current	±10nA
Amplifier Input Offset Voltage G = 1000	
Resistor Programmable/Software Programmable	±400μV/±4μV
Amplifier Input Offset Voltage Drift G = 1000	
Resistor Programmable/Software Programmable	±2μV/°C/±1μV/°C
TRANSFER CHARACTERISTICS	
Resolution	12 Bits
Throughput Time (max) G = 1	
Resistor Programmable/Software Programmable	38μsec/350μsec
Throughput Time G = 1024	
Resistor Programmable/Software Programmable	100μsec/350μsec
ACCURACY	
System Accuracy at +25°C (max)[4] G = 1	±0.0325% FSR[5]
System Accuracy at +25°C[4] G = 1024	
Resistor Programmable/Software Programmable	±0.1% FSR/±0.05% FSR (max)
Linearity	±1/2LSB
Differential Linearity	±1/2LSB
Quantizing Error	±1/2LSB
Gain Error	Adjustable to Zero[6]
Offset Error	Adjustable to Zero
Monotonicity[7]	Guaranteed 0°C to +70°C
STABILITY OVER TEMPERATURE (Bipolar)[8]	
System Accuracy Drift (max) G = 1	±45ppm of FSR/°C
System Accuracy Drift G = 1024	±100ppm of FSR/°C
DYNAMIC ACCURACY	
Sample/Hold Aperture Time	125nsec
Aperture Time Uncertainty	±5nsec
Differential Amplifier CMRR G = 1	86dB (DC to 60Hz)
Channel Crosstalk	80dB down at 1kHz, for OFF Channel to ON Channel
ANALOG OUTPUT SECTION (AO option)	
OUTPUT CHARACTERISTICS	
Number of Channels	2
Output Voltage Ranges (Strap Selectable)	±10V, 0 to 10V, ±5V, 0 to 5V, ±2.5V at 5mA
Output Impedance	1Ω
Short Circuit Protection	Yes
TRANSFER CHARACTERISTICS	
Resolution	12 bits
Output Settling Time (max)	10μsec
ACCURACY	
Output Accuracy	±0.0125% FSR
Temperature Coefficient of Accuracy	±30ppm of FSR/°C
POWER REQUIREMENTS	
MP8418/MP8418-PGA	+5V ±5% at 1.2A
MP8418-AO/MP8418-PGA-AO	+5V ±5% at 2.0A
ENVIRONMENTAL	
Operating Temperature	0°C to +70°C
Relative Humidity	95% noncondensing

NOTES:
1. Factory set for ±10V range.
2. Factory set for Gain = 1.
3. With power off. ±36 volts with power on.
4. Includes linearity errors with gain and offset errors adjusted to zero.
5. FSR means Full Scale Range.
6. When any one gain range is adjusted to zero gain error, the gain error for any other range is less than ±0.02% when using the software programmable amplifier.
7. No missing codes guaranteed.
8. Includes offset drift, gain drift and linearity drift.

FACTORY MODE CONNECTIONS	
MODEL	FACTORY SET MODE
MP8418	HALT
MP8418-AO	HALT
MP8418-PGA	POLLING INTERRUPT*
MP8418-PGA-AO	POLLING INTERRUPT*

Note: Any model can be connected in any mode.
*Int 1 Factory Set

TABLE I. Programming Mode Connections.

JUMPER REQUIRED	
Halt Mode	JP17, JP29, JP30, JP81
Polling and Interrupt Mode	JP17, JP29, JP81
Continuous Mode	JP17, JP31, JP82
External Trigger Mode	JP16, JP29, JP81

TABLE II. Mode Selection Jumpers.

JUMPERS REQUIRED FOR INTERRUPT VECTOR	
INT0/	JP70
INT1/	JP71
INT2/	JP72
INT3/	JP73
INT4/	JP74
INT5	JP75
INT6/	JP76
INT7/	JP77

TABLE III. Interrupt Selection.

MEMORY MAP

Factory Set	ADR7 ... ADR0		READ		WRITE	
F700	0000 0000	CH0	8LSB's of offset		N/A	GAIN 0*
F701	0000 0001	IN	STATUS		CONTROL	
F702	0000 0010	CH1	LSB		N/A	GAIN 1*
F703	0000 0011	IN	MSB		N/A	
F704	0000 0100	CH2	LSB	CH0 OUT	LSB	GAIN 2*
F705	0000 0101	IN	MSB	or GAIN	MSB	
F706	0000 0110	CH3	LSB	CH1 OUT	LSB	GAIN 3*
F707	0000 0111	IN	MSB	or GAIN	MSB	
F708	0000 1000	CH4	LSB		N/A	GAIN 4*
F709	0000 1001	IN	MSB		N/A	
			⋮		⋮	
F71E	0001 1110	CH15	LSB		N/A	GAIN 15*
F71F	0001 1111	IN	MSB		N/A	
F710	0001 0000	CH16	LSB		N/A	GAIN 16*
F711	0001 0001	IN	MSB		N/A	
			⋮		⋮	

N/A - Not used.

*Used only on PGA versions when RAM gain storage is used.

A read instruction (other than a STATUS REGISTER read) should not be made to the board during a conversion. Contact factory for more details.

STATUS REGISTER

D7	D6	D5	D4	D3	D2	D1	D0
Convert Complete	Interrupt Enable	Write* Enable	RAM* Enable	--------	GAIN X*	----------	

*Used only on versions with software programmable amplifier.

Convert Complete - The bit is low during conversion. It goes high on completion of conversion and remains high until the MSB of a data word is read.

Interrupt enable: status of interrupt enable
Write enable: status of write enable
RAM enable: status of RAM enable
GAIN X: current value stored in PGA GAIN control register.

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