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SMLS240D– NOVEMBER 1990 – REVISED SEPTEMBER 1997

- **Organization . . . 262144 by 16 Bits**
- **Single 5-V Power Supply**
- **All Inputs/Outputs Fully TTL Compatible**
- **Static Operations (No Clocks, No Refresh)**
- **Max Access/Min Cycle Time**

  V_{CC} ± 10%
  '27C/PC240-10 100 ns
  '27C/PC240-12 120 ns
  '27C/PC240-15 150 ns
- **16-Bit Output For Use in Microprocessor-Based Systems**
- **Very High Speed SNAP! Pulse Programming**
- **Power-Saving CMOS Technology**
- **3-State Output Buffers**
- **400-mV Minimum DC Noise Immunity With Standard TTL Loads**
- **Latchup Immunity of 250 mA on All Input and Output Lines**
- **No Pullup Resistors Required**
- **Low Power Dissipation (V_{CC} = 5.5 V)**
  - **Active . . . 275 mW Worst Case**
  - **Standby . . . 0.55 mW Worst Case (CMOS-Input Levels)**
- **Temperature Range Options**

PIN NOMENCLATURE	
A0–A17	Address Inputs
DQ0–DQ15	Inputs (programming)/Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
GND	Ground
NC	No Connection
V_{CC}	5-V Supply
V_{PP}	13-V Power Supply‡

† Pins 11 and 30 (J package) and pins 12 and 34 (FN package) must be connected externally to ground.
‡ Only in program mode

description

The TMS27C240 series are 262144 by 16-bit (4194304-bit), ultraviolet-light erasable, electrically programmable read-only memories (EPROMs).

These devices are fabricated using power-saving CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors. Each output can drive one Series 74 TTL circuit without external resistors.

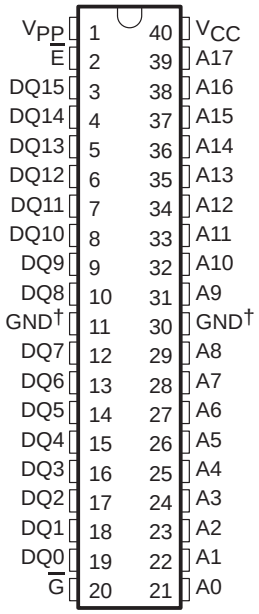
The TMS27C240 EPROM is offered in a dual-in-line ceramic package (J suffix) designed for insertion in mounting hole rows on 15,2-mm (600-mil) centers. The TMS27C240 is offered with two choices of temperature ranges of 0°C to 70°C (JL suffix) and – 40°C to 85°C (JE suffix). See Table 1.

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TMS27C240 J PACKAGE
(TOP VIEW)



description (continued)

The TMS27PC240 OTP PROM is offered in a 44-lead plastic leaded chip carrier package using 1,25-mm (50-mil) lead spacing (FN suffix). The TMS27PC240 is offered with two choices of temperature ranges of 0°C to 70°C (FNL suffix) and –40°C to 85°C (FNE suffix). See Table 1.

Table 1. Temperature Range Suffixes

	SUFFIX FOR OPERATING FREE-AIR TEMPERATURE RANGES	
	0°C TO 70°C	– 40°C TO 85°C
TMS27C240-XXX	JL	JE
TMS27PC240-XXX	FNL	FNE

These EPROMs and OTP PROMs operate from a single 5-V supply (in the read mode), and they are ideal for use in microprocessor-based systems. One other (13 V) supply is needed for programming . All programming signals are TTL level. For programming outside the system, existing EPROM programmers can be used.

operation

The eight modes of operation for the TMS27C240 and TMS27PC240 are listed in Table 2. The read mode requires a single 5-V supply. All inputs are TTL level except for V_{PP} during programming (13 V for SNAP! Pulse), and 12 V on A9 for the signature mode.

Table 2. Operation Modes

	FUNCTION†						
	$\overline{E}$	$\overline{G}$	V_{PP}	V_{CC}	A9	A0	I/O
Read	V_{IL}	V_{IL}	V_{CC}	V_{CC}	X	X	DQ0–DQ7 DQ8–DQ15
Output Disable	V_{IL}	V_{IH}	V_{CC}	V_{CC}	X	X	Hi-Z
Standby	V_{IH}	X	V_{CC}	V_{CC}	X	X	Hi-Z
Programming	V_{IL}	V_{IH}	V_{PP}	V_{CC}	X	X	Data In
Verify	V_{IH}	V_{IL}	V_{PP}	V_{CC}	X	X	Data Out
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	V_{CC}	X	X	Hi-Z
Signature Mode (Mfg)	V_{IL}	V_{IL}	V_{CC}	V_{CC}	V_H‡	V_{IL}	Manufacturer's Code 0097
Signature Mode (Device)	V_{IL}	V_{IL}	V_{CC}	V_{CC}	V_H‡	V_{IH}	Device Code 0030

† X can be V_{IL} or V_{IH}.
‡ V_H = 12 V ± 0.5 V.

read/output disable

When the outputs of two or more TMS27C240s or TMS27PC240s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of a single device, a low-level signal is applied to the $\overline{E}$ and $\overline{G}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins.

latchup immunity

Latchup immunity on the TMS27C240 and TMS27PC240 is a minimum of 250 mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the P.C. board level when the devices are interfaced to industry-standard TTL or MOS logic devices. Input-output layout approach controls latchup without compromising performance or packing density.

power down

Active I_{CC} supply current can be reduced from 50 mA to 1 mA by applying a high TTL input on $\overline{E}$ and to 100 μA by applying a high CMOS input on $\overline{E}$. In this mode all outputs are in the high-impedance state.

erasure (TMS27C240)

Before programming, the TMS27C240 is erased by exposing the chip through the transparent lid to a high intensity ultraviolet light (wavelength 2537 Å). The recommended minimum exposure dose (UV intensity × exposure time) is 15-W·s/cm^2. A 12-mW/cm^2, filterless UV lamp erases the device in 21 minutes. The lamp should be located about 2.5 cm above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TMS27C240, the window should be covered with an opaque label.

initializing (TMS27PC240)

The one-time programmable TMS27PC240 PROM is provided with all bits in the logic high state, then logic lows are programmed into the desired locations. Logic lows programmed into an OTP PROM cannot be erased.

SNAP! Pulse programming

The TMS27C240 and TMS27PC240 are programmed by using the SNAP! Pulse programming algorithm. The programming sequence is shown in the SNAP! Pulse programming flow chart, shown in Figure 1.

The initial setup is V_{PP} = 13 V, V_{CC} = 6.5 V, $\overline{E} = V_{IH}$, and $\overline{G} = V_{IH}$. Once the initial location is selected, the data is presented in parallel (eight bits) on pins DQ0 through DQ15. Once addresses and data are stable, the programming mode is achieved when $\overline{E}$ is pulsed low (V_{IL}) with a pulse duration of $t_{w(PGM)}$. Every location is programmed only once before going to interactive mode.

In the interactive mode, the word is verified at V_{PP} = 13 V, V_{CC} = 6.5 V, $\overline{E} = V_{IH}$, and $\overline{G} = V_{IL}$. If the correct data is not read, the programming is performed by pulling $\overline{E}$ low with a pulse duration of $t_{w(PGM)}$. This sequence of verification and programming is performed up to a maximum of 10 times. When the device is fully programmed, all bytes are verified with $V_{CC} = V_{PP} = 5\ V \pm 10\%$.

program inhibit

Programming can be inhibited by maintaining a high level input on the $\overline{E}$ and $\overline{G}$ pins.

program verify

Programmed bits can be verified with V_{PP} = 13 V when $\overline{G} = V_{IL}$ and $\overline{E} = V_{IH}$.

signature mode

The signature mode provides access to a binary code identifying the manufacturer and type. This mode is activated when A9 (pin 31 for the J package) is forced to 12 V. Two identifier bytes are accessed by toggling A0. DQ0–DQ7 contain the valid codes. All other addresses must be held low. The signature code for these devices is 9730. A0 low selects the manufacturer's code 97 (Hex), and A0 high selects the device code 30 (Hex), as shown in Table 3.

Table 3. Signature Mode

IDENTIFIER†	PINS									
	A0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	HEX
MANUFACTURER CODE	V_{IL}	1	0	0	1	0	1	1	1	97
DEVICE CODE	V_{IH}	0	0	1	1	0	0	0	0	30

† $\overline{E} = \overline{G} = V_{IL}$, A9 = V_H, A1–A8 = V_{IL}, A10–A17 = V_{IL}, $V_{PP} = V_{CC}$, $\overline{PGM} = V_{IH}$ or V_{IL}.

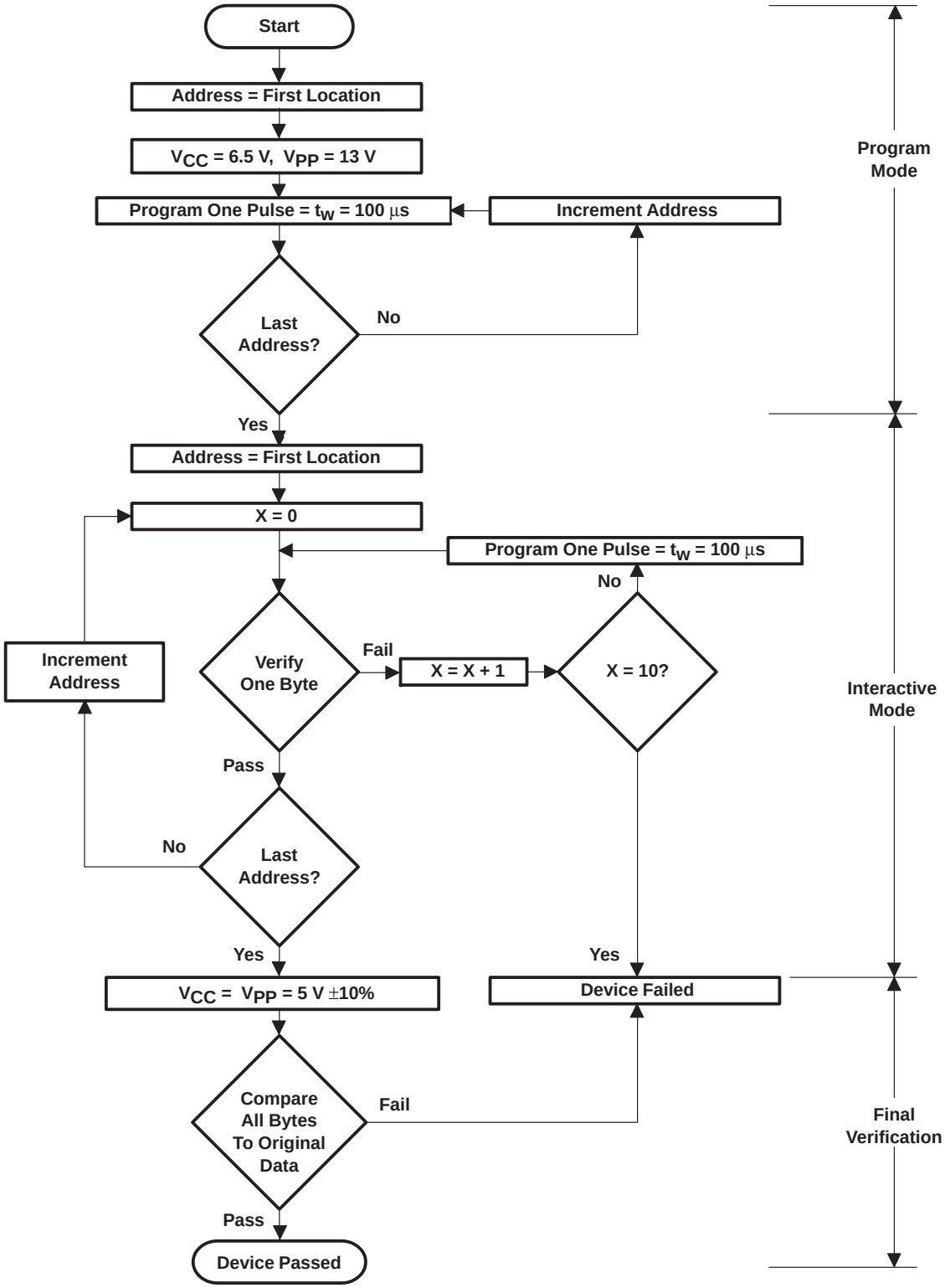
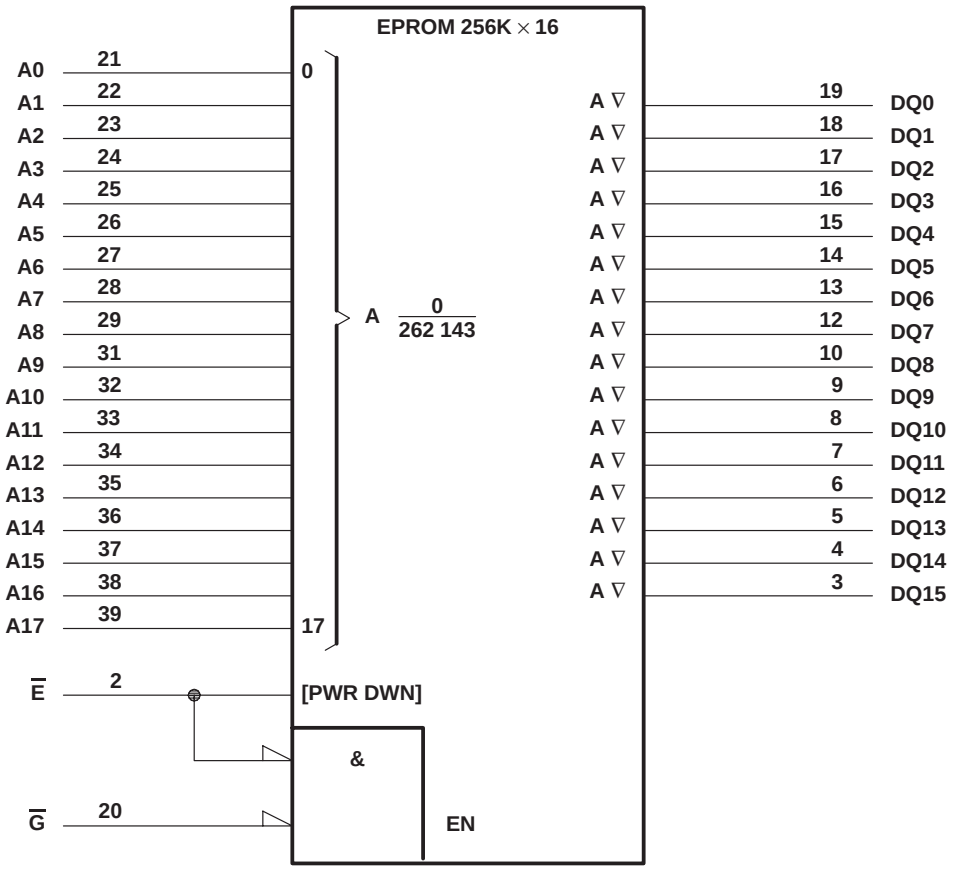


Figure 1. SNAP! Pulse Programming Flow Chart

logic symbol†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers are for the J package.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . –0.6 V to 7 V
Supply voltage range, V_{PP} . . . . . –0.6 V to 13 V
Input voltage range (see Note 1): All inputs except A9 . . . . . –0.6 V to V_{CC} + 1 V
A9 . . . . . –0.6 V to 13.5 V
Output voltage range (see Note 1) . . . . . –0.6 V to V_{CC} + 1 V
Operating free-air temperature range (’27C240-_ _JL; ’27PC240-_ _ FNL) . . . . . 0° C to 70° C
Operating free-air temperature range (’27C240-_ _JE, ’27PC240-_ _FNE) . . . . . – 40° C to 85° C
Storage temperature range, T_{stg} . . . . . –65°C to 150° C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	Read mode (see Note 2)		4.5	5	5.5	V
		SNAP! Pulse programming algorithm		6.25	6.5	6.75	
V_{PP}	Supply voltage	Read mode		V_{CC}–0.6		V_{CC}+0.6	V
		SNAP! Pulse programming algorithm		12.75	13	13.25	
V_{IH}	High-level dc input voltage		TTL	2		V_{CC}+0.5	V
			CMOS	V_{CC} – 0.2		V_{CC}+0.5	
V_{IL}	Low-level dc input voltage		TTL	– 0.5		0.8	V
			CMOS	– 0.5		0.2	
T_A	Operating free-air temperature		’27C240-_ _JL ’27PC240-_ _ FNL	0		70	°C
T_A	Operating free-air temperature		’27PC240-_ _FNE ’27C240-_ _JE	– 40		85	°C

NOTE 2: V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level dc output voltage	I_{OH} = – 400 µA	2.4		V
		I_{OH} = – 20 µA	V_{CC} – 0.1		
V_{OL}	Low-level dc output voltage	I_{OL} = 2.1 mA		0.4	V
		I_{OL} = 20 µA		0.1	
I_I	Input current (leakage)	V_I = 0 V to 5.5 V		±1	µA
I_O	Output current (leakage)	V_O = 0 V to V_{CC}		±1	µA
I_{PP1}	V_{PP} supply current	V_{PP} = V_{CC} = 5.5 V		10	µA
I_{PP2}	V_{PP} supply current (during program pulse)	V_{PP} = 13 V		50	mA
I_{CC1}	VCC supply current (standby)	V_{CC} = 5.5 V, $\overline{E}$ = V_{IH}		1	mA
		V_{CC} = 5.5 V, $\overline{E}$ = V_{CC}		100	µA
I_{CC2}	V_{CC} supply current (active)	V_{CC} = 5.5 V, $\overline{E}$ = V_{IL}, t_{cycle} = minimum cycle time, outputs open		50	mA

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
C_i	Input capacitance	V_I = 0 V		4	8	pF
C_o	Output capacitance	V_O = 0 V		8	12	pF

† Capacitance measurements are made on a sample basis only.
‡ Typical values are at T_A = 25°C and nominal voltages.

switching characteristics over recommended ranges of operating conditions (see Notes 3 and 4)

PARAMETER		TEST CONDITIONS	'27C240-10 '27PC240-10		'27C240-12 '27PC240-12		'27C240-15 '27PC240-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL load, Input $t_r \le$ 20 ns, Input $t_f \le$ 20 ns		100		120		150	ns
$t_{a(E)}$	Access time from chip enable			100		120		150	ns
$t_{en(G)}$	Output enable time from $\overline{G}$			50		50		50	ns
t_{dis}	Output disable time from $\overline{G}$ or $\overline{E}$, whichever occurs first†		0	50	0	50	0	50	ns
$t_{v(A)}$	Output data valid time after change of address, $\overline{E}$, or $\overline{G}$, whichever occurs first§		0		0		0		ns

§ Value calculated from 0.5 V delta to measured level.

NOTES: 3. For all switching characteristics, the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low (see Figure 2).
4. Common test conditions apply for t_{dis} except during programming.

switching characteristics for programming: V_{CC} = 6.5 V and V_{PP} = 13 V (SNAP! Pulse), T_A = 25°C (see Note 3)

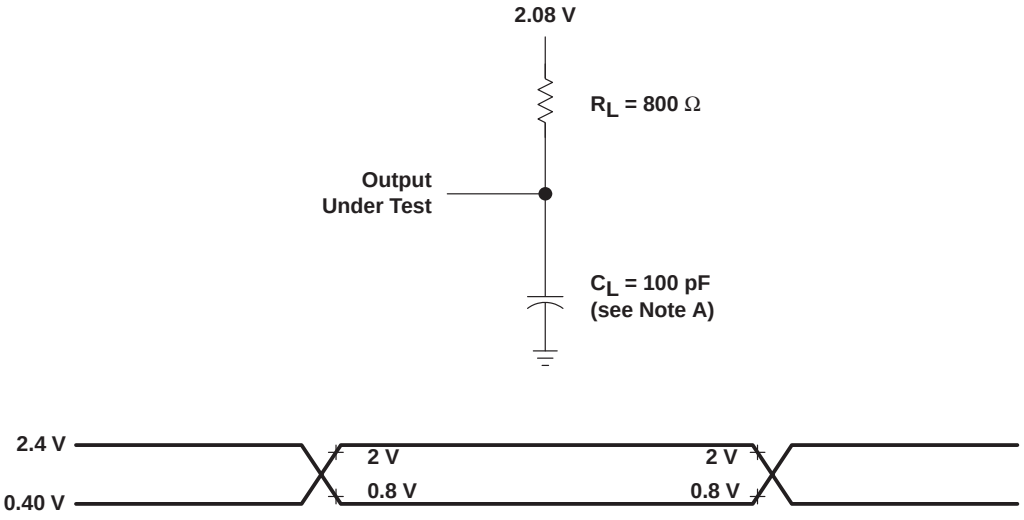
PARAMETER		MIN	MAX	UNIT
$t_{dis(G)}$	Output disable time from $\overline{G}$	0	100	ns
$t_{en(G)}$	Output enable time from $\overline{G}$		150	ns

NOTE 3: For all switching characteristics the input pulse levels are 0.4 V to 2.4 V. Timing measurements are made at 2 V for logic high and 0.8 V for logic low. (See Figure 2)

timing requirements for programming

			MIN	NOM	MAX	UNIT
$t_{w(PGM)}$	Pulse duration, program	SNAP! Pulse programming algorithm	95	100	105	µs
$t_{su(A)}$	Setup time, address		2			µs
$t_{su(E)}$	Setup time, $\overline{E}$		2			µs
$t_{su(G)}$	Setup time, $\overline{G}$		2			µs
$t_{su(D)}$	Setup time, data		2			µs
$t_{su(VPP)}$	Setup time, V_{PP}		2			µs
$t_{su(VCC)}$	Setup time, V_{CC}		2			µs
$t_{h(A)}$	Hold time, address		0			µs
$t_{h(D)}$	Hold time, data		2			µs

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and fixture capacitance.
B. The ac testing inputs are driven at 2.4 V for logic high and 0.4 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low for both inputs and outputs.

Figure 2. The ac Testing Output Load Circuit and Waveform

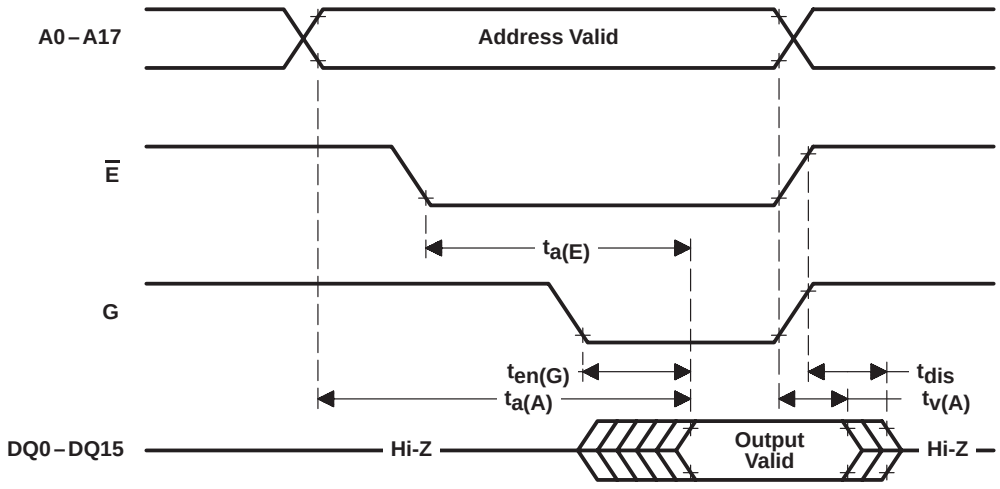
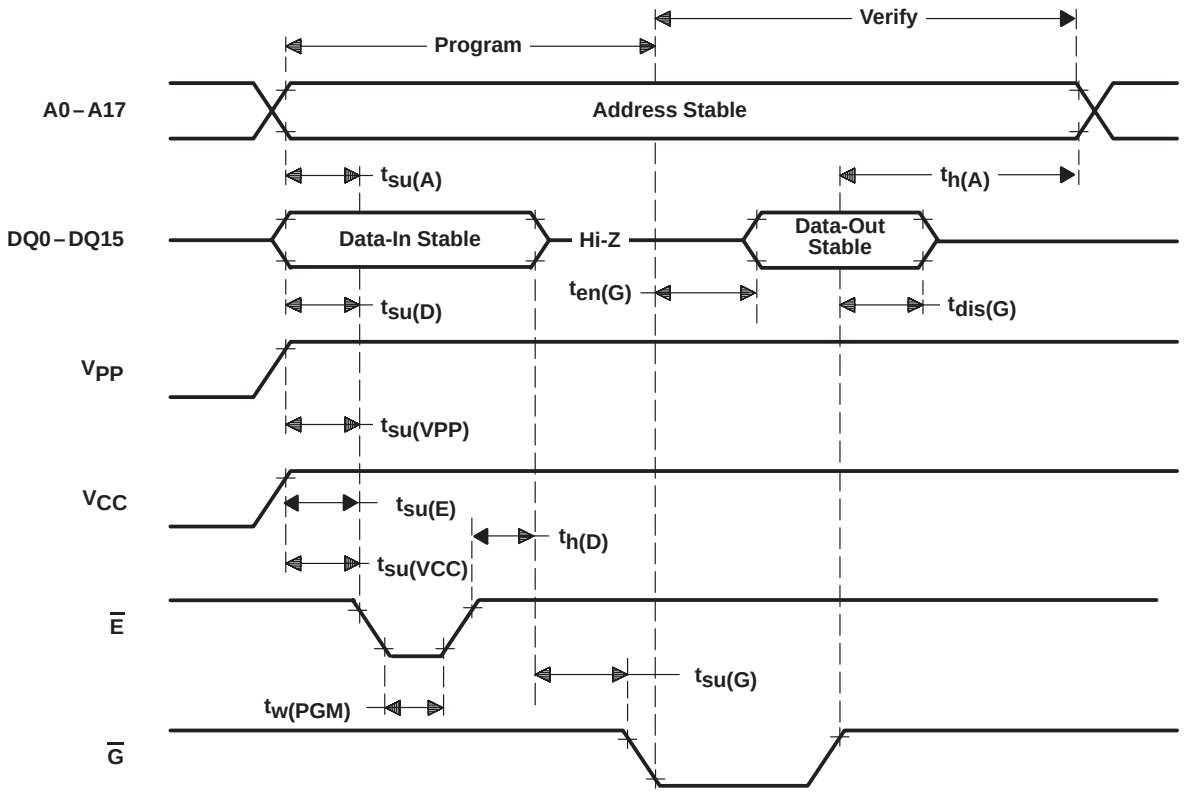


Figure 3. Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

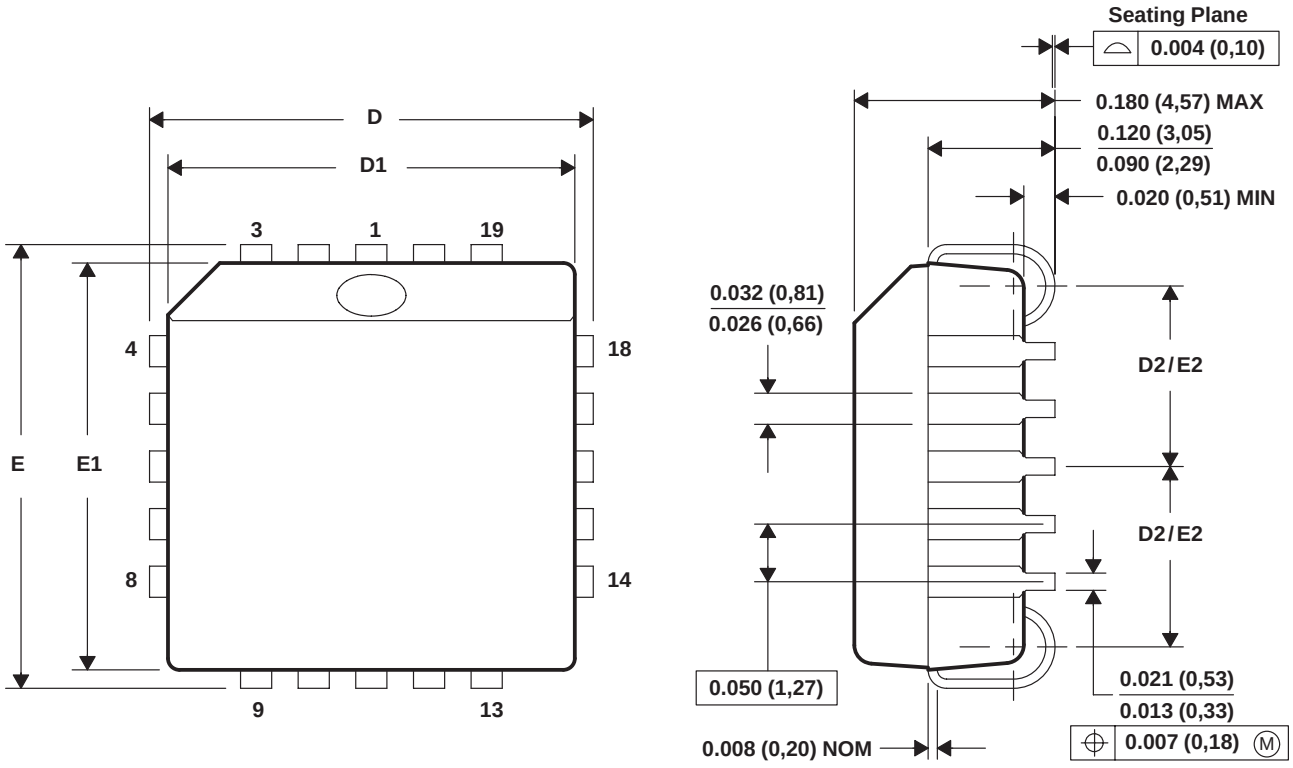


† 13-V V_{PP} and 6.5-V V_{CC} for SNAP! Pulse programming

Figure 4. Programming-Cycle Timing (SNAP! Pulse Programming)

FN (S-PQCC-J)** **PLASTIC J-LEADED CHIP CARRIER**

20 PIN SHOWN



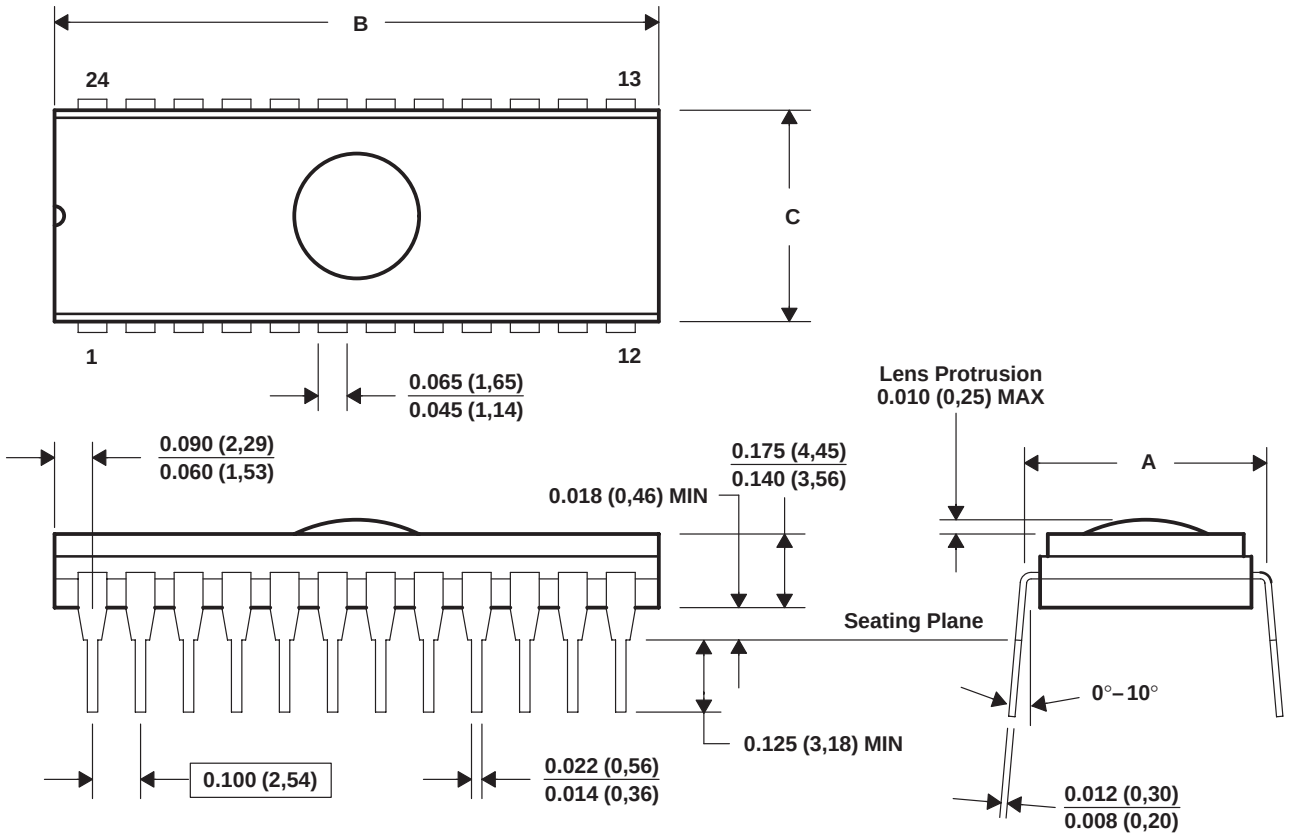
NO. OF PINS **	D/E		D1/E1		D2/E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

4040005/B 03/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

J (R-CDIP-T)** **CERAMIC SIDE-BRAZE DUAL-IN-LINE PACKAGE**

24 PIN SHOWN



DIM	PINS**	24 NARR	24 WIDE	28 NARR	28 WIDE	32 NARR	32 WIDE	40 NARR	40 WIDE
A	MAX	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)	0.624(15,85)
	MIN	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)	0.590(14,99)
B	MAX	1.265(32,13)	1.265(32,13)	1.465(37,21)	1.465(37,21)	1.668(42,37)	1.668(42,37)	2.068(52,53)	2.068(52,53)
	MIN	1.235(31,37)	1.235(31,37)	1.435(36,45)	1.435(36,45)	1.632(41,45)	1.632(41,45)	2.032(51,61)	2.032(51,61)
C	MAX	0.541(13,74)	0.598(15,19)	0.541(13,74)	0.598(15,19)	0.541(13,74)	0.598(15,19)	0.541(13,74)	0.598(15,19)
	MIN	0.514(13,06)	0.571(14,50)	0.514(13,06)	0.571(14,50)	0.514(13,06)	0.571(14,50)	0.514(13,06)	0.571(14,50)

4040084/B 04/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.

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