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DQP-1120
MV-DR11-W Compatible Option Module
Installation Manual

DQP-1120-OM
Revision A

Logical®

Installation Manual for the

DQP-1120

MDB MV-DR11-W Compatible Option Module for NuVAX

Logical®

Document Number MNL_DQP-1120_I1_A
Revision A, October 2017

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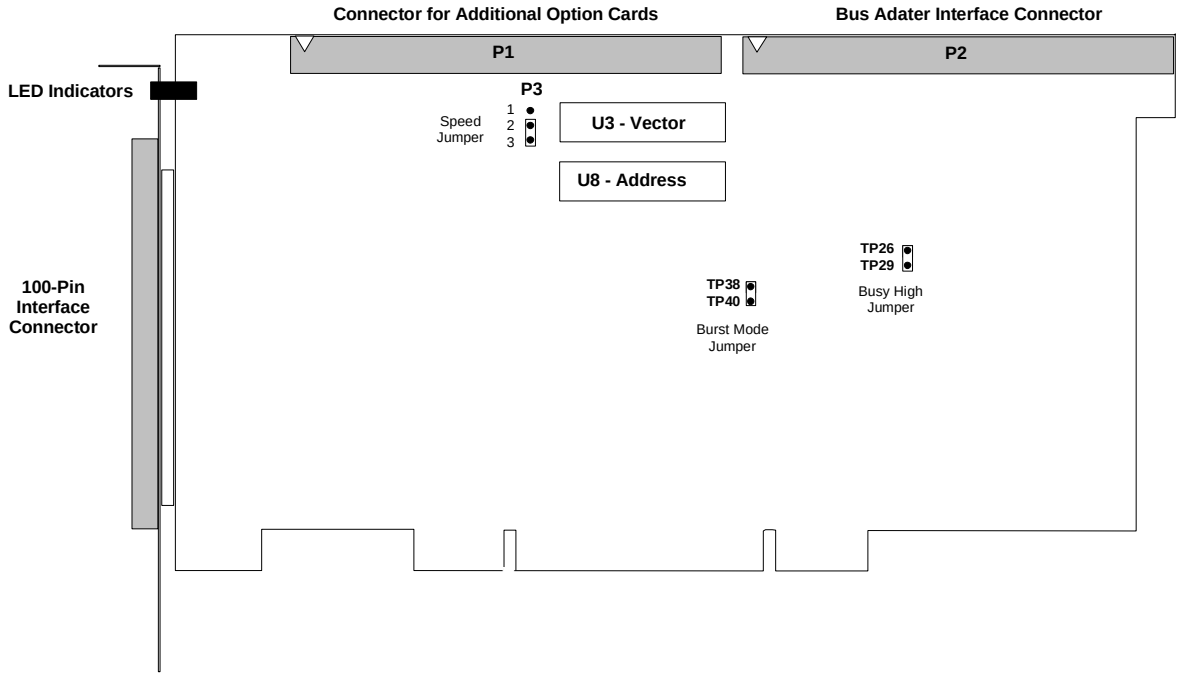
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1 Installation

This chapter lists the steps involved in installing the DQP-1120 option module. The DQP-1120 module is shown in Figure 1-1. Refer to this figure as you follow the steps outlined below.



Status Indicators:
Red indicates that there is a problem with the board.
Green indicates Qbus activity.

Figure 1-1: DQP-1120 Module

1. Set the switches on the DQP-1120 controller

The DQP-1120 contains two ten-position DIP switch-packs that allow the user to select device addresses, interrupt vectors, interrupt level 4 or 5 and 18 or 22-bit addressing mode.

Note

The DQP-1120 has the Unibus DR11-W register layout of the DR11-W board from MDP of Orange CA. When used with a MDB modified VMS XA device driver and VMS auto-configure compatible address and vector, the board will function correctly using the 18-bit DMA addressing mode. However the 22-bit DMA addressing mode is not hardware or software compatible and selection is not recommended or supported by Logical.

Interrupt Level and DMA Addressing Selection

Use positions 9 and 10 of switch-pack U3 to select interrupt level and DMA addressing mode as shown in Figure 1-2.

Switch position 9	Sets interrupt level to 4 or 5, level 4 is the factory setting.
Switch position 10	Sets 18-bit or 22-bit DMA addressing, 18-bit is the factory setting. Note that 22-bit addressing is NOT compatible with the MDB board or MDB modified XA device driver.

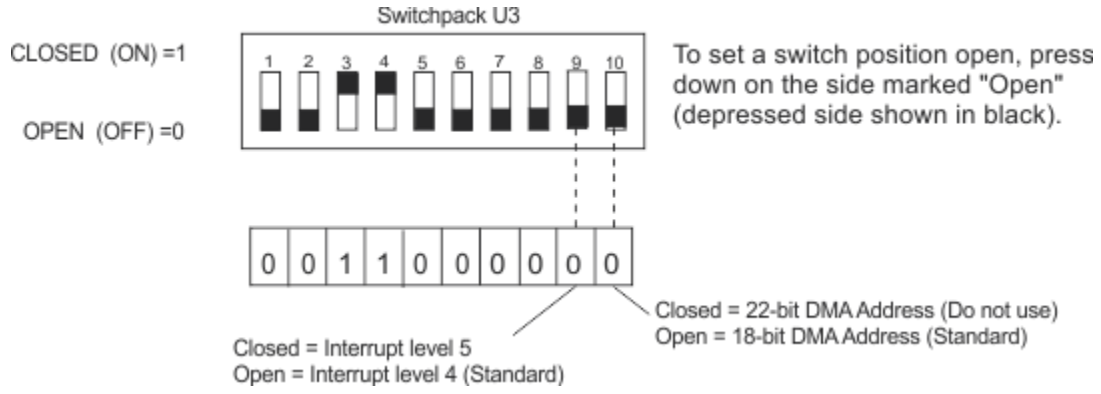


Figure 1-2: Interrupt Level and DMA Addressing Switch Settings

Device Address Selection

Use switch-pack U8 to select the device address for the DQP-1120 as shown in Figure 1-3. For the standard address of 17760240, switch positions 1, 2, 3, 4, 5, 7, 9, and 10 are set open; switch positions 6 and 8 are set closed.

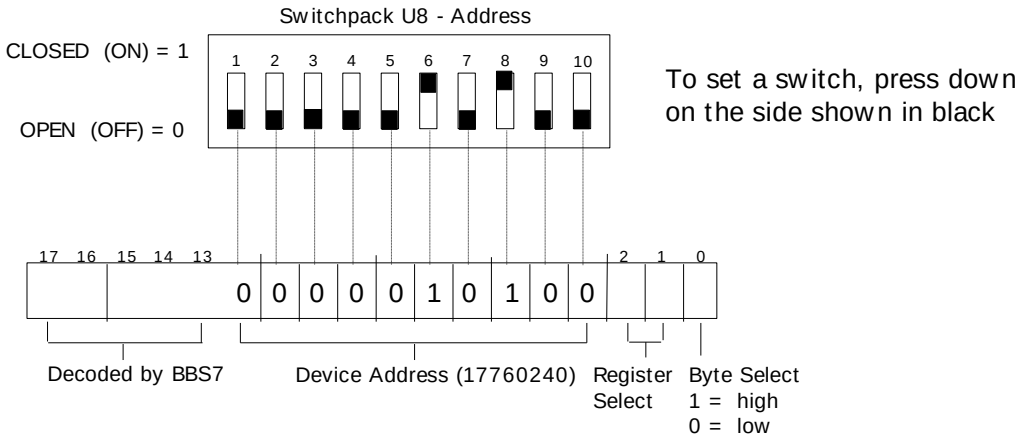


Figure 1-3: Device Address Switch Settings

Interrupt Vector Address Selection

Use switch-pack U3 to select the interrupt vector address for the DQP-1120 as shown in Figure 1-4. For the standard vector of 300, switch positions 1, 2, 5, 6, 7, and 8 are set open; positions 3, 4 are set closed.

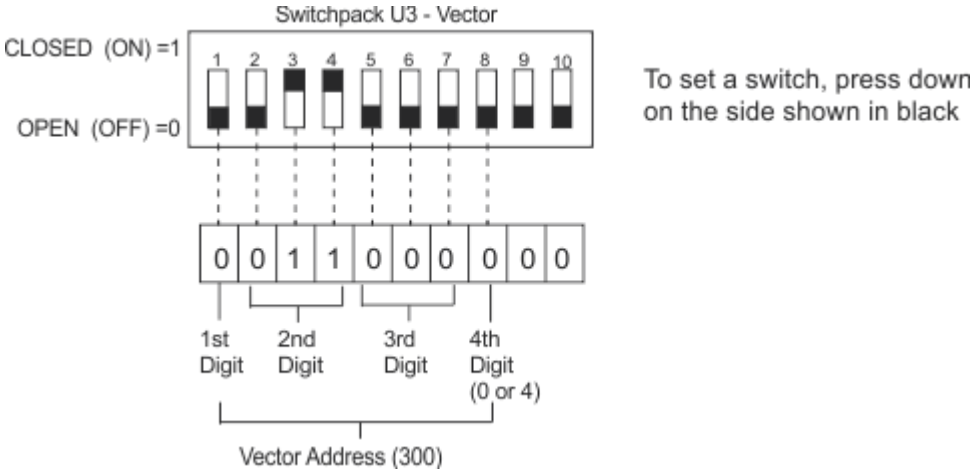


Figure 1-4: Vector Address Switch Settings

2. Configure the DQP-1120 jumpers

The DQP-1120 contains jumpers for selection of burst mode, speed, and busy polarity.

Qbus Burst Mode Jumper

The DQP-1120 is factory set to relinquish Qbus mastership after every eight DMA transfers. The user may select continuous Burst Mode transfers by removing the jumper between TP38 and TP40. When continuous burst mode is selected, the DQP-1120 will relinquish the bus when the CPU or DMA device requests the Qbus, otherwise, the DQP-1120 will retain mastership until the entire transfer is completed.

TP38 to TP40 Installed = Default
TP38 to TP40 Removed = Qbus Burst Mode

Selectable Qbus Burst Mode is provided to support high speed transfers where the DQP-1120 retains mastership of the Qbus for continuous transfers without re-arbitrating for the use of the Qbus. In Qbus Burst Mode, the DQP-1120 only relinquishes the Qbus whenever another DMA device or CPU requests use of the Qbus. When not in Qbus Burst Mode, the DQP-1120 relinquishes the Qbus after eight transfers or whenever another DMA or CPU requests use of the Qbus. In this mode the DQP-1120 needs to have its DMA request re-arbitrated after each eight transfers.

Speed Jumper

This jumper selection allows the user to slow the transfer from the CPU to the user device. Selecting SLOW when operating in user Burst Mode can prevent data overrun conditions. This feature may be especially beneficial when operating in user Burst Mode (SC low) so the user's equipment is not overrun when outputting data to the user equipment. Output data setup time is longer and BUSY low time is increased as shown in Table 1-1.

P3 jumper between 1 and 2 = SLOW
2 and 3 = FAST (Default)

Condition	Fast Mode	Slow Mode	Description
Output Data Setup time	200ns	400ns	The minimum time when data is valid and BUSY trailing edge
BUSY Low Assertion	300ns	500ns	The minimum time between data transfers in User Burst Mode (SC low). In Single Cycle mode (SC high), time between transfers is determined by input signal CYCRQ.

Table 1-1: Slow and Fast Modes

BUSY Signal Jumper

In the default setting (jumper installed), the BUSY signal is true when asserted low. With the jumper removed between TP26 and TP29, the BUSY signal is true when high.

TP26 to TP29 Installed = Default, BUSY low true
TP26 to TP29 Removed = BUSY high true

3. Open the system enclosure

To open the NuVAX system enclosure:

A. If the system is running, shut down the system software as described in the system manual.

B. Remove power to the system unit.

C. Open the enclosure by removing two thumb screws and sliding the cover towards the rear and lifting. Replace the two thumb screws into the chassis rear panel.

D. Remove the PCI card retainer rail by first lifting the black release knob and then lifting the rail up and out.

4. Install the DQP-1120 module

The DQP-1120 is installed in an option slot next to the bus adapter or other option module.

A. If the back of the expansion chassis or system unit has a metal cover plate over the opening of the slot you have selected, remove the anchor screw that holds the cover in place then slide the cover out of the slot.

B. Position the DQP-1120 with the gold fingers on the edge of the module next to the PCI connector of the selected slot. Gently rock the module into the PCI connector while you fit the metal bulkhead into the slot opening. Be sure that the connectors are firmly seated.

Note: If the enclosure contains RFI clips along the slot, take care when inserting the module not to push the clips out of alignment.

C. Secure the DQP-1120 using the anchor screw that you removed in Step A. Retain the cover plate for future use.

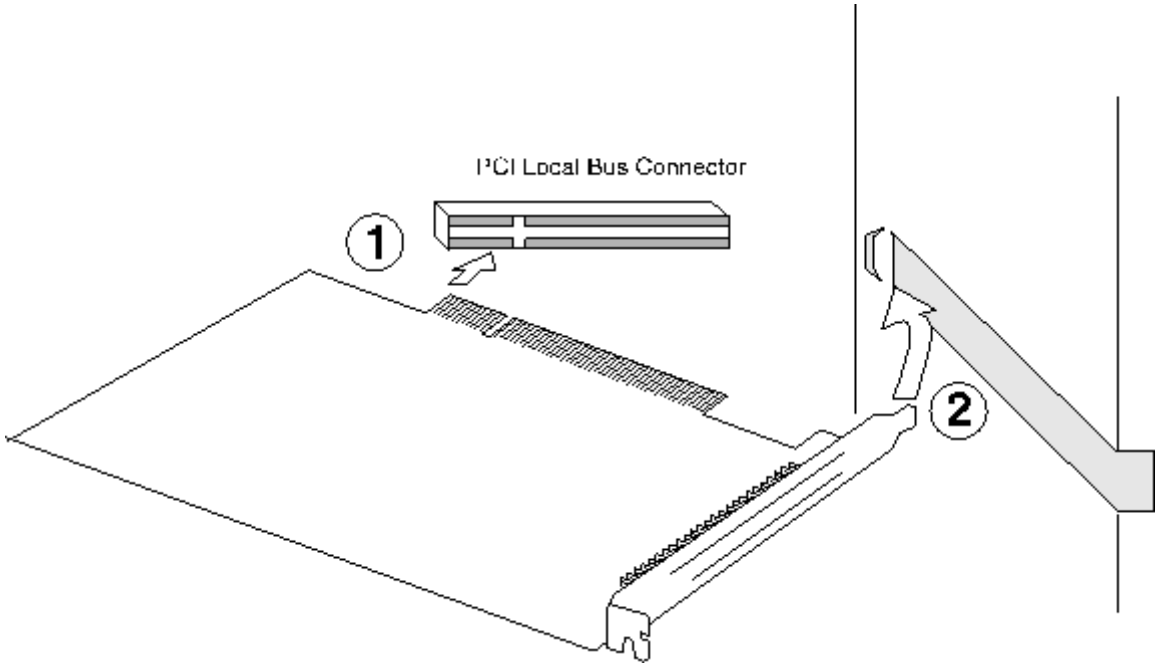


Figure 1-5: Inserting the Board into the PCI Slot

D. Replace the cover on the enclosure and secure.

You are now ready to connect the data cables.

5. Cable the DQP-1120 to the Bus Adapter

Use the supplied CAB-5011-2 cable to connect the first DQP-1120 to the BCI-2300 bus adapter as shown in Figure 1-6. Additional DQP-1120 controllers are added using the CAB-5011-2 as shown in the figure. Align the arrow on the connectors with the red line on the cable.

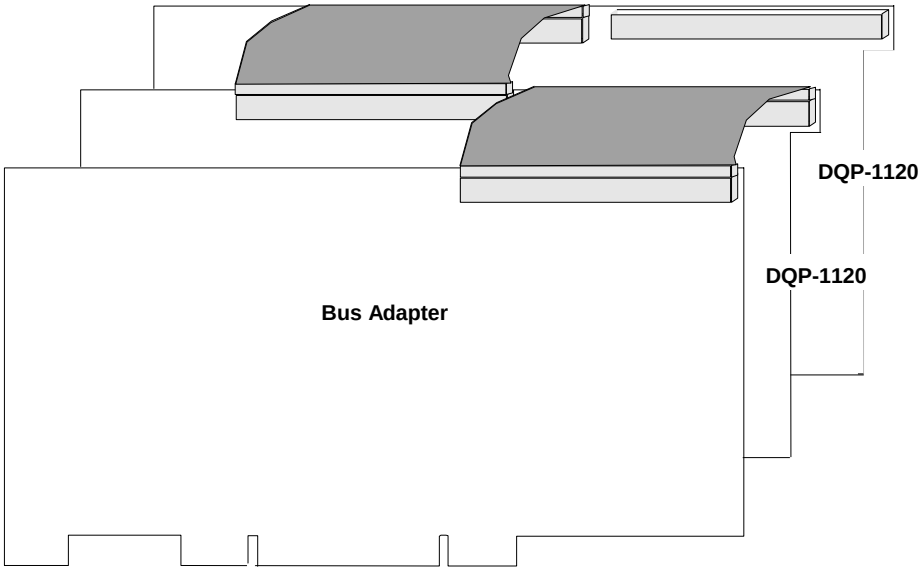
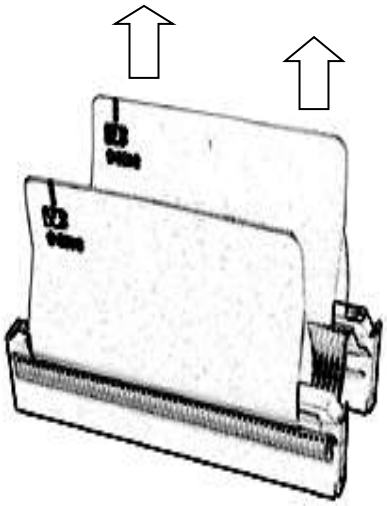


Figure 1-6: Cabling the DQP-1120 and the Bus Adapter

NOTE:
Use care when removing the 60-pin ribbon cable. Use the pull tab and pull the cable straight out from the connector to avoid damage to the connector.



6. Cable the DQP-1120 to the adapter panel

The CPX-1104 adapter panel is shown in Figure 1-7.

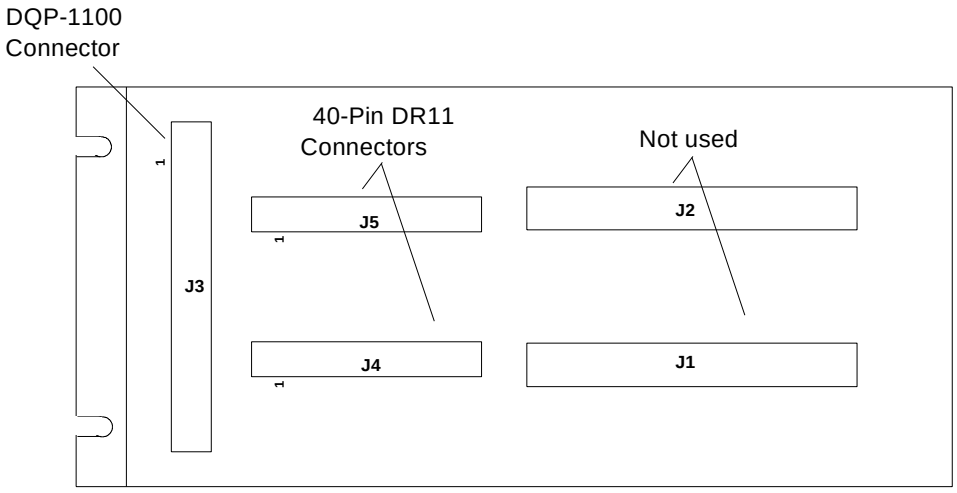


Figure 1-7: CPX-1104 Adapter Panel

Use the supplied 8-foot cable to connect the workstation to the DQP-1120 adapter panel. The adapter panel is provided with screw slots for RETMA rack mount or wall mount. It has no-mar feet for desktop or floor use.

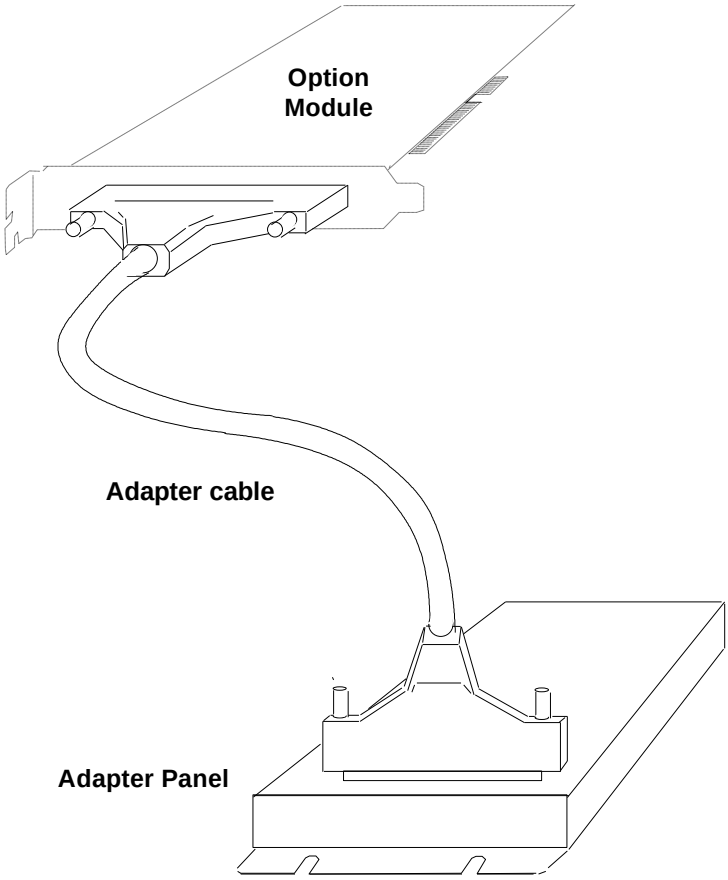


Figure 1-8: Cabling the Option Module to the Adapter Panel

7. Cable the CPX-1104 adapter to user equipment

Use two 40-pin cables to connect the user equipment to the DQP-1120 adapter panel. The function of each interface signal is described in Chapter 2.

J4 and J5 on the CPX-1104 adapter panel correspond to J1 and J2 on Digital's DR11-W or DRV11-WA. Connect user cables to the adapter the same as you would connect to a DR11-W or MDB's MV-DR11-W. If you are unsure, refer to the connector pin assignments in Appendix A. Be sure to align the triangles on each connector with pin 1.

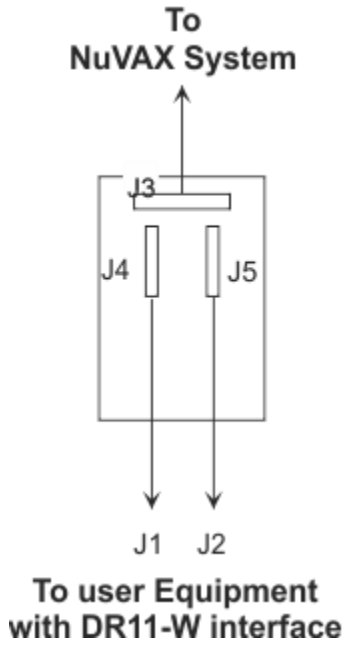


Figure 1-9: Cabling the CPX-1104 Adapter Panel to User Equipment

8. Power up and verify the DQP-1120

This step describes how to verify installation of the DQP-1120 in a NuVAX system. The DQP-1120 is supplied with a CAB-1100-12 loop-back cable to allow you to run diagnostics as described below. Install CAB-1100-12 between J4 and J5 on the CPX-1104 panel before running diagnostics. Figure 1-7 shows the location of J4 and J5 on the panel.

Overview of Testing

Like MDB's MV-DR11-W, the DQP-1120 is not compatible with Digital's MicroVAX diagnostic suite, MD. To develop and support custom products, Logical has created an interactive diagnostic operating environment, TREX, consisting of a set of services to control the execution of individual board level tests. Tests can be created to systematically probe and exercise a controller to determine its operational health. Tests can be logically grouped into a suite and executed via a script for hours or days to determine the reliability of a controller. Error reporting is flexible by allowing the test engineer programmer to determine the content and length of all error messages. Additional test execution controls provide for test looping, script looping, and elapse run time reporting.

TREX services and user diagnostics are written totally in the C programming language and on embedded CPU platforms does require an underlying operating system. Therefore TREX can be married very closely to the test platform hardware. The target hardware, called the Unit Under Test or UUT, is always directly mapped to a software array within TREX allowing all registers and memory elements to be directly accessed by C code. This not only eliminates need for any "device drivers" but allows diagnostics to manipulate the UUT hardware faster than in a normal operating environment.

When the target hardware is on a bus structure created by the "bus adapter" module resident on a platform primary bus, this down-stream bus area can also be described as an array and just requires simple procedures to access attached modules or memory.

Tests are normally written and grouped into two classes, preliminary testing and final testing. Preliminary tests are used to check individual controller base hardware components; CPU, memory, status LEDs, and a communications port and may require operator interaction and observation during testing. Final tests will check all the I/O ports using loop-back testing, where possible, and can be set to run repeatedly until stopped manually or by a detected error.

Running the Diagnostic

```
SETUP           Required Qbus addr: 760240 octal, Qbus vector: 300 octal, a loop-back cable.


                Test script option, -e stop on error, -v list current test, -l loop on script,
                -p print pass and time, or -a all options

                Note: Typing a Ctrl C stops a script at end of current test after pass count
                is satisfied

TESTING         sh -a loop[cr]        Trex full test for DQP-1120 or MV-DR11-W


Descriptions:   The basic format of a test command is: t test_name  pass_count  option_string

                Note: Option string characters are not position sensitive
                Tests accept a decimal pass count from 1 to 32000 and will run all passes
                before stopping


t reg 1         Test device regs using word pattern, CSR and ODR bytes for 1 pass.
t data 1 fd     Test input/output signals using a loop-back cable for 1 pass.
                f = function bits loop-back
                d = data reg loop-back in word and byte mode
t int 1         Test Attention interrupt for 1 pass.
t dma 1 16 0 rwi    Test 16 word DMA out/in using selected pattern for 1 pass.
                    DMA buffer starts at "em 0" addressed as 32-bit long words, em 100 = loc
                    256 (decimal)
                z = zero memory before DMA in (write)
                v = check input buffer (after write), expected value is last current content
                of ODR reg
                w = DMA write to memory, ODR via loop-back cable to memory buffer
                r = DMA read from memory, memory buffer to ODR reg
                i = incrementing pattern
                c = complementing pattern
                p = poll for done, else wait for interrupt and check vector value
                o = start on odd word address

    Display a block of registers
e  hex adr:dec_count    Display n Adapter regs from address
ec hex_adr:dec_count    Display n PCI config regs from address
el hex_adr:dec_count    Display n Local config regs from address
em hex_adr:dec_count    Display n DMA memory locs from address
es hex_adr:dec_count    Display n Sg maps from address
eq hex_adr:dec_count    Display n Qbus word regs from address
ez hex_adr:dec_count    Display n Qus byte regs from address

    Examine/Deposit  (A void deposit will cause no change)
e  hex_adr hex_deposit  Examine adapter reg and wait for change
ec hex_adr hex_deposit  Examine PCI config reg and wait for change
el hex_adr hex_deposit  Examine Local config reg and wait for change
em hex_adr hex_deposit  Examine DMA memory loc and wait for change
es hex_adr hex_deposit  Examine Sg map and wait for change
eq hex_adr hex_deposit  Examine Qbus word reg and wait for change
ez hex_adr hex_deposit  Examine Qbus byte reg and wait for change

    Addresses are 32-bit aligned, unless specified
  Dev reg address = 0 to 3c (16 regs)
  Cfg reg address = 0 to 3c (16 regs)
  Lcr reg address = 0 to 6c (28 regs)
  Mem loc address = 0 to ffffc 128kl at 0 and 128kl at 80000)
  Sg map loc address = 0 to fffc (16kl at 0)
  Qbus loc address = 0 to 3fffe (128kw) 16-bit aligned
  Qbus loc address = 0 to 3ffff (256kb) 8-bit aligned

Address modifiers for the Examine/Deposit address or value
    /  will move up 1 register
    \  will move down 1 register
    =  will redisplay the current register

c octal_address      Convert Octal address to Hexidecimal address
s hex_address        Compute scatter/gather index for memory addr
```

2 General Description

The DQP-1120 is a direct memory access (DMA) parallel input/output option module which allows real-time collection of parallel data at transfer rates exceeding 4 mbytes/sec of 16-bit words. The DQP-1120 provides access to interface signals on an external cable adapter panel which provides two ports for connection to external devices, an input port and an output port.

Interface Signals

This interface consists of two 40-pin connectors available on the cable adapter panel. Each connector has data signals, control signals, and general purpose signals that permit connecting to another compatible interface.

DRV11, DR11 J1

Signal Name	Signal Description
OUT00 H-OUT15 H	Sixteen data output signals. High true. These signals contain the data last written to the P1DREG register and are normally used as input data to the user equipment.
CYCRQ(A) H	CYCLE REQUEST (A) input signal. High true. A low to high transition initiates a DMA operation when READY is false (Low).
CYCRQB H	CYCLE REQUEST B input signal. This signal is OR'ed with CYCRQ(A) and therefore has an identical function. If this signal is not used, it should be grounded.
ENDCY H	END CYCLE output signal. High true. A 100 ns pulse that indicates the completion of a DR11-W data cycle.
READY H	READY output signal. High true. Set by a PCI Local Bus reset, an ATTN signal received from a user device, or a PCI Local Bus error signal received during a DMA operation. Cleared by writing a one to the GO bit in the Function Output Register (FUNCOREG). When READY is cleared (Low), DMA transfers may be initiated by the user device.

Signal Name	Signal Description
INIT H	INITIALIZE output signal. High true. Set when the PCI Local Bus reset signal is asserted or set by software control via the INIT OUT bit in the Function Output Register (FUNCOREG).
INITV2 H	INITIALIZE V2 output signal. High true. Set when the PCI reset is asserted or when software sets the FNCT2 bit in the Function Output Register (FUNCOREG) a 200ns pulse is generated.
WCINC H	Word Count Increment input signal. Incrementation is always enabled on the DQP-1120 and the state of this signal is ignored.
STATA H	STATUS A input signal. High true. The state of this signal can be read by software via Function Input Register (FUNCIREG) bit 5. When the DQP-1120 is connected to a user device, this signal is user defined. When the DQP-1120 is connected to another DRV11 or DR11 compatible controller, this bit reflects the state of the FNCT3 signal from the remote controller.
STATB H	STATUS B input signal. High true. The state of this signal can be read by software via Function Input Register (FUNCIREG) bit 4. When the DQP-1120 is connected to a user device, this signal is user defined. When the DQP-1120 is connected to another DRV11 or DR11 compatible controller, this bit reflects the state of the FNCT2 signal from the remote controller.
STATC H	STATUS C input signal. High true. The state of this signal can be read by software via Function Input Register (FUNCIREG) bit 3. When the DQP-1120 is connected to a user device, this signal is user defined. When the DQP-1120 is connected to another DRV11 or DR11 compatible controller, this bit reflects the state of the FNCT1 signal from the remote controller.

DRV11, DR11 J2

Signal Name	Signal Description
IN00 H-IN00 H	Sixteen data input signals. High true. These signals contain the data received from the user device when reading the P0DREG register.
ATTN H	ATTENTION input signal. High true. If this signal is driven high by the user device, any transfer between the DQP-1120 and the user device is terminated and the READY signal is asserted. When the DQP-1120 is connected to another DRV11 or DR11 compatible controller, this signal is controlled by the FNCT2 (INITV2) signal from the remote controller.
BUSY L	BUSY output signal. Low true. The DQP-1120 drives this signal low when internally retrieving data to present to the user device and the signal transitions to high when data is available for the user device; or the DQP-1120 drives this signal low when accepting data from the user device and the signal transitions to high when the user data has been accepted by the DQP-1120. When the DQP-1120 is connected to another DRV11 or DR11 compatible controller, this signal drives the CYCRQ (A) signal of the remote controller. The polarity of BUSY is controlled by software via the Configuration Register (CONFREG) and can be changed from the standard low true setting to a high true setting.
GO H	GO output signal. High true. When software sets Function Output Register (FUNCOREG) bit 4 to one, a 200ns pulse is generated on the GO output signal and the READY signal is unasserted (Low), allowing transfers to occur between the DQP-1120 and the user device.
C1 H	Control bit 1 input signal. High true. This signal is used to specify the direction that data will move between the DQP-1120 and the user device. When the bit is set high, data is transferred to the DQP-1120 from the user device. When the DQP-1120 is connected to another DRV11 or DR11 compatible controller, this bit is controlled by the FNCT1 signal from the local controller.
C0 H	Control bit 0 input signal. The DQP-1120 does not support byte DMA transfers, therefore the state of this signal is ignored. When the DQP-1120 is connected to another DRV11 or DR11 compatible controller, this bit reflects the state of the INIT signal from the remote controller. The state of the signal can be read by software via Function Input Register (FUNCIREG) bit 1.
A0 H	Address bit 0 input signal. The DQP-1120 does not support byte DMA transfers therefore the state of this signal is ignored. When the DQP-1120 is connected to another DRV11 or DR11 compatible controller, this bit reflects the state of the READY signal from the remote controller. The state of the signal can be read by software via Function Input Register (FUNCIREG) bit 0.
BAINC H	Bus Address Increment input signal. Incrementation is always enabled on the DQP-1120 and the state of this signal is ignored.

Signal Name	Signal Description
FNCT3 H	FUNCTION 3 output signal. High true. The state of this signal is controlled by software via Function Output Register (FUNCOREG) bit 2. When the DQP-1120 is connected to a user device, this signal is user defined. When the DQP-1120 is connected to another DRV11 or DR11 compatible device, this signal controls the state of STATA and SC in the remote controller and when the bit is set to one it specifies single cycle DMA cycles.
FNCT2 H	FUNCTION 2 output signal. High true. The state of this signal is controlled by software via Function Output Register (FUNCOREG) bit 1. When the DQP-1120 is connected to a user device, this signal is user defined. When the DQP-1120 is connected to another DRV11 or DR11 compatible device, this signal controls the state of STATB in the remote controller and when the bit is set to one an INITV2 signal is generated.
FNCT1 H	FUNCTION 1 output signal. High true. The state of this signal is controlled by software via Function Output Register (FUNCOREG) bit 0. When the DQP-1120 is connected to a user device, this signal is user defined. When the DQP-1120 is connected to another DRV11 or DR11 compatible device, this signal controls the state of STATC in the remote controller and the state of C1 in the local controller. When the bit is set to one, the local controller performs DMA write to memory cycles, and when set to zero the local controller performs DMA read from memory cycles.

Specifications

Physical

Controller	Standard short card measuring 6.875 inches by 4.2 inches (17.46 cm by 10.67 cm).

Interface

DQP-1120-A Controller	100-pin high density connector
Adapter Panel (CPX-1104)	Provides user connection to two 40-pin DRV11-WA and DR11-W style connectors
Adapter Cable (CAB-1104-8)	8-foot terminated with 100-pin connectors.

Electrical

Power Required:	
+5 volts DC	0.5 amps
+3.3 volts DC	0.4 amps

PCI Local Bus

Signaling	None

Environmental

Operating Conditions:

Temperature	5° to 50° C (41° to 122° F)
Relative Humidity	20% to 80% non-condensing

Storage Conditions:

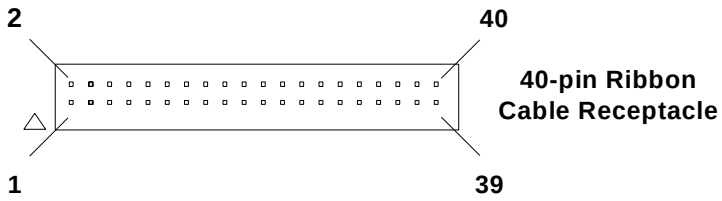
Temperature	-40° to 66° C (-40° to 150° F)
Relative Humidity	10% to 95% non-condensing

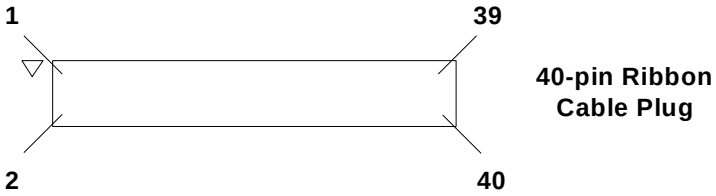
Appendix A - CPX-1104 Adapter Panel Connectors

This appendix lists the pin assignments for the CPX-1104 user connectors. The CPX-1104 contains two 40-pin connectors for DRV11-WA and DR11-W interface connection, and a 100-pin SCSI-style receptacle for connection to the DQP-1120 option module.

DRV11-WA and DR11-W Pin Assignments

The connector used for DRV11-WA and DR11-W interfaces is a 40-pin receptacle, 3M part number 2540-6002-UB. It and the mating cable connector are shown below.





Connector J4 (DR11 J1)

Signal	3M Pin	Berg Pin	Berg Pin	3M Pin	Signal
OUT15 H	1	VV	UU	2	OUT00 H
OUT14 H	3	TT	SS	4	OUT01 H
OUT13 H	5	RR	PP	6	OUT02 H
OUT12 H	7	NN	MM	8	OUT03 H
OUT11 H	9	LL	KK	10	OUT04 H
OUT10 H	11	JJ	HH	12	OUT05 H
OUT09 H	13	FF	EE	14	OUT06 H
OUT08 H	15	DD	CC	16	OUT07 H
GND	17	BB	AA	18	GND
CYCRQB H	19	Z	Y	20	GND
ENDCY H	21	X	W	22	GND
STATC H	23	V	U	24	GND
STATC H	25	T	S	26	GND
STATB H	27	R	P	28	GND
INIT H	29	N	M	30	GND
STATA H	31	L	K	32	SC H,BURST L
WCINC H	33	J	H	34	GND
READY H	35	F	E	36	GND
INITV2 H	37	D	C	38	GND
CYCRQA H	39	B	A	40	GND

Connector J5 (DR11 J2)

Signal	3M Pin	Berg Pin	Berg Pin	3M Pin	Signal
IN15 H	1	VV	UU	2	IN00 H
IN14 H	3	TT	SS	4	IN01 H
IN13 H	5	RR	PP	6	IN02 H
IN12 H	7	NN	MM	8	IN03 H
IN11 H	9	LL	KK	10	IN04 H
IN10 H	11	JJ	HH	12	IN05 H
IN09 H	13	FF	EE	14	IN06 H
IN08 H	15	DD	CC	16	IN07 H
GND	17	BB	AA	18	GND
GND	19	Z	Y	20	GND
GO H	21	X	W	22	GND
FNCT1 H	23	V	U	24	GND
C1 H	25	T	S	26	GND
FNCT2 H	27	R	P	28	GND
C0 H	29	N	M	30	GND
FNCT3 H	31	L	K	32	FNCT3 H
BAINC H	33	J	H	34	GND
A00 H	35	F	E	36	GND
ATTN H	37	D	C	38	GND
BUSY L,BUSY H	39	B	A	40	GND



75 Gateway Blvd.
Cottage Grove, Oregon 97424 USA
http://www.logical-co.com

The Logical Company

Telephone: +1 541-942-3610
Fax: +1 541-942-3640
E-mail: sales@logical-co.com

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