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THE MOVING PIXEL COMPANY
4905 SW Griffith Drive, Suite 106
Beaverton, Oregon 97005-8724
www.movingpixel.com

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PG3A

Digital Pattern Generator Module

Overview:

PG3A Digital Pattern Generator is a powerful, general purpose tool for both engineering and production. Typically it is used for peripheral/ASIC emulation and stimulation, setup/hold verification, production test, small-scale ATE, and general digital stimulus. When coupled with a Tek LA and/or a Tek 'scope, a complete test system is realized

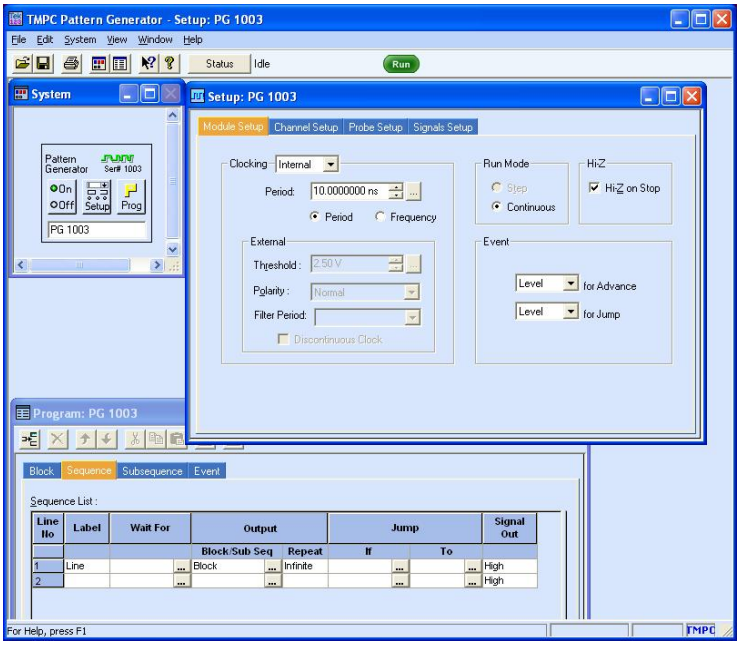
Primary Features:

- 64 channels (merge-able to 256 channels), 300 MHz all channels, 32 MVectors, +/- 200pS (typ) data skew
- Wide range, fine time delay adjustment for each 8 bit group
- Supports both flat and block-based data models (~4000 blocks)
- Probes have built-in LA feedback connection – simplifies connection to user system
- Interactive GUI-to-module interface via USB 2.0 for setup and firmware update
- Inputs probe for clock and events input – independent of output probes
- Small, quiet, cool, color-coded probes
- Firmware is user-updatable to support field feature and other upgrades
- External (user clock) supports gated clocks
- Inputs: 8 external events, 1 trigger, external 10 MHz reference, 8 byte lane inhibits.
- Additional outputs: 4 clocks and 4 configurable strobes (one each per output probe)
- All functions, all pins simultaneously (clocks, strobes, inhibits, data)

Part Numbers and Options:

PG3AMod	Pattern Generator module (for use in 7xx, 7xxx TLA)
PG3ACab	PG3A Module in an external cabinet (w/power supply)
-P3DDR	Option for DDR outputs (600 Mbps/ch/32ch)
-P3R3	Option for 3 year extended warranty on PG
P311	Analog out, 300 MHz dual 8-bit/single 14-bit DAC probe
P321	Low speed serial probe
P370	4.5V-5.5V, 16 channel probe, 150 MHz, square pins
P370LV	1.6V-3.6V, 16 channel probe, 200 MHz, square pins
P370LV2	1.0V-2.5V, 16 channel probe, 200 MHz, square pins
P373	LVDS, 16 channel, 300 MHz (mictor)
P375	Programmable Vol/Voh, bit-variable timing, 16 ch, 300 MHz
P390	Hydra Cable for merging modules (up to 256 bit width)





Contact:
Scott Silver
scott.silver@movingpixel.com
+1.503.626.9663 phone
+1.503.626.9653 fax

THE MOVING PIXEL COMPANY
4905 SW Griffith Drive, Suite 106
Beaverton, Oregon 97005-8724
www.movingpixel.com

PG3A Specifications

Tables 1 through 4 list the characteristics and specifications for the pattern generator.
Table 5 lists details about the shipping container.

All specifications are valid after the unit has been operating for 30 minutes in a temperature-stable environment.

Please note that any operation outside of any of these specifications could cause damage that might take many forms: immediate faulty operation, short-term mis-operation, out-of-spec operation, long-term mis-operation, extreme non-repairable damage, or hazard to the user. The fault may not be obvious after the damage occurs. Do not operate this equipment outside the specifications found below.

Table 1: PG module operational modes and limits

Characteristic	**Description**
Operational mode	
Normal	Pattern data output is synchronized by the internal/external clock input
Step	Pattern data output is synchronized by software command or PGApp directive
Output pattern	
Maximum Data Output Rate	300Mbits per second per channel
Maximum Clock Output Frequency	300 MHz
Maximum Operating Frequency	The maximum operating frequency of the module is a function of the output level, output pattern and the load condition, including the series termination resistor in the probe. Operating conditions exceeding this frequency may result in damage to the probe.
Pattern length	4 to 33554431 (32 MVectors)
Number of channels	64 channels
Sequences Maximum	3965
Number of blocks Maximum	3965
Repeat count	1 to 1048575 or infinite
PGApp software	Control software requirements and limits
Operating system	Microsoft Vista or XP

Table 2: PG Clocking and Reference Input/Output specifications

Characteristic	Description
Internal Clock	
Clock Period	10mS to 3.33nS
Clock Frequency	100 Hz to 300 MHz
Period resolution	
Frequency accuracy (internal timebase)	+/- 300ppm
External Clock Input	via Inputs Probe, both differential and single-ended, jumper-selectable on Inputs Probe
Clock Frequency	DC to 300 MHz
Threshold	-2.0V to +2.5V (single-ended input only) differential clock input is non-adjustable
Resolution	32 bits
Minimum pulse high, low	1.4 nS
Input Impedance	Jumper-selectable, on or off, resistor changeable by user, shipped as 100 ohm differential, 50 ohm single ended
Sensitivity	500mV p-p
Round-trip time, approximate	~80nS (30 MHz and greater), else ~120nS Clock at input probe to clock appearing at output probe output.
Clock delay adjustment range	
30 MHz and above clock	17.25 nS in 20pS steps[1]
Below 30 MHz	500 nS in 20pS steps
External Reference Input	via front panel
Frequency	10 MHz
Sensitivity	500mV, ac-coupled
Termination	50 ohm
Operating Limits	500mV to 5V peak-peak, R-D limiter internal to PG
External Reference Output	via front panel
Frequency	10 MHz
Amplitude (square wave)	
No load	3.3V p-p max, ground-referenced, DC coupled.
50 ohms	1.65Vp-pmax, ground-referenced, DC coupled
Outputs	
Inherent skew, any data output to any data output	+/- 150pS max includes probe cable, skew measured at probe input. Does not include probe skew, which is probe-type dependent.
Byte-skew adjustment range	
30 MHz and above clock	17.25 nS in 20pS steps[2]
Below 30 MHz	500 nS in 20pS steps

[1] An inversion control is also available that effectively doubles the range. This gives the user at least one clock cycle of delay adjustment at the lowest clock frequency.

[2] An inversion control is also available that effectively doubles the range. This gives the user at least one clock cycle of delay adjustment at the lowest clock frequency.

Table 3: PG Event Processing

Characteristic	**Description**
Event Action	Advance or Branch
Number of Event Inputs	9 External: 8 from Inputs Probe, 1 from front panel "Trig In"
Number of Event definitions	8: up to 512 event input patterns can be OR'd to define an event
Event Filtering	0 ns, 25 ns, or 50 ns
Event threshold	-5V to +5V
Sensitivity, minimum	500mV p-p
Signal amplitude, limits	-5VDC to +5VDC
Variable Event Setup Latency (FREQLAT) (used below in Waitfor/Branch setup calculation)	300 MHz = 2 user clocks 250 MHz = 6 user clocks 200 MHz = 8 user clocks 150 MHz = 12 user clocks 100 MHz = 14 user clocks 50 MHz = 18 user clocks <= 10 MHz = 22 user clocks
WaitFor Setup Time	130 ns + <filter dly> + 10 user clocks + FREQLAT
Branch Setup Time	130 ns + <filter dly> + 21 user clocks + FREQLAT
External Trigger Input	via front panel
Sensitivity, minimum	500mV
Threshold	AC-coupled, not adjustable
Termination	1.05 kOhm
Operational limits	500mV to 5V p-p
Risetime	No slower than 10V/uS
External Trigger Output	via front panel
No load	3.3V p-p typ, ground-referenced, DC coupled.
50 ohms	1.6V p-p typ, ground-referenced, DC coupled

Table 4: PG Electrical and Mechanical

Characteristic	Description
PG3AMod	module version of pattern generator
Slot Width	Requires two mainframe slots
Weight, approximate	2.5 kg
Overall dimensions, approximate	Depth: 375mm, Width 275mm, Height: 65mm
Power, maximum	80 watts, drawn from TLA mainframe
PG3ACab	cabinet (stand-alone) version of pattern generator
Weight, approximate	4kg
Overall Dimensions, approximate	Depth: 400mm, Width: 305mm, Height: 97mm
Power, maximum	100 watts
Voltage	100 – 240 VAC, 50-60 Hz
Power Factor Correction	Active, meets EN61000-3-2
Fuse	
110V nominal operation	1 amp fast blow, 3AG 250 V or equivalent, 1.25 inch x 0.25 inch
220V nominal operation	2 x 1 amp fast blow, 250V 5 mm x 20 mm

Table 5: PG Shipping Container Materials

Material	Amount
Cardboard (paper)	~1320 grams
Polyethylene (expanded foam)	~165 grams
Urethane foam pads	~115 grams
Shipping container dimensions	485mm x 420mm x 305mm

Abbreviated Probe Specifications

Please see the individual datasheet for more complete specifications

P370 Series TTL/CMOS Probes

The P370 probe features 16 low voltage data outputs running at up to 200 MHz. There are three different versions of this probe: P370, P370LV, and P370LV2. The differences are in the output drivers used for a given voltage range.

Probe	Range	Driver
P370	adjustable between 4.50 and 5.50 volts	74ACT16244DGG[3]
P370LV	adjustable between 1.65 and 3.60 volts	74AVC16244DGG[4]
P370LV2	adjustable between 0.80 and 2.50 volts	74AUC16244DGG[5]

The two inhibit inputs are CMOS levels with a 1.4 volt threshold regardless of what the driver output voltage is set to. There is an independent inhibit for each data byte. The probe data byte outputs are enabled when these are no-connect or pulled low. The probe does not drive the data byte outputs when the inhibit pin is driven high.

The voltage ranges given above are to keep the output drivers operating within specification. There is a limit in the hardware so that the maximum voltage cannot be exceeded. But the minimum voltage can be set outside the ranges described above. The PGApp software will allow a user to set the voltage lower than the minimum listed above but will issue a warning that operation is outside of the probe specification. **The *Moving Pixel* Company** (TMPC) does not specify operation outside the ranges listed above.

Electrical specification for the P370 probe:

Note: all voltages referenced to ground.

Description	P370	P370LV	P370LV2	Notes
Output voltage adjustment high, max	5.5 volts	3.6 volts	2.5 volts	
Output voltage adjustment high, min	4.5 volts	1.65 volts	0.8 volts	
Max Frequency	150 MHz	200 MHz	200 MHz	[6]
Enable time	18.8 nS max	12.0 nS max	10.4 nS max	[7] At max voltage
Disable time	19.8 nS max	12.0 nS max	10.5nS max	5 At max voltage
Rise/fall time, no load				Uncontrolled [8]
Skew between data outputs	uncontrolled[9]		1.5nS max	At max voltage
Output current, max				[10]

All the outputs of each probe run through a 100 ohm series termination before the output connector. This helps protect the probe from shorts, reflections, and other user-system connection issues.

The user can replace this termination (via desoldering) if there is a more suitable value for your system. If the user changes the resistor, the warranty on the output buffers is voided. The rest of the probe will still be covered under warranty.

The series resistor limits the output current. At any given output current, a new output voltage low and output voltage high can be computed. For example, if the no-load voltage is 3.3 volts and the output current load is 10 mA, the output high voltage at the output of the probe will be no greater than 2.3 volts; the output low voltage will be no less than 1.0 volts.

[3] Datasheet is available: http://www.ti.com/lit/gpn/sn74avc16244
[4] Datasheet is available: http://www.ti.com/lit/gpn/74act16244
[5] Datasheet is available: http://www.ti.com/lit/gpn/sn74auc16244
[6] Operation beyond this specification is possible with unspecified degradation of the output high and output low voltage levels
[7] typical is believed to be about 5 nS less, characterization data is tbd
[8] Characterization data tbd
[9] Characterization data tbd
[10] Series termination lowers output high voltage and raises output low voltage –see discussion above.

The Clock output and Strobe output have 1k ohm pulldown resistors to ground.
The Inhibit inputs have 10k ohm pulldown resistors to ground as well as a negative- voltage protect diode to ground (through a 100 ohm resistor). On the P370LV and P370LV2, there is an additional overvoltage protection diode (via 100 ohms) to 3.3 volts.

On the bottom of the unit, a square pin field is accessable that connect in parallel with the output connector. This enables the user to simultaneously connect the probe to the SUT and to a logic analyzer. The square pin field makes connection to a logic analyzer easy. This square pin field may also useful during pattern development by making a connection to a logic analyzer easier than using the leadset and connecting individual leads to the logic analyzer.

P373 LVDS Probe

The P373 probe features LVDS outputs running at up to 300 MHz. To preserve the signal integrity associated with the very fast edge rates (210pS) of the output drivers, we have chosen to make the connection from the probe to the user system via a AMP Mictor connector and a high-speed, multi-coax ribbon cable.

The two inhibit inputs are TTL levels. There is an independent inhibit for each data byte. The probe data byte outputs are enabled when these are no-connect or pulled low. The probe does not drive the data byte outputs when the inhibit pin is driven high.

The probe expects the user system to be differentially terminated in a purely resistive 100 ohms. All specifications assume this resistive termination.

Electrical specification for the P373 probe

Characteristic	**Specification**		**Notes**
Output Risetime	210pS, typ		
Output Enable time	300nS max		Yes, three hundred nS!
Output Disable time	12nS max		
Skew, nybble	+/- 65pS		4 consecutive bits starting with D0
Skew, worst case, probe-probe	+/- 550pS		Any bit in any probe to any other bit in any other probe
Clock before data	50ps – 400pS typical		Within one probe, all bits
Output Characteristic	**Min**	**Typ**	**Max**
Vod (differential voltage)	250mV	500mV	600mV
Vcm (common mode)	1.05 V	1.18 V	1.475 V

The probe also features a Tektronix P6980 connection from the backside to facilitate connection to a logic analyzer during pattern debug (and perhaps even during system test).

If a user system does not need to run at the highest speeds the probe supports and does not want to connect to the user system via a Mictor, there are adapters available for Mictor to square pins like the Nexus Technology Nex-HD20 (http://www.nexustechnology.com/products/laAccessories/hd20/). Signal integrity will suffer as the risetime on the output of the probe is typically 210 pS. Uncontrolled impedances of longer than 5mm will be noticed in the waveform. Uncontrolled impedances of longer than 3 cm may make the signal unusable, especially the clock signal.

P375 Universal Variable Probe

This probe is called “Universal” because its output high-level (“1”) can be adjusted to any voltage between –2.00Vdc and +6.5Vdc. Similarly the output low-level (“0”) can be adjusted to any voltage between –2.00Vdc and +6.5Vdc, allowing it to address all modern I/O levels. Further, channels can be paired to form differential channels, again, at any voltage setting. Each output is series terminated in 50 ohms.

This probe is called “Variable” in that any channel can be skewed in time from any other channel in 20pS steps across a range of 2.4nS. This is independent of any delay settings the PG offers.

Electrical specification for the P375 probe

All specifications assume no output load unless otherwise noted.
All specifications are at 25 degrees Celsius ambient temperature, 30 minutes for stabilization of both the PG and the probe.
The user can adjust the time skews shown down to zero +/- 20pS.

Characteristic	**Specification**		**Notes**
Output Risetime Selections			
unloaded	~1V/nS, ~2V/nS		
50 ohm load	~0.5V/nS, ~1V/nS		
Output Enable time	5 nS		typ
Output Disable time	5 nS		typ to +/- 10 uA
Skew, nybble	+/- 300pS		Uncalibrated, 4 consecutive bits starting with D0. Can be user-calibrated to +/- 20pS
Skew, worst case, probe-probe	+/- 600pS		Uncalibrated, Any bit in any probe to any other bit in any other probe. Can be user-calibrated to +/- 20pS
Clock before data	50ps – 400pS typical		Within one probe, all bits
Output impedance	50 ohms +/- 10%		Early units were 48.5 ohm
Output Characteristic	**Min**	**Max**	
Output voltage high	-2.000 V	+6.500 V	+/- 25mV of set point
Output voltage low	-2.000 V	+6.500 V	+/- 25 mv of set point
Noise		10mVp-p	Output voltage –1.8 - +6.5V
		40mVp-p	Output voltage –2.0 - -1.8V
Weight	710 grams		Approximate, without external power supply
Overall Dimensions	Length: 145mm, Width 125mm, Height: 75mm		approximate
External power supply	24 volts, 2 Amps, typical		provided

Special Purpose Probes

Please see the datasheet for details

P311 – Dual 8-bit DAC, Single 14-bit DAC
P321 – Low-speed serial probe for I2C, SPI, RS232, RS422
P331 – MIPI DPhy 1Gb probe (see MIPI web page for specs)

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