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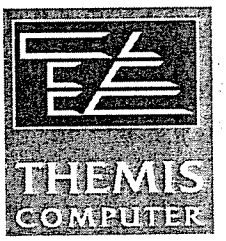
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SPARC 20MP User Manual

Version 2.0 (Rev B) — November 1996



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Changes:	Pg 3-16	Clarify Flash#0 Write Enable Switch descriptions.
	Pg 3-41	Correct typographical error.
	Pg 4-8	Clarify Switch Status Register Bit 0 descriptions.
	Pg 4-12	Add word "DVMA" to paragraph title.

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1

Getting Started

1.1 Introduction

Thank you for purchasing the Themis SPARC 20MP single board computer with VMEbus interface. Themis Computer is a leading manufacturer of SPARC based processor boards for the VMEbus market. We value our customers comments and concerns. Our Marketing department is eager to know what you think of our products. A "Reader Comment Card" is located at the end of this manual for your use.



Caution — Before you begin, carefully read each of the procedures in this manual. Improper handling of the equipment can cause serious damage to the equipment.

1.2 How to Start Quickly

This document presents the Theory of Operation of the Themis SPARC 20MP. It is intended to be a general purpose guide to the SPARC 20MP for system architects, programmers, technicians, and other users. Technical discussions begin from an architectural perspective of a given topic and then proceed to those aspects of a general Sun architecture as it is implemented in the SPARC 20MP board from a programmer's view. The information presented here is also written for the technician so that, in most cases, all that will be needed in the laboratory is this document and the appropriate toolkit. Finally the discussion retains a global, yet general view that is useful to a less technical user.

1.2.1 Product Warranty and Registration

Please review the Themis Computer warranty information packaged with your SPARC 20MP processor board. Your SPARC 20MP single board computer is automatically registered when it leaves the factory based on the information provided in the sales order. All Themis Computer single board computers are tracked via the serial number and any warranty service period is based on the original shipment date from the factory.

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1.2.2 Intended Audience

This manual is written for end-users, integrators and programmers. It contains all the necessary information to install and configure the SPARC 20MP processor board. It is assumed that the Sun Open Boot PROM (OBP) is installed. If you intend to use another operating system or a real-time kernel such as VxWorks, please consult the appropriate documentation accompanying your OS or kernel software.

The reader is assumed to be familiar with and have a working knowledge of the SPARC processor architecture, SPARCclassic chip-set, and current VMEbus, SBus, Ethernet, and SCSI specifications. Although all SPARC 20MP specific hardware and software features are described in detail in this manual, programmers wishing to code the SPARC 20MP without the benefit of an operating system or real-time kernel will require additional data sheets and documentation for the SPARCclassic chip-set, the hyperSPARC or SuperSPARC processors and other system components comprising the SPARCstation™20 design.

1.2.3 Unpacking the SPARC 20MP



Caution — The SPARC 20MP contains statically sensitive components. Industry standard measures (use of a grounded wrist strap) must be observed when removing the SPARC 20MP from its shipping container and during any subsequent handling.

Remove the SPARC 20MP and accessories from its shipping container and check the contents against the packing list. The package should include:

- SPARC 20MP
- SPARC 20MP Warranty information
- Integration Kit (if ordered separately)
  - Paddleboard
  - A/B Serial Cable
  - Front Panel SCSI Cable
  - Flat Ribbon SCSI Cable
  - AUI Ethernet Cable
- SPARC 20MP User Manual (if ordered separately)

Please report any discrepancies to the Themis Computer Customer Support department immediately.

1.2.4 In Case of Difficulties

Our Customer Support department is committed to providing the best product support in the industry. Customer support is available 8am - 5pm (PST), Monday through Friday via telephone, fax, e-mail or our World Wide Web site.

Themis Customer Support

Telephone: 510-252-0870
Fax: 510-490-5529
E-mail: support@themis.com
Web Site: http://www.themis.com

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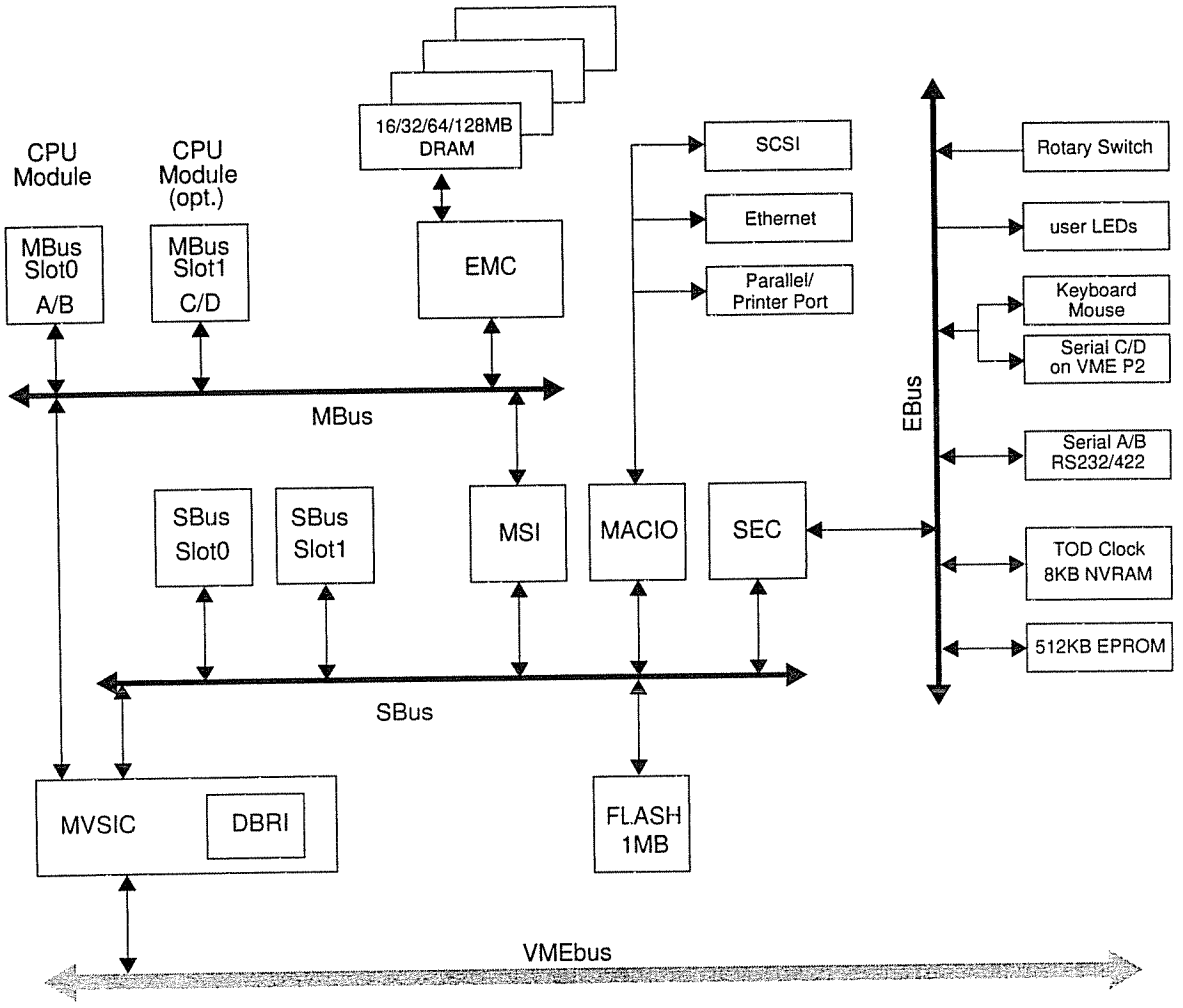


Figure 2-1. SPARC 20MP System Bus Topology

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2

SPARC 20MP Architecture

2.1 Introduction

The SPARC 20MP is a multi-processing single board computer. The SPARC 20MP has two MBus slots that are MBus Level 2 compliant, which can accept any processor that implements the SPARC processor architecture. MBus processor modules can contain the CPU, FPU, Cache, and MMU.

The SPARC 20MP has additional features in comparison to the SPARCstation™20 design which include a VMEbus interface, sockets for up to four memory mezzanine board modules with a 128-bit data path and up to 128MB per memory module, and both Twisted-Pair (10Base-T) and thickwire (AUI) Ethernet.

The SPARC processor architecture is implemented via MBus modules. The MBus is a 64-bit multiplexed address/data bus that supports single (Level 1) and multiple (Level 2) processors. The SPARC 20MP can support up to four processors, two per MBus slot, using MBus module IDs 8 and 9 in slot0 and MBus module IDs A and B in slot1.

The SPARC 20MP implements the SPARC processor architecture, the SPARC Reference MMU, the Sun4M system architecture for MBus-based SPARC processors, as well as the SBus system bus architecture. The SPARC reference MMU is implemented on the MBus modules. The SRMMU is a standard MMU which translates virtual addresses to physical addresses that can be used by all SPARC processors.

2.2 Major ASICs

2.2.1 EMC

The Memory Controller (EMC) ASIC implements the Fault Status, the Address Register, the ECC Memory Enable, and the Fault Status Register of the Sun4M architecture.

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2.2.2 MSI

The MBus to SBus Interface (MSI) ASIC implements the IOMMU including the TLB, the Base Address Register, the IOMMU Control Register, the Arbiter Enable Register, the MBus to SBus Asynchronous Fault Address Register, and the MBus to SBus Asynchronous Error Register of the Sun4M architecture.

2.2.3 SEC

The SBus to EBus Controller (SEC) ASIC implements the Counter/Timers as well as the System Interrupt Registers of the Sun4M architecture. The SPARC 20MP includes a Sun4M architecture SPARC IOMMU (a MMU for I/O devices) in the SEC ASIC as part of the cache controller.

2.2.4 MACIO

The MACIO (NCR89C100 Master I/O Controller) ASIC implements the SBus interface to three master I/O devices: Ethernet, SCSI and parallel port. It contains three DMA channels implemented in its DMA2 block, one for each device supported.

2.2.5 DBRI

The DBRI (AT&T T7259) ASIC has been implemented to offer optional 16-bit audio capability on the MVSIC (**M**Bus - **V**MEbus - **S**Bus **I**nterface **C**ontrol) daughterboard.

2.3 Connectors

2.3.1 MBus Connectors

The SPARC 20MP processor modules are installed in MBus slot0 and possibly also MBus slot1, depending upon your specific processor configuration. The two MBus slots are designed to accept any Level 2 compatible MBus module. MBus slot0 is located on the solder side and MBus slot1 is located on the component side.



Warning — MBus slot1 and SBus slot0 occupy the same physical space, so they can not be used at the same time. If MBus slot1 is used, only SBus slot1 is available. If both SBus slots are used, only MBus slot0 is available for use.

2.3.2 SBus Connectors

The two SBus slots are designed to accept any SBus compatible module. SBus slot0 is located near the VME P2 connector while SBus slot1 is located near the center of the board.

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Note — SBus modules require additional software. Please check the SBus module documentation for information specific to the SBus module.

2.3.3 Memory Connectors

There are four high-density SMT connectors used to connect the SPARC 20MP baseboard to up to four mezzanine memory modules. Each mezzanine memory module can provide up to 128MB of memory.

Note — Memory configurations utilizing more than two mezzanine memory modules extend beyond the SPARC 20MP front panel and require an additional VMEbus slot.

2.3.4 MVSIC Connectors

There are seven high-density SMT connectors to connect the SPARC 20MP baseboard to the MVSIC (**M**Bus - **V**MEbus - **S**Bus **I**nterface **C**ontrol) daughterboard which implements the VMEbus interface control logic and the Audio Controller.

2.4 System Buses

The six main system buses on the SPARC 20MP are as follows:

- MBus
- Memory Bus
- SCSI Bus
- SBus
- VMEbus
- EBus

2.4.1 MBus

The MBus is the processor-to-memory controller interface bus. The MBus consists of 64 multiplexed address and data lines, with additional signals to handle master and slave transactions and multiprocessor cache coherency operations. There are also signals that signify the transactions. The size of the transfer, from byte transfers up to 128 byte burst transfers, is encoded into the MAD-bits MAD[42:40], the Transaction Type MAD[39:36], Cachability MAD[43], Supervisor Mode MAD[59], and the Module Identifier Code MAD[63:60].

In the SPARC 20MP MBus implementation, operating at 50MHz, there are two ASICs, two MBus slots, and the MBus to VMEbus implemented on the MVSIC daughterboard. The two ASICs are the EMC (Memory Controller) and the MSI (MBus to SBus Interface). The MBus has a main arbiter which is inside the MSI chip in the SPARC 20MP implementation.

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2.4.2 Memory Bus

The Memory Bus is the interface between the memory controller and the memory modules. The Memory Bus consists of 128 data lines, 16 ECC Check-bit lines, and the signals needed to conduct DRAM memory accesses. These signals consist of one RAS* per module, 2 CAS* total, 1 WE* total, 1 reset line, one IOSEL line, 4 JTAG interface lines, and 12 address-bit lines. The Memory Bus can access data in 100 ns from RAS assertion.

2.4.3 SCSI Bus

The SCSI Bus is the interface between the system and internal/external data storage devices such as disk drives, tape drives, or CD-ROM drives. The SCSI Bus is the standard single ended 8-bit SCSI Bus interfacing the MACIO to disk drives, tape drives and CD-ROM drives. In the SPARC 20MP implementation the MACIO can transfer data on the SCSI Bus at 10MB per second.

2.4.4 SBus

The SBus is the system bus used to interface the system to the SCSI Bus, Ethernet and the EBus. The SBus consists of 32 data lines and 28 address lines. There are point-to-point Bus Request and Bus Grant signals for Master transfers, as well as signals to signify the transaction size from 1 byte to 64 bytes. In the SPARC 20MP implementation using MSI, only transfers up to 32 bytes are supported. There are also Acknowledge signals to acknowledge the state of a transaction.

In the 20MP implementation, operating at 25MHz, there are three ASICs and two SBus slots on the SBus. The ASICs are the MSI (MBus to SBus Interface), the SEC (SBus to EBus Controller), and the MACIO (SBus to Ethernet/SCSI/Parallel Port). The SBus has a main arbiter/controller which is inside the MSI chip in the SPARC 20MP implementation.

2.4.5 EBus

The EBus in the SPARC 20MP implementation is 8-bits of data and 16-bits of address. The SEC is the arbiter/controller for the EBus and interfaces the EBus to the SBus. The SEC along with the TOD (Time of Day NVRAM) chip, the 27C040 (or 29F040) EEPROM, and the two 85C30 chips (Serial Ports A/B and Keyboard/Mouse) reside on the EBus. The EBus permits access speeds of 5MHz or less.

2.4.6 VMEbus

The VMEbus is the system bus used to interface the SPARC 20MP to VMEbus devices (i.e. general purpose processors, I/O cards, memory cards, etc). The VMEbus consists of 32 data lines and 32 address lines. There are four bus request levels, and seven interrupt request levels. In the SPARC 20MP implementation the MVSIC is used to interface the VMEbus to the MBus.

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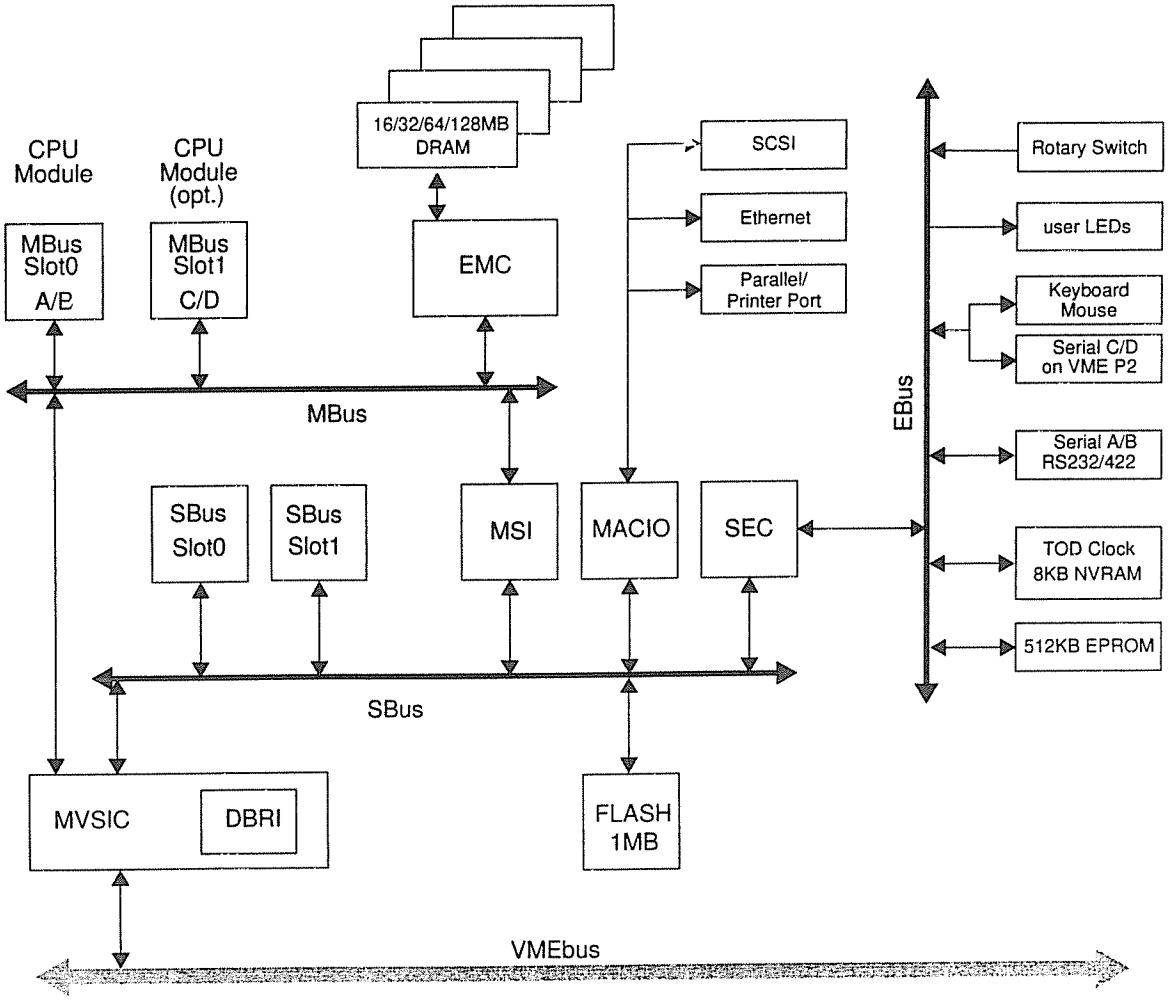


Figure 2-1. **SPARC 20MP System Bus Topology**

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3

SPARC 20MP Hardware

3.1 Introduction

Themis Computer's SPARC 20MP is the highest level of SPARC multiprocessing technology available on the VMEbus. The SPARC 20MP combines the highest performance hyperSPARC, SuperSPARC or SuperSPARC II processors with multiple SBus interface options. The SPARC 20MP implements innovative multiprocessor technology with memory expansion from 16 to 512Mbytes, Ethernet, SCSI 2-FAST, two serial ports, a keyboard/mouse port, an optional audio port, and a high performance VME64 interface. Designed with demanding telecom and embedded application environments in mind.

This chapter provides illustrations of the SPARC 20MP hardware and user configurable devices. These illustrations are listed below:

- Front Panel
- SPARC 20MP Baseboard
- MVSIC Daughterboard
- Mezzanine Memory Module
- Paddleboard
- Positive Temperature Coefficient Device Locations
- SPARC 20MP Baseboard Switch Locations
- MVSIC Daughterboard Switch Location
- SPARC 20MP Baseboard Solder Bead Locations
- SPARC 20MP Baseboard Jumper Location

Also included in this chapter are various tables detailing:

- Power Requirements
- Environmental Requirements
- Switches, Solder Beads, and Jumper Settings
- Connector Pinouts

The chapter concludes with a brief discussion of the diagnostic tools that are available for the SPARC 20MP.

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3.2 Front Panel

The Front Panel, shown in *Figure 3-1*, provides access to the following features:

- CPU Status LEDs
- User Status LEDs
- System Status LEDs
- Reset / Abort Switch
- Rotary Switch
- Serial Ports A/B
- Keyboard / Mouse
- 10Base-T Ethernet
- AUI Ethernet
- Audio
- SCSI
- SBus Slots

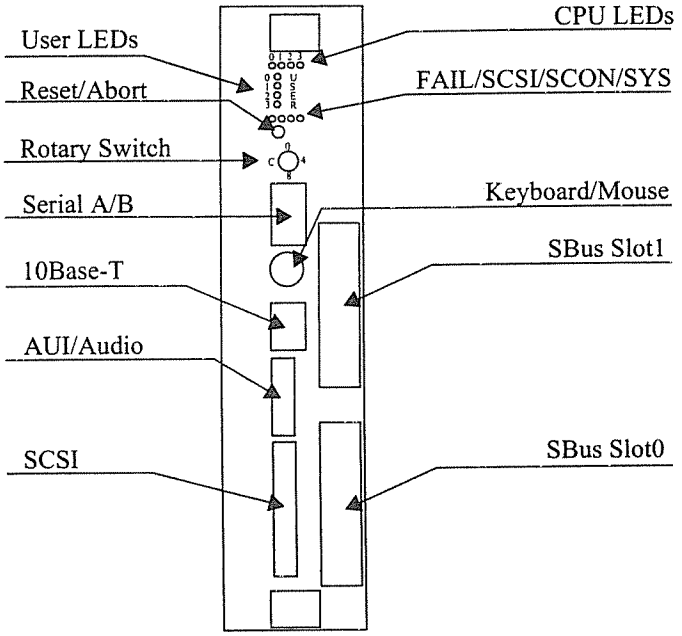


Figure 3-1. **SPARC 20MP Front Panel LEDs, Switches and Connectors**

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3

SPARC 20MP Hardware

3.1 Introduction

Themis Computer's SPARC 20MP is the highest level of SPARC multiprocessing technology available on the VMEbus. The SPARC 20MP combines the highest performance hyperSPARC, SuperSPARC or SuperSPARC II processors with multiple SBus interface options. The SPARC 20MP implements innovative multiprocessor technology with memory expansion from 16 to 512Mbytes, Ethernet, SCSI 2-FAST, two serial ports, a keyboard/mouse port, an optional audio port, and a high performance VME64 interface. Designed with demanding telecom and embedded application environments in mind.

This chapter provides illustrations of the SPARC 20MP hardware and user configurable devices. These illustrations are listed below:

- Front Panel
- SPARC 20MP Baseboard
- MVSIC Daughterboard
- Mezzanine Memory Module
- Paddleboard
- Positive Temperature Coefficient Device Locations
- SPARC 20MP Baseboard Switch Locations
- MVSIC Daughterboard Switch Location
- SPARC 20MP Baseboard Solder Bead Locations
- SPARC 20MP Baseboard Jumper Location

Also included in this chapter are various tables detailing:

- Power Requirements
- Environmental Requirements
- Switches, Solder Beads, and Jumper Settings
- Connector Pinouts

The chapter concludes with a brief discussion of the diagnostic tools that are available for the SPARC 20MP.

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3.2 Front Panel

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- System Status LEDs
- Reset / Abort Switch
- Rotary Switch
- Serial Ports A/B
- Keyboard / Mouse
- 10Base-T Ethernet
- AUI Ethernet
- Audio
- SCSI
- SBus Slots

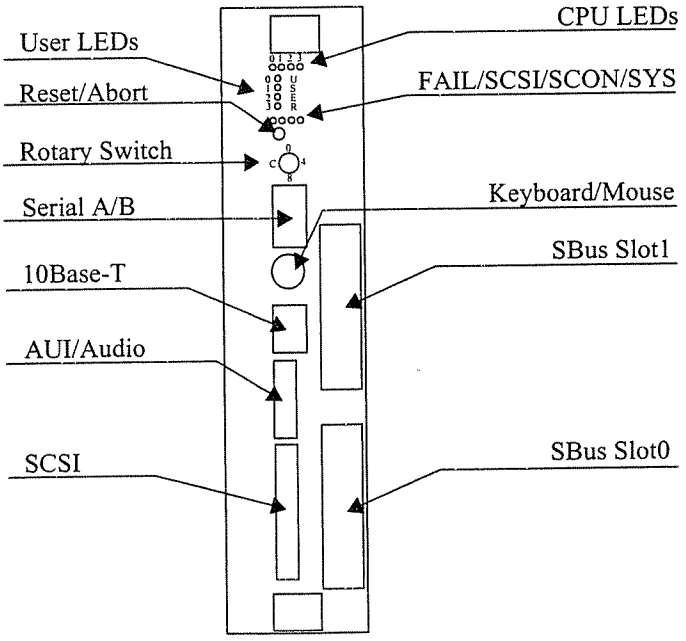


Figure 3-1. **SPARC 20MP Front Panel LEDs, Switches and Connectors**

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3.3 Baseboard

Located on the SPARC 20MP Baseboard, shown in *Figure 3-2*, are major components with the following functions:

- EMC, MSI, SEC, and MACIO ASICs
- MBus Slots
- SBus Slots
- Flash#0 Write Enable Switch (see *Figure 3-9*)
- Serial Ports and SCSI Termination Switch (see *Figure 3-9*)
- VMEbus Reset and NVRAM Write Protect Switch (see *Figure 3-9*)
- 11 Factory Configurable Solder Beads (see *Figure 3-11* and *Figure 3-12*)
- MBus Slot1 Jumper (see *Figure 3-13*)

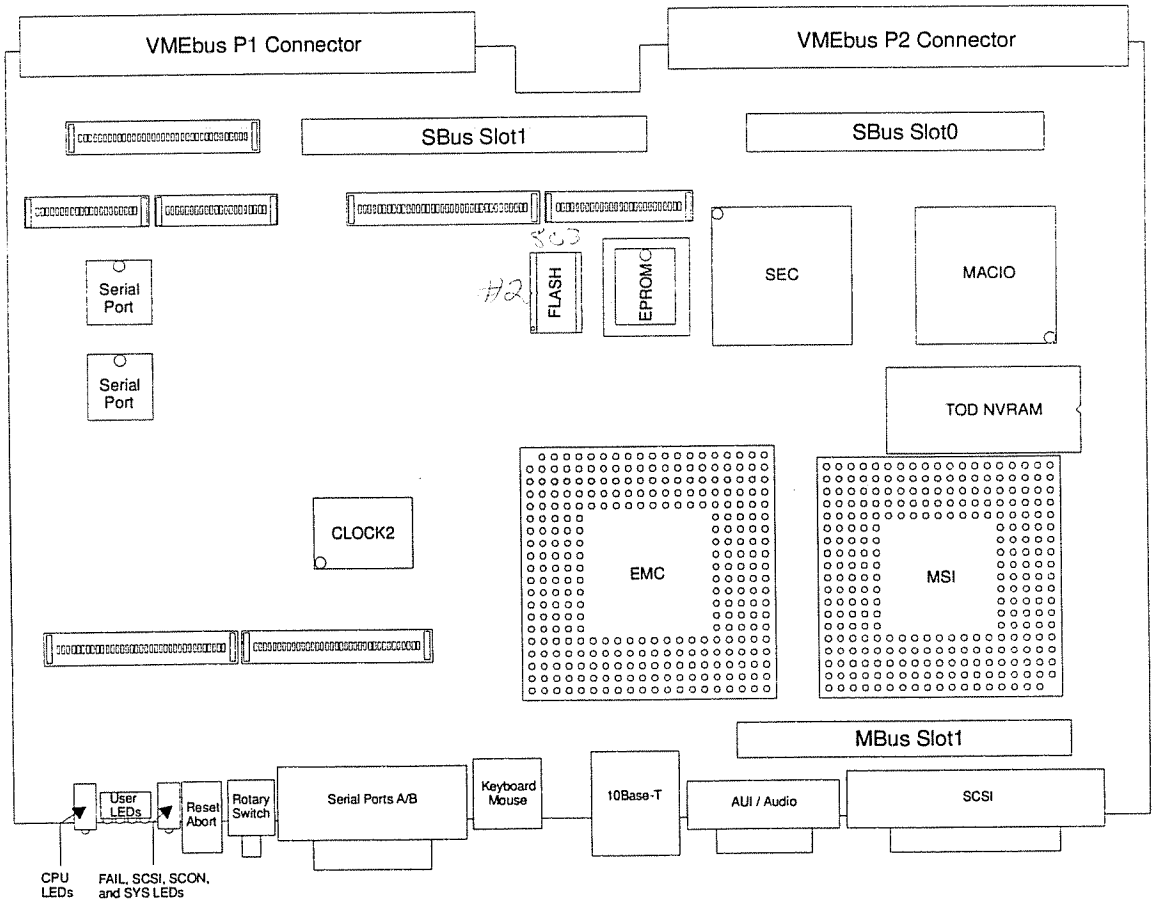


Figure 3-2. **SPARC 20MP Baseboard with Major Component Locations (Component Side)**

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3.4 MVSIC Daughterboard

The MVSIC daughterboard, shown in *Figure 3-3* and *Figure 3-4*, provides the interface between the MBus, VMEbus, and SBus. *Table 3-1* and *Table 3-2* list the various functions of the chipsets located on the MVSIC daughterboard.

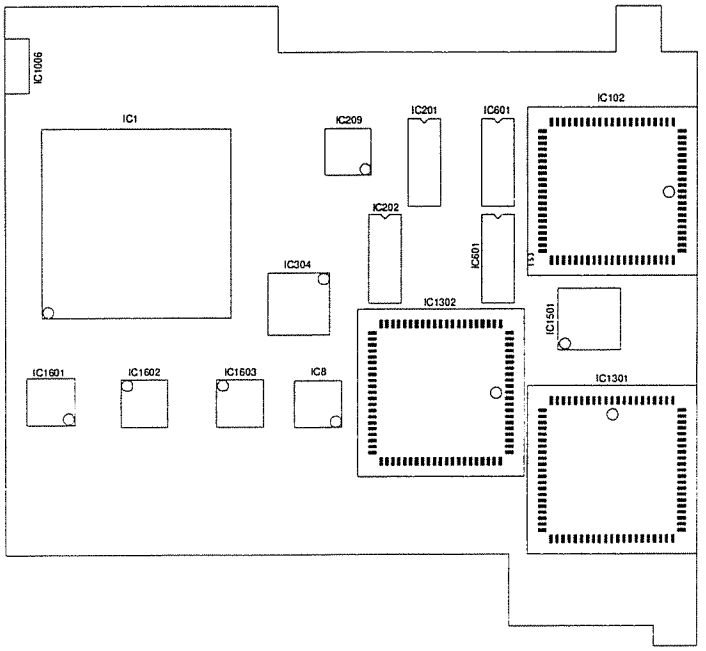


Figure 3-3. **MVSIC Daughterboard with Major Component Locations (Component Side)**

Table 3-1. **MVSIC Daughterboard Chipset Descriptions (Component Side)**

Reference Designator				Description
IC1				SCV64 VMEbus Interface
IC8	IC1601	IC1602	IC1603	VMEbus Requester and DTB
IC102				SBus Decoding and Interrupts
IC201	IC202	IC209		KBus to SBus FIFO
IC601	IC602			SBus to KBus FIFO (DMA)
IC1006				32 MHz Clock
IC1301	IC1302			DMA and Slave Control Logic
IC1501				VMEbus Interface Registers

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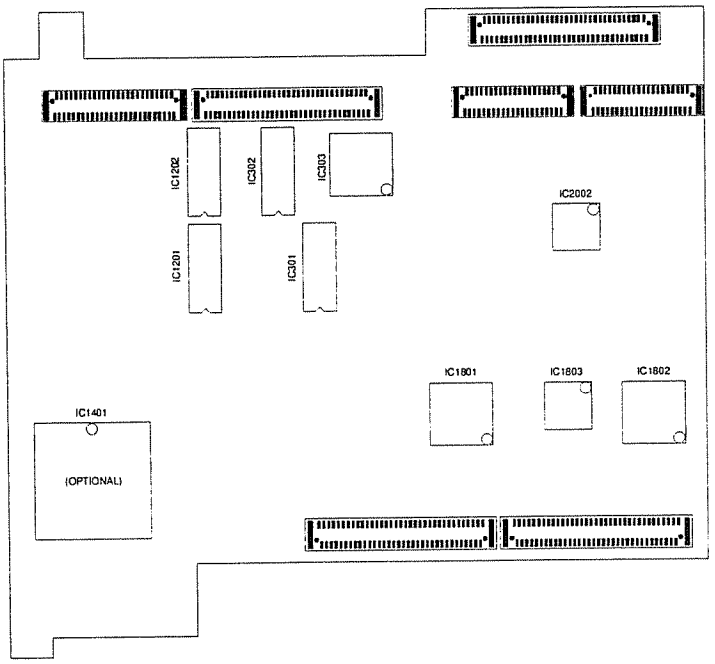


Figure 3-4. **MVSIC Daughterboard with Major Component Locations (Solder Side)**

Table 3-2. **MVSIC Daughterboard Chipset Descriptions (Solder Side)**

Reference Designator				Description
IC301	IC302	IC303	**IC304***	VMEbus to SBus FIFO
IC1201	IC1202			SBus to VMEbus FIFO (Slave)
IC1401				Audio Interface
IC1801	IC1802	IC1803		MBus / VMEbus Data Buffers
IC2002				VMEbus Address Decoding
*** This component is located on the "Component Side"**				

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3.5 Memory Module

The Mezzanine Memory Module provides the SPARC 20MP system memory. The Mezzanine Memory Module is available in four different configurations (16MB, 32MB, 64MB, and 128MB). The SPARC 20MP can accommodate up to four Mezzanine Memory Modules for a total of up to 512MB of system memory.

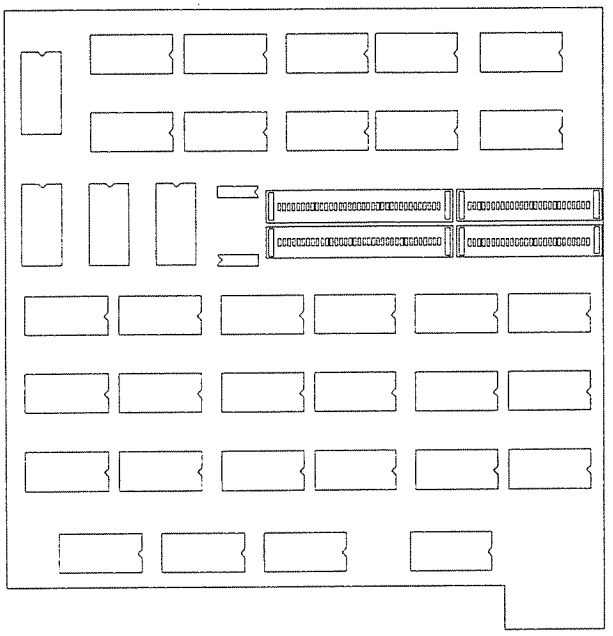


Figure 3-5. **SPARC 20MP 128MB Mezzanine Memory Module**

Note — Memory configurations utilizing more than two mezzanine memory modules extend beyond the SPARC 20MP front panel and require an additional VMEbus slot.

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3.6 Paddleboard

The SPARC 20MP Paddleboard is an optional component and must be purchased separately or as part of the SPARC 20MP integration kit (see *§ 1.2.3 Unpacking the SPARC 20MP* on page 1-2). The SPARC 20MP Paddleboard utilizes additional VCC and GND pins from the adjacent VMEbus P2 connectors on each side to increase the number of VCC and GND pins typically available in a standard VMEbus slot.

The Paddleboard, shown in *Figure 3-6*, provides access to the following additional features:

- SCSI 2-FAST
- Serial Ports C/D
- Parallel Printer Port
- AUI Ethernet

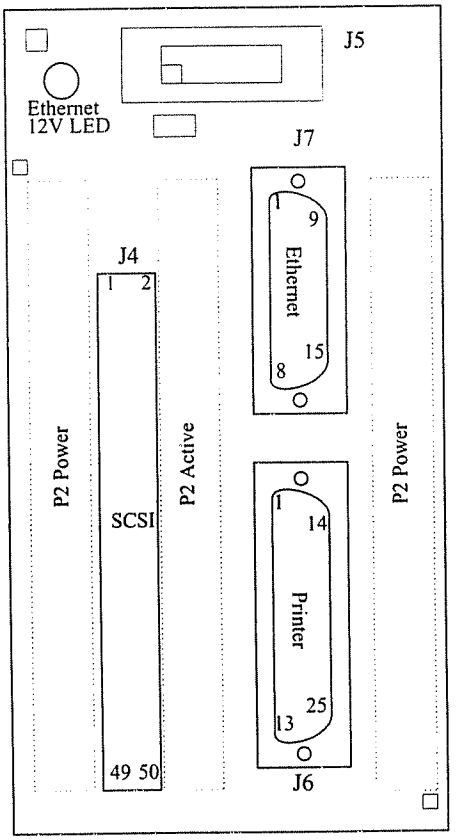


Figure 3-6. **SPARC 20MP Paddleboard**

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3.7 Electrical Requirements

The SPARC 20MP typical power requirements are indicated below and apply to a basic VMEbus chassis with no additional boards:

Table 3-3. **Power Supply Requirements**

Output	Current	Regulation	Noise and Ripple
+5V	24A	+3% / - 3%	50 mV p-p
+12V	3.5., 5A peak	+10% / -7%	100 mV p-p
12V	0.1A	+10% / -10%	120 mV p-p

The AC outlet for the display monitor should be rated at 5A (80 A inrush). The AC outlet must have a world-wide AC input range of 87.5 to 264 VAC and from 47 to 63 Hz. It should have a high conversion efficiency of >75% with a high power density of 3.7 W/in**2. It should provide for fan speed control based on ambient air temperature.

3.8 Power Requirements

The following typical measured power requirements are for various configurations of the SPARC 20MP. These measurements are peak power consumption with the MVSIC daughterboard installed on the SPARC 20MP baseboard.

Table 3-4. **Power Requirements**

MBus Slot0	MBus Slot1	Voltage	Memory (Mbyte)	Amp (A)
90 MHz Hyper		5.0	64	7.4
90 MHz Hyper	90 MHz Hyper	5.0	64	11.40
90 MHz Dual Hyper		5.0	64	11.45
90 MHz Dual Hyper	90 MHz Hyper	5.0	64	14.15
90 MHz Dual Hyper	90 MHz Dual Hyper	5.0	64	17.15
75 MHz Super		5.0	64	8.8
75 MHz Super	75MHz Super	5.0	64	11.8
125 MHz Dual Hyper		5.0	64	13
125 MHz Dual Hyper	125MHz Dual Hyper	5.0	64	20

Memory Module Power Consumption: 200 mA for 64 MByte (Using 16 Mbit DRAM)

Listed below in are the peak worst case current/power requirements of the devices in the SPARC 20MP power supply implementation. The SPARC 20MP power supply should supply 140 W of average power, and 166W, peak. Since all devices won't be at their peak power demands at the same time, the average power should be used for estimating the power budget.

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WEIGHT 2 LBS 3.2 OZ WITH 2HE MODULE

Table 3-5. **Components Peak Power Requirements**

Component	+5V	+12V	-12V
SuperSPARC w/E	5.0A	0.0A	0.0A
SuperSPARC 2	5.0A	0.0A	0.0A
Motherboard	2.0A	0.01A	0.01A
SBus Slot 1	2.0A	0.03A	0.03A
SBus Slot 2	2.0A	0.03A	0.03A
Memory Modules	2.0A	0.0A	0.0A
Ethernet XCVR	0.0A	0.4A	0.0A
KB/Mouse	0.1A	0.0A	0.0A
Fans	0.0A	0.5A	0.0A
Total Current	18.1A	0.97A	0.07A
Total Power	90.5W	11.64W	0.84W

3.9 Environmental Requirements

The table below lists the environmental requirements for the operating and non-operating environments.

Table 3-6. **Environmental Requirements**

	Requirement
Operating Environment	
Temperature	0 - 50 ° C
Humidity	5 - 95% relative humidity
Altitude	70.1 kpa (3 km or 9,843 ft equivalent)
Air Flow (Cooling)	300 lfm airflow at 50°C
Non-Operating Environment	
Temperature	-40 - 75 ° C
Humidity	95% relative humidity
Altitude	19.3 kpa (12 km or 38,370 ft equivalent)

Note — Any and all functional or reliability predictions for the SPARC 20MP when used outside the ranges listed in the above table are the sole responsibility of the hardware integrator's company, and should be so indicated in all related product documentation.

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3.10 Front Panel LEDs

The SPARC 20MP has three sets of LEDs: CPU Status LEDs, User Status LEDs, and System Status LEDs as shown in *Figure 3-1* on page 3-2.

3.10.1 CPU Status LEDs

There are four green CPU Status LEDs on the SPARC 20MP Front Panel. These LEDs light to indicate the number of processors that are installed and will flicker to indicate CPU activity.

3.10.2 User Status LEDs

There are four red User Status LEDs provided on the SPARC 20MP. These LEDs are intended to be visual indicators for users to implement as needed. Please refer to *§ Table 4-11. LED Control Register Read Access* on page 4-7 and *§ Table 4-12. LED Control Register Write Access* on page 4-7 for detail on programming the User Status LEDs.

3.10.3 System Status LEDs

There are four System Status LEDs Provided on the SPARC 20MP. The System Status LEDs are FAIL (red), SCSI (orange), SCON (yellow), and SYS (green). These LEDs indicate the following:

- **FAIL** - This LED (red) lights during Power On Self Tests (POST). At the end of successful POST testing the FAIL LED will not be lighted. This LED also lights to indicate a VMEbus SYSFAIL.

- **SCSI** - This LED (orange) lights to indicate that SCSI termination is enabled on the SPARC 20MP via the Serial Ports and SCSI Termination Switch (SW703). See *§ 3.12.1.2 Serial Ports and SCSI Termination Switch* on page 3-16 for more information.

- **SCON** - This LED (yellow) lights to indicate that the SPARC 20MP is set to System Controller via the System Controller and VMEbus Reset Receive Switch (SW1501). See *§ 3.12.1.4 System Controller and VMEbus Reset Receive Switch* on page 3-17 for more information.

- **SYS** - This LED (green) lights at the end of successful POST testing. During normal operation this LED should always be lighted.

3.11 Positive Temperature Coefficient Devices

Positive Temperature Coefficient (PTC) devices, shown in *Figure 3-7* and *Figure 3-8*, are located on the SPARC 20MP instead of fuses. These devices are self healing and reset after a fault occurs and do not require replacement.

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3.11.1 AUI Ethernet

The AUI Ethernet PTC (F1), shown in *Figure 3-7*, protects the network transceiver from short circuits or overcurrent. If you plug an AUI Ethernet Cable into the SPARC 20MP Front Panel AUI Connector and the network transceiver LED does not light:

- The network transceiver may be bad
- The AUI Ethernet Cable may be bad
- The AUI Ethernet Cable or the network transceiver may have a bad connection, a shorted center conductor to the shield, or a broken cable segment

or the AUI Ethernet PTC may be open.

Note — The network transceiver is not a part of the SPARC 20MP. It is a device used to connect the SPARC 20MP to the main ethernet network.

3.11.2 Keyboard / Mouse

The Keyboard / Mouse PTC (F1001), shown in *Figure 3-8*, protects the keyboard / mouse from short circuits or overcurrent. If you power on a system and:

- The keyboard speaker does not beep
- The keyboard LEDs do not flash
- A message is displayed on the system monitor:

```
No keyboard connected
```

the Keyboard / Mouse PTC may be open.

3.11.3 SCSI Termination Power

The SCSI Termination Power PTC (F1202), shown in *Figure 3-7*, protects external SCSI devices from short circuits or overcurrent. To determine if the SCSI Termination Power PTC is open, use an ohmmeter to test the SCSI Termination Power PTC for a lack of continuity.

3.11.4 Audio Loud Speaker

The Audio Loud Speaker PTC (F1302), shown in *Figure 3-8*, protects the SPARC 20MP from short circuits or overcurrent caused by the external Audio Loud Speaker. To determine if the Audio Loud Speaker PTC is open, use an ohmmeter to test the Audio Loud Speaker PTC for a lack of continuity.

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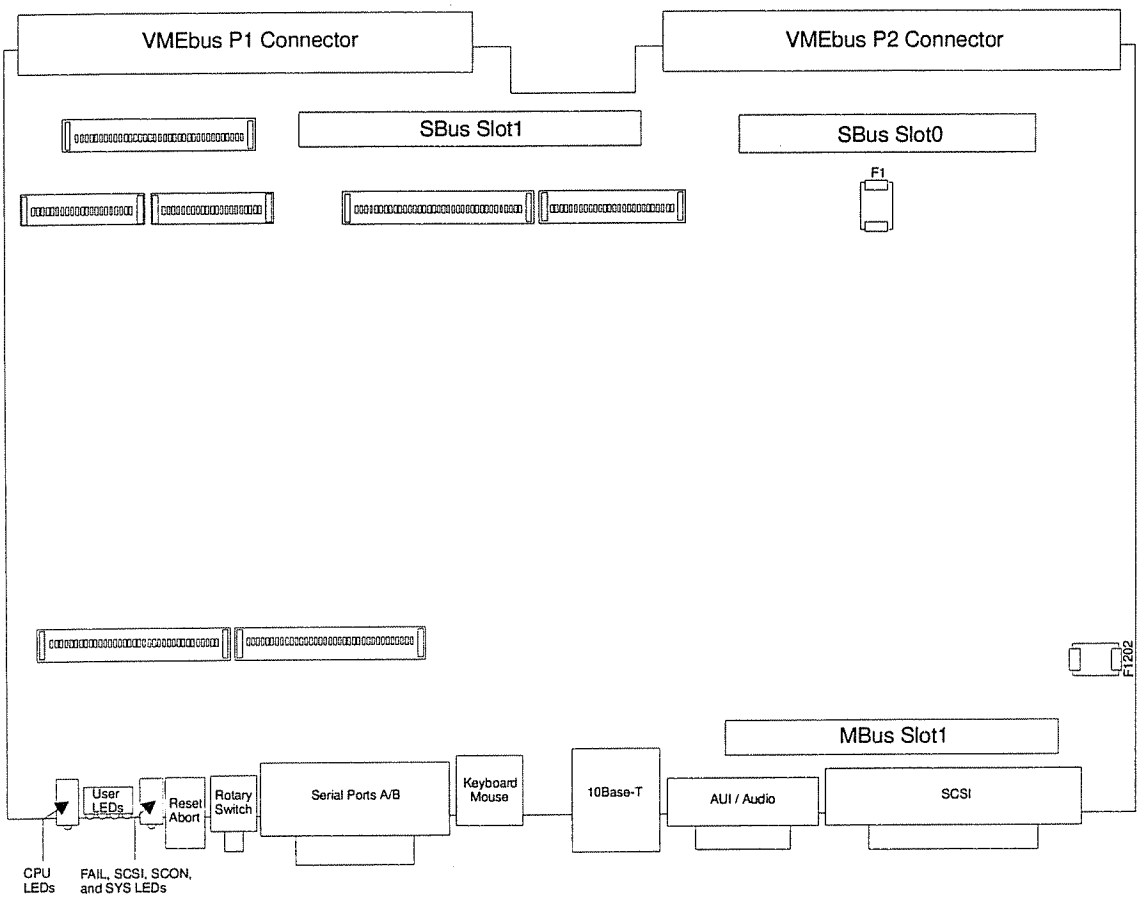


Figure 3-7. **SPARC 20MP Baseboard with Positive Temperature Coefficient Device Locations (Component Side)**

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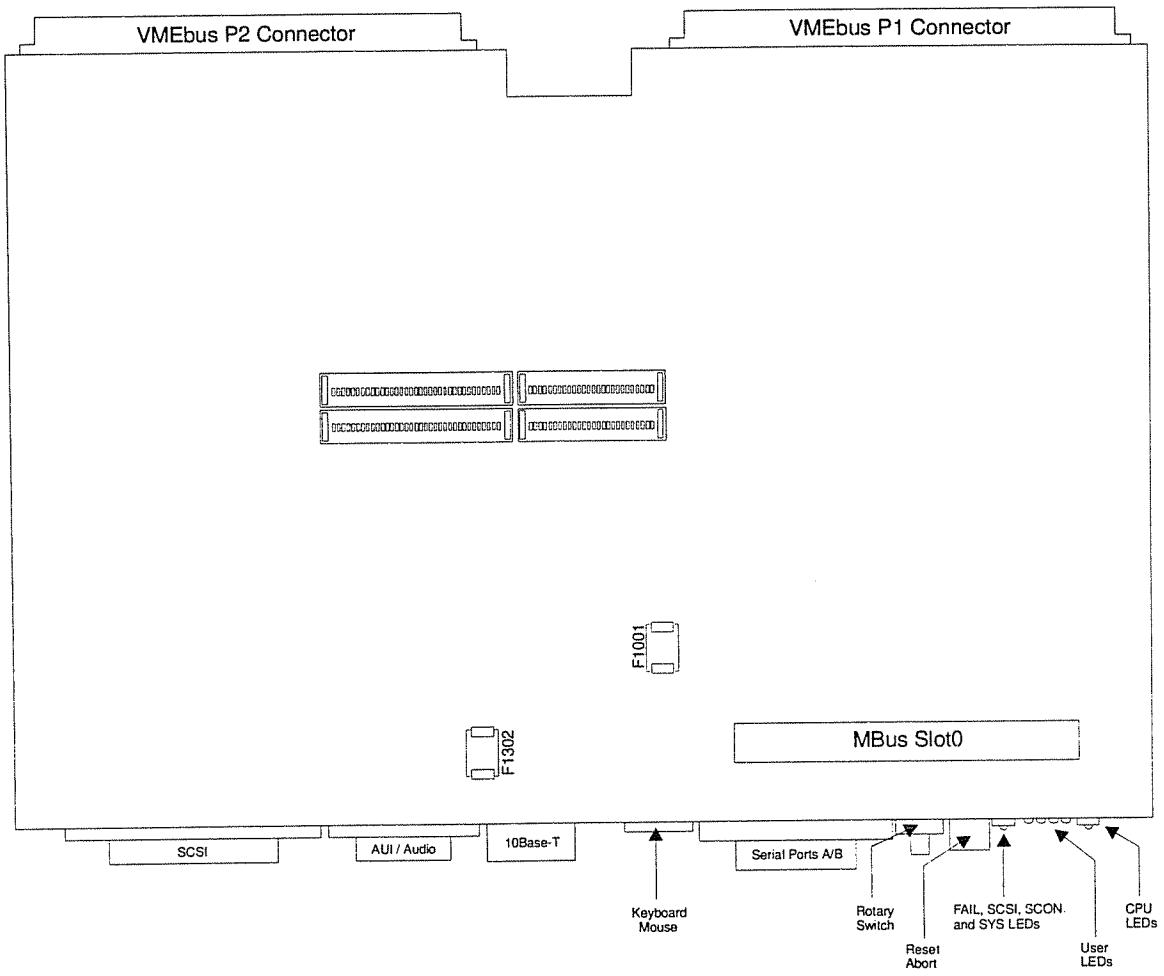


Figure 3-8. **SPARC 20MP Baseboard with Positive Temperature Coefficient Device Locations (Solder Side)**

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3.12 Switches, Solder Beads and Jumper Settings

The SPARC 20MP contains a number of user configurable switches, solder beads, and jumper settings. The function and location of each of these devices is described in the following sections:

- **Switches:**
  - **Flash#0 Write Enable Switch (SW701)** - The function of this switch is to enable or disable Flash#0 write capabilities.
  - **Serial Ports and SCSI Termination Switch (SW703)** - The function of this switch is to select Serial Port B interface mode, select Keyboard/Mouse or Serial Ports C/D (on the paddleboard), and select SCSI termination options.
  - **VMEbus Reset and NVRAM Write Protect Switch (SW704)** - The function of this switch is to enable or disable a VMEbus reset via the Front Panel Reset Switch and enable or disable the write protect of NVRAM.
  - **System Controller and VMEbus Reset Receive Switch (SW1501)** - The function of this switch is to enable or disable the System Controller feature and enable or disable VMEbus Reset Receive capabilities.
- **Solder Beads:**
  - **Front Panel Reset Solder Bead (SB200)** - The function of this solder bead is to enable or disable the Reset/Abort switch on the front panel.
  - **MBus Clock Frequency Solder Bead (SB301)** - The function of this solder bead is to set the MBus clock speed to 50MHz.
  - **Phase Lock Loop Frequency Solder Bead (SB303)** - The function of this solder bead is to set the Phase Lock Loop frequency at IC306 to 50MHz.
  - **EMC MBus Clock Skew Solder Bead (SB304)** - The function of this solder bead is to adjust the EMC MBus clock skew delay.
  - **MSI MBus Clock Skew Solder Bead (SB305)** - The function of this solder bead is to adjust the MSI MBus clock skew delay.
  - **EPROM Type Solder Beads (SB801 and SB802)** - The function of these solder beads is to set the proper pinout depending on whether there is an EPROM or a flash device installed in the IC802 socket.
  - **SCSI Termination Power Solder Bead (SB1201)** - The function of this solder bead is to determine whether the SPARC 20MP supplies SCSI termination power to SCSI devices attached to the optional Paddleboard.
  - **SCSI Status LED Solder Bead (SB1202)** - The function of this solder bead is to light the Front Panel SCSI LED when the SPARC 20MP SCSI termination is enabled.
  - **MVSIC JTAG Bypass Solder Bead (SB1501)** - The function of this solder bead is to allow the MVSIC daughterboard to be bypassed.
  - **VMEbus Error (BERR) Signal Solder Bead (SB2001)** - The function of this solder bead is to connect or isolate the VMEbus Error (BERR) Signal.
- **Jumper Settings:**
  - **MBus Slot1 JTAG Testing Jumper (JP401)** - The function of this jumper is to change the configuration of the scan data daisy-chain for factory boundary scan testing.

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3.12.1 Switches

The SPARC 20MP has four user configurable switches. Three of these switches are located on the left edge of the component side of the SPARC 20MP baseboard as shown below in *Figure 3-9*. These switches are partially obscured when the MVSIC daughterboard is installed. The fourth user configurable switch is located on the MVSIC daughterboard as shown in *Figure 3-10*. These switches provide the following functionality:

- Flash#0 Write Enable
- Serial Port B RS232/RS422 Mode Selection
- Keyboard / Mouse or Serial Ports C/D Mode Selection
- SCSI Termination Options
- VMEbus Reset Initiate Enable
- NVRAM Write Protect Enable
- System Controller Enable
- VMEbus Reset Receive Enable

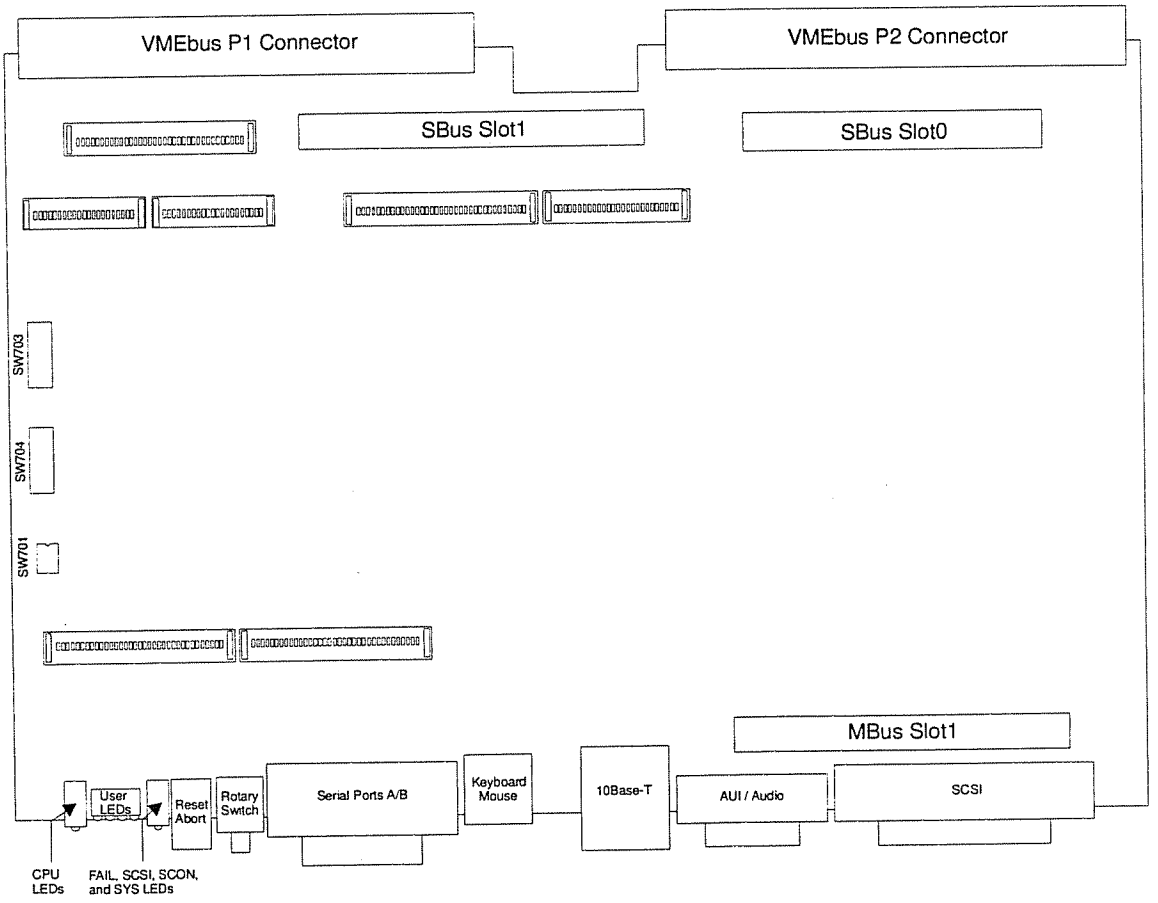


Figure 3-9. **SPARC 20MP Baseboard with Switch Locations (Component Side)**

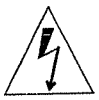
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3.12.1.1 Flash#0 Write Enable Switch

The Flash#0 Write Enable Switch (SW701) is located on the left edge of the SPARC 20MP baseboard under the MVSIC daughterboard as shown in *Figure 3-9.*

Table 3-7. **Flash#0 Write Enable Switch Settings**

SW701-1	SW701-2	SW701-3	SW701-4	Description
ON	-	-	-	**Flash#0 Write Protect Disabled**
OFF	-	-	-	Flash#0 Write Protect Enabled
" - "Switch position is not used to determine function				**Bold** type indicates the factory default settings



Warning — Flash#0 Write Enable Switch Positions 2,3, and 4 are **not** user configurable and should be left in their factory default settings in the "OFF" position.

3.12.1.2 Serial Ports and SCSI Termination Switch

The Serial Ports and SCSI Termination Switch (SW703) is located on the left edge of the SPARC 20MP baseboard under the MVSIC daughterboard as shown in *Figure 3-9.* In *Table 3-8* below the "ON" designation refers to the "DOWN" position (towards the SPARC 20MP baseboard).

Table 3-8. **Serial Ports and SCSI Termination Switch Settings**

SW703-1	SW703-2	SW703-3	SW703-4	Description
ON	-	-	-	**Serial Port B - RS232 Enabled**
OFF	-	-	-	Serial Port B - RS422 Enabled
-	**ON**	-	-	**Keyboard / Mouse Enabled**
-	OFF	-	-	Serial Port C/D Enabled on VMEbus P2 Connector
-	-	**ON**[a]	**ON**	**SCSI Termination Auto-Sensing Enabled**
-	-	ON	OFF	SCSI Termination Enabled
-	-	OFF[b]	X[c]	SCSI Termination Disabled
" - "Switch position is not used to determine function				**Bold** type indicates the factory default settings

a. **SCSI Termination Auto-Sensing Enabled** - SCSI Termination is automatically disabled on the SPARC 20MP baseboard if SCSI devices are attached to both the front panel SCSI connector and the SCSI connector located on the paddleboard. In this instance the SPARC 20MP baseboard is not at either end of the SCSI daisy-chain and should not be terminated.

b. This setting should only be used when the SPARC 20MP is in the middle of the SCSI daisy-chain. Otherwise selftests will fail if a terminated SCSI device is not connected. The selftests fail because the SCSI bus is left floating in this configuration.

c. "X" indicates that the switch position does not matter.

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3.12.1.3 VMEbus Reset and NVRAM Write Protect Switch

The VMEbus Reset and NVRAM Write Protect Switch (SW704) is located on the left edge of the SPARC 20MP baseboard under the MVSIC daughterboard as shown in *Figure 3-9*. In *Table 3-9* below the "ON" designation refers to the "DOWN" position (towards the SPARC 20MP baseboard).

Table 3-9. **VMEbus Reset and NVRAM Write Protect Switch Settings**

SW704-1	SW704-2	SW704-3	SW704-4	Description
ON[a]	-	-	-	**Front Panel Reset Switch resets the VMEbus**
OFF	-	-	-	Front Panel Reset Switch does not reset the VMEbus
-	ON	-	-	NVRAM Write Protect Enabled
-	**OFF**	-	-	**NVRAM Write Protect Disabled**
-	-	X[b]	-	User Defined
-	-	-	X[b]	User Defined
" - "Switch position is not used to determine function				**Bold** type indicates the factory default settings

a. The SPARC 20MP must be the System Controller (see *§ 3.12.1.4 System Controller and VMEbus Reset Receive Switch* on page 3-17) for this switch setting to be in effect.

b. "X" indicates that the switch postion does not matter. This switch is provided for user defined programming. The switch setting can be read at address 0xE F500 0010 (see *§ 4.4.2 Switch Status Register* on page 4-8 for more information).

3.12.1.4 System Controller and VMEbus Reset Receive Switch

The System Controller and VMEbus Reset Receive Switch (SW1501) is located on the right edge of the MVSIC daughterboard as shown below in *Figure 3-10*.

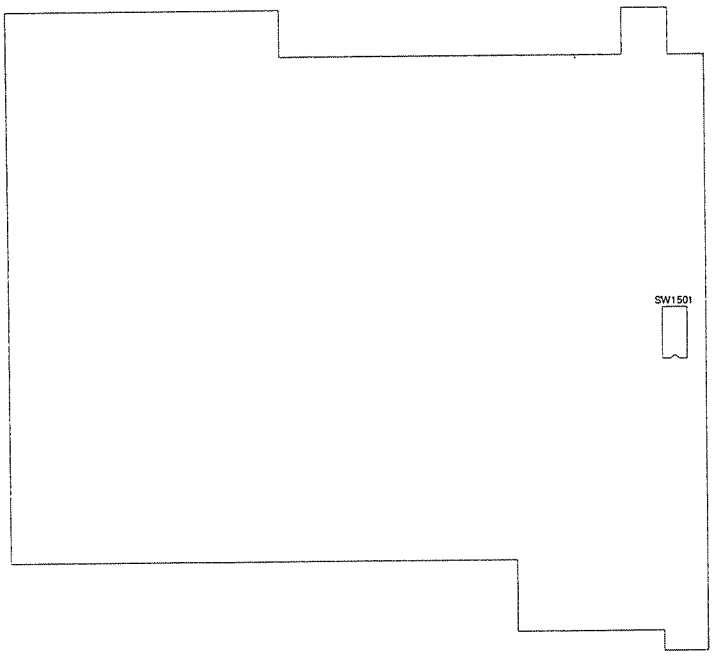


Figure 3-10. **MVSIC Daughterboard with Switch Location (Component Side)**

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Table 3-10. **System Controller and VMEbus Reset Receive Switch Settings**

SW1501-5	SW1501-6	SW1501-7	SW1501-8	Description
-	-	-	**ON**	**System Controller Override Enabled**
-	-	-	OFF[a]	System Controller Override Disabled
ON	-	-	-	**VMEbus Reset Signal resets the SPARC 20MP**
OFF	-	-	-	VMEbus Reset Signal does not reset the SPARC 20MP
" - "Switch position is not used to determine function				**Bold** type indicates the factory default settings

CORRECT

a. **System Controller Override Disabled** - When the System Controller feature is disabled, the SPARC 20MP will automatically determine whether or not it should be the System Controller. The SPARC 20MP uses the VMEbus signal BG3IN to automatically determine whether or not the SPARC 20MP is the System Controller. If the BG3IN signal is low, the SPARC 20MP is the System Controller. If the BG3IN signal is high, the SPARC 20MP is not the System Controller. The status of the BG3IN signal is displayed by OpenBoot, and is visible in the SYSC bit of the SCV64 STAT1 register.

Warning — System Controller and VMEbus Reset Receive Switch (SW1501) Positions 1,2,3,4,6,and 7 are **not** user configurable and should be left in their factory default settings in the "OFF" position.

OVERRIDE MEANS YES (T1)
THE SYSTEM CONTROLLER
OBP 2.1 ABOVE IS CORRECT

CG MUSIC ON DOES NOT RESET 20MP WITH VMESYSRESET
OFF DOES RESET 20MP

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3.12.2 Solder Beads

The SPARC 20MP has eleven factory configurable solder beads. Seven of these solder beads are located on the component side of the SPARC 20MP baseboard as shown below in *Figure 3-11*. The remaining four solder beads are located on the solder side of the SPARC 20MP baseboard as shown in *Figure 3-12*. An additional solder bead (SB803) is reserved for future use. These solder beads provide the following functionality:

- Front Panel Reset - SB200 (see *Figure 3-12*)
- MBus Clock Frequency - SB301 (see *Figure 3-12*)
- Phase Lock Loop Frequency- SB303 (see *Figure 3-11*)
- EMC MBus Clock Skew - SB304 (see *Figure 3-11*)
- MSI MBus Clock Skew - SB305 (see *Figure 3-11*)
- EPROM Type - SB801 and SB802 (see *Figure 3-11*)
- SCSI Termination Power- SB1201 (see *Figure 3-12*)
- SCSI Status LED - SB1202 (see *Figure 3-11*)
- MVSIC JTAG Bypass - SB1501 (see *Figure 3-11*)
- VMEbus Error (BERR) Signal - SB2001 (see *Figure 3-12*)

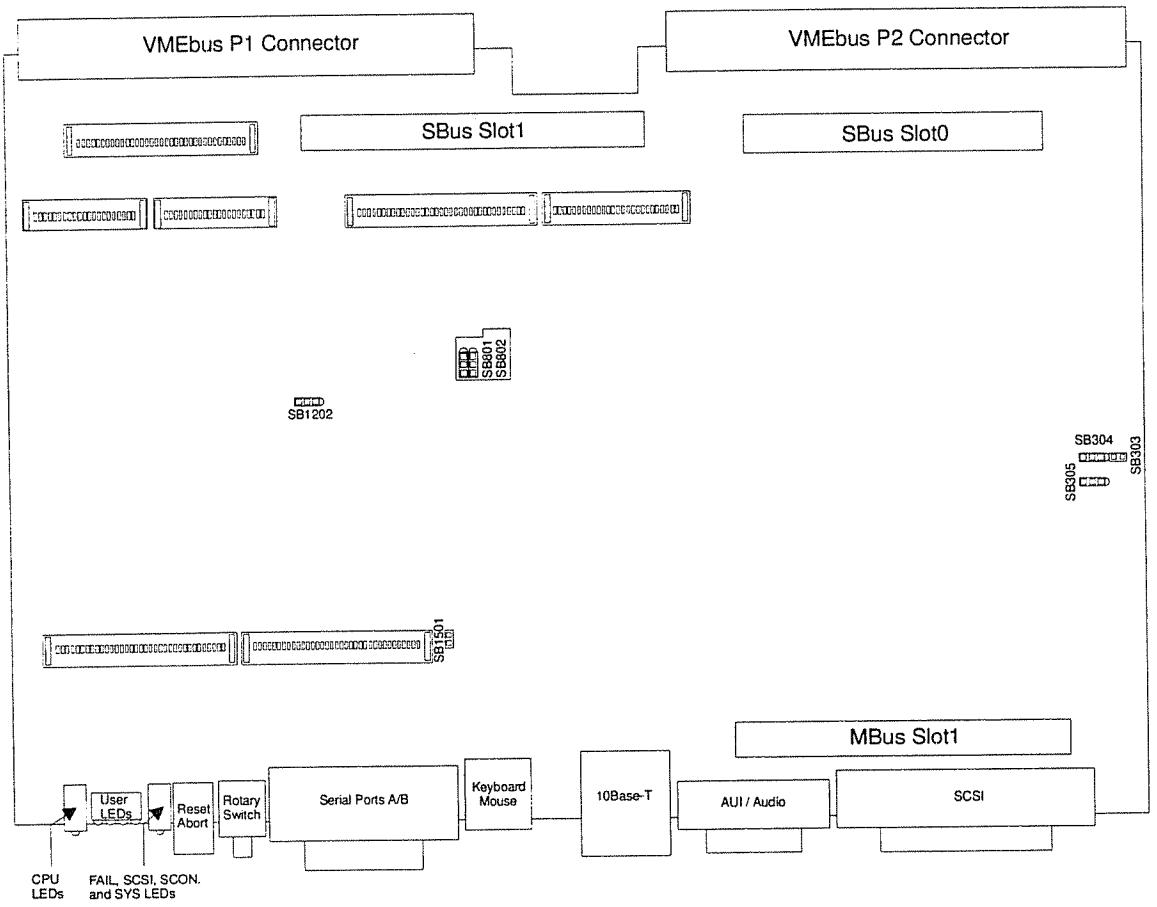


Figure 3-11. **SPARC 20MP Baseboard with Solder Bead Locations (Component Side)**

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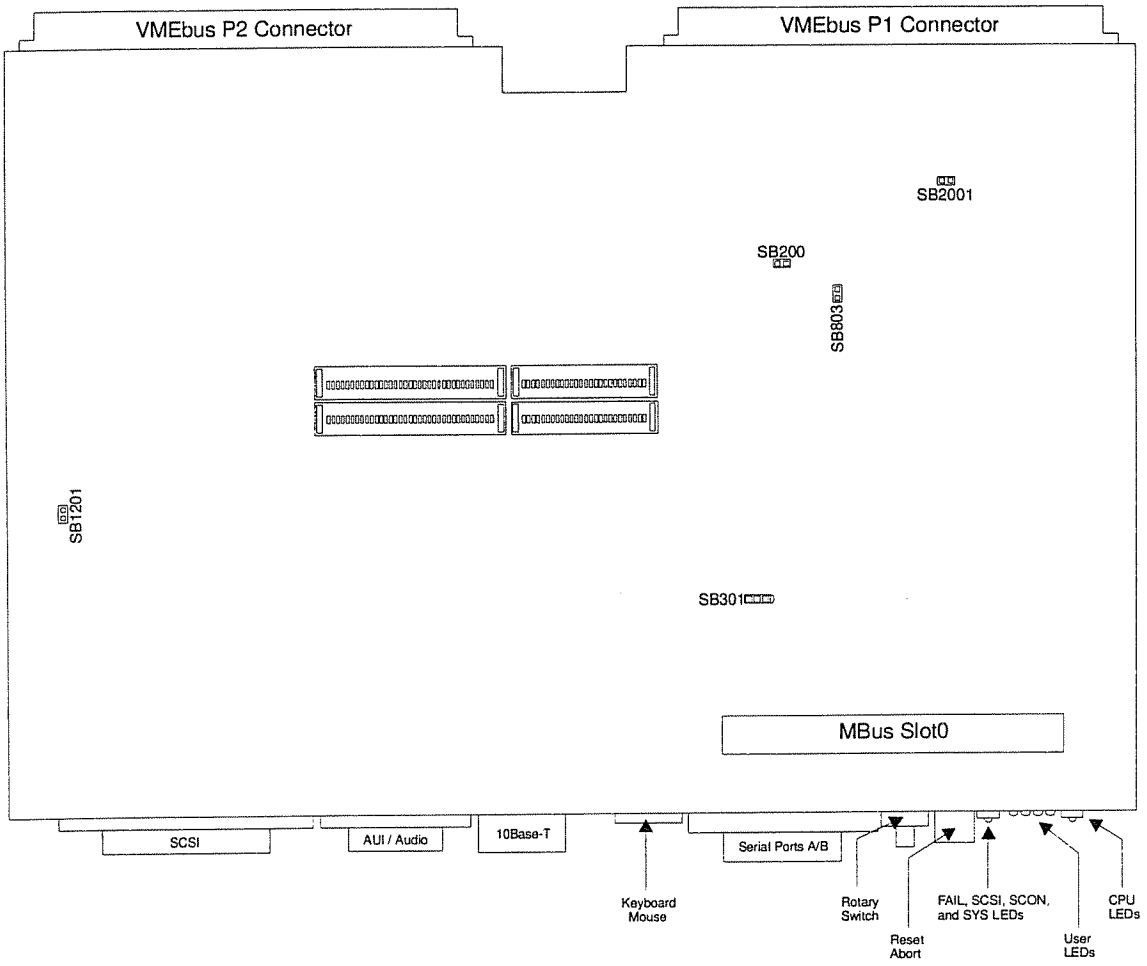


Figure 3-12. **SPARC 20MP Baseboard with Solder Bead Locations (Solder Side)**



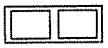
Warning — Solder Beads with three positions should **never** be set to the closed position of connecting all three positions. Connecting all three positions of a solder bead could damage the SPARC 20MP.

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3.12.2.1 Front Panel Reset Solder Bead

The Front Panel Reset Solder Bead (SB200) is located on the solder side of the SPARC 20MP baseboard as shown in *Figure 3-12* on page 3-20. The function of this solder bead is to enable or disable the Reset/Abort switch on the front panel.

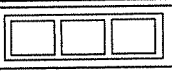
Table 3-11. **Front Panel Reset Solder Bead Settings**

Open	**Closed**
	
The Front Panel Reset Switch is non-operational	The Front Panel Reset Switch will reset the SPARC 20MP
	Factory Default

3.12.2.2 MBus Clock Frequency Solder Bead

The MBus Clock Frequency Solder Bead (SB301) is located on the solder side of the SPARC 20MP baseboard as shown in *Figure 3-12* on page 3-20. The function of this solder bead is to set the MBus clock speed to 50MHz.

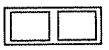
Table 3-12. **MBus Clock Frequency Solder Bead Settings**

Open	**Positions 1-2 Closed**	**Positions 2-3 Closed**
		
Reserved	Reserved	MBus Clock speed set to 50MHz
		Factory Default

3.12.2.3 Phase Lock Loop Frequency Solder Bead

The Phase Lock Loop Frequency Solder Bead (SB303) is located on the component side of the SPARC 20MP baseboard as shown in *Figure 3-11* on page 3-19. The function of this solder bead is to set the Phase Lock Loop frequency at IC306 to 50MHz.

Table 3-13. **Phase Lock Loop Frequency Solder Bead Settings**

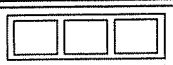
Open	**Closed**
	
Phase Lock Loop frequency is set to 50MHz	Reserved
Factory Default	

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3.12.2.4 EMC MBus Clock Skew Solder Bead

The EMC MBus Clock Skew Solder Bead (SB304) is located on the component side of the SPARC 20MP baseboard as shown in *Figure 3-11* on page 3-19. The function of this solder bead is to adjust the EMC MBus clock skew delay.

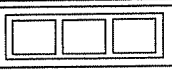
Table 3-14. **EMC MBus Clock Skew Solder Bead Settings**

Open	Positions 1-2 Closed	Positions 2-3 Closed
		
EMC MBus Clock is not skewed	EMC MBus Clock is skewed by +0.77ns	EMC MBus Clock is skewed by -0.77ns
Factory Default		

3.12.2.5 MSI MBus Clock Skew Solder Bead

The MSI MBus Clock Skew Solder Bead (SB305) is located on the component side of the SPARC 20MP baseboard as shown in *Figure 3-11* on page 3-19. The function of this solder bead is to adjust the MSI MBus clock skew delay.

Table 3-15. **MSI MBus Clock Skew Solder Bead Settings**

Open	Positions 1-2 Closed	Positions 2-3 Closed
		
MSI MBus Clock is not skewed	MSI MBus Clock is skewed by +0.77ns	MSI MBus Clock is skewed by -0.77ns
Factory Default		

3.12.2.6 EPROM Type Solder Beads

The EPROM type Solder Beads (SB801 and SB802) are located on the component side of the SPARC 20MP baseboard as shown *Figure 3-11* on page 3-19. The function of these solder beads is to set the proper pinout depending on whether there is an EPROM or a flash device is installed in the IC802 socket.

Table 3-16. **EPROM Type Solder Beads Settings**

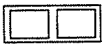
Positions 1-2 Closed	Positions 2-3 Closed
	
27C040 EPROM is installed	29F040 flash device is installed
	Factory Default
NOTE: Both solder beads (SB801 and SB802) **must** be installed according to the above illustrations. Any other combination of settings could damage the SPARC 20MP.	

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3.12.2.7 SCSI Termination Power Solder Bead

The SCSI Termination Power Solder Bead (SB1201) is located on the solder side of the SPARC 20MP baseboard as shown in *Figure 3-12* on page 3-20. The function of this solder bead is to determine whether the SPARC 20MP supplies SCSI termination power to SCSI devices attached to the optional Paddleboard.

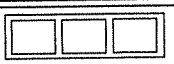
Table 3-17. **SCSI Termination Power Solder Bead Settings**

Open	Closed
	
SCSI device supplies own termination power	SPARC 20MP supplies termination power
	Factory Default

3.12.2.8 SCSI Status LED Solder Bead

The SCSI Status LED Solder Bead (SB1202) is located on the component side of the SPARC 20MP baseboard as shown in *Figure 3-11* on page 3-19. The function of this solder bead is to light the Front Panel SCSI LED when the SPARC 20MP SCSI termination is enabled. SPARC 20MP SCSI termination is can be enabled either through the auto-sensing capabilities or the settings of switch SW703 positions 3 and 4 (see *§ 3.12.1.2 Serial Ports and SCSI Termination Switch* on page 3-16).

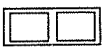
Table 3-18. **SCSI Status LED Solder Bead Settings**

Open	Positions 1-2 Closed	Positions 2-3 Closed
		
Reserved	SPARC 20MP SCSI Termination is enabled	Reserved
	Factory Default	

3.12.2.9 MVSIC JTAG Bypass Solder Bead

The MVSIC JTAG Bypass Solder Bead (SB1501) is located on the component side of the SPARC 20MP baseboard as shown in *Figure 3-11* on page 3-19. The function of this solder bead is to allow the MVSIC daughterboard to be bypassed.

Table 3-19. **MVSIC JTAG Bypass Solder Bead Settings**

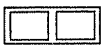
Open	Closed
	
The MVSIC daughterboard is not bypassed	The MVSIC daughterboard is bypassed
Factory Default	

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3.12.2.10 VMEbus Error (BERR) Signal Solder Bead

The VMEbus Error (BERR) Signal Solder Bead (SB2001) is located on the solder side of the SPARC 20MP baseboard as shown *Figure 3-12* on page 3-20. The function of this solder bead is to connect or isolate the VMEbus Error (BERR) Signal.

Table 3-20. **VMEbus Error (BERR) Signal Solder Bead Settings**

Open	Closed
	
The VMEbus Error (BERR) Signal is isolated from the VME backplane	The VMEbus Error (BERR) Signal is connected to the VME backplane
	Factory Default

3.12.3 Jumpers

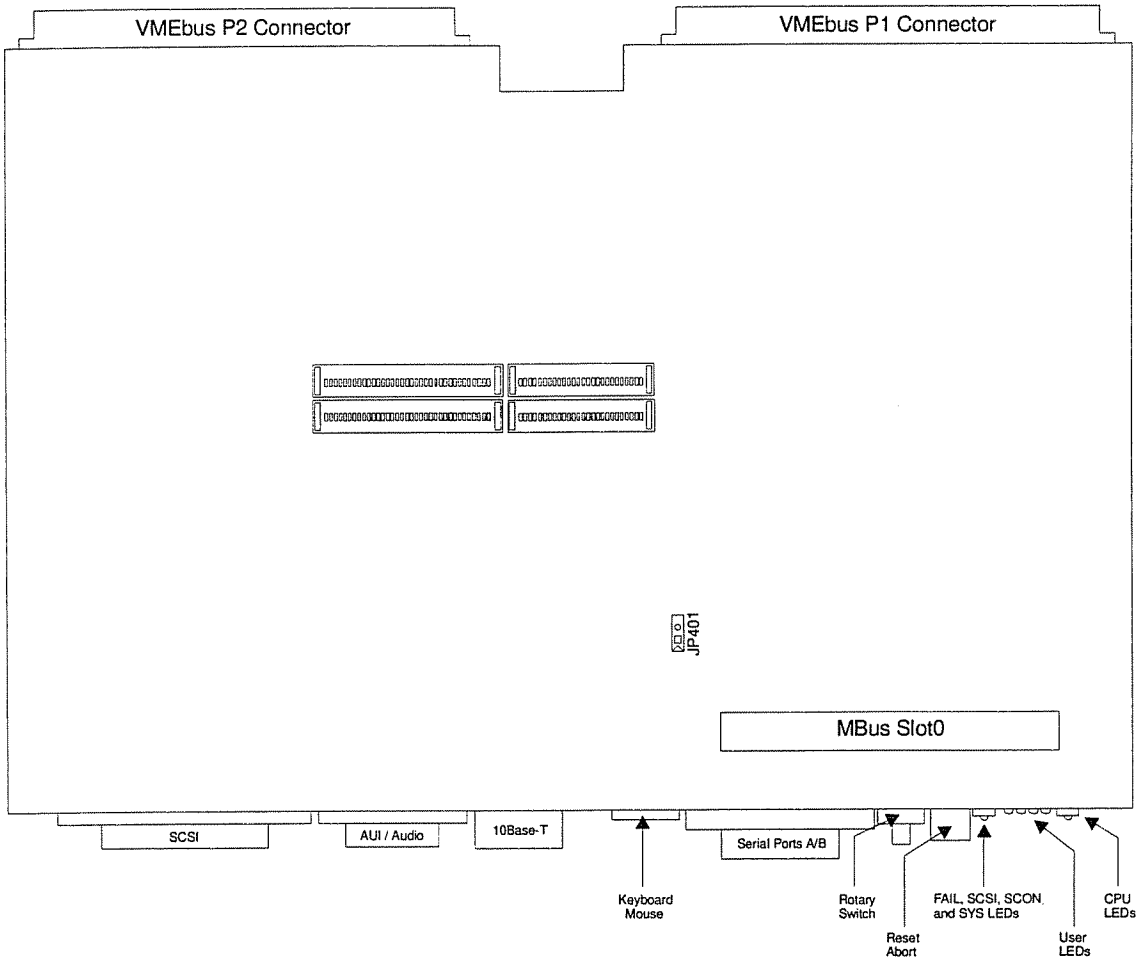


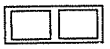
Figure 3-13. **SPARC 20MP Baseboard with Jumper Location (Solder Side)**

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3.12.3.1 MBus Slot1 JTAG Testing Jumper

The MBus Slot1 JTAG Testing Jumper (JP401) is located on the solder side of the SPARC 20MP baseboard as shown in *Figure 3-13*. The function of this jumper is to change the configuration of the scan data daisy-chain for factory boundary scan testing.

Table 3-21. **MBus Slot1 JTAG Testing Jumper Settings**

Open	Closed
	
Do not bypass MBus Slot1 JTAG scan data daisy-chain in the whole board data daisy-chain.	Bypass MBus Slot1 JTAG scan data daisy-chain in the whole board data daisy-chain.
	Factory Default

3.13 Connectors

The SPARC 20MP has various connectors which are located on the front panel, attached to the baseboard, and on the optional paddleboard. Each of these connectors are listed below and has a section with illustrations and/or tables with a complete listing of the connector pinouts.

- **Front Panel Connectors**
  - Serial Ports A/B
  - Keyboard / Mouse
  - 10Base-T Ethernet
  - AUI / Audio
  - SCSI
- **Baseboard Connectors**
  - VMEbus P1 Connector
  - VMEbus P2 Connector
- **Paddleboard Connectors**
  - SCSI
  - Serial Ports C/D
  - Parallel Port
  - AUI Ethernet

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3.13.1 Front Panel Connectors

Described below are the connectors located on the front panel of the SPARC 20MP. Included are illustrations and/or tables with a complete listing of the connector pinouts.

3.13.1.1 Serial Ports A/B Connector

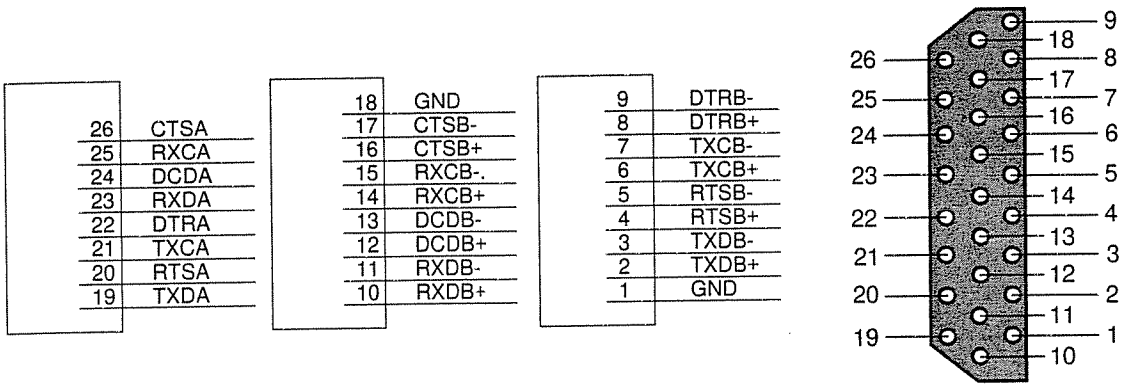


Figure 3-14. **Serial Ports A/B Connector Pinouts**

Table 3-22. **Serial Ports A/B Connector Pinouts**

Pin	Signal Name	Description	Direction	Level
1	GND	Ground		Ground
2	TXDB+	Transmit Data	Output	RS232 / RS422
3	TXDB-	Transmit Data	Output	RS422
4	RTSB+	Request To Send	Output	RS232 / RS422
5	RTSB-	Request To Send	Output	RS422
6	TXCB+	Transmit Clock	Output	RS232 / RS422
7	TXCB-	Transmit Clock	Output	RS422
8	DTRB+	Data Terminal Ready	Output	RS232 / RS422
9	DTRB-	Data Terminal Ready	Output	RS422
10	RXDB+	Receive Data	Input	RS232 / RS422
11	RXDB-	Receive Data	Input	RS422
12	DCDB+	Data Carrier Detect	Input	RS232 / RS422
13	DCDB-	Data Carrier Detect	Input	RS422
14	RXCB+	Receive Clock	Input	RS232 / RS422
15	RXCB-	Receive Clock	Input	RS422
16	CTSB+	Clear To Send	Input	RS232 / RS422
17	CTSB-	Clear To Send	Input	RS422

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Table 3-22. **Serial Ports A/B Connector Pinouts** (Continued)

Pin	Signal Name	Description	Direction	Level
18	GND	Ground		Ground
19	TXDA	Transmit Data	Output	RS232
20	RTSA	Request To Send	Output	RS232
21	TXCA	Transmit Clock	Output	RS232
22	DTRA	Data Terminal Ready	Output	RS232
23	RXDA	Receive Data	Input	RS232
24	DCDA	Data Carrier Detect	Input	RS232
25	RXCA	Receive Clock	Input	RS232
26	CTSA	Clear To Send	Input	RS232

3.13.1.2 Keyboard / Mouse Connector

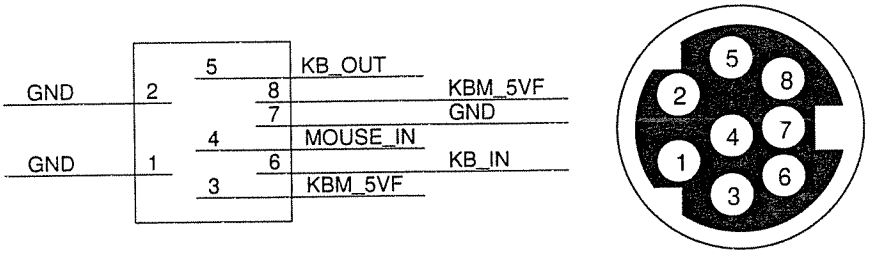


Figure 3-15. **Keyboard / Mouse Connector Pinouts**

Table 3-23. **Keyboard / Mouse Connector Pinouts**

Pin	Signal Name	Description	Direction	Level
1	GND	Ground		Ground
2	GND	Ground		Ground
3	KBM_5VF	+5 VDC	Output	VCC
4	MOUSE_IN	Mouse Read	Input	TTL
5	KB_OUT	Keyboard Write	Output	TTL
6	KB_IN	Keyboard Read	Input	TTL
7	GND	Ground		Ground
8	KBM_5VF	+5 VDC	Output	VCC

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3.13.1.3 10Base-T Ethernet Connector

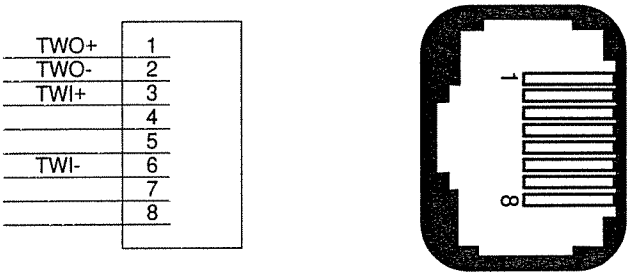


Figure 3-16. **10Base-T Ethernet Connector Pinouts**

Table 3-24. **10Base-T Ethernet Connector Pinouts**

Pin	Signal Name	Description	Direction	Level
1	TWO+	Transmit Data	Output	Analog
2	TWO-	Transmit Data	Output	Analog
3	TWI+	Receive Data	Input	Analog
4		Not Connected		
5		Not Connected		
6	TWI-	Receive Data	Input	Analog
7		Not Connected		
8		Not Connected		

3.13.1.4 AUI / Audio Connector

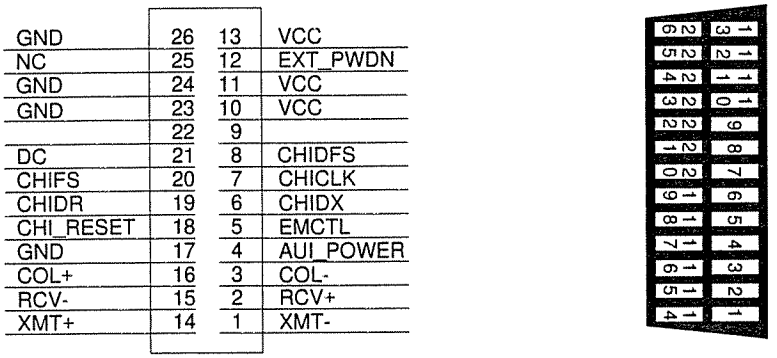


Figure 3-17. **AUI / Audio Connector Pinouts**

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Table 3-25. **AUI / Audio Connector Pinouts**

Pin	Signal Name	Description	Direction	Level
1	XMT-	Data Transmit	Output	Analog
2	RCV+	Data Receive	Input	Analog
3	COL-	AUI Collision	Input	Analog
4	AUI_POWER	+12 VDC	Output	DC
5	EMCTL		Input / Output	TTL
6	CHIDX	Audio Data Transmit	Input / Output	TTL
7	CHICLK	Audio Clock	Input / Output	TTL
8	CHIDFS	Audio Frame Select	Input / Output	TTL
9	NC	Not Connected		
10	VCC	Audio Power	Output	DC
11	VCC	Audio Power	Output	DC
12	EXT_PWDN	External Power Down	Input	TTL
13	VCC	Audio Power	Output	DC
14	XMT+	Data Transmit	Output	Analog
15	RCV-	Data Receive	Input	Analog
16	COL+	AUI Collision	Input	Analog
17	GND	Ground		GND
18	CHI_RESET	Audio Reset	Input / Output	TTL
19	CHIDR	Audio Data Receive	Input / Output	TTL
20	CHIFS	Audio Frame Select	Input / Output	TTL
21	DC		Input / Output	TTL
22	NC	Not Connected		
23	GND	Speaker Ground		GND
24	GND	Speaker Ground		GND
25	NC	Not Connected		
26	GND	Speaker Ground		GND

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3.13.1.5 SCSI Connector

SCSI_IO*	50	25	GND
SCSI_REQ*	49	24	GND
SCSI_CD*	48	23	GND
SCSI_SEL*	47	22	GND
SCSI_MSG*	46	21	GND
SCSI_RST*	45	20	GND
SCSI_ACK*	44	19	GND
SCSI_BSY*	43	18	GND
	42	17	GND
SCSI_ATN*	41	16	GND
	40	15	GND
	39	14	GND
TERMPWR+	38	13	
	37	12	GND
	36	11	FRONT_SCSI*
	35	10	GND
SCSI_D8	34	9	GND
SCSI_D7	33	8	GND
SCSI_D6	32	7	GND
SCSI_D5	31	6	GND
SCSI_D4	30	5	GND
SCSI_D3	29	4	GND
SCSI_D2	28	3	GND
SCSI_D1	27	2	GND
SCSI_D0	26	1	GND

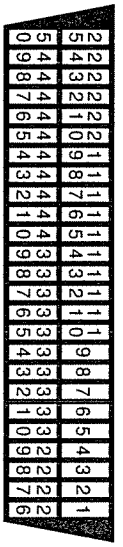


Figure 3-18. **SCSI Connector Pinouts**

Table 3-26. **SCSI Connector Pinouts**

Pin	Signal Name	Description	Direction	Level
1	GND	Ground		GND
2	GND	Ground		GND
3	GND	Ground		GND
4	GND	Ground		GND
5	GND	Ground		GND
6	GND	Ground		GND
7	GND	Ground		GND
8	GND	Ground		GND
9	GND	Ground		GND
10	GND	Ground		GND
11	FRONT_SCSI*	SCSI Auto Sense - Front Panel	Input	TTL
12	GND	Ground		GND
13		Not Connected		
14	GND	Ground		GND
15	GND	Ground		GND
16	GND	Ground		GND

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Table 3-26. **SCSI Connector Pinouts** (Continued)

Pin	Signal Name	Description	Direction	Level
17	GND	Ground		GND
18	GND	Ground		GND
19	GND	Ground		GND
20	GND	Ground		GND
21	GND	Ground		GND
22	GND	Ground		GND
23	GND	Ground		GND
24	GND	Ground		GND
25	GND	Ground		GND
26	SCSI_D0	Data Bit	Input / Output	TTL
27	SCSI_D1	Data Bit	Input / Output	TTL
28	SCSI_D2	Data Bit	Input / Output	TTL
29	SCSI_D3	Data Bit	Input / Output	TTL
30	SCSI_D4	Data Bit	Input / Output	TTL
31	SCSI_D5	Data Bit	Input / Output	TTL
32	SCSI_D6	Data Bit	Input / Output	TTL
33	SCSI_D7	Data Bit	Input / Output	TTL
34	SCSI_D8	Data Parity Bit	Input / Output	TTL
35		Not Connected		
36		Not Connected		
37		Not Connected		
38	TERMPWR+	Termination Voltage	Input / Output	TTL
39		Not Connected		
40		Not Connected		
41	SCSI_ATN*	Attention	Output	TTL
42		Not Connected		
43	SCSI_BSY*	Busy	Output	TTL
44	SCSI_ACK*	Acknowledge	Output	TTL
45	SCSI_RST*	Reset	Output	TTL
46	SCSI_MSG*	Message	Output	TTL
47	SCSI_SEL*	Select	Output	TTL
48	SCSI_CD*	Control / Data	Output	TTL
49	SCSI_REQ*	Request	Output	TTL
50	SCSI_IO*	Input / Output	Output	TTL

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3.13.2 Baseboard Connectors

Described below are the connectors located on the baseboard of the SPARC 20MP. Included are illustrations and/or tables with a complete listing of the connector pinouts.

3.13.2.1 VMEbus P1 Connector

	ROW C		ROW B		ROW A
	C1	D8	B1	BUSY*	A1	D0
	C2	D9	B2	BCLR*	A2	D1
	C3	D10	B3	ACFAIL*	A3	D2
	C4	D11	B4	BGI0*	A4	D3
	C5	D12	B5	BGO0*	A5	D4
	C6	D13	B6	BGI1*	A6	D5
	C7	D14	B7	BGO1*	A7	D6
	C8	D15	B8	BGI2*	A8	D7
	C9	GND	B9	BGO2*	A9	GND
	C10	SYSFAIL*	B10	BG13*	A10	SYSCLOCK+
(1)	C11	BERR*	B11	BGO3*	A11	GND
	C12	SYSRESET*	B12	BR0*	A12	DS1*
	C13	LWORD*	B13	BR1*	A13	DS0*
	C14	AM5	B14	BR2*	A14	RW
	C15	A23	B15	BR3*	A15	GND
	C16	A22	B16	AM0	A16	DTACK*
	C17	A21	B17	AM1	A17	GND
	C18	A20	B18	AM2	A18	AS*
	C19	A19	B19	AM3	A19	GND
	C20	A18	B20	GND	A20	IACK*
	C21	A17	B21		A21	IACKI*
	C22	A16	B22		A22	IACKO*
	C23	A15	B23	GND	A23	AM4
	C24	A14	B24	IRQ7*	A24	A7
	C25	A13	B25	IRQ6*	A25	A6
	C26	A12	B26	IRQ5*	A26	A5
	C27	A11	B27	IRQ4*	A27	A4
	C28	A10	B28	IRQ3*	A28	A3
	C29	A9	B29	IRQ2*	A29	A2
	C30	A8	B30	IRQ1*	A30	A1
	C31	+12V	B31		A31	-12V
	C32	+5V	B32	+5V	A32	+5V

(1) Can be isolated through SB2001

Figure 3-19. **VMEbus P1 Connector Pinouts**

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3.13.2.2 VMEbus P2 Connector

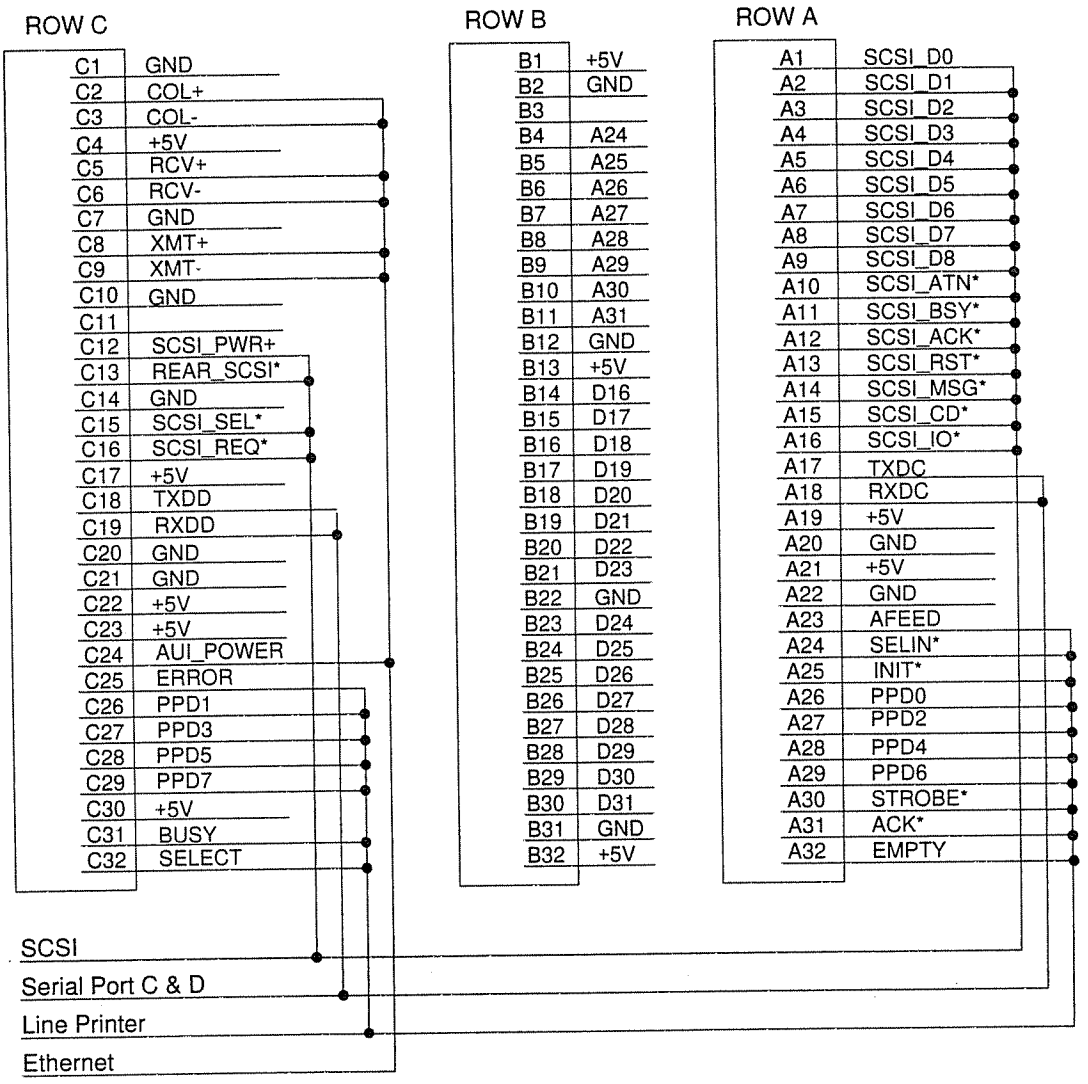


Figure 3-20. **VMEbus P2 Connector Pinouts**

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The VMEbus P2 Connector accommodates user-defined signals. The optional paddleboard is one way of easily accessing the SPARC 20MP VMEbus P2 Connector user-defined signals. The following table lists the VMEbus P2 Connector user-defined signals.

Table 3-27. **VMEbus P2 Connector Pinout of User-defined Signals**

Pin	Signal Name	Description	Direction	Level
A1	SCSI_D0	SCSI Data Bit	Input / Output	TTL
A2	SCSI_D1	SCSI Data Bit	Input / Output	TTL
A3	SCSI_D2	SCSI Data Bit	Input / Output	TTL
A4	SCSI_D3	SCSI Data Bit	Input / Output	TTL
A5	SCSI_D4	SCSI Data Bit	Input / Output	TTL
A6	SCSI_D5	SCSI Data Bit	Input / Output	TTL
A7	SCSI_D6	SCSI Data Bit	Input / Output	TTL
A8	SCSI_D7	SCSI Data Bit	Input / Output	TTL
A9	SCSI_D8	SCSI Parity Bit	Input / Output	TTL
A10	SCSI_ATN*	SCSI Attention	Output	TTL
A11	SCSI_BSY*	SCSI Busy	Input / Output	TTL
A12	SCSI_ACK*	SCSI Acknowledge	Output	TTL
A13	SCSI_RST*	SCSI Reset	Input / Output	TTL
A14	SCSI_MSG*	SCSI Message	Input	TTL
A15	SCSI_CD*	SCSI Control / Data	Input	TTL
A16	SCSI_IO*	SCSI Input / Output Control	Input	TTL
A17	TXDC	Data Transmit	Output	RS232
A18	RXDC	Data Receive	Input	RS232
A19	+5V	+5V	Output	+5V
A20	GND	Ground		GND
A21	+5V	+5V	Output	+5V
A22	GND	Ground		GND
A23	AFEED	Parallel Port Auto Feed	Output	-15mA / 64mA TTL
A24	SELIN*	Parallel Port Select	Output	-15mA / 64mA TTL
A25	INIT*	Parallel Port Reset	Output	-15mA / 64mA TTL
A26	PPD0	Parallel Port Data Bit	Input / Output	-15mA / 64mA TTL
A27	PPD2	Parallel Port Data Bit	Input / Output	-15mA / 64mA TTL
A28	PPD4	Parallel Port Data Bit	Input / Output	-15mA / 64mA TTL
A29	PPD6	Parallel Port Data Bit	Input / Output	-15mA / 64mA TTL
A30	STROBE*	Parallel Port Data Strobe	Input / Output	-15mA / 64mA TTL
A31	ACK*	Parallel Port Acknowledge	Input / Output	-15mA / 64mA TTL
A32	EMPTY	Parallel Port Paper Empty	Input	TTL

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Table 3-27. **VMEbus P2 Connector Pinout of User-defined Signals** (Continued)

Pin	Signal Name	Description	Direction	Level
C1	GND	Ground		GND
C2	COL+	Ethernet Port Collision	Input	Analog
C3	COL-	Ethernet Port Collision	Input	Analog
C4	+5V	+5V	Output	+5V
C5	RCV+	Receive Data	Input	Analog
C6	RCV-	Receive Data	Input	Analog
C7	GND	Ground		GND
C8	XMT+	Transmit Data	Output	Analog
C9	XMT-	Transmit Data	Output	Analog
C10	GND	Ground		GND
C11		Not Connected		
C12	SCSI_PWR+	+5V	Output	+5V
C13	REAR_SCSI*	SCSI Auto Sense - Paddleboard	Input	TTL
C14	GND	Ground		GND
C15	SCSI_SEL*	SCSI Select Output	Input / Output	TTL
C16	SCSI_REQ*	SCSI Request Output	Input / Output	TTL
C17	+5V	+5V	Output	+5V
C18	TXDD	Transmit Data	Output	RS232
C19	RXDD	Receive Data	Input	RS232
C20	GND	Ground		GND
C21	GND	Ground		GND
C22	+5V	+5V	Output	+5V
C23	+5V	+5V	Output	+5V
C24	AUI_POWER	Ethernet Power (+12V)	Output	+12V
C25	ERROR	Parallel Port Error	Input	TTL
C26	PPD1	Parallel Port Data Bit	Input / Output	-15mA / 64mA TTL
C27	PPD3	Parallel Port Data Bit	Input / Output	-15mA / 64mA TTL
C28	PPD5	Parallel Port Data Bit	Input / Output	-15mA / 64mA TTL
C29	PPD7	Parallel Port Data Bit	Input / Output	-15mA / 64mA TTL
C30	+5V	+5V	Output	+5V
C31	BUSY	Parallel Port Busy	Input / Output	-15mA / 64mA TTL
C32	SELECT	Parallel Port Select Input	Input	TTL

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3.13.3 Paddleboard Connectors

The paddleboard is designed for connecting external devices (SCSI devices, serial devices, parallel devices, and AUI ethernet) to the SPARC 20MP. Described below are the connectors located on the optional SPARC 20MP Paddleboard. Included are illustrations and/or tables with a complete listing of the connector pinouts.

3.13.3.1 SCSI Connector

GND	1	2	SCSI_D0
GND	3	4	SCSI_D1
GND	5	6	SCSI_D2
GND	7	8	SCSI_D3
GND	9	10	SCSI_D4
GND	11	12	SCSI_D5
GND	13	14	SCSI_D6
GND	15	16	SCSI_D7
GND	17	18	SCSI_D8
GND	19	20	GND
GND	21	22	REAR_SCSI*
GND	23	24	GND
	25	26	SCSI_PWR+
GND	27	28	GND
GND	29	30	GND
GND	31	32	SCSI_ATN*
GND	33	34	GND
GND	35	36	SCSI_BSY*
GND	37	38	SCSI_ACK*
GND	39	40	SCSI_RST*
GND	41	42	SCSI_MSG*
GND	43	44	SCSI_SEL*
GND	45	46	SCSI_CD*
GND	47	48	SCSI_REQ*
GND	49	50	SCSI_IO*

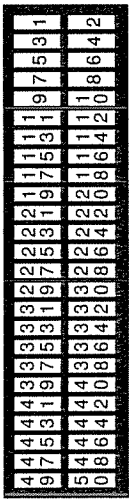


Figure 3-21. **SCSI Paddleboard Connector Pinouts**

Table 3-28. **SCSI Paddleboard Connector Pinouts**

Pin	Signal Name	Description	Direction	Level
1	GND	Ground		GND
2	SCSI_D0	Data Bit	Input / Output	TTL
3	GND	Ground		GND
4	SCSI_D1	Data Bit	Input / Output	TTL
5	GND	Ground		GND
6	SCSI_D2	Data Bit	Input / Output	TTL
7	GND	Ground		GND
8	SCSI_D3	Data Bit	Input / Output	TTL
9	GND	Ground		GND
10	SCSI_D4	Data Bit	Input / Output	TTL
11	GND	Ground		GND
12	SCSI_D5	Data Bit	Input / Output	TTL

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Table 3-28. **SCSI Paddleboard Connector Pinouts** (Continued)

Pin	Signal Name	Description	Direction	Level
13	GND	Ground		GND
14	SCSI_D6	Data Bit	Input / Output	TTL
15	GND	Ground		GND
16	SCSI_D7	Data Bit	Input / Output	TTL
17	GND	Ground		GND
18	SCSI_D8	Data Bit	Input / Output	TTL
19	GND	Ground		GND
20	GND	Ground		GND
21	GND	Ground		GND
22	REAR_SCSI*	SCSI Auto Sense - Paddleboard	Input	TTL
23	GND	Ground		GND
24	GND	Ground		GND
25		Not Connected		
26	SCSI_PWR+	Termination Power	Output	+5V
27	GND	Ground		GND
28	GND	Ground		GND
29	GND	Ground		GND
30	GND	Ground		GND
31	GND	Ground		GND
32	SCSI_ATN*	Attention	Output	TTL
33	GND	Ground		GND
34	GND	Ground		GND
35	GND	Ground		GND
36	SCSI_BSY*	Busy	Input / Output	TTL
37	GND	Ground		GND
38	SCSI_ACK*	Acknowledge	Output	TTL
39	GND	Ground		GND
40	SCSI_RST*	Reset	Input / Output	TTL
41	GND	Ground		GND
42	SCSI_MSG*	Message	Input	TTL
43	GND	Ground		GND
44	SCSI_SEL*	Select Output	Input / Output	TTL
45	GND	Ground		GND
46	SCSI_CD*	Control / Data	Input	TTL
47	GND	Ground		GND

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Table 3-28. **SCSI Paddleboard Connector Pinouts** (Continued)

Pin	Signal Name	Description	Direction	Level
48	SCSI_REQ*	Request Output	Input / Output	TTL
49	GND	Ground		GND
50	SCSI_IO*	Input / Output Control	Output	TTL

3.13.3.2 Serial Ports C/D Connector

In order to use Serial Ports C/D you must select the Serial Ports C/D option on switch SW703-2 (see *§ 3.12.1.2 Serial Ports and SCSI Termination Switch* on page 3-16). Please note that the use of the Serial Ports C/D option will disable the Keyboard / Mouse connector on the front panel.

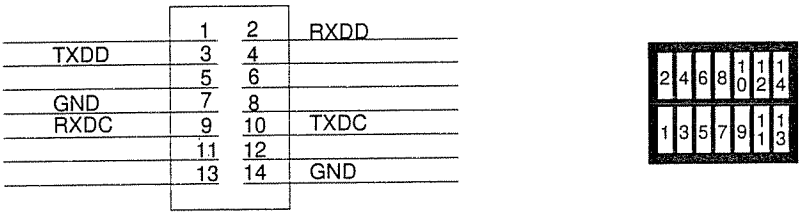


Figure 3-22. **Serial Ports C/D Connector Pinouts**

Table 3-29. **Serial Ports C/D Connector Pinouts**

Pin	Signal Name	Description	Direction	Level
1		Not Connected		
2	RXDD	Receive Data	Input	RS232
3	TXDD	Transmit Data	Output	RS232
4		Not Connected		
5		Not Connected		
6		Not Connected		
7	GND	Ground		GND
8		Not Connected		
9	RXDC	Receive Data	Input	RS232
10	TXDC	Transmit Data	Output	RS232
11		Not Connected		
12		Not Connected		
13		Not Connected		
14	GND	Ground		GND

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3.13.3.3 Parallel Port Connector

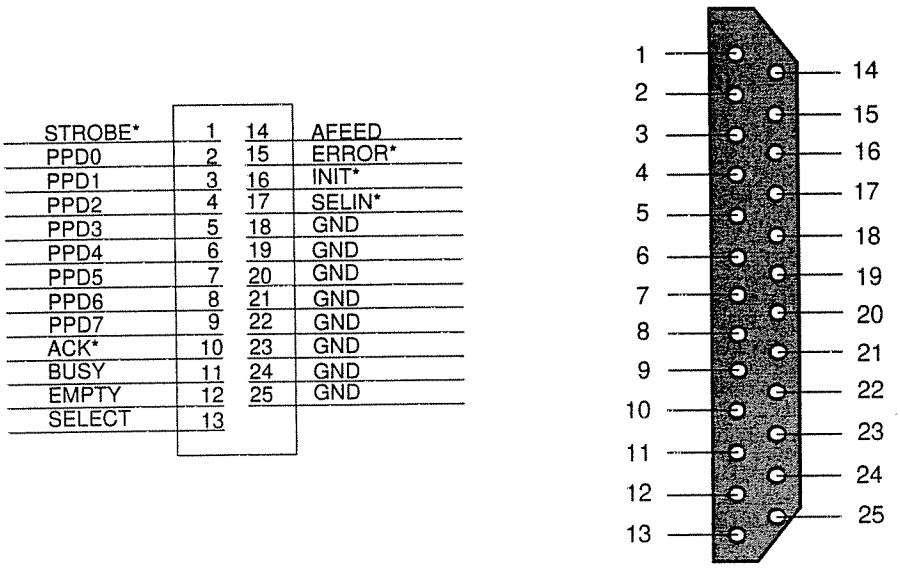


Figure 3-23. **Parallel Port Connector Pinouts**

Table 3-30. **Parallel Port Connector Pinouts**

Pin	Signal Name	Description	Direction	Level
1	STROBE*	Data Strobe	Input / Output	-15mA / 64mA TTL
2	PPD0	Data Bit	Input / Output	-15mA / 64mA TTL
3	PPD1	Data Bit	Input / Output	-15mA / 64mA TTL
4	PPD2	Data Bit	Input / Output	-15mA / 64mA TTL
5	PPD3	Data Bit	Input / Output	-15mA / 64mA TTL
6	PPD4	Data Bit	Input / Output	-15mA / 64mA TTL
7	PPD5	Data Bit	Input / Output	-15mA / 64mA TTL
8	PPD6	Data Bit	Input / Output	-15mA / 64mA TTL
9	PPD7	Data Bit	Input / Output	-15mA / 64mA TTL
10	ACK*	Acknowledge	Input / Output	-15mA / 64mA TTL
11	BUSY	Busy	Input / Output	-15mA / 64mA TTL
12	EMPTY	Paper Empty	Input	TTL
13	SELECT	Select Input	Input	TTL
14	AFEED	Auto Feed	Output	-15mA / 64mA TTL
15	ERROR*	Error	Input	TTL
16	INIT*	Reset	Output	-15mA / 64mA TTL
17	SELIN*	Select	Output	-15mA / 64mA TTL

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Table 3-30. **Parallel Port Connector Pinouts** (Continued)

Pin	Signal Name	Description	Direction	Level
18	GND	Ground		Ground
19	GND	Ground		Ground
20	GND	Ground		Ground
21	GND	Ground		Ground
22	GND	Ground		Ground
23	GND	Ground		Ground
24	GND	Ground		Ground
25	GND	Ground		Ground

3.13.3.4 AUI Ethernet Connector

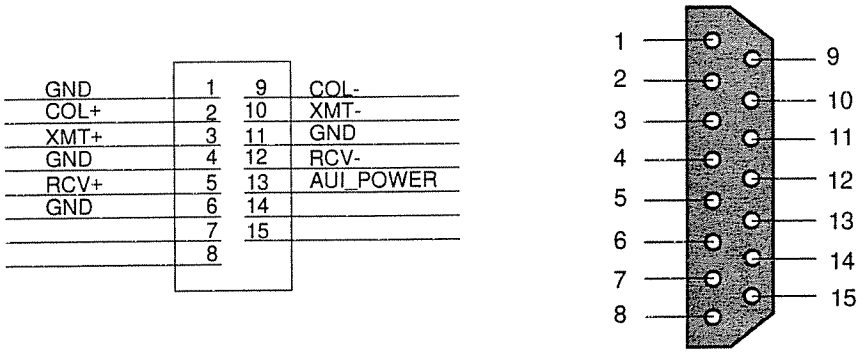


Figure 3-24. **AUI Ethernet Connector Pinouts**

Table 3-31. **AUI Ethernet Connector Pinouts**

Pin	Signal Name	Description	Direction	Level
1	GND	Ground		GND
2	COL+	Collision	Input	Analog
3	XMT+	Transmit Data	Output	Analog
4	GND	Ground		GND
5	RCV+	Receive Data	Input	Analog
6	GND	Ground		GND
7		Not Connected		
8		Not Connected		
9	COL-	Collision	Input	Analog
10	XMT-	Transmit Data	Output	Analog
11	GND	Ground		GND

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Table 3-31. **AUI Ethernet Connector Pinouts** (Continued)

Pin	Signal Name	Description	Direction	Level
12	RCV-	Receive Data	Input	Analog
13	AUI_POWER	+12V	Output	+12V
14		Not Connected		
15		Not Connected		

3.14 Cable Descriptions

3.14.1 Front Panel Serial Ports A/B Cable

Themis P/N 101495 - This is an 80 inch split-end cable. A 26-pin male D-Sub connector attaches to the Front Panel Serial Port A/B Connector. The other end of the cable is split into two 25-pin ~~female~~ male D-Sub connectors. This cable is included in the optional SPARC 20MP Integration Kits.

3.14.2 Sun Compatible Keyboard

Themis P/N 101834 - The SPARC 20MP can use any Sun compatible Type-4 or Type-5 keyboard. The keyboard cable is an 8-pin male mini-DIN connector that attaches to the Front Panel Keyboard / Mouse Connector.

3.14.3 AUI Ethernet / Audio Cable

Themis P/N 103284 - This is a 14 inch cable. A 26-pin male micro D-Sub connector attaches to the Front Panel AUI / Audio Connector. The other end of the cable is split into a 26-pin female micro D-Sub connector (Audio) and a 15-pin female D-Sub connector (AUI Ethernet). The audio connector is intended to be used with a Sun Speakerbox audio unit. Use of any other audio device may cause damage to the audio device and / or the SPARC 20MP. This cable is included in the optional SPARC 20MP Audio Integration Kit

Themis P/N 104293 - This is a 20 inch AUI Ethernet only cable. A 26-pin male micro D-Sub connector attaches to the Front Panel AUI / Audio Connector. The other end of the cable is a 15-pin female D-Sub connector. This cable is included in the optional SPARC 20MP Integration Kit.

3.14.4 Front Panel SCSI Cable

Themis P/N 101371 - This is a 40 inch cable. A 50-pin male micro D-Sub connector attaches to the Front Panel SCSI connector. The other end of the cable is a 50-pin female IDC connector. This cable is included in the optional SPARC 20MP Integration Kits.

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3.14.5 Flat Ribbon SCSI Cable

Themis P/N 101372 - This is a 36 inch flat ribbon cable. A 50-pin female IDC connector attaches to the optional Paddleboard SCSI Connector. The other end of the cable contains two 50-pin female IDC connectors. This cable is included in the optional SPARC 20MP Integration Kits.

3.14.6 Other Cables

The SPARC 20MP uses widely available industry standard cables for the following connectors:

- Front Panel 10Base-T Ethernet Cable
- Parallel Port (Centronics) Cable
- AUI Ethernet Cable

3.15 20MP Diagnostics

This section describes the different types of diagnostic firmware and software tools available to you and how they are related. The main categories of diagnostics are:

- Boot PROM diagnostics
  - Power-On Self-Test (POST)
  - On-Board Diagnostics
- Forth Toolkit
- SunDiag System Exerciser

3.15.1 How It Fits Together

Note — This description assumes you are using a Sun compatible keyboard as well as a graphics monitor to view test results.

The Power On Self Test (POST) will run automatically at power up when:

- the `Stop (L1)-D` keys are pressed
- the `diag-switch?` parameter is set true.

While the low-level POST code executes, the CAPSLOCK LED on the keyboard flashes to indicate that POST testing is in progress. If a failure occurs in POST, the failing replaceable unit is encoded on three LEDs located on the Type-5 keyboard. See *§ 3.15.3 Power-On Self Test (POST)* on page 3-44 for more information.

If the POST passes, the system probes for SBus devices and interprets their drivers. Next, high level test are performed. You will see the word Testing while the high level tests are running. After `Testing` is displayed, if you want to enter the Forth Toolkit, (indicated by the `ok` prompt), press the `Stop-A` (L1-A) keys simultaneously.

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If the `autoboot?` switch parameter is set to false (not the default), you will obtain the `ok` prompt. To change to the Monitor prompt (>) see the *OpenBoot Command Reference*.

If the `autoboot?` switch parameter is set to true (default), and the diagnostic switch parameter is set to false (default), Solaris is booted using the device alias "disk". If the `autoboot?` switch parameter is set to true (default), and the diagnostic switch parameter is set to true (not the default), Solaris is booted using the device alias "net".

To boot user-specified programs, you must be at the `ok` prompt. See *§ 3.15.4 On-Board Diagnostics* on page 3-44 for a detailed procedure on how to obtain the `ok` prompt.

Table 3-32. **Autoboot?, diag-switch?, and diag-device Settings**

autoboot?	diag-switch?	diag-device	Result
TRUE	TRUE	NET	Boot Solaris from network; run POST and memory tests
TRUE	FALSE	NET	Boot Solaris from network; no tests run
FALSE	TRUE	NET	ok prompt (Forth Toolkit); run POST and memory tests
FALSE	FALSE	NET	ok prompt (Forth Toolkit); no tests run
TRUE	TRUE	DISK	Boot Solaris from disk; run POST and memory tests
TRUE	FALSE	DISK	Boot Solaris from disk; no tests run
FALSE	TRUE	DISK	ok prompt (Forth Toolkit); run POST and memory tests
FALSE	FALSE	DISK	ok prompt (Forth Toolkit); no tests run

3.15.2 When to Use Diagnostics

You should use the appropriate diagnostic tool depending upon the circumstances. The table below provides a summary of the available diagnostic tools and indicates when each tool should be used.

Table 3-33. **Summary of Available Diagnostic Tools**

Diagnostic Tool	When or Why to Use Diagnostic Tool
Power On Self Test (POST)	The POST executes at power up when Stop (L1) -D keys are pressed or the diag-switch? parameter is set to true. POST tells you if the main logic board (MLB) or the MBus module in slot0 fails.
On-Board Diagnostics	The On-Board Diagnostics can test the ethernet ports and the diskette drive controller. You must be at the ok prompt to run On-Board Diagnostics.
Sundiag System Exerciser[a]	The Sundiag System Exerciser runs under Solaris. It displays real-time use of the system resources and peripherals. If the Sundiag System Exerciser fails, run the POST. See the *Sundiag User's Guide* for more information.
Forth Toolkit	The Forth Toolkit allows input to the system at the boot PROM level. It supports changing NVRAM parameters, resetting the system, running diagnostic tests, displaying system information, and redirecting input and output. See the *OpenBoot Command Reference* for more information.

a. Sundiag System Exerciser is not longer available beginning with Solaris 2.5.

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3.15.3 Power-On Self Test (POST)

The Power-On Self-Test (POST) runs when you turn on the system power switch and one of the following conditions apply:

- Press `Stop(L1)-D` keys
- The `diag-switch?` NVRAM parameter is set true
- The system Keyboard is disconnected

The POST code, which resides in the boot PROM, is executed when the POK (Power OK) signal is received from the power supply. The POST consists of a sequence of tests designed to test the major hardware components of the Main Logic Board (MLB) before Solaris is booted. POST does not perform extensive testing on any component of the MLB and only major failures can be detected by POST.

If a failure occurs in POST, a specific LED pattern is displayed. The LEDs are on the Compose, Scroll Lock, and Num Lock keys. The Caps Lock key LED, located just above the left-hand Shift key, is not used as a power-on test failure indicator, but flashes on and off while POST is running. During normal system operation, the LEDs should not be interpreted as diagnostic error indicators.

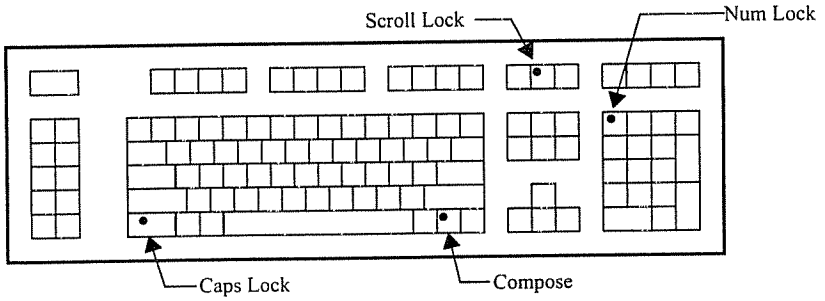


Figure 3-25. **Arrangement of the Keyboard LEDs**

Table 3-34. **Keyboard LED Status During POST**

Keyboard LED	Description of Status
CAPS LOCK is flashing	POST is running
NUM LOCK is ON	SPARC 20MP system failure
SCROLL LOCK is ON	MBus Module Slot0 failure
COMPOSE is ON	DSIMM failure (J201)

Following the successful system initialization, Solaris is booted automatically, unless the NVRAM configuration options specify not to do so.

3.15.4 On-Board Diagnostics

You have a access to a number of On-Board Diagnostics tests. To invoke these tests, you must enter the Forth Toolkit and have the `ok` prompt.

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Caution — In order to run On-Board Diagnostics, you must halt the system in an orderly manner. When the operating system or any other stand-alone program has already booted, do not use the `Stop (L1) - A` keys to halt the system. Abruptly aborting program execution may cause damage to data files.

To run On-Board diagnostics:

1. **Save all your work and quit all applications**
2. **With root permissions, halt the system by entering** `/usr/sbin/halt`
3. **Enter** `help diag` **to get a listing of tests comprising the On-Board Diagnostics**

The screen text below shows the screen output for steps 2 and 3 above.

```
hostname# /usr/sbin/halt

ok help diag

    Category:Diag(diagnostic routines)
test device-specifier ( -- ) run selftest method for specified device
    Example:
        test /iommu/sbus/ledma@f,400010/le- test net
        test net            - test net (device-specifier is an alias)
        test scsi           - test scsi (device-specifier is an alias)
        watch-clock         (--)    - show ticks of real-time clock
watch-net       (--)    - monitor broadcast packets using auto-selected interface
watch-aui       (--)    - monitor broadcast packets using AUI interface
watch-tpe       (--)    - monitor broadcast packet using TPE interface
watch-net-all   (--)    - monitor broadcast packets on all net interfaces
probe-scsi      (--)    - show attached SCSI devices
probe-scsi-all  (--)    - show attached SCSI devices for all host adapters
test-all        (--)    - execute test for all devices with selftest method
test-memory     (--)    - test all memory if diag-switch? is true, otherwise test
memory                    specified by selftest-#megs
```

3.15.4.1 Running On-Board Diagnostic Tests

- **test <device name> Command**

The Forth Toolkit test command, combined with a device alias or device pathname, will execute that device self-test program. If a device has no self-test program, this message will be displayed: `No self-test method for <device name>`. To run the self-test program for a device, type the test command followed by the device alias or device pathname. The following screen gives and example of a `test <device name>` command.

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```
ok test net

Testing net system.
Using AUI Ethernet interface.....succeeded
Internal loopback test.............succeeded
External loopback test.............succeeded

Using TP Ethernet Interface
Lance register test................succeeded
Internal loopback test.............succeeded
External loopback test.............succeeded
```

Table 3-35. **Supported On-Board Diagnostic Device Tests on the SPARC 20MP**

test screen	Tests the system video graphics hardware and monitor. The diag-switch? NVRAM parameter must be set true in order for the test to run.
test scsi	Tests the SCSI interface logic on the MLB. The diag-switch? NVRAM parameter must be set true in order for the test to run.
test net-aui	Performs an internal and external loopback test on the AUI Ethernet interface. A cable must be connected to the system AUI Ethernet port and to an ethernet tap or the test will fail the external loopback phase.
test net-tpe	Performs an internal and external loopback test on the 10Base-T Ethernet interface. A cable must be connected to the system 10Base-T Ethernet port and to a network hub or the test will fail the external loopback phase. If the tpe-link-test? parameter is false (disabled), the external loopback test will appear to pass even if a cable is not connected.
test net	Performs an internal and external loopback test on the auto-selected system Ethernet interface. A cable must be attached to the system and to an ethernet tap or network hub or the external loopback test will fail.
test disk / test disk0 test disk1 test disk2 test disk3	Tests internal or external SCSI disks which have a self diagnostic program contained in the drive controller. The drive must be spinning before this test is executed or the test will fail. Enter a boot <disk alias> command to cause the drive to spin up (disk / disk0 = SCSI ID 3, disk1 = SCSI ID 1, disk2 = SCSI ID 2, disk3 = SCSI ID 0).
test cdrom	Performs a self-test diagnostic on the CDROM drive. The CDROM must be set to SCSI ID 6 and have a CD inserted or the test will fail.
test tape / test tape0 test tape1	Tests the SCSI tape drive by executing the drive self-test program (tape / tape0 = SCSI ID 4, tape1 = SCSI ID 5).
test ttya test ttyb	This test outputs an alphanumeric test pattern on the system serial ports (ttya = Serial Port A, ttyb = Serial Port B). You must attach a terminal to the tested port to observe the output.
test keyboard	This test executes the keyboard self-test. The four LEDs on the keyboard should flash on once, and this message is displayed: Keyboard Present

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- **watch-clock Command**

The `watch-clock` test reads a register in the NVRAM/TOD chip on the SPARC 20MP and displays the result as a seconds counter. The counter should count from 0 to 59 repeatedly until you interrupt it by pressing any key on the keyboard. The following screen gives you an example of a `watch-clock` test.

```
ok watch-clock

Watching the 'seconds' register of the real-time clock chip.
It should be 'ticking' once a second.
Type any key to stop
41
```

- **watch-net, watch-aui, watch-tpe, and watch-net-all Commands**

These tests monitor broadcast ethernet packets on the ethernet cable(s) connected to the system. Good packets received by the system are indicated by a period (.) displayed on the screen. Errors are indicated with an X and the error description. The following screen gives you an example of a `watch-net` test.

```
ok watch-net
    Internal loopback test -- succeeded.
    External loopback test -- Auto-selecting Ethernet cable I/F
Trying AUI
Received packet on AUI
Select cable - AUI
succeeded.
Looking for Ethernet packets.
'.' is a good packet. "X" is a bad packet.
Type any key to stop.
................................................................................
........................................
.........Framing error CRC error X.........................
```

The 20MP system has two types of on-board ethernet interfaces, 10BaseT and AUI. Only one on-board interface may be connected at a time. The system can automatically detect which interface is connected and active. The AUI port is first tested by transmitting packet and checking for No Carrier or response packets. If the AUI test fails, the 10Base-T port is then tested. Typing `watch-net` causes this automatic selection to take place. You may see these messages:

```
ok watch-net

    Internal loopback test -- succeeded.
    External loopback test -- Auto-selecting Ethernet cable I/F
Trying AUI
AUI Carrier Loss
Trying TPE
Received packet on TPE
Select cable - TPE
succeeded
```


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You may also control the selection of ethernet interfaces to monitor by using specific commands. Use `watch-tpe` to monitor the 10BaseT connection or `watch-aui` to monitor the AUI connection.

The `watch-net-all` command monitors ethernet packets on any ethernet interface installed in the system. For example, if you have an SBus Ethernet module installed in one of the SBus slots, `watch-net-all` will start by monitoring ethernet transmissions detected by that module. When you interrupt the test on that interface by pressing any key, `watch-net-all` then goes on to test the next ethernet interface it finds in the system. The following screen shows an example of the `watch-net-all` test with multiple ethernet interfaces.

```
ok watch-net-all
/iommu@f,e0000000/sbus@f,e0001000/lebuffered@1,40000/le@1,60000
    Internal loopback test -- succeeded.
    External loopback test -- succeeded.
Looking for Ethernet packets.
'.' is a good packet. 'X' is a bad packet.
Type any key to stop.
................................................................................
.....(keyboard key pressed here)

/iommu@f,e0000000/sbus@f,e0001000/ledma@f1,400010/le@f,c00000
    Internal loopback test -- succeeded.
    External loopback test -- succeeded.
Looking for Ethernet packets.
'.' is a good packet. 'X' is a bad packet.
Type any key to stop.
................................................................................
........................................
```

- **probe-scsi and probe-scsi-all Commands**

The `probe-scsi` test sends an inquiry command to internal and external SCSI devices connected to the SPARC 20MP on-board SCSI interface. If a SCSI device is connected and powered up, the target address, unit number, device type, and manufacturer name should be displayed. For example:

```
ok probe-scsi
Target 3
    Unit 0 Disk SEAGATE ST1480 SUN04245828 Copyright(c) 1991 Seagate
```

The `probe-scsi-all` test sends an inquiry command to all SCSI devices on all the SCSI host adapters installed in the system. The first identifier listed in the display is the SCSI host adapter address in the system device tree, followed by the SCSI device identification data. For example:

```
ok probe-scsi-all
/iommu@f, e0000000/sbus@f, e0001000/dma@1, 81000/esp@1,80000
Target 2
    Unit 0 Disk SEAGATE ST41600N SUN1.3 G00286965 Copyright(c)1991
/iommu@f, e0000000/sbus@f, e0001000/espdma@f, 400000/esp@f, 800000
Target 3
    Unit 0 Disk SEAGATE ST1480 SUN04245828 Copyright(c) 1991 Seagate
```

:

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- **test-all Command**

The `test-all` command test all devices in the system which have a self-test program. The tests are executed in order using the device tree (viewed with the `show-devs` command) as reference. Disks, tapes, and CDROMs are not tested by the `test-all` command.

- **test-memory Command**

The `test-memory` command will test all of the SPARC 20MP main memory if the `diag-switch?` parameter is true. If the `diag-switch?` parameter is false, the `test-memory` test uses the `selftest-#megs` parameter in NVRAM to determine how much memory to test. The `selftest-#megs` default is 1, so only 1 megabyte of memory is tested. To change the amount of memory tested using the `selftest-#megs` parameter, enter the following command inserting any whole number as long as it does not exceed the actual size of memory (in megabytes) installed in the system.

```
ok setenv selftest-#megs 16
```

The above command sets the desired memory test size to 16 MB. When the `test-memory` diagnostic is running, the number of megabytes being tested is displayed and counted down to zero during the test.

3.15.5 Sundiag System Exerciser

Use the Sundiag System Exerciser, which runs under Solaris, to determine real-time use of system resources and peripheral equipment. The Sundiag System Exerciser verifies that the system is functioning properly. The Sundiag System Exerciser is shipped with Solaris 1.x. If it has been selected during the SunInstall (operating system loading) procedure, it can be run at any time. If the Sundiag System Exerciser is not found on the system hard disk or server, you can load it from the installation CD.

For information on how to use the Sundiag System Exerciser, see the *Sundiag User's Guide*. If Sundiag System Exerciser passes, the system is operating properly. If Sundiag System Exerciser fails, the error messages should indicate the part of the system which has failed. If the error messages are not descriptive enough, you may need to run the POST.

3.15.6 Forth Toolkit

The Forth Toolkit is a basic diagnostic utility and system interface. If there is any problem with your operating system, the Forth Toolkit automatically starts, indicated by the ok prompt. You can also choose to enter the Forth Toolkit by halting the system in the same manner as described in *§ 3.15.4 On-Board Diagnostics* on page 3-44. For extensive information on tests you can run from the Forth Toolkit see the *OpenBoot Command Reference*.

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4.1 Introduction

This chapter contains the programmer's model for SPARC 20MP. Detailed breakdowns of the following address spaces as well as descriptions of the register bits and functions can be found in the following sections. These address spaces include:

- SPARC Reference MMU addresses
- MBus control register addresses
- SBus/IOMMU Control register addresses
- Timer and Counter register address
- Interrupt register addresses
- Reset register address
- Memory register addresses
- I/O register addresses
- Hardware interrupt mapping

Note — Where a lowercase "n" is shown as part of an address, it signifies that there are multiple options for that particular address space.

4.2 MBus

ASI bits ASI[7:0] are interpreted by the MMUs on each MBus module. They are accessed using the SPARC instructions lda, sta, and swapa. These instructions can only be used in supervisor mode. No ASI information is available on the MBus. ASIs 0x8 - 0xB (user/supervisor instruction/data) are the only ones that cause the MMU to translate a virtual address to a MBus physical address.

MBus physical address bits PA [35:32] are used to define 16 different physical address spaces of 4GB each. Note that in a sense the four bits are acting as ASIs in defining separate Alternate Space Identifiers, but are not the same as the ASIs described above.

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Note that ASI = 0x20 to 0x2F is the SRMMU bypass mode; thus the second nibble of the ASI is used as MBus physical address bits PA[35:32] as shown in the ASIs listed here.

Table 4-1. **ASI Assignments**

ASI	Function
0x0	Reserved
0x1	Unassigned
0x2	Unassigned (system register)
0x3	Reference MMU flush/probe
0x4	Reference MMU register
0x5	Reference MMU diagnostic for instruction PDC (TLB)
0x6	Reference MMU diagnostic for data, or combined I&D PDC
0x7	Reference MMU diagnostic for I/O PDC (TLB)
0x8	User Instruction Space
0x9	Supervisor Instruction Space
0xA	User data space
0xB	Supervisor Data Space
0xC	Cache tag for instruction cache
0xD	Cache data for instruction cache
0xE	Cache tag for data cache or combined I&D cache
0xF	Cache data for data cache or combined I&D cache
0x10	Flush combined I&D cache line (page)
0x11	Flush combined I&D cache line (segment)
0x12	Flush combined I&D cache line (region)
0x13	Flush combined I&D cache line (context)
0x14	Flush combined I&D cache line (user)
0x15	Reserved
0x16	Reserved
0x17	Block-copy
0x18	Flush instruction cache line (page)
0x19	Flush instruction cache line (segment)
0x1A	Flush instruction cache line (region)
0x1B	Flush instruction cache line (context)
0x1C	Flush instruction cache line (user)
0x1D	Reserved
0x1E	Reserved
0x1F	Block-fill
0x20-0x2F	Reference MMU physical address by-pass mode

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Table 4-1. **ASI Assignments** (Continued)

ASI	Function
0x30	SuperSPARC Store Buffer Tags
0x31	SuperSPARC Store Buffer Data
0x32	SuperSPARC Store Buffer Controller
0x33	SuperSPARC Reserved
0x34	SuperSPARC Pre-fetch Buffer Tag
0x35	SuperSPARC Pre-fetch Buffer Data
0x36	SuperSPARC I-Cache Flash Clear
0x37	SuperSPARC D-Cache Flash Clear
0x38	SuperSPARC M-Unit Diags
0x39	SuperSPARC E-Unit Diags
0x3A-0x3F	SuperSPARC Reserved
0x40-0x7F	Unused
0x80-0xFF	Reserved

Table 4-2. **ASI Assignments - SRMMU Bypass Mode**

ASI	Function
0x20	EMC0's physical memory (DRAM)
0x21	Unused
0x22 - 0x27	Reserved
0x28	Unused
0x29	Unused
0x2A - 0x2D	Reserved
0x2E	SBus Space
0x2F	Control space (system control space, and memory control space)

Table 4-3. **SPARC Reference MMU Registers**

ASI	VA<31:0>	Register
0x4	0x000	Module Control Register
0x4	0x100	Context Table Pointer Register
0x4	0x200	Context Register
0x4	0x300	Synchronous Fault Status Register
0x4	0x400	Synchronous Fault Address
0x4	0x500	Asynchronous Fault Status Register
0x4	0x600	Asynchronous Fault Address Register
0x4	0x700	Reset Register

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Table 4-4. **MBus Control Register**

ASI	VA<35:0>	Register
0x2F	0xF E000 1000	MBus to SBus Synchronous Error FSR
0x2F	0xF E000 1004	MBus to SBus Asynchronous FAR
0x2F	0xF E000 1008	MBus Arbiter Enable Register
0x2F	0xF E000 100C	MBus Current Master Register

Table 4-5. **SBus and I/O MMU Control Register**

ASI	VA<35:0>	Register
0x2F	system dependent	IOMMU Page Table Entry
0x2F	system dependent	IOMMU TLB Tag
0x2F	0xF E000 100n	SBus Configuration Register
0x2F	0xF E000 0000	IOMMU Control Register
0x2F	0xF E000 0004	IOMMU Base Address Register
0x2F	0xF E000 0014	IOMMU Flush TLB Register
0x2F	0xF E000 0100	IOMMU Tags Diagnostics
0x2F	0xF E000 0200	IOMMU TLB Data Diag

Table 4-6. **Timer and Counter Register**

ASI	VA<35:0>	Register
0x2F	0xF F130 0000	Counter Register
0x2F	0xF F130 n004	Limit Register
0x2F	0xF F130 n008	Limit Register (no counter reset)
0x2F	0xF F130 n000	User Timer Register
0x2F	0xF F130 n00C	User Timer Start/Stop Register
0x2F	0xF F130 4000	System Counter Register
0x2F	0xF F130 4004	System Limit Register
0x2F	0xF F130 4008	System Limit Register (no counter reset)
0x2F	0xF F130 4010	System Timer Configuration Register

Table 4-7. **Interrupt Registers**

ASI	VA<35:0>	Register
0x2F	0xF F140 n000	Pending Interrupts Register
0x2F	0xF F140 n004	Clear Pending Interrupt Register
0x2F	0xF F140 n008	Set Interrupt Register
0x2F	0xF F141 0000	System Pending Interrupts Register
0x2F	0xF F141 0004	System Interrupt Target Mask Register

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Table 4-7. **Interrupt Registers** (Continued)

ASI	VA<35:0>	Register
0x2F	0xF F141 0008	System Interrupt Target Mask Clear Register
0x2F	0xF F141 000C	System Interrupt Target Mask Set Register
0x2F	0xF F141 0010	System Interrupt Target Register

Table 4-8. **Reset Register**

ASI	VA<35:0>	Register
0x2F	0xF FF10 0000	System Control/Status Register

Table 4-9. **Memory Registers**

ASI	VA<35:0>	Register
0x2F	0xF 0000 0000	Memory Enable Register
0x2F	0xF 0000 0008	Memory Fault Status Register
0x2F	0xF 0000 0010	Memory Fault Address Register 0
0x2F	0xF 0000 0014	Memory Fault Address Register 1
0x2F	0xF 0000 0018	Memory Diagnostics Register

Table 4-10. **I/O Address Space**

I/O Address Space	Device
0xE F040 0000 to 0xE F040 000C	DMA2 SCSI
0xE F040 0010 to 0xE F040 001C	DMA2 Ethernet
0xE F080 0000 to 0xE F080 003C	53C90
0xE F0C0 0000 to 0xE F0C0 0002	LANCE
0xE F100 0000 to 0xE F107 FFFF	Flash #1
0xE F200 0000 to 0xE F207 FFFF	Flash #2
0xE F480 0000 to 0xE F480 0018	Parallel Port
0xE F801 0000 to 0xE F801 0027	DBRI Controller
0xE FC00 0000 to 0xE FC00 0400	On Board I/O Registers
0xE FD00 0000 to 0xE FD00 01FF	SCV64 Registers
0xE FE00 0000 to 0xE FE00 000F	FPGA / EPLD Programming Registers
0xE FE00 0400	VME Reset Control Register
0xF F000 0000 to 0xF F007 FFFF	Flash #0 / EEPROM (Read Only)
0xF F100 0000 to 0xF F100 0006	Keyboard / Mouse
0xF F110 0000 to 0xF F110 0006	Serial Ports A/ B
0xF F120 0000 to 0xF F120 1FFF	TOD / NVRAM
0xF F150 0000 to 0xF F15F FFFF	Audio / ISDN

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Table 4-10. **I/O Address Space** (Continued)

I/O Address Space	Device
0xF F180 0000	System LED

4.3 VMEbus

The latest VMEbus specification, is the 64-bit address version, specified by VITA, the VMEbus Industry Trade Association, known as VME64-1994. The SPARC 20MP conforms to the VMEbus specifications, and supports 64-bit address (VME64 mode) and 64-bit MBLT block transfer of the VME64-1994 specification.

Under the VMEbus specification, different VME-compliant modules may be plugged into a compliant chassis and use the capabilities of the VMEbus to access the various resources provided by the modules and any attached peripherals.

A compliant VME system (chassis, power supply, rack, modules) provides a framework for multiprocessing and high bandwidth input/output. All boards installed on the VMEbus simply require a compliant logic interface to the VMEbus that supports the needs of the other modules in the system and any software native to the module itself. For example, if the module needs to read or write from/to another VME module, then it needs logic for a Master interface to the VMEbus. A basic list of VMEbus module features is:

- Supports byte, double byte, quad byte (32-bit) transfers with any alignment (the modules involved must support the desired transfer).
- Provides a block-transfer mechanism (BLT for 32-bit and MBLT for 64-bit data), with which the address overhead for large continuous transfers is reduced to a single address phase, followed by multiple data phases.
- Provides an efficient, centralized 4-level bus arbitration protocol with dedicated "physical layer" signaling. This is a mechanism by which any compliant module may obtain "ownership" of the VMEbus and perform "master" cycles on it, with respect to a "slave" board. That is, the Master performs a read or write cycle type with respect to a Slave or Slaves. The master and slave role is established each time the VMEbus is arbitrated. The arbitration protocol can be implemented as either fixed priority or round-robin, depending on the slot1 module, whose VME interface is responsible for activating the arbiter for the VMEbus.
- The board installed in slot1 (leftmost) is the "system controller", with special required functions:
  - system clock driver (16MHz)
  - power monitor
  - arbiter
  - IACK (interrupt acknowledge) daisy-chain driver
  - bus timer (for time-outs)
- The VMEbus data transfers are asynchronous, with the 16 MHz system clock driven by the slot1 module being not related to transfer rates over the bus.
- Provides seven interrupt levels, with an interrupt acknowledge daisy-chain (giving positional priority to multiple boards assigned to the same interrupt level).
- Provides support for a common "short address" (16-bit address) area where global input/output and mailbox interrupt spaces may be located.

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4.4 On-Board SPARC 20MP Registers

4.4.1 User LED Control Register

- **Address: 0xE F500 0000**
- **Access: Byte (Read / Write)**

Table 4-11. **LED Control Register Read Access**

Bit	Feature	Description
7	Diagnostic Flag #3	0 = LOW 1 = HIGH
6	Diagnostic Flag #2	0 = LOW 1 = HIGH
5	Diagnostic Flag #1	0 = LOW 1 = HIGH
4	Diagnostic Flag #0	0 = LOW 1 = HIGH
3	LED #3	0 = ON 1 = OFF
2	LED #2	0 = ON 1 = OFF
1	LED #1	0 = ON 1 = OFF
0	LED #0	0 = ON 1 = OFF

Table 4-12. **LED Control Register Write Access**

Bits 7:4	Bit 3	Bits 2:0	Feature	Bit 3 Description
XXXX XXXX	0 1	111 111	Diagnostic Flag #3	0 = LOW 1 = HIGH
XXXX XXXX	0 1	110 110	Diagnostic Flag #2	0 = LOW 1 = HIGH
XXXX XXXX	0 1	101 101	Diagnostic Flag #1	0 = LOW 1 = HIGH
XXXX XXXX	0 1	100 100	Diagnostic Flag #0	0 = LOW 1 = HIGH
XXXX XXXX	0 1	011 011	LED #3	0 = ON 1 = OFF
XXXX XXXX	0 1	010 010	LED #2	0 = ON 1 = OFF
XXXX XXXX	0 1	001 001	LED #1	0 = ON 1 = OFF

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Table 4-12. **LED Control Register Write Access** (Continued)

Bits 7:4	Bit 3	Bits 2:0	Feature	Bit 3 Description
XXXX[a] XXXX	0 1	000 000	LED #0	0 = ON 1 = OFF

a. "X" indicates "Don't Care" value

4.4.2 Switch Status Register

- **Address: 0xE F500 0010**
- **Access: Byte (Read Only)**

Table 4-13. **Switch Status Register Read Access**

Bit	Feature	Description
7	Serial Port B RS232 / RS422 Enable	0 = RS232 1 = RS422
6:5	SCSI Termination Status	00 = Auto Sensing Enabled 10 = Termination Enabled X1[a] = Termination Disabled
4	User Defined	0 = SW704-3 is in the ON position 1 = SW704-3 is in the OFF position
3	User Defined	0 = SW704-4 is in the ON position 1 = SW704-4 is in the OFF position
2	VMEbus Reset	0 = Front Panel Reset Switch does not reset the VMEbus 1 = Front Panel Reset Switch resets the VMEbus
1	Keyboard / Mouse or Serial Ports C/D Enable	0 = Keyboard / Mouse 1 = Serial Ports C/D
0	Flash#0 Protection	0 = Not Write Protected 1 = Write Protected

a. "X" indicates "Don't Care" value

4.4.3 Rotary Switch Status Register

- **Address: 0xE F500 0020**
- **Access: Byte (Read Only)**

Only bits 3:0 are meaningful. They indicate the 2's complement encoded value of the rotary switch setting.

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Table 4-14. **Rotary Switch Status Register Settings**

Rotary Switch Setting	Register Value	Rotary Switch Setting	Register Value
0	F	8	7
1	E	9	6
2	D	A	5
3	C	B	4
4	B	C	3
5	A	D	2
6	9	E	1
7	8	F	0

4.4.4 Miscellaneous Control Register

- **Address: 0xE F500 0030**
- **Access: Byte (Read / Write)**

Table 4-15. **Miscellaneous Control Register Read Access**

Bit	Feature	Description
7:4	Reserved	
3	NVRAM Protection (Read Only)	0 = Not Write Protected 1 = Write Protected
2	MVSIC Daughterboard Installed (Read Only)	0 = Not Installed 1 = Installed
1	Reserved	
0	Serial Port B	0 = Loopback Mode 1 = Normal Mode

Table 4-16. **Miscellaneous Control Register Write Access**

Bits 7:4	Bit 3	Bits 2:0	Feature	Bit 3 Description
XXXX[a]	0	000	Serial Port B	0 = Loopback Mode
XXXX	1	000		1 = Normal Mode

a. "X" indicates "Don't Care" value

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4.4.5 IACK Registers

Table 4-17. **IACK Registers Base Addresses**

Base Address	IACK Register
0xE FF00 0403	SCVISR
0xE FF00 0007	SCVIACK1
0xE FF00 000B	SCVIACK2
0xE FF00 000F	SCVIACK3
0xE FF00 0013	SCVIACK4
0xE FF00 0017	SCVIACK5
0xE FF00 001B	SCVIACK6
0xE FF00 001F	SCVIACK7

The SVC64 signals an interrupt occurred on the VME or locally by asserted a code on its IPL lines. This code is decoded by hardware to generate an interrupt on the SBus. The decoded value can be accessed through the SCVISR (SCV64 IPL status register). There is no latching mechanism implemented on MVSIC.

When the CPU gets an interrupt (from the SEC chip), it will look at the SEC internal register to determine the source of the interrupt. If the interrupt is generated on the SBus, the CPU needs to poll every interrupt status register to find out which SBus device is interrupting. This is the purpose of the SCVISR register to provide such information. Because there is no latching capability in the H/W implementation it is necessary to be very cautious when deciding if an interrupt is pending in the SCV64/VME.

Also, because the interrupt can be sourced locally or on the VME, it is necessary to clear all local interrupt sources before initiating a VME interrupt acknowledge cycle.

VME interrupt acknowledge cycles are initiated by reading the SCVIACK registers. An interrupt acknowledge cycle on VME will be generated if:

- There is no local interrupt in the SCV64 pending on the same level
- The user initiates a byte read access at the location:
  - 0xE FF00 0003 + 4 * i (i is the level number)

All interrupt sources are maskable through the SCV64's registers.

4.5 MVSIC Registers

The MVSIC Registers are used for controlling the VMEbus access. There are several registers which are located within MVSIC: SCV64 which controls DMA access, PIO logic which controls Programmed Input/ Output, and Slave access.

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4.5.1 SCV64 Registers

The base address of these SCV64 registers is: 0xE FD00 0000

The VME interface implemented on the MVSIC uses some of the SCV64 resources. The following functions are currently used in the SCV64:

- System controller:
  - Arbiter
  - VME bus time-out
  - VME SysReset
- DMA engine
- Interrupter
- Interrupt Handler
- IACK daisy chain driver
- VME Sysfail

Other functions are implemented by additional extra and complex logic.

- Master VME access (Read/Write)
- Slave VME interface

The SCV64 is only used for DMA transfers, location monitor, interrupt handler, interrupter and system controller functions (Arbitration, Reset, VME bus time-out). Therefore, ALL slave pages in the APR registers should be disabled. The A24 and A32 slave windows must be disabled. The A64 slave mode should not be programmed.

4.5.2 VME Registers

4.5.2.1 VME Slave Base Address Register

– **Address: 0xE FC00 0000 and 0xE FC00 0001**

Table 4-18. **VME Slave Base Address Register**

Address / Bits	Function
0xE FC00 0001 (bits 3:0)	VME base address (31:28)[a]
0xE FC00 0000 (bits 7:0)	VME base address (27:20)[a]

a. These bits are used for A24 and A32 slave accesses. The significant bits depend on the slave window size programmed into registers 0xE.FC00.0006 (see *§ 4.5.2 VME Registers* on page 4-11). **A24 Slave Window Size Significant Bits** - 1 MB (bits 23:20), 2 MB (bits 23:21), 4 MB (bits 23:22); **A32 Slave Window Size Significant Bits** - 4MB (bits 31:22), 8MB (bits 31:23), 16MB (bits 31:24), 32 MB (bits 31:25), 64 MB (bits 31:26), 128 MB (bits 31:27).

25 NOT 24

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4.5.2.2 VME A24 DVMA Slave Address Register

– **Address: 0xE FC00 0002 and 0xE FC00 0003 (lower nibble)**

The number of meaningful bits depends on the A24 slave window size. For 1Mbyte A24 slave windows all bits will be used to generate the SBus DVMA address on A24 VME slave access. For 2Mbyte A24 slave window, only bits (7:1) are used to generate the local DVMA address. For a 4Mbyte A24 slave window, only bits(7:2) are used to generate the local DVMA address. Lower DVMA address bits are the corresponding VMEbus address bits. The top four DVMA A24VA(31:28) are provided by the register at 0xE FC00 0003 bits (3:0).

Table 4-19. **VME A24 Slave Address Bit Definitions**

Address / Bits	Feature	Description
0xE FC00 0002 (bits 7:0)	A24 Virtual Address Bits	A24 Virtual Address (27:20)
0xE FC00 0003 (bits 3:0)	A24 Virtual Address Bits	A24 Virtual Address (31:28)

4.5.2.3 VME Interface Design Revision Register

– **Address: 0xE FC00 0003 (upper nibble)**

Table 4-20. **VME Interface Design Revision Register Bit Definitions**

Bit	Feature	Description
7:4	Current Hardware Design Revision (Set by the microswitches installed on the MVSIC Daughterboard)	0xF = Temporary Revision 0x0 = Reserved All other values return Hardware Revision

4.5.2.4 VME A32 DVMA Slave Address Register

– **Address: 0xE FC00 0004**

The number of meaningful bits depends on the A32 slave window size. For 32Mbyte A32 slave window all bits will be used to generate the SBus DVMA address on A32 VME slave access. For 64Mbyte A32 slave window, only bits (7:2) are used to generate the local DVMA address. For 128Mbyte A32 slave window, only bits (7:3) are used to generate the local DVMA address. The lower DVMA address bits are the corresponding VMEbus address bits.

Table 4-21. **VME A32 DVMA Slave Address Bit Definitions**

Bit	Feature	Description
7:1	A32 Virtual Address Bits	A32 Virtual Address (31:25)
0	Reserved	

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4.5.2.5 VME DVMA DMA Base Address Register

– **Address: 0xE FC00 0005**

Lower DVMA address bits come straight from the SVC64 DMALAR register. The DMA status bit has to be checked at the end of each DMA transfer to make sure no error during VME to SPARC 20MP transfer has happened on the SBus side after all data has been transferred from the SCV64 into the external receive file.

Table 4-22. **VME DVMA DMA Base Address Bit Definitions**

Bit	Feature	Description
7:3	SCV64 DMA Virtual Address Bits	SCV Virtual Address (31:27)
2	Reserved	
1	DMA Error Status	0 = No DMA error has occured 1 = DMA error has occured
0	Reserved	

4.5.2.6 VME A32 Slave Address Register

– **Address: 0xE FC00 0006**

Table 4-23. **VME A32 Slave Address Bit Definitions**

Bit	Feature	Description
7	Reserved	
6	A24 Slave Status	0 = Disabled 1 = Enabled
5:4	A24 Slave Window Size	00 = 1 MB 01 = 2 MB 10 = (Not Used) 11 = 4 MB
3	A32 Slave Status	0 = Disabled 1 = Enabled
2:0	A32 Slave Window Size	000 = 4 MB 001 = 8 MB 010 = (Not Used) 011 = 16 MB 100 = 32 MB 101 = 64 MB 110 = (Not Used) 111 = 128 MB

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4.5.2.7 VME PIO Control Register

– **Address: 0xE FC00 0007**

Table 4-24. **VME PIO Control Register Bit Definitions**

Bit	Feature	Description
7	VME SYSRESET status on the VMEbus (Read Only)	0 = Asserted 1 = Not Asserted
6	VME Busy Signal Generated by the MVSIC (Read Only)	0 = Not Asserted 1 = Asserted
5:4	VMEbus Request Level for PIO Access	00 = VMEbus Request 0 01 = VMEbus Request 1 10 = VMEbus Request 2 11 = VMEbus Request 3
3	Reserved	
2	VMEbus Ownership Control (This bit is used to oblige the VMEbus requester to get the VMEbus ownership without initiating a transfer and for as long as this bit remains asserted.)	0 = Normal Mode 1 = Force VMEbus Ownership
1	Release Mode	0 = Release When Done 1 = Release On Request
0	Requester Mode	0 = Unconditional Mode 1 = Fair Mode

4.5.2.8 DMA / Slave External FIFOs Status Register

– **Address: 0xE FC00 0400**

Between the SBus and the KBus, two FIFOs have been implemented to boost the data transfer during DMA. The two other FIFOs have been implemented between the VME and the SBus to boost VME slave transfer. This register returns the status of those four FIFOs. When a DMA transfer is done, this register should be checked out for consistency. For slave, this register is used more specifically for troubleshooting purpose.

Table 4-25. **DMA / Slave External FIFOs Status Register Bit Definitions**

Bit	Feature	Function
7	Slave RxFIFO Empty	0 = Empty 1 = Not Empty
6	Slave RxFIFO Almost empty / Almost full	
5	Slave TxFIFO Empty	0 = Empty 1 = Not Empty
4	Slave TxFIFO Almost empty / Almost full	
3	DMA RxFIFO Empty	0 = Empty 1 = Not Empty
2	DMA RxFIFO Almost empty / Almost full	
1	DMA TxFIFO Empty	0 = Empty 1 = Not Empty

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Table 4-25. **DMA / Slave External FIFOs Status Register Bit Definitions** (Continued)

Bit	Feature	Function
0	DMA TxFIFO Almost empty / Almost full	

4.5.2.9 VME Reset Control Register

-- **Address: 0xE FE00 0400**

Table 4-26. **VME Reset Control Register Bit Definitions**

Bit	Feature	Description
7:4	Hardware Design Rev of the PAL Sbus_dec	
3	VMEbus sysreset Receive Status (Read Only) (If JP1001 is installed this bit will always read 0)	0 = SPARC 20MP will not be reset by VMEbus sysreset signal 1= SPARC 20MP will be reset by VMEbus sysreset signal
2[a]	VMEbus sysreset Control (This bit is not affected by System Controller Status)	0 = Do Not Assert VMEbus sysreset 1 = Assert VMEbus sysreset
1	VMEbus sysreset Receive Mask (If JP1001 is installed writing a 0 to this bit will have no effect)	0 = SPARC 20MP will be reset by VMEbus sysreset signal 1 = SPARC 20MP will not be reset by VMEbus sysreset signal
0	Reserved	

a. This bit is not self clearing. The VMEbus SYSRESET will be asserted until this bit is cleared.

4.6 Address Maps

The 20MP address maps consist of the Sbus and Mbus mapping as described further below.

4.6.1 MBus Global Address Map

The MBus is a physical address bus with sixteen 4 Gigabytes address spaces: PA [35:00]. *Table 4-27* shown below indicates the assignment of the 16 MBus address spaces.

Table 4-27. **Mbus Address Spaces**

Address Space	Address Range	Function
#0	0x0 0000 0000 to 0x0 FFFF FFFF	Main memory
#1	0x1 0000 0000 to 0x1 FFFF FFFF	Not assigned
#2	0x2 0000 0000 to 0x2 FFFF FFFF	Not assigned

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Table 4-27. **Mbus Address Spaces** (Continued)

Address Space	Address Range	Function
#3	0x3 0000 0000 to 0x3 FFFF FFFF	Not assigned
#4	0x4 0000 0000 to 0x4 FFFF FFFF	Not assigned
#5	0x5 0000 0000 to 0x5 FFFF FFFF	Not assigned
#6	0x6 0000 0000 to 0x6 FFFF FFFF	VME master D32
#7	0x7 0000 0000 to 0x7 FFFF FFFF	VME master D16
#8	0x8 0000 0000 to 0x8 FFFF FFFF	Not assigned
#9	0x9 0000 0000 to 0x9 FFFF FFFF	Not assigned
#A	0xA 0000 0000 to 0xA FFFF FFFF	Not assigned
#B	0xB 0000 0000 to 0xB FFFF FFFF	Not assigned
#C	0xC 0000 0000 to 0xC FFFF FFFF	Not assigned
#D	0xD 0000 0000 to 0xD FFFF FFFF	Not assigned
#E	0xE 0000 0000 t0 0xE FFFF FFFF	Sbus space
#F	0xF 0000 0000 to 0xF FFFF FFFF	Control space

4.6.2 MBus Main Memory

The memory data path is 144-bit wide (16 bytes + 16ECC bits). Using 1Mx4 memory components, 36 1Mx4 chips is 16MB and 36 4Mx4 chips is 64MB.

The EMC memory controller allows up to 512MB, 64MB per RAS line. It is responsible to respond to that MBus address range.

Table 4-28. **Main Memory Physical Address Locations**

Address Range	Function	Size
0x0 0000 0000 to 0x0 003F FFFF	Memory bank #0	64 MB
0x0 0040 0000 to 0x0 007F FFFF	Memory bank #1	64 MB
0x0 0080 0000 to 0x0 00BF FFFF	Memory bank #2	64 MB
0x0 00C0 0000 to 0x0 00FF FFFF	Memory bank #3	64 MB
0x0 0100 0000 to 0x0 013F FFFF	Memory bank #4	64 MB
0x0 0140 0000 to 0x0 017F FFFF	Memory bank #5	64 MB
0x0 0180 0000 to 0x0 01BF FFFF	Memory bank #6	64 MB
0x0 01C0 0000 to 0x0 01FF FFFF	Memory bank #7	64 MB
0x0 0200 0000 to 0x0 FFFF FFFF	Not assigned	

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4.6.3 Flash Memories

There are three 512KB Flash memories on the board. One is the boot device and the two others are for general purpose data storage. The boot device can be read at two different address spaces. The first address space (0xF F000 0000) is a read-only space and is used for fetching the boot code. The second address space (0xF F128 0000) is a read/write space used for the programming of the boot device if the boot device is a flash-device. The last two devices are located in SBus space slot #F.

- Flash #1 - 0xE F100 0000 ------ 0xE F107 FFFF
- Flash #2 - 0xE F200 0000 ------ 0xE F207 FFFF

The Flash device is a 29F040 from AMD. The programming algorithm is explained in the relevant AMD Flash data book.

4.6.4 FPGA / EPLD Programming

There are three registers used to download Programmable Logic devices implemented on the VMEbus interface.

- **Clock Register: 0xE FE00 0003**

Only bit D0 is used to toggle the clock input of the EPLD Atmel AT6002 or Altera EPF8282.

- 0 = Force the clock signal to low
- 1 = Force the clock signal to high

- **EPLD select: 0xE FE00 0007**

On write access, it is a one-bit exclusively register. If you set bit 1, you select the ATMEL parts for programming. By clearing bit 1 you deselect the ATMEL devices from the programming phase. If you set bit 6, you select the ALTERA part for programming. By clearing bit 6 you deselect the ALTERA device from the programming phase. On read access, you can determine which device has been selected.

Table 4-29. **FPGA / EPLD Programming**

Bit	Feature	Function
7	Reserved	
6	Altera Select Status	0 = Devices are not selected 1 = Devices are selected
5:2	Reserved	
1	Atmel Select Status	0 = Devices are not selected 1 = Devices are selected
0	Reserved	

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– **EPLD Status / Control: 0xE FE00 000B**

This register is used to control and get the status of the parts currently under programming. The procedure to download the code will be detailed later. The EPLD/FPGA code might be loaded into the OBP Prom to be able to download the EPLD/FPGA code automatically on Power up reset.

Table 4-30. **EPLD Status Control Register**

Bit	Function
7:5	Reserved
4	Atmel Mode (Forced to 1)
3	Altera CONF_DONE
2	Altera status
1	Atmel Data 0
0	Atmel status signal

4.6.5 MBus Control Space

– **Address: 0xF 0000 0000 - 0xF FFFF FFFF**

The MBus control space is divided into sixteen 16MB addressing spaces.

Table 4-31. **MBus Control Space Address Ranges**

Address Range	Function
0xF 0000 0000 to 0xF 0FFF FFFF	Memory Control Space
0xF 1000 0000 to 0xF DFFF FFFF	Not Assigned
0xF E000 0000 to 0xF EFFF FFFF	SBus Control Space
0xF F000 0000 to 0xF FFFF FFFF	System Control Space

4.6.6 MBus VME Space Address

These two 4GB pages on the MBus address space are allocated to PIO transaction (or Master VME access initiated by any MBus Master). The first page (#6) is dedicated to D32 VME devices and the second page (#7) is assigned to D16 VME targets. The hardware supports the dynamic bus sizing. In other words, the hardware master VME interface takes care of splitting the transactions in as many accesses as required by the transfer size and the VME port size. If the CPU tries a 32-bit or 64-bit access to a D16 device on the VME, two or four back-to-back 16-bit transfers will run on the VME. If the CPU tries a 64-bit access to a D32 device on the VME, two back-to-back 32-bit transfers will run on the VME.

All of that is done without any software intervention. The software does not have to worry about the VME port size when initiating a VME transaction. For performance reasons, it is important to implement CPU-initiated D64 transfers. The VME master interface supports the following VME addressing modes:

– A16

– A24

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– A32

Each of the 4Gbyte pages has been hard-mapped to let the CPU trigger these addressing modes:

– 6 0000 0000 ----> 6 FEFF FFFF A32:D32

– 6 FF00 0000 ----> 6 FFFE FFFF A24:D32

– 6 FFFF 0000 ----> 6 FFFF FFFF A16:D32

– 7 0000 0000 ----> 7 FEFF FFFF A32:D16

– 7 FF00 0000 ----> 7 FFFE FFFF A24:D16

– 7 FFFF 0000 ----> 7 FFFF FFFF A16:D16

Therefore, the last 16Mbyte of the 4Gbyte A32 address space is reserved for A24 and A16 address space. Also, the last 64KB of the 16Mbyte A24 address space is reserved for A16 address space. The master VME interface supports lock transactions using the Load and Store or the Swap instructions. All programmed I/O transfers run directly form the MBus to the VMEbus. The master VMEbus interface supports multiprocessing configurations. That is to say that VMEbus accesses from two different CPUs will be interleaved on the VMEbus. This is fully transparent to the software.

In case of long latency time on the VMEbus, the MBus master is rerun by forcing a retry and relinquish acknowledge. This will immediately re-initialize the MBus time-out counter (desertion of MBB). Therefore, a PIO transaction on the VMEbus cannot time-out on the MBus. The completion of the transfer will be done by an acknowledgment generated on the VME.

4.6.7 SBus Space

– **Address: 0xE 0000.0000 to 0xE FFFF FFFF**

This MBus address space is dedicated to address SBus devices located on up to 5 different 256MB SBus slots as per the MSI, MBus/SBus bridge interface chip. SBus slots are numbered from 0 to F. On-board SBus resources are located on slot F. Four expansion SBus slots are available: slot 0 to 3.

Table 4-32. **SBus Slot Address Ranges**

Address Range	Function
0xE 0000 0000 to 0xE 0FFF FFFF	SBus Slot #0
0xE 1000 0000 to 0xE 1FFF FFFF	SBus Slot #1
0xE 2000 0000 to 0xE 2FFF FFFF	SBus Slot #2
0xE 3000 0000 to 0xE 3FFF FFFF	SBus Slot #3
0xE 4000 0000 to 0xE EFFF FFFF	Not assigned
0xE F000 0000 to 0xE FFFF FFFF	On-board Devices (Ethernet, SCSI, Parallel Port)

4.6.8 SBus On-board Devices

– **Address: 0xE F000 0000 - 0xE FFFF FFFF**

On-board peripherals include all devices and/or registers controlled by the SEC, MACIO and DBRI through the MSI chip.

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- The last SBus space (0xE Fxxx xxxx) is split to allow access to:
  - the VME interface controller (SCV64)
  - the VME IACK registers (IACK)
  - the DBRI controller (CHI interface) (DBRI)

Therefore the global assignment of the 256MB address is given below:

Table 4-33. **Assignment of the 256MB address**

Address	Device	Function
0xE F0xx xxxx	MACIO	Ethernet and SCSI
0xE F1xx xxxx	Flash #1	29F040
0xE F2xx xxxx	Flash #2	29F040
0xE F3xx xxxx	N/A	
0xE F4xx xxxx	MACIO	Parallel port
0xE F5xx xxxx	On-Board I/O	User LED, Rotary Switch, etc.
0xE F6xx xxxx	N/A	
0xE F7xx xxxx	N/A	
0xE F8xx xxxx	DBRI	Audio Multimedia
0xE F9xx xxxx	N/A	
0xE FAxx xxxx	N/A	
0xE FBxx xxxx	N/A	
0xE FCxx xxxx	VME I/F	VME PIO and Slave I/F control
0xE FDxx xxxx	SCV64	DMA, Arbitrater, Interrupt, etc,
0xE FExx xxxx	On Board Configuration	FPGA / EPLD Programming and VME Reset Control
0xE FFxx xxxx	IACK	

The address map of each device determines the details of their register implementation.

4.7 Controllers

The SPARC 20MP controllers consist of the MACIO, and DBRI controllers. A full description and identification register are explained below.

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4.7.1 MACIO Controller

The MACIO integrates high performance I/O macrocells and logic including a 7990-compatible Ethernet controller core, a fast 8-bit SCSI core, a high-speed parallel port, a DMA2 controller and an SBus interface. Only two 16MB pages are used partially by the MACIO.

Table 4-34. **MACIO Controller**

Address	Function	Description
0xE F000 0000	DMA2	ID Register
0xE F040 0000 to 0xE F040 000C	DMA2	SCSI
0xE F040 0000		Control/Status Register
0xE F040 0004		Address Register
0xE F040 0008		Byte Count Register
0xE F040 000C		Test Control / Status
0xE F040 0010 to 0xE F040 001C	DMA2	Ethernet
0xE F040 0010		Control / Status Register
0xE F040 0014		Test Control / Status
0xE F040 0018		Cache Valid Bits Register
0xE F040 001C		Base Address Register
0xE F080 0000 to 0xE F080 003C	NCR	53C90
0xE F080 0000		Transfer Count Low (7:0)
0xE F080 0004		Transfer Count Middle (15:8)
0xE F080 0008		FIFO Data
0xE F080 000C		Command
0xE F080 0010		Status/Select-Reselect Bus ID
0xE F080 0014		Interrupt/Select-Reselect Time-out
0xE F080 0018		Sequence Step/Synchronous transfer period
0xE F080 001C		FIFO flags/Synchronous offset
0xE F080 0020		Configuration #1
0xE F080 0024		Clock Conversion Factor
0xE F080 0028		Test (chip test use only)
0xE F080 002C		Configuration #2
0xE F080 0030		Configuration #3
0xE F080 0038		Transfer Count High (23:16)
0xE F0C0 0000 to 0xE F0C0 0002	AMD	7990 LANCE
0xE F0C0 0000		Register Data Port (RDP)
0xE F0C0 0002		Register Address Port (RAP)
0xE F480 0000 to 0xE F480 .0018	Parallel	PORT

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Table 4-34. **MACIO Controller** (Continued)

Address	Function	Description
0xE F480 0000		P-Port DMA Control/Status Register (P_CSR)
0xE F480 0004		P-Port Address Register (P_ADDR)
0xE F480 0008		P-Port Byte Count Register (P_BCNT)
0xE F480 000C		P-Port Test Control/Status Register (P_TST_CSR)
0xE F480 0010		P-Port Hardware Configuration Register (P_HCR)
0xE F480 0012		P-Port Operation Configuration Register (P_OCR)
0xE F480 0014		P-Port Parallel Data Register (P_DR)
0xE F480 0015		P-Port Transfer Control Register (P_TCR)
0xE F480 0016		P-Port Output Register (P_OR)
0xE F480 0017		P-Port Input Register (P_IR)
0xE F480 0018		P-Port Interrupt Control Register (P_ICR)

4.7.2 DBRI Controller

– Address: 0xE F801 0000 to 0xE F801 0024

Table 4-35. **DBRI Controller**

Address	Description
0xE F801 0000	REG0 Control / Status Register
0xE F801 0004	REG1 Mode and Interrupt Register
0xE F801 0008	REG2 Parallel I/O Register
0xE F801 000C	REG3 Test Mode Register
0xE F801 0020	REG8 Program Counter
0xE F801 0024	REG9 Interrupt Queue Pointer

4.8 VME Transfers

Transfer of the VMEbus can be one of the following types:

- PIO transfer
- VME slave transfer
- VME DMA transfer

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4.8.1 PIO Transfer

The PIO transfer is initiated by the on-board MBus master. The transfer is generated from the MBus to the VMEbus through a customized VME master interface. There is no bus cross-over involved during these transactions. The interface is designed in such a way that word concatenation is done transparently to the software. That means that a 32-bit access to a D16 device will be split into two back-to-back transaction on the VME. This also applies to 64-bit MBus data transfers to either D16 or D32 devices. There is no posted access. All transactions are atomic.

Long latency time on the VMEbus will not impact the MBus throughout as a MBus rerun counter is built-in to the master VMEbus interface in order to force the currently waiting MBus master to retry and relinquish the MBus. Also, two different masters can initiate transactions with no risk of mis-acknowledgment the rerun feature may cause. In other words, the processor ID is latched before issuing a retry and relinquish acknowledgment. During the VME master access the data transfer time-out is monitored by the VMEbus controller or the VME target if the target has a local time-out shorter than the VMEbus time-out.

4.8.2 VME Slave Transfer

Slave VME transfers pass through the SBus to become a DVMA transaction. The lowest part of the virtual address is generated from the VMEbus address and the highest part of that address is programmable. The number of bits in the lowest section is function of the slave window size. The upper bits are filled up from the programmable registers.

4.8.3 VME DMA Transfer

Those transactions are controlled by the SCV64 interface controller. In order to speed up the data transfer, a fifo has been implemented. The transfers pass through the SBus, therefore the virtual address generation is required. The lower bits (0 to 26) are fully programmable in the SCV64. The remaining bits are set to "1".

Note — The DMA transfer requires address alignment at 128 byte boundary and does not support D16 access.

4.8.4 Mail Box

Mailboxes are handled by the SCV64. Therefore, a small slave VME image (4K) in the A32 space should be programmed for that purpose. The SCV64 uses the upper 4 bits of the A32 slave image for the Location Monitor mailboxes. This A32 slave image should be protected from access by configuring the SCV64 Access Protect Boundry Register (APBR) to prevent slave access from the SCV64 interface. See the SCV64 documentation for more details on using the Location Monitor for VMEbus mailboxes.

4.8.5 OBP Environment Variables

To control the VMEbus related system settings, a number of environmental variables have been added to the Sun OpenBoot PROM (OBP).

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Table 4-36. **SPARC 20MP OBP Environment Variables**

Variable	Default	Descriptions
enable-a24-slave-access	true	Enable VME A24 slave access
enable-a32-slave-access	true	Enable VME A32 slave access
vme24-slave-window-size	100000(hex)	VME A24 slave window size, valid values are: 0x100000 0x200000 0x400000
vme32-slave-window-size	2000000(hex)	VME A32 slave window size, valid values are: 0x0200 0000 0x0400 0000 0x0800 0000
vme24-slave-base	0	Set VME slave base address in A24 mode.
vme32-slave-base	0	Set VME slave base address in A32 mode.
vme-bus-mode	round-robin	Set VMEbus arbitration mode, valid modes are: round-robin, priority, priority3, priority32.

These variables can be set / changed at either the ok OBP prompt using `setenv variable_name value`, or at the Solaris eeprom command using `eeprom variable_name=value`.

Note — In order for a new value to take effect, a board RESET is required

4.8.6 OBP VME and Support Commands

The SPARC 20MP has implemented a few forth commands for customers to program and/or display registers and VMEbus setup under Sun OBP. They are described below with the forth stack diagram enclosed in parenthesis.

*.hw-version (--)

- display current hardware's revision number.
  - example: ok .hw-version

*show-scv64-regs (--)

- display the register contents of the Newbridge SCV64 chips.
  - example: ok show-scv64-regs

*get-scv64-bus-req-mode (-- val)

- get scv64 bus request mode, 0 for fair mode and 1 for demand mode.

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– example: ok get-scv64-bus-req-mode

*set-scv64-bus-req-mode (mode --)

- set SCV64 bus request mode, 0 for fair mode and 1 for demand mode.
  – example: ok 0 set-scv64-bus-req-mode

*get-scv64-bus-req-level (-- val)

- get SCV64 bus request level.
  – example: ok get-scv64-bus-req-level

*set-scv64-bus-req-level (level --)

- set SCV64 bus request level, valid levels are 0, 1, 2, 3.
  – example: ok 2 set-scv64-bus-req-level

*get-pio-bus-req-mode (-- val)

- get bus request mode for VME master access, 0 for unconditional mode and 1 for fair mode.
  – example: ok set-pio-bus-req-mode

*get-pio-bus-req-level (-- val)

- get bus request level for VME master access.
  – example: ok get-pio-bus-req-level

*set-pio-bus-req-level (level --)

- set bus request level for VME master access. Valid levels are 0, 1, 2, and 3.
  – example: ok # set-pio-bus-req-level

*vme-int-mask (level --)

- disable a vme interrupt at level <#>. Valid levels are 1 - 7.
  – example: ok # vme-int-mask

*vme-int-unmask (level --)

- enable a vme interrupt at level <#>. Valid levels are 1 - 7.
  – example: ok # vme-int-unmask

4.8.7 Flash Update



Caution — GREAT CARE must be taken when you perform the flash-update. If an invalid or corrupted prom file was downloaded, or you experienced a power outage during flash-update, the SPARC 20MP board may NOT be bootable. DO NOT interrupt the command while it's in progress.

Themis Computer has implemented a new OBP command to update the OBP PROM. This command allows you to update flash prom through the ethernet.

– *flash-update filename (--)

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The following steps will load the OBP:

1. Load the prom supplied by Themis Computer to a FTP Server and enter it into its corresponding directory.
2. Configure the SPARC 20MP to be a client FTP server.
3. Enter the command `ok flash-update (prom name)`.

4.9 Overview of VME Interface Under Solaris 1.1.x / 2.x

Great effort has been taken to achieve complete compatibility between Sun VME implementation and the SPARC 20MP under Solaris. The VMEbus interface of the SPARC 20MP is transparently implemented under Solaris 1.1.x and Solaris 2.x. The software interface is fully compatible with generic Sun4m VME architecture. Any VME device driver that conforms to the appropriate Solaris Device Driver Interface will run unmodified on the Themis Computer platforms.

Themis Computer has developed a number of sample device drivers to provide the necessary software interface needed by system programmers. These drivers can be classified into three categories:

- VMEbus Nexus drivers
- Utility drivers
- Sample drivers

Themis Computer also provides detailed on-line manual pages for all the drivers included in the software interface.

Note — Before you begin Themis Computer suggests that you consult the Sun Solaris 1.1.x System Installation Manual or SPARC: Installing Solaris Software 2.x Manual, depending on which SunOS you have. These documents are available through Sun Microsystems.

4.9.1 VMEbus Nexus Driver

The vme driver forms the core of the software interface provided by Themis Computer. The vme driver is a bus Nexus driver that encapsulates all the architectural features of supporting the SPARC 20MP on Solaris systems. This driver is configured to be permanently loaded as the bus Nexus driver for the VMEbus.

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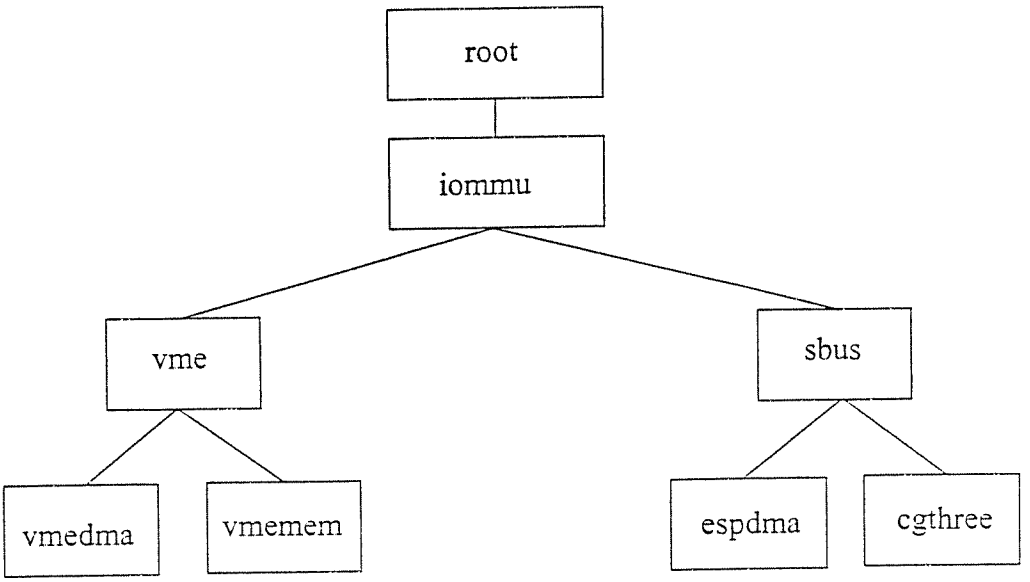


Figure 4-1. **VME Driver Directory Structure**

Any driver that specifies its class or parent as vme will be attached to the vme driver. The vme driver provides support for all VMEbus operations, including VMEbus interrupt processing, Direct Virtual Memory Access (DVMA) on the VMEbus, mapping of registers on the VMEbus to kernel space, and mapping of VMEbus memory to user address space through mmap(), etc.

The vme driver also exports certain capabilities that can be used by VMEbus leaf drivers. This enables leaf drivers to perform operations like Direct Memory Access. The vme driver recognizes the standard configuration file for VMEbus device drivers (see the vme(4) man page (File Formats) for additional information). The configuration of any VME device driver specifies the VMEBus interrupt level and the interrupt vector.

Table 4-37. **VMEbus Interrupt Mapping to SPARC Interrupt Priority Level**

VMEbus Interrupt	1	2	3	4	5	6	7
SPARC Interrupt Priority Level	2	3	5	7	9	11	13

4.9.2 Utility Drivers

These drivers provide a useful interface to system programmers who wish to utilize the different features of the VMEbus architecture and are a standard part of the software interface provided by Themis Computer.

The vmemem device driver provides the standard `/dev` devices for accessing the VMEbus from user processes.

Table 4-38. **VME Device Drivers**

Device File	Address Size	Data Transfer Size
/dev/vme32d32	32	32
/dev/vme32d16	32	16

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Table 4-38. **VME Device Drivers** (Continued)

Device File	Address Size	Data Transfer Size
/dev/vme24d32	24	32
/dev/vme24d16	24	16
/dev/vme16d32	16	32
/dev/vme16d16	16	16

read(), write() and mmap() calls are supported and no special ioctl() calls are required to configure the interface. VME interface configuration is performed under OBP and should not be modified while the operating system is running.

On Themis SPRAC 20MP platforms, DMA access to the VMEbus is provided by the Newbridge SCV64 VMEbus Controller. The vmedma driver provides user access to the DMA features of the SCV64 controller. Using the ioctl interface provided by the driver, the user program can utilize the DMA engine and achieve high rates of data transfer.

4.9.3 Sample Drivers

The software interface provided for the SPARC 20MP fully supports standard VMEbus device drivers written for Solaris environments. It is the intention of Themis Computer to fully support users who wish to write their own VME device drivers that would run on the SPARC 20MP. To aid these users and to illustrate the specific features of the VMEbus architecture, Themis Computer provides a number of sample device drivers with complete source code and the necessary configuration files for these drivers.

- **vmeintr** is a sample driver provided by Themis Computer to illustrate the vectored interrupt mechanism of the VMEbus. The vmeintr driver relies on the driver configuration files to specify the interrupts it should handle. Each instance of the driver registers the interrupts with the system. Through the ioctls implemented by the driver, the user can generate interrupts and send them to the appropriate driver instances. The interrupt generator and the interrupt receiver need to run on different computers.

- **vmedvma** is a sample driver provided by Themis Computer to illustrate the use of Direct Virtual Memory Access within a device driver. The user can ask the driver to allocate a DMA region on the VMEbus. The driver allocates all the necessary resources to support a DVMA transfer to this region. The driver also implements mechanisms by which the user program can write to or read from the DVMA region.

- **simpledma** is a sample driver provided by Themis Computer to illustrate the use of Direct Memory Access within a device driver. It is a simplified version of the standard vmedma driver. This driver is mainly intended for programmers writing device drivers that perform DMA operations on the VMEbus.

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5

SuperSPARC

5.1 Introduction

This chapter discusses the different implementations of the SuperSPARC CPU Architecture on MBus modules that are used in the SPARC 20MP. There are two different implementations, the SuperSPARC with External Cache module (which includes a MXCC ASIC) and the SuperSPARC only module without External Cache. The following sections discuss the implementation details of the different MBus modules such as the differences between the registers in these MBus modules and the Sun4M architecture specification.

5.2 SuperSPARC

SuperSPARC is a 3-wide SPARC processor which uses a Harvard architecture (separate instruction and data caches). Bus snooping is implemented via the second level external cache directory. The first level caches are inside the processor chip. The instruction cache is a 20KB physical address 5-way set associative cache. The tag for each block in the instruction cache contains the physical tag PA<35:12> plus a valid bit for each sub-block.

Set replacements are made on a limited history LRU replacement scheme and sets may also be selectively locked. To insure consistency with self modifying code a SPARC FLUSH must be executed to synchronize on the completion of all pending writes and to flush the instruction pre-fetch buffer.

The internal SuperSPARC data cache is physical address 16K byte 4-way set associative with block size of 32 bytes. The SuperSPARC MMU contains a 64 bit entry TLB that is fully associative with a second level Page Table Pointer cache. The external cache for SuperSPARC is a direct mapped cache consisting of 8K blocks of 128 bytes each with each block divided into 4 sub-blocks of 32 bytes. The external cache is a write-back store cache with a write-allocate policy.

The external cache (E-cache) tags contain the physical address bits PA<35:19> for the block, plus a shared, owned, valid, and pending bit for each of the four sub-blocks. The E-cache snoops on physical addresses to maintain Level-2 MBus cache consistency. Since SuperSPARC caches are physically addressed the contents of the cache lines always correspond to a backing in physical memory. Thus no flush mechanism is supported as there is never a need to de-reference the contents of any cache line.

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The SuperSPARC's MMU LRU replacement algorithm first sweeps TLB entries sequentially until all TLBs have the valid bit set. Replacement cycles will take the first TLB that is not "used". The de-map-all operation will clear all "used" and "valid" bits. The root pointer and the level-2 PTP are cached in the MMU. Context switches invalidate the root pointer. Thus upon the first miss after a context switch, an extra-level of table walk will be needed to fetch the context's root pointer.

The SuperSPARC MBus module with external cache contains a SuperSPARC processor with a MXCC cache controller and MMU ASIC as well as 1M bytes of cache. In this module, the SuperSPARC CPU runs at 40 MHz and the MXCC interfaces with the 40 MHz MBus in the 20MP. The MXCC in MBus mode, supports physically addressed block copy or block fill operations on 32-byte blocks. Filling the stream data register via a stream read performs a block copy operation which can then be written to its destination via a stream write. Stream Reads (Writes) occur by writing the block address to the Stream Source (Destination) Register. Block fills are performed by writing the fill data to the Stream Data Register, then issuing a series of streams writes.

The SuperSPARC chip is packed in a 293 CPGA with a copper tungsten slug, which, with a heat sink, provides for a Theta-JA of 3.5 degrees C per Watt in 300 LFPM of air flow. The SuperSPARC only MBus module contains only a SuperSPARC processor with no external cache and no MXCC.

5.3 SPARC Reference MMU

Physical addresses (PA) consist of bits 35:12 containing a Physical Page Number and bits 11:0 containing the Page Offset. Note that PA<11:0> = VA<11:0> (where VA = Virtual Address); thus the lower 12 bits of a virtual address never need translation. A virtual address is composed of the following:

Table 5-1. **Virtual Address Definition**

Bits	Description
35:32	ASI
31:24	Index 1
23:18	Index 2
17:12	Index 3
11:0	Page Offset

Each index field provides an offset into the corresponding level of page table, starting with the root pointer which provides the offset to Index 1 in the Level-1 table. A full set of tables is rarely needed as the virtual address space is usually sparsely populated. It is possible to map a 256 KB, 16 MB or 4 GB section of linear memory with a single Page Table Entry. This is useful when mapping in items such as frame buffers which normally can cause many pages to get thrashed in the TLB when drawing a vertical line, for example.

The Translation Look-aside Buffer (TLB) holds the virtual-address to physical-address translations of recent memory accesses. When making a memory access, the translation for the virtual address is not found in the TLB, then one must perform a table walk through the MMU to find a valid Page Table Entry. This process begins by finding the Root Pointer for that context by using the Context number as an index into the Context Table to generate a Root Pointer. The Root Pointer is used as an offset into the Level-1 table to find either a offset into a Level-2 table or that the Level-1 entry is already a Page Table entry. Note that upon the first miss after a context switch, an extra level of table walk must be made to fetch that context's root pointer. The two low order bits of the Page Table Descriptor determines if the entry is a Page Table Descriptor (PTD), i.e. a

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pointer to the next level of the MMU, or a Page Table Entry (PTE), i.e., Physical Page number. If the Physical Page number is found, then the table-walk stops there. PTDs are determined from the two lower order bits of the PTD being equal to 1, if the two lower order bits are equal to 2, then it is a page table entry. If the PTE wasn't found, then the PTD from the Level-1 table is used as a offset into the Level-2 table. The process is repeated again. Either the PTD is a PTE or it is another offset into the Level-3 table. Note that once we get to the Level-3 table, all entries are PTEs, and the table walk is finished.

5.4 IOMMU

The Sun4M IOMMU is used to perform address translations when SBus masters request the SBus. In the SPARC 20MP implementation, the IOMMU resides within the MSI. In contrast there is a MMU for the MBus inside the MBus modules that is used for processor accesses to main memory. In the SPARC 20MP implementation of the IOMMU within the MSI ASIC, there is a 16 entry TLB (Translation Look-aside Buffer) for already-translated virtual to physical translations. The IOMMU inside the MSI uses 4 KB sized pages with a single level table, i.e., there are no region or segment maps. In diagnostic mode the MSI supports direct read/writes of the TLB entries. The address translation can be turned off in the IOMMU bypass mode.

The IOMMU is a one-level memory-based MMU which provides address translation between the Virtual Address on the SBus and the Physical Address used in the MBus system. There is a base pointer that points to a table in memory, and part of the DVMA virtual address is used to index into this table to access an IOPTE (page table entry) which contains a physical page number, a valid-bit for the entry, a write-allowed-bit, and a cacheability-bit. The page table size and the corresponding DVMA virtual address range are configured in the IOMMU Control register RANGE field. The table consists of (DVMA Range/Pagesize) 32-bit entries. The IOMMU maps (DVMA Range) virtual address space for DVMA activity. The Virtual Address used is a VA<X:0>, where X is the highest VA-bit in the translatable range. The bits VA<X:12> provide a Virtual Page number which is used as an index into the IOMMU table in memory, and the Physical Page number PA<35:12> is concatenated with the in-page VA<11:0> to generate the Physical Address of the access.

TLBs in the IOMMU are allocated based upon an LRU algorithm. There are 16 TLB entries. TLB misses are serviced in hardware. The IOMMU Base Address is loaded from segment address 0-0 which places it on the MBus. Thus the TLB fetch mechanism fetches from the MBus. In Bypass mode the TLB goes to address 0x00XXX XXXX.

5.5 Instruction Cache Formats

5.5.1 Instruction Cache Tag Address Format

– ASI = 0xC

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Table 5-2. **Instruction Cache Tag Address Format**

Bit	Function
31:30	0 = Reserved 1 = Set Tag 2 = Physical Tag 3 = Reserved
29	Reserved
28:26	0 = Line within set 1 = Line with set 2 = Line with Set 3 = Line with set 4 = Line with set 5 = Reserved 6 = Reserved 7 = Reserved
25:12	Reserved
11:6	Set (1 of 64)
5:3	Reserved
2:0	Zeros

5.5.2 Instruction Cache PTAG (Physical Tag) Format

Table 5-3. **Instruction Cache PTAG (Physical Tag) Format**

Bit	Function
63:58	Reserved
57:56	Valid bit for 32 byte sub-block V <1> (<0> = high (low) order block)
55:24	Reserved
23:0	Physical tag address bits PA<35:12>

5.5.3 Instruction Cache STAG (Set Tag) Format

Table 5-4. **Instruction Cache STAG (Set Tag) Format**

Bit	Function
63:14	Reserved
13:8	Access history bits used in partial LRU algorithm
7:6	Reserved
5:0	Lock bits

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5.5.4 Instruction Cache Data Address Format

– ASI = 0xD

Table 5-5. **Instruction Cache Data Address Format**

Bit	Function
31:29	Reserved
28:26	Line within set (0-4), 5 = 6-7=reserved
25:12	Reserved
11:6	Set (1 of 64)
5:3	Double word within line
2:0	Zeros

5.5.5 Instruction Cache Flash Clear

– ASI = 0x36

Table 5-6. **Instruction Cache Flash Clear**

Bit	Function
31	0 = clear all Valid and MRU bits in Ptags and Stags 1 = clear all lock bits in Stags
30:0	Reserved

5.6 Data Cache Formats

5.6.1 Data Cache Tag Address Format

– ASI = 0xE

Table 5-7. **Data Cache Tag Address Format**

Bit	Function
31:30	0 = Reserved 1 = Set Tag, 2 = Physical Tag 3 = Reserved
29:28	Reserved
27:26	Line within set (0-4) 5 through 7 = Reserved
25:12	Reserved

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Table 5-7. **Data Cache Tag Address Format** (Continued)

Bit	Function
11:5	Set (1 of 128)
4:3	Reserved
2:0	Zeros

5.6.2 Data Cache PTAG (Physical Tag) Format

Table 5-8. **Data Cache PTAG (Physical Tag) Format**

Bit	Function
63:57	Reserved
56	Valid-bit for 32 byte block
55:49	Reserved
48	Dirty
47:41	Reserved
40	Shared
39:24	Reserved
23:0	Physical Tag address bits PA<35:12>

5.6.3 Data Cache STAG (Set Tag) Format

Table 5-9. **Data Cache STAG (Set Tag) Format**

Bit	Function
63:12	Reserved
11:8	Access history bit used in partial LRU algorithm
7:4	Reserved
3:0	Lock bits

5.6.4 Data Cache Data Address Format

– **ASI = 0xF**

Table 5-10. **Data Cache Data Address Format**

Bit	Function
31:28	Reserved
27:26	Line with set (0-3),

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Table 5-10. **Data Cache Data Address Format** (Continued)

Bit	Function
25:12	Reserved
11:5	Set (1 of 128)
4:3	Double word within line
2:0	Zeros

5.6.5 Data Cache Flash Clear

– ASI = 0x37

Table 5-11. **Data Cache Flash Clear**

Bit	Function
31	0 = clear all Valid and MRU bits in Ptags and Stags
	1 = clear all lock bits in Stags
30:0	Reserved

5.7 Register Differences

5.7.1 Module Control Register

Table 5-12. **Module Control Register**

Bit	Function
8	Data-cache enable
9	Instruction cache enable
10	Store buffer enable
11	Data cache = Copy back = 1 write through = 0
12	Parity check enable
13	Boot mode = 0 normal = 1
14	Snoop enable
15	Alternate cacheable
16	Table-walk cacheable

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5.7.2 Context Table Pointer Register

Table 5-13. **Context Table Pointer Register**

Bit	Function
31:8	DCTP<35:12>

5.7.3 Context Register

Table 5-14. **Context Register**

Bit	Function
N = 15	64K contexts supported

5.7.4 Synchronous Fault Status Register

Table 5-15. **Synchronous Fault Status Register**

Bit	Function
13	Undefined Error set by MXCC signals a Retry and asserts Data Ready
14	Control Space Access Error

5.7.5 Asynchronous Fault Status Register

SuperSPARC does not support an Asynchronous Fault Status Register.

5.7.6 Reset Register

SuperSPARC has no internal Reset Register, it resides in the MXCC.

5.7.7 MBus Port Address Register

The MBus Port Address Register resides in the MXCC.

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5.8 SuperSPARC MXCC Implementation Details

5.8.1 SuperSPARC MXCC Register Addresses

Table 5-16. **SuperSPARC MXCC Register Addresses**

VA[31:0]	Description
0x0100 0000 - 0x 010F FFFF	E-cache Data
0x0180 0000 - 0x 018F FFFF	E-cache Tag
0x01C0 0000 - 0x 01CF FFFF	MXCC Control Register
0x01C0 0000	Stream Data Register
0x01C0 0100	Stream Source Register
0x01C0 0200	Stream Destination Register
0x01C0 0300	Reference/Miss Count Register
0x01C0 0400	Interrupt Pending (Not used in MBus systems)
0x01C0 0500	Interrupt Mask (Not used in MBus systems)
0x01C0 0600	Interrupt Pending Clear (Not used in MBus systems)
0x01C0 0700	Interrupt Generation (Not used in MBus systems)
0x01C0 0800	Reserved
0x01C0 0900	Reserved
0x01C0 0A00	MXCC Control Register
0x01C0 0B00	MXCC Status Register
0x01C0 0C00	Module Reset Register
0x01C0 0D00	Reserved
0x01C0 0E00	Error Register
0x01C0 0F00	MBus Port Address Register

5.8.2 Module Control / Status Register Addresses

– ASI = 0x4

Table 5-17. **Module Control / Status Register Addresses**

VA[31:0]	Description
0x0000 0000	Module Control / Status Register
0x0000 0100	Context Table Pointer Register
0x0000 0200	Context Register
0x0000 0300	Synchronous Fault Status Register
0x0000 0400	Synchronous Fault Address Register

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Table 5-17. **Module Control / Status Register Addresses** (Continued)

VA[31:0]	Description
0x0000 0500	Asynchronous Fault Status Register
0x0000 0600	Asynchronous Fault Address Register
0x0000 0700	Reset Register
0x0000 0800 - 0xFFFF FFFF	Implementation Dependent

5.8.3 E-Cache Data Address Format

Table 5-18. **E-Cache Data Address Format**

Bit	Function
31:25	Reserved
24:23	10
22:20	Reserved
19:7	Cache Block number
6:5	Sub-Block number
4:3	Double Word within Block
2:0	Byte within double word

5.8.4 E-Cache Tag Address Format

Table 5-19. **E-cache Tag Address Format**

Bit	Function
31:25	Reserved
24:22	100
21:20	Reserved
19:7	Cache Block Number
6:0	Reserved

5.8.5 E-Cache Tag Format

Table 5-20. **E-cache Tag Format**

Bit	Function
63:36	Reserved
35:19	PA<35:19>
18:16	Reserved

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Table 5-20. **E-cache Tag Format** (Continued)

Bit	Function
15	Shared-bit sub-block 3
14	Owned-bit, sub-block 3
13	Valid-bit sub-block 3
12	Pending-bit sub-block 3
11	Shared-bit sub-block 2
10	Owned-bit, sub-block 2
9	Valid-bit sub-block 2
8	Pending-bit sub-block 2
7	Shared-bit sub-block 1
6	Owned-bit, sub-block 1
5	Valid-bit sub-block 1
4	Pending-bit sub-block 1
3	Shared-bit sub-block 0
2	Owned-bit, sub-block 0
1	Valid-bit sub-block 0
0	Pending-bit sub-block 0

5.8.6 Stream Source/Destination Register Format

Table 5-21. **Stream Source/Destination Format**

Bit	Function
63	Ready - indicates pending stream read/write
62:37	Reserved
36	Cacheable
35:5	PA<35:5>
4:0	Zeros

5.8.7 Reference / Miss Count Register

Table 5-22. **Reference / Miss Count Register**

Bit	Function
63:32	Cache Miss Count - clear on read
31:0	Cache Reference Count

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5.8.8 MXCC Count Register

Table 5-23. **MXCC Count Register**

Bit	Function
31:9	Reserved
8:7	Unused in MBus implementations
6	Unused in MBus implementations
5	Pre-fetch enable
4	Multiple Command Block
3	Parity Checking
2	Enable E-cache
1	E-cache size
0	Half-cache

5.8.9 MXCC Status Register

Table 5-24. **MXCC Status Register**

Bit	Function
63:40	Reserved
39	Store Exception
38	Synchronous Mode
37:36	Unused in MBus implementations
35:12	Unused in MBus implementations
11	Unused in MBus implementations
10:8	Unused in MBus implementations
7	Reserved
6:4	Store Pending Count
3	Unused in MBus implementations
2	Write Miss Pending
1	Read Miss Pending
0	Pre-fetch Pending

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5.8.10 Module Reset Register

Table 5-25. **Module Reset Register**

Bit	Function
31:3	Reserved
2	Watchdog Reset
1	Software Internal Reset
0	Reserved

5.8.11 MXCC Error Register

Table 5-26. **MXCC Error Register**

Bit	Function
63	Multiple errors
62	Unused in MBus implementations
61	Cache Consistency Error
60	Write-back Error
59	SuperSPARC Bus parity Error on SuperSPARC write
58	SuperSPARC bus parity Error on MXCC read
57	Asynchronous Error
56	Reserved
55	Error Invalid
54:45	Err<7:0>
44:37	CC Operation Code (see MXCC spec)
36	Reserved
35:0	PA<35:0>

5.8.12 MBus Port Address Register

Table 5-27. **MBus Port Register**

Bit	Function
31:28	Reserved
27:24	MID<3:0>
23:16	Reserved
15:8	MBus device number = 0x0
7:4	MBus Revision number = 0x0
3:0	MBus vender number = 0x3

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5.9 SuperSPARC MXCC MMU Implementation Details

5.9.1 TLB RAM Diagnostic Access Address Format

Table 5-28. **TLB RAM Diagnostic Access Address Format**

Bit	Function
31:18	Reserved
17:12	Entry in Page Descriptor Cache (1 of 64)
11	Reserved
10:8	TLB portion Select: 0 = VA 1 = Context 2 = Lock-bit 3 = PTE 4 = Root Pointer 5 = Level-2 PTP 6 = Level-2 VA
7:0	reserved

5.9.2 Virtual Address Format

– (sel = 0 and sel = 6)

Table 5-29. **Virtual Address Format**

Bit	Function
31:12	VA<31:12>
11:0	Reserved

5.9.3 Context Format

– (sel = 1)

Table 5-30. **Context Format**

Bit	Function
31:16	Reserved
15:0	Context Tag <15:0>

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5.9.4 Lock Format

– (sel = 2)

Table 5-31. **LOCK Format**

Bit	Function
31:1	Reserved
0	LOCK if content of TLB entry will not be replaced

5.9.5 PTE (Page Table Entry) Format

– (sel = 3)

Table 5-32. **PTE (Page Table Entry) Format**

Bit	Function
31:8	Physical page number <35:12>
7	Cacheable
6	Modified
5	Valid TLB entry
4:2	Access permissions
1:0	PTE level: 0 = root 1 = region 2 = segment 3 = page

5.9.6 Root Pointer Cache Format

– (sel = 4)

Table 5-33. **Root Pointer Format**

Bit	Function
31:0	Root Pointer

5.9.7 Level-2 PTP Cache Format

– (sel = 5)

Table 5-34. **Level-2 PTP Cache Format**

Bit	Function
31:0	Level-2 PTP Cache <31:0>

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5.9.8 TLB Probe Access Format

Table 5-35. **TLB Probe Access Format**

Bit	Function
31:12	Virtual Flush/Probe Address
11	Reserved
10:8	De-mapping type: 0 = page 1 = segment 2 = region 3 = context 4 = entire MMU 5-7 reserved
7:0	Reserved

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6.1 Overview

The hyperSPARC is designed as a tightly-coupled chipset to be utilized in SPARC MBus module. Each hyperSPARC CPU supports either 128 or 256 Kbytes of second-level cache, and each module may contain one or two CPUs. The chipset is comprised of the RT620 Central Processing Unit (CPU), the RT625 Cache Controller, Memory Management, and Tag Unit (CMTU0, and two or four RT627 Cache Data Units (CDUs) for 128 Kbytes or 256 Kbytes of second-level cache, respectively. The chipset can be configured for uniprocessing (Level 1 MBus) or multiprocessing *Level 2 MBus).

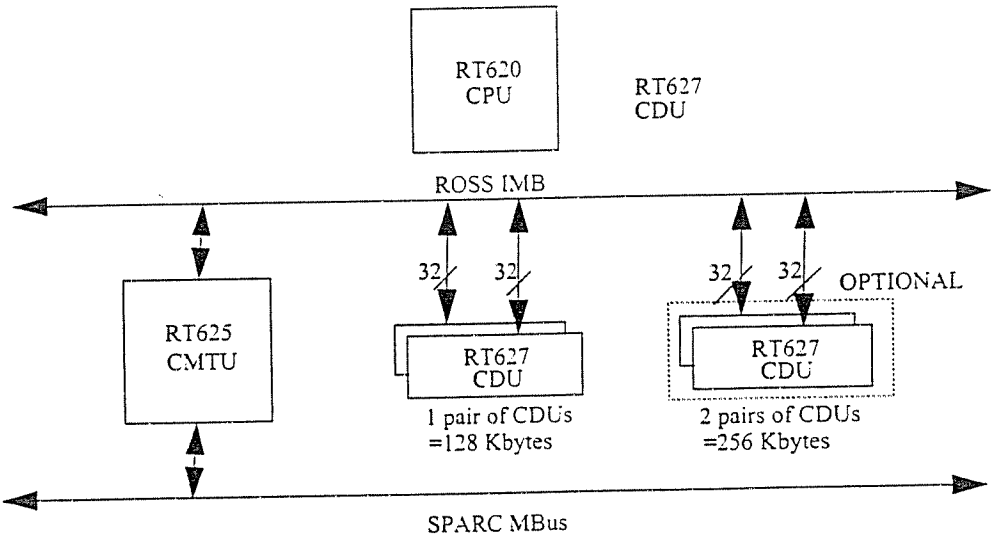


Figure 6-1. **hyperSPARC CPU Chipset Block Diagram**

The RT620 is the primary processing unit in hyperSPARC. This chip is comprised of an integer unit, a floating-point unit, and an 8-Kbyte, 2-way set-associative instruction cache. The integer unit contains the ALU and separate Load/Store data path, constituting two of the chip's four execution units. There is also the floating-point unit and a Branch/Call unit (for processing control transfer instructions). Two instructions are fetched every clock cycle, In general, as long as these two instructions require different execution units and have no data dependencies, they can be launched simultaneously. Two floating-point instructions may also be

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simultaneously dispatched, due to the inclusion of a floating-point instruction pre-queue. The RT620 contains two register files: 136 integer register configured as eight register windows, and 32 separate floating-point registers in the floating-point unit.

The hyperSPARC's second-level cache is built around the RT625 CMTU, a combined cache controller and memory management unit that supports shared-but multiprocessing. The cache controller portion supports 128-Kbytes or 256-Kbytes of cache, made up of two or four RT627 CDUs. The cache is direct-mapped with 4-Kbytes of cache tags. The cache is physically tagged and virtually indexes so that the RT625's cache coherency logic can quickly determine snoop hits and misses without stalling the RT620's access to the cache. Both copyback and write-through caching modes are supported.

The SPARC reference MMU of the RT625 provides a 64-entry, fully set-associative TLB that supports 4096 contexts. The RT625 contains a read buffer 932 bytes deep) and a write buffer (64 bytes deep) for buffering the 32-byte cache lines in and out of the second-level cache, and synchronization logic for interfacing the virtual IMB to the SPARC MBus.

The RT627 is a custom-designed 16-Kbyte X 32-bit SRAM. It is organized as four arrays of 16-Kbyte SRAM with byte write logic, registered inputs, and data-in and data-out latches. The RT627s provide a zero-wait-state cache to the CPU with no pipeline penalty (i.e., stalls) for loads and stores that hit the cache. The RT627 requires no glue logic for interfacing to the RT620 (CPU) and the RT625 (CMTU).

6.2 Design Features

The micro-architecture of hyperSPARC boasts classic RISC and superscalar features for improving instruction processing throughput. In addition, hyperSPARC also employs architectural enhancements that differentiate it from other next-generation microprocessor designs. The following sections highlight some of hyperSPARC's most important attributes.

6.2.1 High Frequency Operation

Fundamentally, hyperSPARC is built for speed. In order to facilitate high clock frequencies, particular attention is paid to the 6-stage integer and floating-point pipelines, keeping them simple and well-balanced. Each stage of the pipelines is carefully partitioned in order that the number of gates per stage is similar, thus more easily lending itself to process shrinks for scaling to higher clock rates.

The hyperSPARC allows processor clock rates to be increased independently of the external bus (MBus). The hyperSPARC chipset was partitioned to allow synchronous or asynchronous operation through synchronization logic contained in the RT625. This decoupling of the CPU bus from the external bus allows scaling of hyperSPARC's clock frequency independent of the memory and I/O subsystems. This provides longer product life cycles since upgrades to higher performance hyperSPARC modules require no hardware changes to the underlying system design.

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6.2.2 Instruction Scheduling

Instruction scheduling and dispatching is a critical portion of any superscalar design. Optimal instruction scheduling involves both minimizing pipeline stalls (costly enough for any RISC machine, but even more costly when multiple instructions are being held) and minimizing conditions that prevent simultaneous instruction launching.

All superscalar microprocessors are not the same. The ability to fetch and launch multiple instructions is only as good as the number of times this feature is actually taken advantage of. compilers can help reduce the occurrences of instructions that cannot be launched together by scheduling instructions accordingly. However, the software can only optimize for the hardware; the microprocessor design must be intelligently partitioned to provide opportunities for software enhancements.

The hyperSPARC is partitioned into four execution units in order to facilitate parallel processing of major instruction types. These execution units are the Load/Store unit, Branch/Call unit, integer unit, and floating-point unit. The floating-point unit is actually comprised of an instruction queue and two parallel pipelines, an adder and a multiplier.

Poorly architected designs require more frequent splits of instruction groupings. Internal constraints, such as bus design/bandwidth and number of read/write register ports, sometimes prevent the scheduler from having any opportunity to launch multiple instructions together. These design constraints manifest themselves in many ways, especially restricting simultaneous launch based on the types of instructions, and or order of the instructions, within groupings. The result is frequent sequential (instead of simultaneous) instruction launches.

hyperSPARC's ability to launch multiple instructions simultaneously is not restricted by the order and type[1] of instructions within groupings. Sequential launch is required, of course, for cases involving resource conflicts or data dependencies. But unlike some other superscalar designs, any instruction can occupy and position in the grouping and still be considered for simultaneous launch.

hyperSPARC also provides special support for the launching of floating-point instructions. The hyperSPARC floating-point unit employs two queues: a *pre-queue and post-queue*. The post-queue maintains information on instructions currently in execution in either the floating-point adder or multiplier units. This information includes the instruction type, address, and stage of the pipeline for any given clock. Information of this type is required for exception handling to recover the instructions aborted when the floating-point pipeline is flushed due to a trap.

ROSS, however, extends this principle to a floating-point pre-queue, which holds the same information for up to four instructions that are pending execution. The significance of this pre-queue is that it allows floating-point instructions to be sent to the pre-queue from the normal integer instruction stream. The hyperSPARC scheduler is capable of fetching and dispatching any two floating-point instruction at a time, sending both to the pre-queue in the same clock cycle. If the floating-point unit is not busy, one of the two floating-point instructions bypasses the pre-queue and begins final instruction decode and execution immediately. The integer pipeline proceeds uninterrupted to fetch, decode, and execute more instructions in the next clock cycle. This made possible with hyperSPARC's dual-level instruction decoding, which off-loads final instruction decode to the floating-point unit. In hyperSPARC, integer multiplies and divides are executed in the integer ALU, removing this work load from the floating-point unit.

---

1. There is a group of infrequently occurring instructions that must be launched sequentially (e.g. JMPL, RETT, FCMP, FLUSH, etc., and privileged instructions such as RDY and WRY), but they represent only a small fraction of most executable programs.

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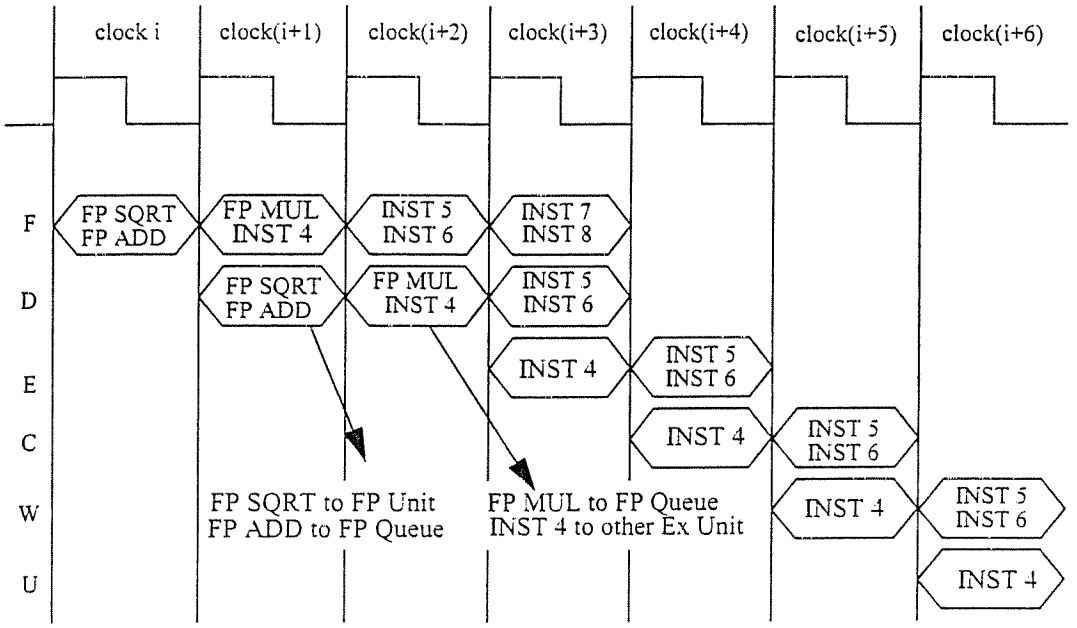


Figure 6-2. **RT620 Instruction Pipeline Example**

6.2.3 Multiprocessing

Multiprocessing is a key to dramatically higher performance from existing silicon technology. hyperSPARC provides full hardware support for tightly-coupled multiprocessing system architectures.

hyperSPARC provides a high-performance snoop mechanism to facilitate efficient data transfers between processors. In a write-invalidate protocol, such as the one implemented in Level 2 MBus, caches residing on a shared bus must check, or "snoop," each address request to shared memory space. If a cache owns the cache line at the address being requested, it can respond to the request by copying the data to memory (which later forwards the data to the requesting cache) or supply the data directly to the requesting processor (direct data intervention). In the case of a direct data intervention transfer, t he cache supplying the data must prevent memory from obtaining the bus and responding to the request.

The SPARC architecture allows a window of MBus clock cycles within which a cache must assert the Memory InHibit (MIH) signal if it owns the requested cache line (i.e., there is a snoop hit). That window is A + 2 cycles to A + 7 cycle, the "A" representing the cycle in which the address of the cache line being requested is placed on the MBus. The hyperSPARC responds on snoop hits with MIH in the A + 3 cycle. This means that memory is free to respond beginning A + 4. Using the full window allowed by MBus would impose a three-cycle penalty for every memory access. Responding this quickly, even though the MBus specification offers more relaxed timing, enables a very high-performance memory subsystem to be built around hyperSPARC.

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6.2.4 Cache Architecture

hyperSPARC was designed as a tightly-coupled chipset in order to achieve optimal performance between processor and cache. the ROSS designers' understanding of the CPU's relationship with the cache is demonstrated in the RT620's design, which imposes only a one-cycle primary cache (instruction cache) miss penalty. A pipeline stage is allotted in the RT620 for accessing the second-level cache so that no additional stall in CPU throughput is realized if the on-chip cache is missed and the second-level cache is hit.

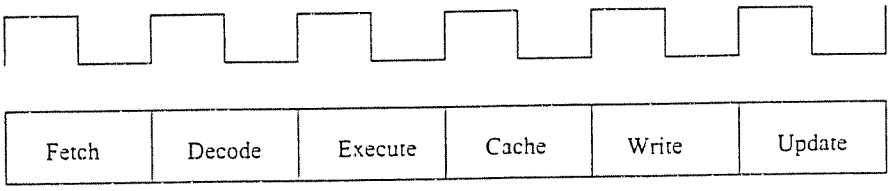


Figure 6-3. **RT620 Pipeline Stages**

The RT620 utilizes a six-stage pipeline, as shown in *Figure 6-3*. The first three stages are typical RISC pipeline stages: Fetch, Decode, and Execute. the fourth stage of the pipeline is the Cache stage, which is a built-in recognition of the latency of accessing the second-level cache for data access.

Instruction fetches will cause the RT620 to initiate two accesses: one to the on-chip 8-Kbyte instruction cache, and, at the same time, one to the second-level cache. If the address for this instruction is found within the on-chip cache, the access to the second-level cache is cancelled and the instruction is available at the Decode stage of the pipeline.If there is a miss on the internal cache, and a hit on the second-level cache, the instruction is available after a one-cycle miss penalty built into the pipeline. The significance of this design is that it allows the pipeline to proceed uninterrupted as long as the instruction accesses hit either the on-chip cache or the second-level cache, which has been found to be about 90% of the time, respectively, for typical workstation applications. Since the integer and floating-point pipelines mirror these six stages for reasons of architectural balance and ease of exception handling, this design enables the RT620 to achieve its high throughput rate at speeds that would otherwise not be possible.

The RT627 Cache Data Units utilize a unique single-stage pipeline and data forwarding similar to that used in microprocessor designs. This pipeline design allows the RT627 to keep up with the data rate of the processor, which requires latching and writing data into the RAM core within a short period. Writes into the RT627 are buffered by latching the address and data during the write cycle. The RT620 is then free to perform read operations. The write into the RAM core is delayed until the next write access. Each write access operation provides the opportunity to write the previous write data into RAM without incurring a timing penalty.

The obvious drawback of this approach is the possibility of a read of the data being held in the latches before the RAM core is updated. The RT627 addresses this problem by using data forwarding. A comparator checks the address of the pending write with the incoming read address. If a match occurs, data is forwarded from the input data latches directly to output pins, bypassing the RAM core. In this way, the most recent data is provided by the RT627 CDUS

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6.3 Special Features

There are a number of subtle but clever design features implemented in hyperSPARC that improve performance for common functions required of the CPU. One such feature is the RT620 CPU's Fast Constant/ Index/Branch capability.

Fast Constant, for example. represents a commonly occurring combination of two ALU instructions that are used to generate 32-bit constants, Specifically, the SETHI and OR instruction pair is used frequently to create the 22 high-order and 10 low-order bits, respectively (in fact, the current SPARC compilers generate these two instructions from the pseudo-instruction SET for sufficiently large constants). When hyperSPARC's scheduler encounters this instruction pair, it launches them for execution in parallel, as if they were a single instruction. Thus, an operation that normally takes two cycles (i.e., the setting of the high-and-low-order bits for the designated register) is reduced to one cycle. Fast Index works similarly, combining the SETHI and LD instruction pair commonly used to generate a 32-bit base address for array indexing.

Fast Branch is a feature which avoids waiting for condition codes to be set by an ALU instruction before initiating a Branch Target Fetch. This feature allows a branch and an associated ALUcc instruction to be launched simultaneously. The hyperSPARC uses a branch-taken prediction strategy, and fetches the branch target address. This reduces the number of cycles between branch resolution and target instruction Fetch and Execute if the branch is taken, or continued instruction processing if the branch is not taken.

Block Copy and Block Fill are special features of the RT625 CMTU. These are software-initiated operations to increase the performance of data movement in and out of main memory. Taking full advantage of the RT625's read and write buffers, these block manipulations functions allow data to be moved to or from main memory without having to be brought into cache. This not only saves the latency of filling the cache, but also allows the RT620 to continue processing at the same time.

Block Copy copies an entire 32-byte block of data from a cache or main memory location to another location in main memory. This is particularly useful when copying files, databases or other large memory blocks to other memory locations. If data is being copied from main memory to another location in main memory, for example, it is first read into the read buffer, transferred to the write buffer, and then written to the specified memory location in memory. Block Copy saves more than 10 clock cycles that would be encountered if the block were read into, and then out of, cache.

Block Fill copies into the specified memory location the double-word embedded in the special block fill STA instruction. The Block Fill works similarly to the Block Copy, only the read transaction is not required since the source data comes from the processor. The specified double-word pattern is written throughout the 32-byte block of memory, which is very useful in initializing large blocks of memory. The alternative solution would require a cache line in main memory to be brought into cache, initialized with a data pattern, and then written back out to main memory.

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7

MBus

7.1 MBus Specification

The SPARC MBus is a high speed interface between SPARC processor modules and physical memory and input / output devices. The MBus is developed to operate at clock rates starting at 33 MHz. Due to its high clock frequency, the topology of a given MBus implementation must occupy a small physical area due to the limit of the speed of light on information transfer. The MBus interface has the following features:

- Fully synchronous
- Circuit switched
- 64-bit, multiplexed address and data
- 64 GB of physical address space
- Multiple master
- Centralized arbitration, reset, interrupt and clock distribution
- Overlapped arbitration with "parking"
- Shared memory multiprocessor (MP) signals and transactions
- Supports a write-invalidate cache coherency protocol

7.2 MBus Levels

Level 1 includes the basic MBus signals and transactions needed to design a complete uni-processor system, while Level 2 includes the signals and transactions needed to design a cache coherent, shared memory multiprocessor system. The SPARC 20MP implements the full Level-2 functionality of which Level-1 is a subset. What this means is that the SPARC 20MP can use Level-1 or Level-2 MBus modules, the module itself determining whether it can support multiprocessing (Level-2) or not (Level-1). The basics of both are presented as background.

Level-1 MBus supports two transactions, Read and Write. Level-2 MBus is a super-set of Level-1 that contains four additional transactions and two additional signals to support cache coherency, to allow for the design of shared memory multiprocessor systems. The additional signals are Shared (MSH*) and Inhibit

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(MIH*). The four additional transactions are Coherent Read (CR), Coherent Invalidate (CI), Coherent Read and Invalidate (CRI), and Coherent Write and Invalidate (CWI). For a cache to support Level-2 transactions it must minimally support the following:

- a "write-back" policy on data writes
- "allocate" policy on write misses
- have a cache sub-block or block size of 32 bytes.

Furthermore cache lines are assumed to have at least five states:

- invalid
- exclusive clean
- exclusive dirty
- shared clean
- shared dirty.

7.3 MBus Modules

In the Level-2 architecture, there are multiple processors each with its own cache. A piece of data may reside in any of these caches. In some caches the data may be altered from its initial value stored in memory. In other caches it may not be altered. When such a piece of data is requested, a cache coherency protocol must function so that all requesting processors receive the up to date value for that piece of data. The Level-2 MBus cache coherency mechanism requires that all processors snoop the MBus to determine if they have entries in their cache that are currently being accessed by another processor or I/O. This is in contrast to a directory structure mechanism which keeps a central database of cache entries.

The cache coherency protocol is a "write invalidate" protocol where the cache being written issues a Coherent Invalidate transaction if the line is not exclusive. This indicates to all caches that they should immediately invalidate the line since it contains "stale data". All caches "snoop" Coherent Read transactions and assert MSH* if the address of the transaction is present in their cache. If a cache is the owner, it asserts MIH* to tell memory to stop sending data then supplies the data to the requesting cache.

For example, if a processor requests data from main memory to be placed in its cache, and it is the first processor to request this data, then the data is marked RW in that processor's cache. The first processor's cache is now the "owner" of that data. If a second processor requests the same data, that data is marked Read Only in the second processor's cache. When another processor wants to write that data back to main memory, the first processor, since it is the owner, asserts MIH*. The second processor asserts MSH* to note that the data is actually shared.

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7.4 MBus Specification

7.4.1 Multiplexed Address Definitions

Table 7-1. **Multiplexed Address Definitions**

Signal Name	Physical Signal	Signal Description
PA[35.0]	MAD [35:0]	Physical Address
Type[3:0]	MAD[39:36]	Transaction Type
SIZE[2:0]	MAD[42:40]	Transaction Data Size
C	MAD[43]	Data cacheable (advisory)
Lock	MAD[44]	Bus lock Indicator (advisory)
MBL	MAD[45]	Boot Mode/local bus (advisory) (optional)
VA[19:12]	MAD[53:46]	Virtual address (optional) (Level-2)
Reserved	MAD[58:54]	Reserved for future expansion
SUP	MAD[59]	Supervisor Access indicator (advisory) (optional)
MID[3:0]	MAD[63:60]	Module identifier

7.4.2 Transaction Status-Bit Encoding

Table 7-2. **Transaction Status-Bit Encoding**

MERR*	MRDY*	MRTY*	Meaning
H	H	H	Idle cycle
H	H	L	Relinquish and Retry
H	L	H	Valid Data Transfer
H	L	L	Reserved
L	H	H	ERROR1 => Bus Error
L	H	L	ERROR2 => Time-out
L	L	H	ERROR3 => Un-correctable
L	L	L	Retry

7.4.3 MID Assignments

Table 7-3. **MID Assignments**

MID<3:0>*	Owner	Non-Harvard	Harvard
0000	DVMA		

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Table 7-3. **MID Assignments** (Continued)

MID<3:0>*	Owner	Non-Harvard	Harvard
0001-0010	Reserved		
0011	MVSIC VME Interface		VME Interface
0100-0111	Reserved		
1000	MBus master 0x8	Processor 0	Processor 0 I-Cache
1001	MBus master 0x9	Processor 1	Processor 0 D-Cache
1010	MBus master 0xA	Processor 2	Processor 2 I-Cache
1011	MBus master 0xB	Processor 3	Processor 2 D-Cache
1100	MBus master 0xC	(future)	(future)
1101	MBus master 0xD	(future)	(future)
1110	MBus master 0xE	(future)	(future)
1111	MBus master 0xF	Processor 0 - Level-1	Processor 0 - Level-1

7.4.4 Transaction Type One

Table 7-4. **Transaction Type One**

TYPE[3]	TYPE[2]	TYPE[1]	TYPE[0]	Data Size	
H	H	H	H		Reserved
H	H	H	L		Reserved
H	H	L	H		Reserved
H	H	L	L		Reserved
H	L	H	H		Reserved
H	L	H	L		Reserved
H	L	L	H		Reserved
H	L	L	L		Reserved
L	H	H	H		Reserved
L	H	H	L		Reserved
L	H	L	H	32B	Coherent Read & Invalidate (CRI)
L	H	L	L	ANY	Coherent Write & Invalidate (CWI)
L	L	H	H	32B	Coherent Read (CRI)
L	L	H	L	32B	Coherent Invalidate (CI)
L	L	L	H	ANY	Read (RD)
L	L	L	L	ANY	Write (WR)

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7.4.5 Transaction Type Two

Table 7-5. **Transaction Type Two**

SIZE[2]	SIZE[1]	SIZE[0}	Transaction Size	# of 64-bit Transactions
L	L	L	Byte	1
L	L	H	2 Bytes	1
L	H	L	4 Bytes (Word)	1
L	H	H	8 Bytes (Double-word)	1
H	L	L	16 Bytes	2
H	L	H	32 Bytes	4
H	H	L	64 Bytes	8
H	H	H	128 Bytes	16

7.5 MBus Module Address Space

7.5.1 CPU Core Addresses

– (ASI = 0x4)

Table 7-6. **CPU Core Addresses**

A[31:0]	Description
0x0000 0000	Module Control Register
0x0000 0100	Context Table Pointer Register
0x 0000 0200	Context Register
0x0000 0300	Synchronous Fault Status Register
0x0000 0400	Synchronous Fault Address Register
0x0000 0500	Asynchronous Fault Status Register
0x0000 0600	Asynchronous Fault Status Register
0x0000 0700	Reset Register

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7.5.2 MBus Module System Space

Table 7-7. **MBus Module System Space**[a]

PA[35:24]	Description
0xFF0	EPROM
0xFF1	System Control Space
0xFF2 - 0xFF7	Reserved
0xFF8	Control space for Module MBus master #8
0xFF9	Control space for Module MBus master #9
0xFFA	Control space for Module MBus master #A
0xFFB	Control space for Module MBus master #B
0xFFC	Control space for Module MBus master #C
0xFFD	Control space for Module MBus master #D
0xFFE	Control space for Module MBus master #E
0xFFF	Control space for Module MBus master #F

a. The 4M timer/counter register and interrupt address mapping is given in the SCC address map, instead of duplicating it here.

7.6 Transaction Semantics

7.6.1 Read Semantics

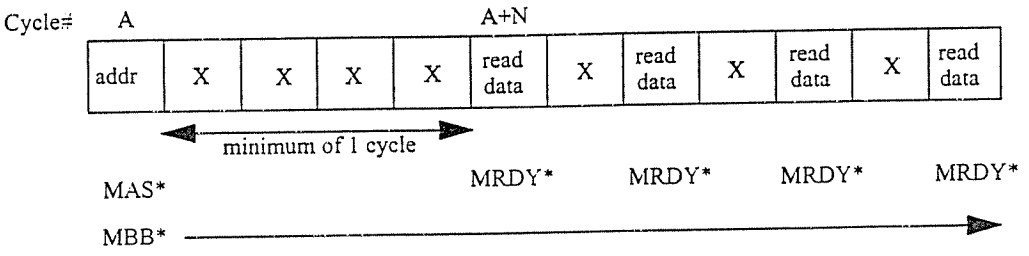


Figure 7-1. **Read Semantics Definition**

MBus Read operations can read data every cycle, i.e., the X delay is not necessary. The signals below the boxes in *Figure 7-1*show when the MBus signals are asserted. Read Transactions smaller than 8 bytes will have undefined values on the unused bytes. Note also that the delay between data reads can be any number of cycles.

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7.6.2 Write Semantics

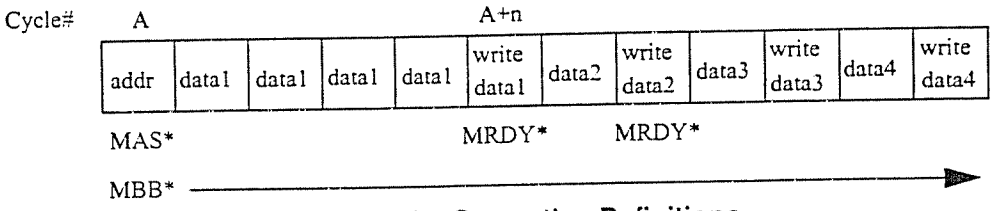


Figure 7-2. **Write Semantics Definitions**

On MBus writes, MRDY* signifies receipt of valid data. Due to the nature of the cache-consistency protocol, the Write transaction works equally well in Level-1 and Level-2 MBus systems. Thus write transactions do not need to be snooped and the MIH* and MSH* signals must not be asserted during writes.

Relinquish and Retry transactions to cacheable locations introduce a problem in that the write back buffer may be the only source of the most up to date data. The MBus specification eliminates the need of processors to snoop the write back buffers by requiring modules issue R&R jacks to capture the address of the cache line until they complete the transaction. If other modules attempt to read this line during the R&R transaction, the R&R issuing module must detect this and issue a R&R to the intervening CR, CRI transactions.

7.6.3 Relinquish and Retry Semantics

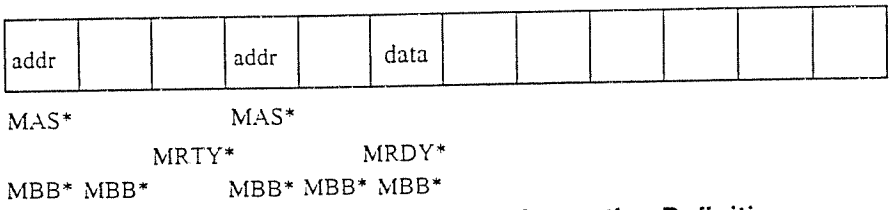


Figure 7-3. **Relinquish and Retry Semantics Definition**

When a slave device cannot accept or supply data immediately from the time of the request, it can issue a Relinquish and Retry acknowledgment cycle by asserting MRTY* for one cycle. The master relinquishes the bus and requests it again. Once the master has been granted the bus again, it retries the transaction that originally produced the R&R acknowledge. Note that there is a problem in Level-2 when a Coherent Invalidate turns into a Coherent Read and Invalidate, see CI Transaction Semantics below in *§ 7.6.6 Coherent Invalidate Semantics* on page 7-8. To resolve this situation for Level-2 modules, R&R acknowledges can only be issued on the first acknowledgment. Relinquish and Retry can occur when, e.g., a processor writes to the SBus, and while the SBus transfer is occurring, the processor releases the MBus. Another processor attempting to write to the same SBus location, would receive a Relinquish and Retry from the MSI.

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7.6.4 Retry Semantics

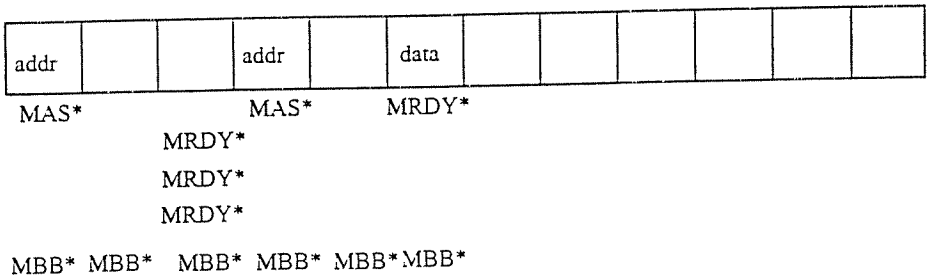


Figure 7-4. **Retry Semantics Definition**

Figure 7-4 represents a simple retry with no relinquishing of the bus by the master.

7.6.5 Coherent Read Semantics

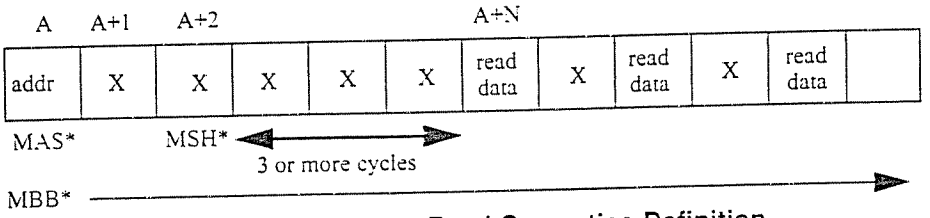


Figure 7-5. **Coherent Read Semantics Definition**

Coherent Read operations are block read operations that maintain cache coherency. If a snooping cache has a copy of the requested block, but is not the owner it asserts MSH* at cycle A+2 for one cycle and marks its copy as shared. If a snooping cache owns the requested block it will assert both MSH* and MIH* during cycle A+2 and start shipping the requested data no sooner than cycle A+6. If its copy of the block was market Exclusive, it will change that to Shared. If no other caches asserts MSH* during cycle A+2, the requesting master will mark its block Exclusive, if MSH* is asserted it will mark its block as Shared.

MIH* tells the requesting cache that it may have received stale data from memory, to ignore that data and to wait until the fourth clock after MIH* for the correct data. Memory upon seeing MIH* stops sending data immediately.

Note — Coherent Read and Coherent Read and Invalidate operations are the only cases where MIH* is asserted. The delay between data reads can be any number of cycles.

7.6.6 Coherent Invalidate Semantics

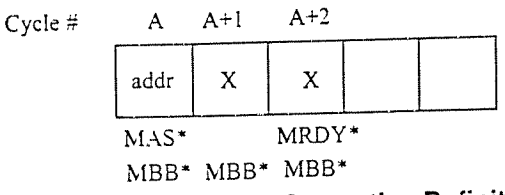


Figure 7-6. **Coherent Invalidate Semantics Definition**

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If an Invalidate operation hits in a cache, the copy in that cache will be marked invalid, immediately, regardless of its state. One module (usually the memory controller) is responsible for acknowledging the Coherent Invalidate transaction at cycle A+2 or later. Coherent Invalidate is issued when a write is performed into a cache line that is Shared. Before the write can occur, all other caches must have their copies of the block marked invalid. If a Coherent Invalidate transaction should receive a R&R acknowledgment, it is possible for the line which was about to be written to become invalid via an intervening invalidation transaction. If this occurs, when the original cache regains the bus it must execute a Coherent Read and Invalidate transaction to again allocate the block.

7.6.7 Coherent Read and Invalidate Semantics

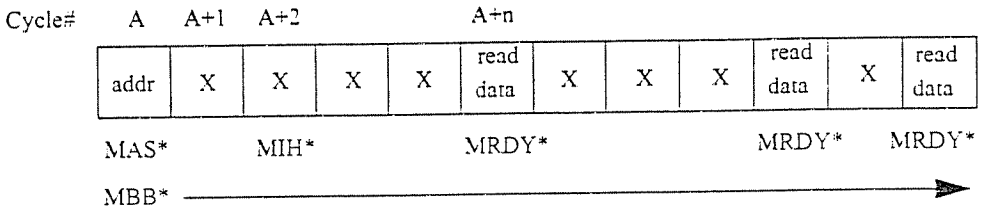


Figure 7-7. **Coherent Read and Invalidate Semantics Definition**

Caches that are performing a read and know that they intend to immediately modify the read data can decrease the MBus overhead by issuing this instruction. MIH* is asserted only if the data is exclusively owned and not shared. If a cache does not own the block then it invalidates the block regardless of the block's state. If the cache does own the block, then it asserts MIH* and supplies the data. After the data is successfully supplied, its copy is then invalidated. This is identical to a coherent read except that all caches will invalidate this block. MSH* is not driven during coherent read and invalidate operations.

Note — The delay between data reads can be any number of cycles.

7.6.8 Coherent Write and Invalidate Semantics

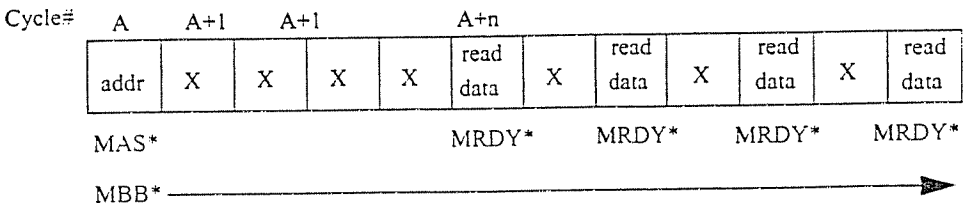


Figure 7-8. **Coherent Write and Invalidate Semantics Definitions**

Coherent Write an invalidate transactions combine Write transaction with Invalidate truncations. If the requested address hits in a cache, then the other snooping caches will invalidate their copies of this block regardless of its state.

Systems that have MBus modules that use write through caches on one module and write back caches on another module are not guaranteed to preserve cache consistency and hence are not recommended as a possible MBus configuration.

Note — The delay between data reads can be any number of cycles.

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7.7 Cache Coherency State Machine

In the figure below, dirty means that the block of data has been written to a write back cache which means that cache "owns" the data. A block of data is exclusive if there is only one cache in the system that has a valid copy of that block. A block of data is shared if there is more than one cache in the system that has a valid copy of the data. Missing from *Figure 7-9* below are the lines for the CI, CRI and CWI operations which lead any state to the invalid state.

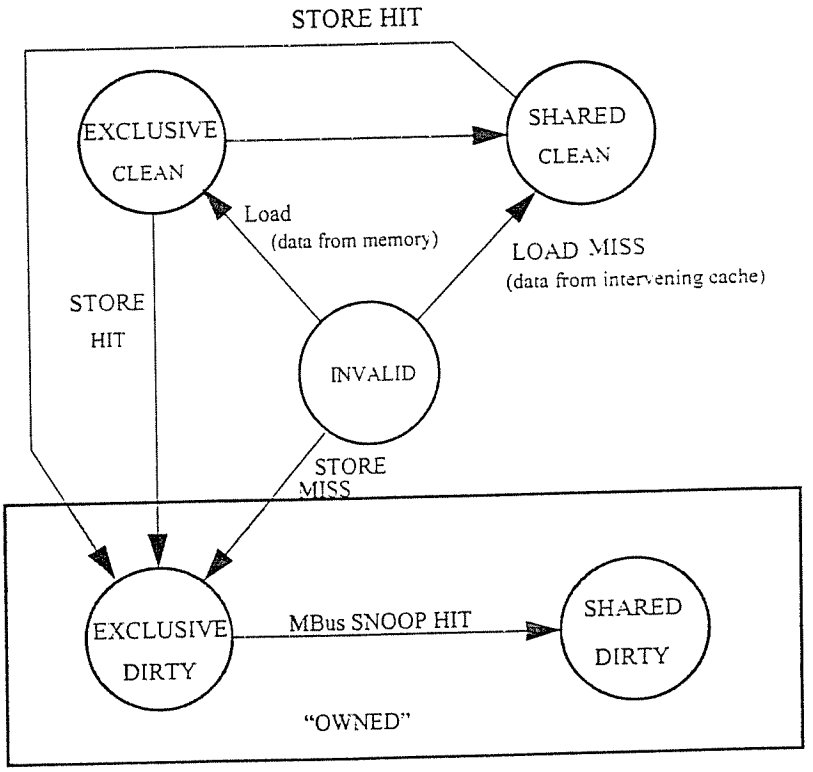


Figure 7-9. **Hit / Miss Cache Diagram**

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8

Memory Sub-System

8.1 Architecture and Implementation

8.1.1 EMC ASIC

The EMC is the ASIC that interfaces the MBus and the Memory Bus, operates as a MBus Slave only, and implements the full Level-2 MBus protocol. The EMC services MBus data requests by MBus masters from main memory (DRAM TSOPs). The EMC can receive data from the memory system after RAS* assertion in 4 clock cycles or 100ns. (Note that actual read access times are 7 clocks and line read time is at least 10 clocks. Cycle time is at least 11 clocks). The EMC can generate 128-byte burst transfers with sustained 32-byte transfers at a rate of 87MB per second. The EMC MBus read latency from MAS to first data is 7 MBus clocks. The SPARC 20MP memory system uses 60ns DRAMs.

8.1.2 Memory Bus

The memory bus in the SPARC 20MP is 128 bits wide for data and has 16 ECC checkbits. The SPARC 20MP's memory system accommodates up to four mezzanine memory boards. See *§ 8.5 Memory Board* on page 8-7 for additional details on the Mezzanine Memory Board.

8.1.3 Memory Board Slot Address Mapping

Each Mezzanine Memory Board (MMB) slot has 128MB of address space allocated to it (i.e., slot0 starts at address 0, slot1 starts at address 0x800 0000, and slot2 starts at address 0x1000 0000). Thus regardless of whether or not there is a 128MB MMB in slot0, the MMB in slot1 responds to addresses starting at 128MB from 0 or 0x800 0000. The Boot PROM determines what MMB is in which slot by observing the response from each slot while writing and then subsequently reading from the appropriate addresses.

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8.2 EMC Transaction Semantics

8.2.1 Read Semantics

– 32 Bytes

A Memory Read operation begins with a MBus data request from a MBus address, which is performed by asserting MAS* along with the address data is requested from being driven on the MAD[64] lines. If the EMC finds this data within its memory space, it puts the associated ROW Address (RowAD) onto the memory bus address lines, and then asserts RAS*. The EMC then puts the associated Column Address (ColAD) on the memory bus address lines while asserting CAS*. After the assertion of CAS*, the first data returns on the memory bus data [144] lines, 100ns after the initial assertion of RAS*. The data is buffered through the EMC in one cycle and sent out onto the MBus MAD[64] multiplexed data/address lines. Finally MRDY* is asserted while the data is returned on the MBus to acknowledge that the data transfer was successfully completed. The gap in the data transferred in the MBus at cycle 9 is because after the data is returned on the Memory MMB bus, the new address has to be sent out.

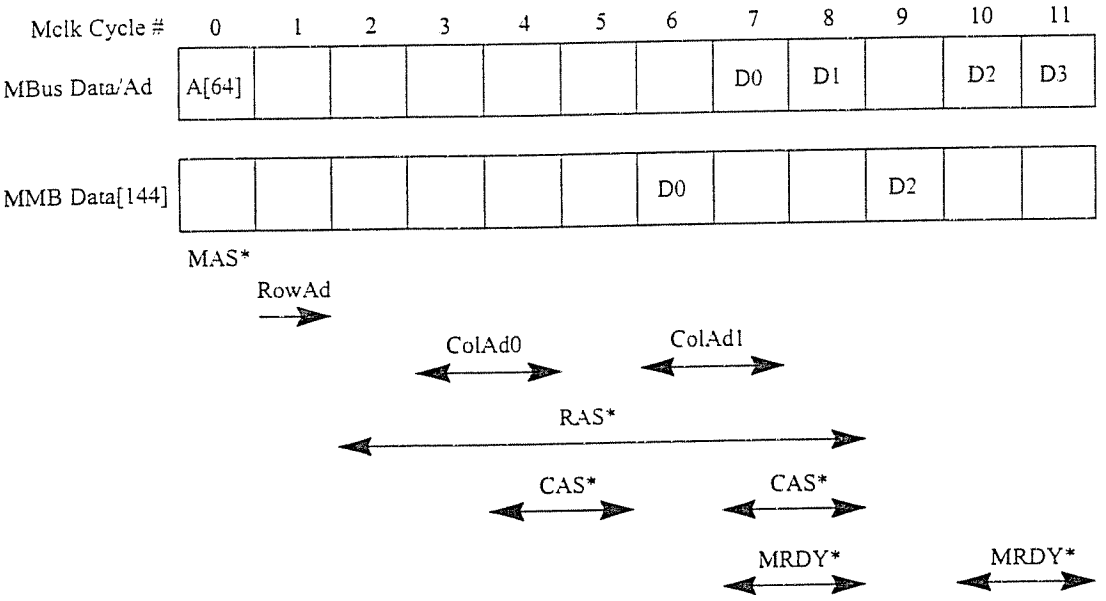


Figure 8-1. **Transaction Semantics Read Definition**

8.2.2 Write Semantics

– 32 Bytes

A Memory Write transaction begins with a MBus write request consisting of a main memory address asserted on the MBus MAD{64] lines, along with MAS*. The next cycle, the data to be written is asserted on the MBus MAD[64] lines, the first 4 Bytes being asserted on the MAD lines for two cycles, and then each consecutive 4 bytes being asserted on the MAD lines for one cycle. During the four cycles that each 4 bytes is asserted on the MBus MAD lines, MRDY* is asserted to acknowledge that this is a Valid Data Transfer. Once MRDY* is asserted, Ras* is asserted along with the specified Row MMB (RowAd). On the fifth cycle the data is asserted on the main memory MMB bus, along with Write Enable (WE*) which remains asserted

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for the next three cycles. On the third cycle the Column Address (ColAd0) is asserted and three cycles later Cas* is asserted at cycle 6, in which the first 144 bits of data are written. A new Column Address (ColAd1) is asserted on cycles 7 and 8 for which the data that was asserted on cycle 7 and 8 is written when Cas* is asserted on cycle 8.

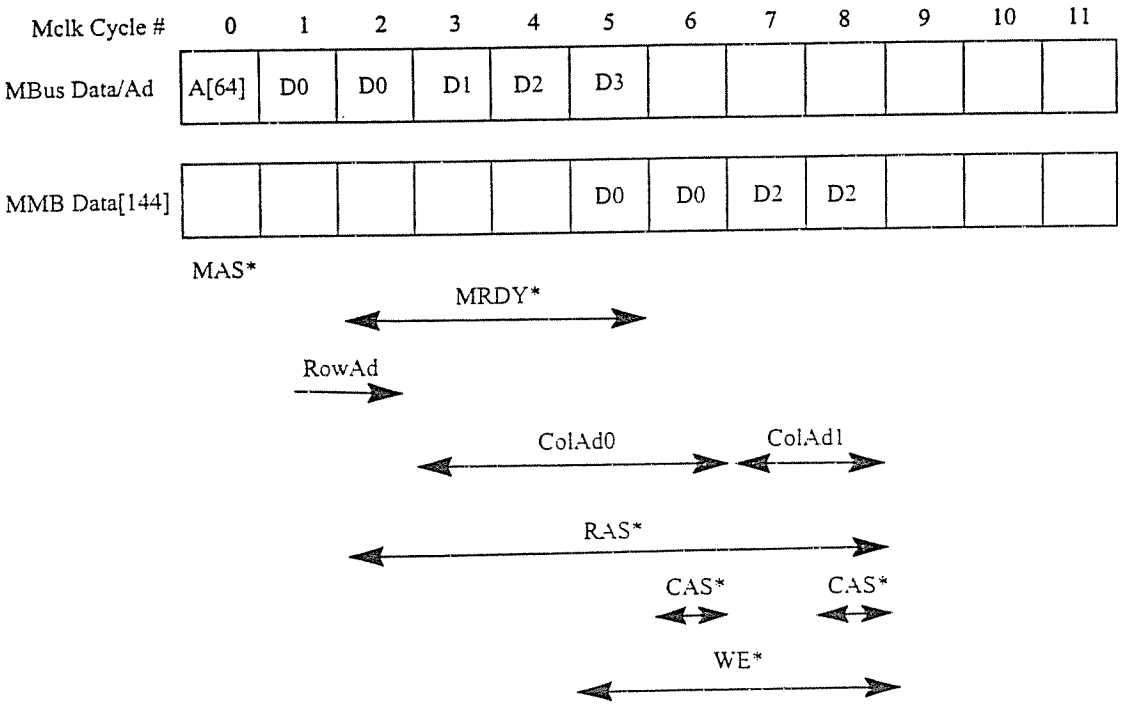


Figure 8-2. **Transaction Semantics Write Definition**

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8.3 EMC Address / Data / Control Paths

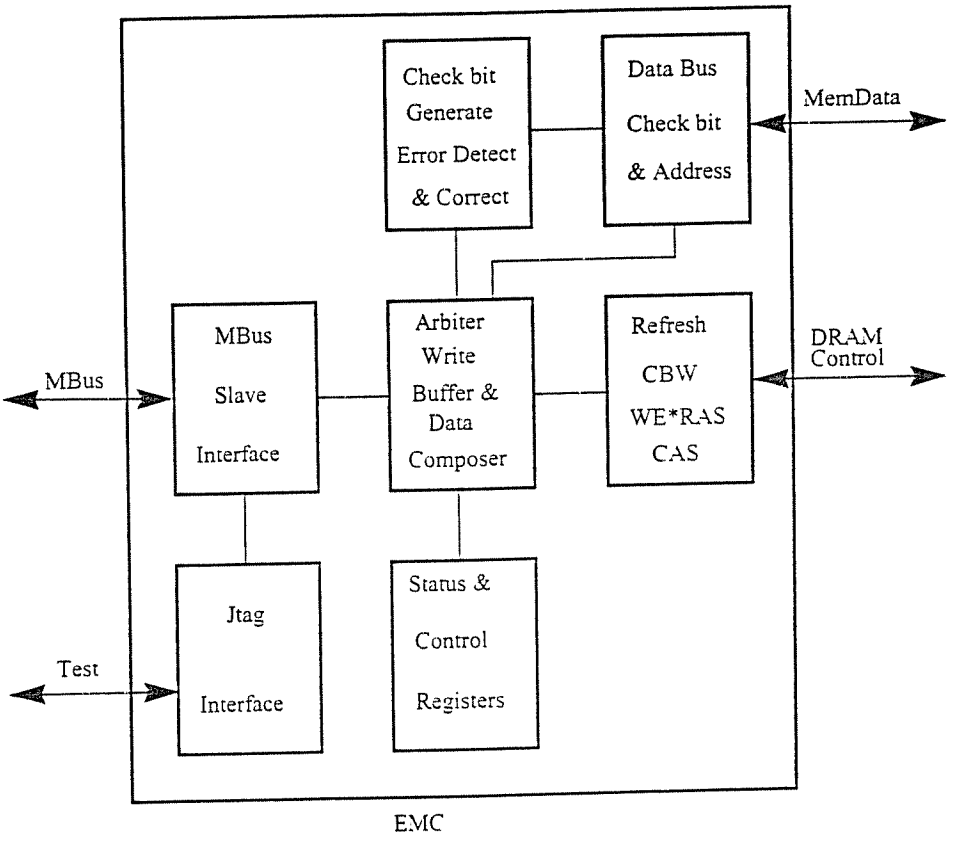


Figure 8-3. **EMC Address / Data / Control Paths**

8.4 Memory Enable Register

8.4.1 Memory Enable Register

Table 8-1. **Memory Enable Register Bit Definitions**

Bits	Type	Function
31:28	R	Implementation Number 0 = SPARCserver 10 1 = EMC 2 = SMC
27:24	R	Version Number
23:12		Reserved

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Table 8-1. **Memory Enable Register Bit Definitions** (Continued)

Bits	Type	Function
11	RW	CI 0 = Normal 1 = Inhibit
10	R	Memory Controller address map specifies EMC0 (=0) or EMC1 (=1) type of memory controller
9:2	RW	Memory Row Refresh. Specifies DRAM MMBs that need to be EMC refreshed
1	RW	Enable Correctable Error Interrupt
0	RW	Enable ECC defect and Correct

8.4.2 Memory Delay Register

Table 8-2. **Memory Delay Register Bit Definitions**

Bits	Type	Function
31	RW	Refresh Synchronize Count Reload (for clip-vector testing)
30:26	RW	Graphics arbitration delay from MBus. Zero allows MBus transfers to complete.
25:21	RW	MBus master MID = 8-F arbitration delay. Specifies maximum delay from a logged MBus request. before forcing interruption of in-progress graphics transfer.
20:16	RW	MBus master MID = 0-7 arbitration delay. Same as bits 25:21 except for MID = 0-7
15:13	RW	CINV response delay - The delay from MAS to MRDY for coherent invalidate cycles is given by a = [15:13] = 2. During the delay window, another master can preempt the EMC response. Only EMC0 can respond to CI cycles.
12:10	RW	Minimum Coherent MIH delay window - The delay from MAS to MRDY for coherent reads is given by a + [12:10] + 7
9:0	RW	Refresh request interval - Number of MBus clocks between refresh requests of the eight MMB rows.

8.4.3 Memory Fault Status Register

Table 8-3. **Memory Fault Status Register Bit Definitions**

Bits	Type	Function
31:18		Reserved
17	R	Transfer induced memory error. Set when DE or UE occurs during a graphics access
16	R	Multiple error. Multiple error occurring before clearing FAR sets this bit.

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Table 8-3. **Memory Fault Status Register Bit Definitions** (Continued)

Bits	Type	Function
15:8	R	Syndrome code for bit in error or stored check bits. This field contains syndrome code of memory fault
7:4	R	Double Word in a block with CE or UE. Pointer to double word in error
3	R	Un-correctable ECC error
2	R	Reserved
1	R	Mis-referenced slot error.
0	R	Correctable ECC error

8.4.4 Fault Address Register 0

Table 8-4. **Fault Address Register 0 Bit Definitions**

Bits	Type	Function
31:28	R	Module identifier of transaction's origin
27	R	Supervisor access indicator
26.22	R	Reserved
21:14	R	MBus virtual address VA[19:12]
13	R	Boot mode/local bus
12	R	Bus lock Indicator
11	R	Data cacheable
10:8	R	MBus transaction size-same encoding as MAD [42:40}
7:4	R	Transaction type - same encoding as MAD[39:36]
3:0	R	Higher 4 bits of Physical Address

8.4.5 Fault Address Register 1

Table 8-5. **Fault Address Register 1 Bit Definitions**

Bits	Type	Function
31:0	R	Lower 32 bits of the faulty Physical Address

8.4.6 ECC Diagnostics Register

Table 8-6. **ECC Diagnostics Register Bit Definitions**

Bits	Type	Function
31:11	R	Reserved

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Table 8-6. **ECC Diagnostics Register Bit Definitions** (Continued)

Bits	Type	Function
10	RW	0 = Normal 1 = Diagnostics Mode
9:8		Reserved
7:0	RW	Diagnostics forced check bits. When bit 10 =1, bits 7:0 are written to memory instead of the actual check bits. => allows arbitrary check bits to be written to memory

8.5 Memory Board

The SPARC 20MP memory system has a 128 bit wide data path with 16 bits of ECC (Error Correcting Code). The memory bus can have two RAS lines per MMB, two CAS lines, one WE*, and 12 bits of address. The SPARC 20MP Mezzanine Memory Boards (MMB) are double-sided using TSOP DRAMs and can be populated on either side or both sides. Each side of a MMB is equal to a SIMM in a SPARCstation 20. Thus, each MMB has the capacity of two SPARCstation 20 SIMMS.

The SPARC 20MP supports two types of memory modules, a 16/32MB version using 1Mx4 DRAMs and a 64/128MB version using 4Mx4 DRAMs. The SPARC 20MP memory system implementation with the EMC uses 60ns DRAMs to achieve 100ns data access time from RAS generation. The EMC supports the following densities of DRAMs on the MMBs:

Table 8-7. **Mezzanine Memory Board RAM Configurations**

RAM	Density	# of Rams	Capacity	
4MBit	(1Mx4)	36	16MB	ECC DRAM
16MBit	(4Mx4)	36	64MB	ECC DRAM

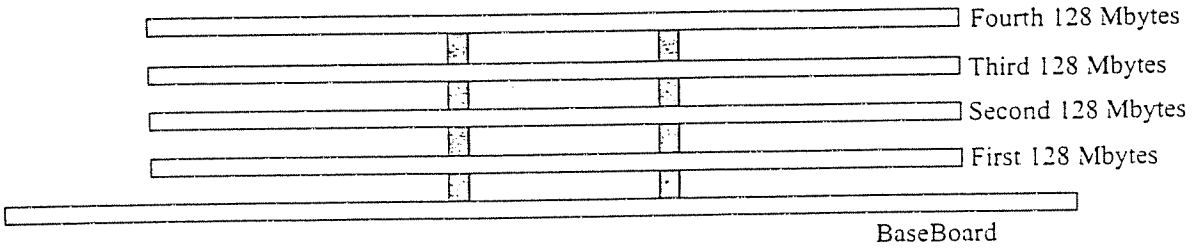


Figure 8-4. **SPARC 20MP Mezzanine Memory Board Positions**

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9

SBus

9.1 Introduction

The SBus is a system bus specification for Sun workstations. The SBus has a 32-bit data path, 28 bits of physical address, 3 data transfer size bits, 3 data transfer acknowledge bits, Bus Request and Bus Grant lines for Master transfer control of the bus, 6 Interrupt Request lines, Slave Select and Address Strobe lines to validate transfers a Late Error signal, a central Clock, a Data Parity line, a Reset* line, and power supply voltages at +/-12V and +5V and Ground for powering SBus cards.

Data transfers on the SBus are capable of one-byte transfers to DVMA burst transfers of 128 bytes, but the MSI implementation transfers a maximum of 32-bytes per DVMA burst. The reasons for this are two-fold.

- Since the data is buffered in the MSI ASIC, to buffer 128-byte data transfers require data buffers 4 times as large as those needed for 32-byte transfers. Since already half of the MSI chip is data buffers, larger buffers would be quite expensive.
- 32 bytes is a cache line size, and if the transfer is larger than that, the MSI would have to do a bit of work breaking the transfer up into cache line chunks. Transfers that are less than the cache line size, such as 16-byte transfers from the SBus to the MBus can saturate the MBus due to the concatenating of these 16 bytes into cache line chunk sizes, while executing Coherent Read Invalidate operations on the Mbus.

In DVMA data burst transfers, data can be transferred every cycle, as it is in the SPARC 20MP implementation. DVMA data transfer cycles begin with a Bus Request cycle. The bus request is then granted by the bus controller, and in the next cycle the bus master then sends out the virtual address of the place in main memory where it wants to transfer data to. That virtual address is translated in the bus controller's MMU to a physical address, and following that address translation, Address Strobe is brought low signaling the beginning of the data transfer cycle. Thus in the SPARC 20MP implementation, a 32-byte DVMA transfer would look like RGVTPKKKKKKKK, where:

- R = request
- G = grant
- V = virtual address
- T = translation
- P = physical address
- K = data transfer acknowledge

Then this cycle could be repeated again. Some performance and latency values are given in the MSI arbitration section.

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9.2 Slave Access

A SBus slave access transfer begins with that Slave's SlaveSel* being asserted along with AddressStrobe*. Read and Size<2:0> should have been asserted one cycle before SlaveSel* and AddressStrobe*. Physical Address bits <27:0> are asserted in the same cycle as Address Strobe*. When the Slave acknowledges the transfer, Address Strobe* is de-asserted as well as SlaveSel*, Read, Size<2:0>, and PA<27:0> signaling the send of the Slave Access Transfer.

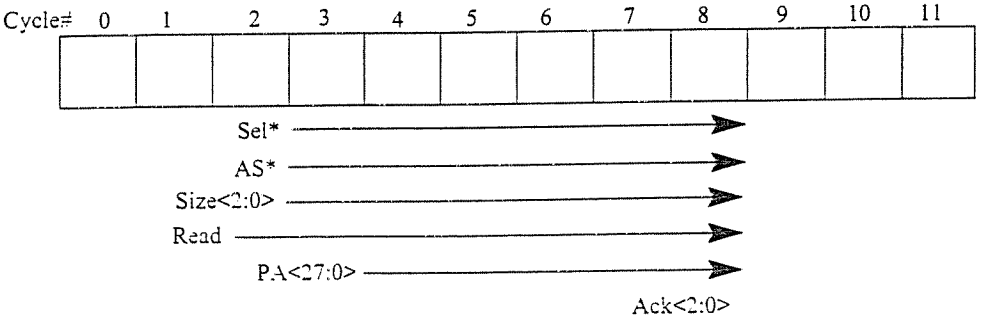


Figure 9-1. **Slave Access Timing Diagram**

9.3 Master Data Transfer

Master data transfer begins with a master requesting the SBus by asserting its own BusRequest* signal. The SBus controller (in the SPARC 20MP implementation the MSI) grants the bus to this master by asserting that master's BusGrant* signal. After the bus is granted to that master, the master sends out the virtual address on the data lines of where it wants to read (write) data from (to). In the case of a SBus card being accessed via a device drive, the device driver will select that physical memory, that the driver wants to use for transfers to/ from that card, will have the MMU translate the physical address of that section of memory to a virtual address and send that virtual address down the SBus to that device driver's SBus card for storage. It is this virtual address that the SBus card operating as a master sends out onto the SBus to have translated by the IOMMU (in the MSI) into a physical address. Read and Size<2:0> are sent out at the same time as the virtual address. Once the virtual address has been translated into a physical address, the master read/write transfer can occur, and this is indicated by the SBus controller asserting AddressStrobe* and SlaveSel*. After the slave acknowledges the transfer. AddressStrobe* and SlaveSel*. After the slave acknowledges the transfer, AddressStrobe* is de-asserted along with BusGrant* and SlaveSel*, Read, Size<2:0> are de-asserted one cycle later.

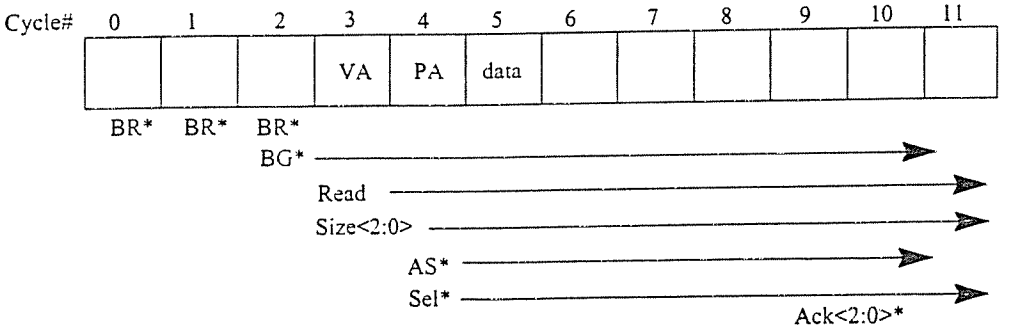


Figure 9-2. **Master Data Transfer Timing Diagram**

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9.4 DVMA Transfer

DVMA transfer (also called burst transfers) are data transfers that are greater than 4-bytes (= 32 bits) as indicated by the Size<2:0> bits. Since the transfer is larger than 32 bits, it takes more than one data transfer cycle to transfer all of the data. DVMA transfers are very similar to Master transfers except that there is an acknowledgment after each data transfer and before the next data transfer. Data can be transferred every cycle if the acknowledgments occur every cycle as well.

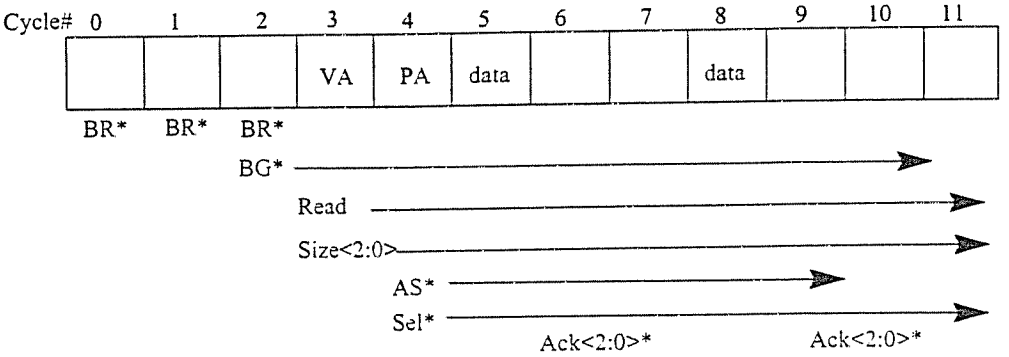


Figure 9-3. DVMA Transfer Timing Diagram

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10

MBus to SBus Interface (MSI)

10.1 Architecture and Implementation

The MSI ASIC provides the interface between the MBus and the SBus. The MSI internally contains the IOMMU of the Sun4M architecture including the TLB, the Base Address register, the IOMMU control register, Arbiter Enable register, M-to-S Asynchronous Fault Address register as well as the M-to-S Asynchronous Error register.

The MSI contains the SBus arbiter, and hence generates all SBus bus grants and receives all SBus bus requests. The MSI also contains the MBus arbiter, hence the MSI receives all MBus Bus Requests and generates all MBus Bus Grants. The MSI also has bi-directional pins for the following MBus signals: MAS*, MRDY*, MRTY*, MERR*, MBB*.

Table 10-1. **MSI Organization**

Transfer Type/Size	One Time Transfer(latency)	Sustained transfer(latency)
M->S Write / 32 bytes / 32	182 MB/s (7 MBus cycles)	71 MB/s (18 MBus cycles)
M->S Read / 32 bytes / 32	61 MB/s (21 MBus cycles)	61 MB/s (21 MBus cycles)
S->M Write / 32 bytes / 32	53 MB/s (12 SBus cycles)	
S->M Read / 32 bytes / 32	38 MB/s (17 SBus cycles)	

Note — The MSI allows for up to 16-word burst on the SBus, but only 8-word bursts or less between the SBus and MBus.

10.1.1 MBus and SBus Arbitration

The MSI is the main arbitration controller for both the MBus and SBus. The MBus and SBus are similar in function for master data transfers in that there are Bus Request and Bus Grant lines, which are point to point signals, and active low. Bus Request is used to signal to the bus controller (in the SPARC 20MP implementation the MSI is the bus controller for both the MBus and the SBus) that master requests exclusive use of the bus.

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The bus controller, when using its arbitration scheme, determines that it is a requesting master's turn to have the bus, signals that master by pulling that master's Bus Grant line low. The master then begins a master data transfer. The arbitration scheme is round robin, i.e., the last master to which the bus was granted is lowest on the priority list after that master relinquishes the bus. That master's neighbor is the next on the priority list for Bus Grants, and if the bus is not requested, then the last master's neighbor's neighbor is next on the priority list. This is true for both MBus and SBus.

There is one exception to this rule in that the MSI always has priority over the other bus requestors when the MSI wants the bus, either SBus or MBus. Of course to every exception to the rule there is an exception to the exception, which is that for the MBus, if for the last 16 Bus Grant cycles, the MSI was the bus master, then it becomes the lowest on the priority list. This exception is not true for the SBus. Upon reset, on the SBus the MSI has the highest priority and on the MBus, MBus module 0 has highest priority.

In the MBus, the master data transfer cycles begin with the MBus master requesting the bus by asserting its own MBus Bus Request signal, MBR*. When the bus is granted to this master, the MBus controller grants the bus by answering that master's MBus Bus Grant signal, MBG*. The granted MBus master can start using the bus by asserting MAS* (MBus Address Strobe) and MBB* (MBus Bus Busy), as soon as MBB* is de-asserted by the previous master. MBB* should be asserted immediately after the bus is granted as it is necessary to acquire and hold the bus. For atomic cycles it is possible for the granted master to keep MBB* active to retain control of the bus. One of the MBus address decoded fields is called Bus Lock, which allows the master to lock the device it is using, which prevents this device from being allocated to another bus master until MBB* is inactive, which unlocks the device.

In the SBus, master data transfer cycles begin with the SBus master requesting the bus using its dedicated SB_BR* (SBus Bus Request) signal, and the SBus controller granting the bus by activating that master's dedicated SB_BG* (SBus Bus Grant) signal.

If a MBus master starts a read-modify-write cycle to a SBus device, the MSI will freeze the arbiter until the atomic cycle is over. MBus to SBus device accesses always have the highest priority. Note also that the CPU cannot lock out I/O since once a MBus transaction has been processed, then the next SBus transaction is processed. For back to back SBus writes to MBus, the SBus is given highest priority.

10.1.2 MSI Address Map

Table 10-2. **MSI Memory Map**

PA[35:0]	Descriptions
0xE 0xxx xxxx	SBus Slot #0
0xE 1xxx xxxx	SBus Slot #1
0xE 2xxx xxxx	SBus Slot #2
0xE 3xxx xxxx	SBus Slot #3
0xE F0xx xxxx	Ethernet and SCSI
0xE F1xx xxxx	Flash #0, #1 (29F040)
0xE F2xx xxxx	Flash #2 (29F040)
0xE F3xx xxxx	Reserved
0xE F4xx xxxx	MACIO / Parallel
0xE F5xx xxxx	On-Board I/O / User LED, Rotary Switch

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Table 10-2. **MSI Memory Map** (Continued)

PA[35:0]	Descriptions
0xE F6xx xxxx	Reserved
0xE F7xx xxxx	Reserved
0xE F8xx xxxx	DBRI
0xE F9xx xxxx	Reserved
0xE FAxx xxxx	Reserved
0xE FBxx xxxx	Reserved
0xE FCxx xxxx	VME PIO and Slave I/F Control
0xE FDxx xxxx	SCV64
0xE FExx xxxx	Reserved
0xE FFxx xxxx	IACK
0xF xxxx xxxx	System Control Space
0xF E000 0000	IOMMU Control Register
0xF E000 0004	IOMMU Base Address Register
0xF E000 0014	Flush All TLB Entries
0xF E000 0018	Address Flush Register
0xF E000 0100 - 0xF E000 013F	IOMMU TLB CAM TLB TAG
0xF E000 014x	IOMMU TLB CAM WR VA
0xF E000 015x	IOMMU TLB CAM RD COMPARE
0xF E000 0200	IOMMU TLB RAM
0xF E000 1000	M-to-S Async Error Fault Status Register
0xF E000 1004	M-to-S Async. Error Fault Address Register
0xF E000 1008	Arbiter Enable Register
0xF E000 1010	Configure SBus Slot 0
0xF E000 1014	Configure SBus Slot 1
0xF E000 1018	Configure SBus Slot 2
0xF E000 101C	Configure SBus Slot 3
0xF E000 2000	MID Register
0xF F0xx xxxx - 0xF F1xx xxxx	SEC Register

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10.1.3 ECC Diagnostics Register

Table 10-3. **ECC Diagnostics Register-bit Definitions**

Bits	Type	Function
31:11		Reserved
10	RW	0 = Normal 1 = Diagnostics Mode

10.1.4 MSI Data and Control Path

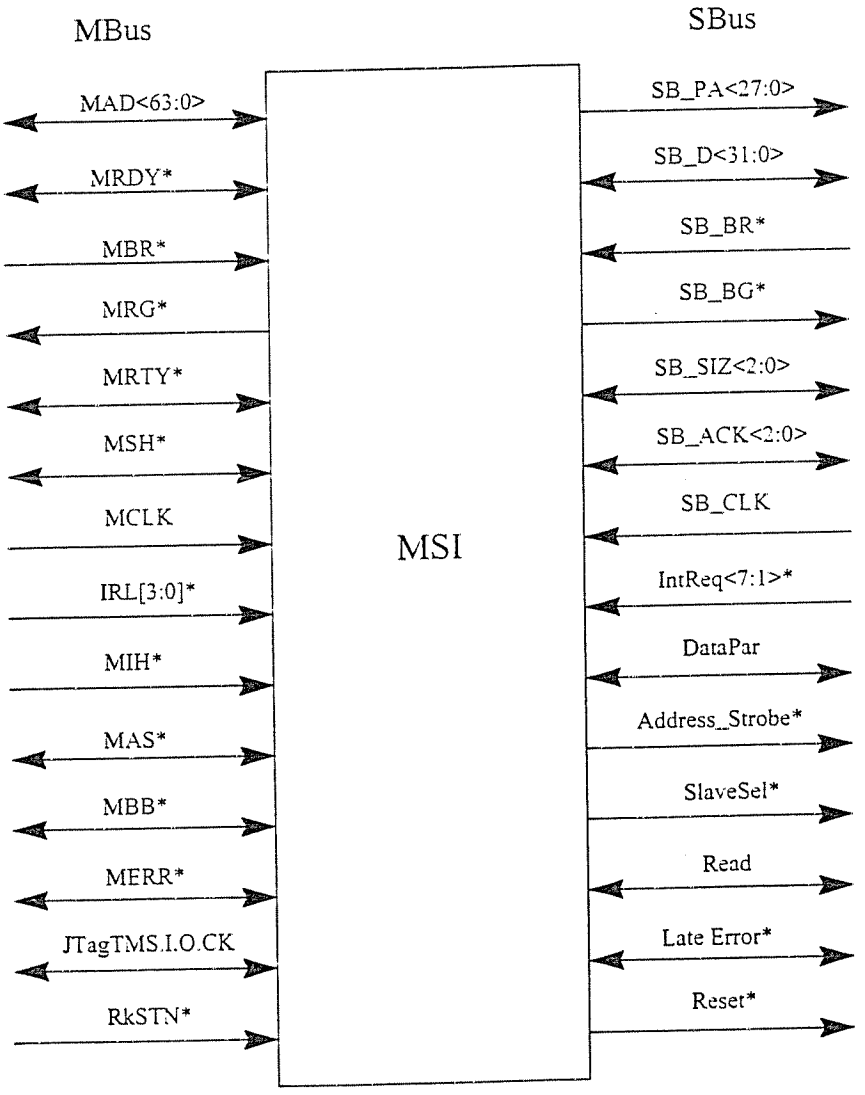


Figure 10-1. **MSI Data and Control Path Diagram**

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11.1 Architecture and Implementation

The peripheral DMA module resides within the MACIO chip. It provides the interface between the SBus and the following devices:

- SCSI
- AUI Ethernet
- 10Base-T Ethernet
- Parallel Printer Port

The DMA2 provides a 16-bit data and 24-bit address interface to the AMD 7990 LANCE chip. The AMD 7990 provides a data, clock and control interface to the AT&T 7213 Ethernet chip. The AT&T 7213 block interfaces to the isolation transformers for AUI and 10Base-T Ethernet. The DMA2 pin TP_AUI* is connected to the 7213, which selects between the AUI and 10Base-T types of Ethernet connection. The DMA2 block has a data and control bus that connects to a block (FAS101) directly interfacing to the SCSI bus. The DMA2 ASIC has a standard parallel port interface that connects to the VMEbus P2 connector. The parallel port signals are available directly on the VMEbus P2 connector or via an optional paddleboard with a standard DB25 connector. The pinout of the DB25 connector is identical to the IBM PC parallel port standard.

11.1.1 SBus to DMA2 Data and Control Paths

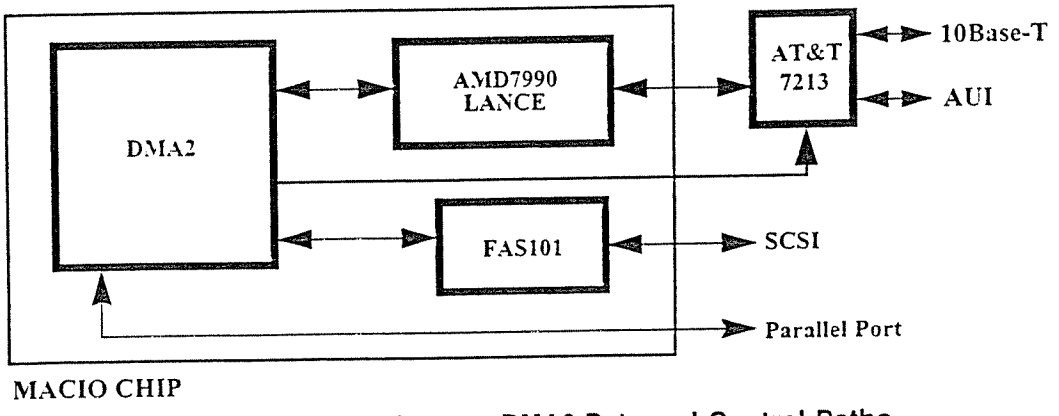


Figure 11-1. **SBus to DMA2 Data and Control Paths**

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11.2 DMA2 Address Map

Table 11-1. **DMA2 Address Map**

PA[35:0]	Descriptions
0xE F000 0000	DMA2 SBus ID Register
0xE F040 0000	DMA2 SCSI Control/Status Register (D_CSR)
0xE F040 0004	DMA2 SCSI Address Register (D_ADDR) / DMA2 SCSI Next Address Register (NEXT_ADDR)
0xE F040 0008	DMA2 SCSI Byte Count Register (D_BCNT) / DMA2 SCSI Next Byte Count Register (NEXT_BCNT)
0xE F040 000C	DMA2 SCSI Test Control/Status Register (D_TST_CSR)
0xE F040 0010	DMA2 LANCE Ethernet Control/Status Register (E_CSR)
0xE F040 0014	DMA2 LANCE Ethernet Test Cntrl/Status Register (E_TST_CSR)
0xE F040 0018	DMA2 LANCE Ethernet Cache Valid bits (E_VLD)
0xE F040 001C	DMA2 LANCE Ethernet Base Address Register (E_BASE_ADDR)
0xE F480 0000	DMA2 Parallel Port DMA Control/Status Register (P_CSR)
0xE F480 0004	DMA2 Parallel Port Address Register (P_ADDR)
0xE F480 0008	DMA2 Parallel Port Byte Count Register (P_BCNT)
0xE F480 000C	DMA2 Parallel Port Test Control/Status Register (P_TST_CSR)
0xE F480 0010	DMA2 Parallel Port Hardware Configuration Register (P_HCR)
0xE F480 0012	DMA2 Parallel Port Operation Configuration Register (P_OCR)
0xE F480 0014	DMA2 Parallel Port Parallel Data Register (P_DR)
0xE F480 0015	DMA2 Parallel Port Transfer Control Register (P_TCR)
0xE F480 0017	DMA2 Parallel Port Input Register (P_IR)
0xE F480 0018	DMA2 Parallel Port Interrupt Control Register (P_ICR)

11.2.1 ESP Address Map

Table 11-2. **ESP Address Map**

PA[35:0]	Type	Descriptions
0xE F080 0000	RW	Transfer Count Low Register
0xE F080 0004	RW	Transfer Count High Register
0xE F080 0008	RW	FIFO Data Register
0xE F080 000C	RW	Command Register
0xE F080 0010	RW	Status/Bus ID Register
0xE F080 0014	RW	Interrupt/Status Time-out Register

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Table 11-2. **ESP Address Map** (Continued)

PA[35:0]	Type	Descriptions
0xE F080 0018	RW	Seq Step/Sync Transfer Register
0xE F080 001C	RW	FIFO Flags Register
0xE F080 0020	RW	Configuration #1 Register
0xE F080 0024	RW	Clock Conversion Factor Register
0xE F080 0028	RW	Test Register
0xE F080 002C	RW	Configuration #2 Register

11.2.2 LANCE Ethernet Address Map

Table 11-3. **Lance Ethernet Address Map**

PA[35:]	Type	Descriptions
0xE F0C0 0000	RW	LANCE Data Port Register
0xE F0C0 0002	RW	LANCE Address Port Register

11.2.3 SCSI Control / Status Register

Table 11-4. **SCSI Control / Status Register Bit Definitions**

Bits	Type	Function
31:28	R	Device ID= ob1010
27	R	Next Address Loaded
26	R	Address Loaded
25	R	DMA On
24	RW	Enable Next
23	RW	Terminal Count Interrupt Disable
22	RW	Faster Mode - 3 SBus clocks/byte
21	RW	Two Cycle -2 SBus clocks/byte
20	RW	Diagnostics Mode
19:18	RW	Burst Size
17	RW	Disables draining of D-FIFO on Slave Reads
16	RW	Disable Draining of D-FIFO on Slave Writes
15		Reserved
14	RW	Terminal Count
13	RW	Enable internal byte count
12:10		Reserved

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Table 11-4. **SCSI Control / Status Register Bit Definitions** (Continued)

Bits	Type	Function
9	RW	Enable DMA
8	RW	DMA Write Direction
7	RW	Reset
6	RW	Slave Error
5	RW	Invalidate D-FIFO data
4	RW	Interrupt Enable
3:2	R	Draining D-FIFO to Memory
1	R	Error Pending
0	R	Interrupt Pending

11.2.4 Address and (Next Address) Register

Table 11-5. **Address and (Next Address) Register Bit Definitions**

Bits	Type	Function
31:0	RW(W)	VA[31:0]

11.2.5 Byte Counter and DMA Next Byte Counter Register

Table 11-6. **Byte Counter and DMA Next Byte Counter Bit Definitions**

Bits	Type	Function
31:24		Reserved
23:0	W	Byte Count

11.2.6 SCSI Test Control / Status Register

Table 11-7. **SCSI Test Control/Status Register Bit Definitions**

Bits	Type	Function
31	W	Load D-FIFO Address Register
30	W	Initiate a DMA burst Read from memory into D-FIFO
29	R	D-FIFO makes request for a SBus read or write
28	W	Write Count loads internal counter register
27	RW	Write Mode
26	RW	Force D-FIFO to drain

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Table 11-7. **SCSI Test Control/Status Register Bit Definitions** (Continued)

Bits	Type	Function
25	R	D-FIFO buffer is empty
24	R	D-FIFO buffer is full
23	R	D-FIFO is one SBus read burst short of full
22:6	R	D-FIFO has one SBus write burst of data left
5:0	RW	Number of bytes in D-FIFO buffer

11.2.7 Ethernet Control / Status Register

Table 11-8. **Ethernet Control / Status Register Bit Definitions**

Bits	Type	Function
31:28	R	Device ID = 0b1010
27:23		Reserved
22	RW	TP_AUI* - Switches between 10Base-T and AUI Ethernet
21	RW	Loopback Test
20	RW	Polarity of Pin-35
19:18	RW	Burst Size - 0 = 4 words, 1 = 8 words
17	RW	E-cache invalidated on slave writes to LANCE
16	RW	Disables buffering of slave writes to LANCE
15	RW	Modifies LANCE DMA Cycle
14:13		Reserved
12	RW	Read E-cache Draining Disable
11	RW	Write E-cache Draining Disable
10:8		Reserved
7	RW	Reset
6	RW	Slave Error
5	W	Marks E-Cache bytes invalid
4	RW	Interrupt Enable
3:2	R	Drain Dirty E-cache Data to Memory
1	R	Error Pending
0	R	Interrupt Pending

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11.2.8 Ethernet Address Register

Table 11-9. **Ethernet Address Register Bit Definitions**

Bits	Type	Function
31:24		Reserved
23:0	R	VA[23:0] - address at which LANCE is requesting a DMA transfer

11.2.9 Ethernet Test Control / Status Register

Table 11-10. **Ethernet Test Control / Status Register Bit Definitions**

Bits	Type	Function
31	W	Loads Address tag of LRU cache line
30	RW	Initiate burst read from memory into LRU cache line from Ethernet address
29	R	1 = Address in the Ethernet Address Register matches cache address tag
28	RW	R - Cache line is LRYU, W - Cache line market as LRU
27	RW	R - Cache line1 is draining, W - Causes cache line1 to drain
26	RW	R - Cache line0 is draining, W - Causes cache line0 to drain
25	RW	Determines meaning of Valid/Dirty bits of cache line 1
24	RW	Determines meaning of Valid/Dirty bits of cache line 1
23:0	RW	Reads (Writes) LANCE Address Register

11.2.10 Ethernet Cache Valid Bits Register

Table 11-11. **Ethernet Cache Valid Bits Register Bit Definitions**

Bits	Type	Function
31:0	RW	Valid / Dirty bits for LRU Ethernet cache line. Each bit corresponds to the byte of the same member in the LRU cache line.

11.2.11 Ethernet Base Address Register

Table 11-12. **Ethernet Base Address Register Bit Definitions**

Bits	Type	Function
31:0	RW	High order 8 bits of address for Ethernet DMA transfers

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11.2.12 Parallel Port DMA Control / Status Register

Table 11-13. **Parallel Port DMA Control / Status Register Bit Definitions**

Bits	Type	Function
31:28	R	Device ID = 0b1010
27	R	Next Address and Byte Count Valid
26	R	Address Valid
25	R	DMA On
24	RW	Enable DMA Chaining
23	RW	Terminal Count Interrupt
22:21		Reserved
20	RW	Diagnostics
19:18	RW	Burst Size
17:15		Reserved
14	RW	Terminal Count
13	RW	Enable Byte Counter
12:10		Reserved
9	RW	Enable DMA
8	R	DMA Direction
7	RW	Hardware Reset to Parallel Port
6	R	Slave Error
5	W	Invalidate P-FIFO data
4	RW	Interrupt Enable
3:2	R	P-FIFO is draining
1	R	Error Pending
0	R	Interrupt Pending

11.2.13 Parallel Port DMA Address Register

Table 11-14. **Parallel Port DMA Address Register Bit Definitions**

Bits	Type	Function
31:0	RW	Parallel Port DMA Address Counter

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11.2.14 Parallel Port Byte Count Register

Table 11-15. **Parallel Port Byte Count Register Bit Definitions**

Bits	Type	Function
31:24		Reserved
23:0		Parallel Port Byte Count

11.2.15 Parallel Port Test Control / Status Register

Table 11-16. **Parallel Port Test Control / Status Register Bit Definitions**

Bits	Type	Function
31	W	Loads Address tag of LRU cache line
30	RW	Initiate burst read from memory into LRU cache line from Ethernet address
29	R	1 = Address in the Ethernet Address Register matches cache address tag
28	RW	R - Cache line is LRYU W - Cache line market as LRU
27	RW	R - Cache line1 is draining W - Causes cache line1 to drain
26	RW	R - Cache line0 is draining W - Causes cache line0 to drain
25	RW	Determines meaning of Valid/Dirty bits of cache line 1
24	RW	Determines meaning of Valid/Dirty bits of cache line 1
23:0	RW	Reads (Writes) LANCE Address Register

11.2.16 Parallel Port Hardware Configuration Register

Table 11-17. **Parallel Port Hardware Configuration Register Bit Definitions**

Bits	Type	Function
15		Allows the buried counter to be read
14:8	RW	Data Strobe and Acknowledge Pulse Widths
7		Reserved
6:0	RW	Data Setup to Strobe

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11.2.17 Parallel Port Operation Configuration Register

Table 11-18. **Parallel Port Operation Configuration Register Bit Definitions**

Bits	Type	Function
15	RW	Enables Memory Clear
14	RW	Data Source for memory clear operation
13	RW	Data Strobe bi-directional select
12	RW	Busy Bi-directional Select
11	RW	Acknowledge Bi-directional Select
10	RW	Enable Diagnostics Mode
9	RW	Buy Operation
8	RW	Acknowledge Operation
7	RW	Resets the Parallel Port
6:4		Reserved
3	R	Puts state machines in IDLE state
2		Reserved
1	R	V_ILCK bit
0	RW	Enable Versatec Operation

11.2.18 Parallel Port Data Register

Table 11-19. **Parallel Port Data Register Bit Definitions**

Bits	Type	Function
7:0	RW	8-bit read/write port

11.2.19 Parallel Port Transfer Control Register

Table 11-20. **Parallel Port Transfer Control Register Bit Definitions**

Bits	Type	Function
7:4		Reserved
3	RW	Direction Control
2	RW	Busy
1	RW	Acknowledge
0	RW	Data Strobe

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11.2.20 Parallel Port Output Register

Table 11-21. **Parallel Port Output Register Bit Definitions**

Bits	Type	Function
7:6		Reserved
5	RW	Versatec output 3
4	RW	Versatec output 2
3	RW	Versatec output 1
2	RW	Initialize
1	RW	Auto Feed
0	RW	Select In

11.2.21 Parallel Port Input Register

Table 11-22. **Parallel Port Input Register Bit Definitions**

Bits	Type	Function
7:3		Reserved
2	R	Paper Empty
1	R	Select Input
0	R	Error Input

11.2.22 Parallel Port Interrupt Control Register

Table 11-23. **Parallel Port Interrupt Control Register Bit Definitions**

Bits	Type	Function
15	RW	Data Strobe IRQ Pending
14	RW	Acknowledge IRQ Pending
13	RW	Busy IRQ Pending
12	RW	Paper Empty IRQ Pending
11	RW	Select IRQ Pending
10	RW	Error IRQ Pending
9	RW	Enables DS interrupt on rising edge of ds
8	RW	Enables ACK interrupt on rising edge of ack
7	RW	Busy Interrupt Polarity
6	RW	Enables Busy Interrupts
5	RW	Error Interrupt Polarity

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Table 11-23. **Parallel Port Interrupt Control Register Bit Definitions** (Continued)

Bits	Type	Function
4	RW	Enables PE Interrupts
3	RW	SLCT Interrupt Polarity
2	RW	Enables SLCT Interrupts
1	RW	Error Interrupt Polarity
0	RW	Enables ERR Interrupts

11.2.23 SCSI Control Register

Table 11-24. **SCSI Control Register Bit Definitions**

Bits	Type	Function
31:28	R	Engraves Type = 0x4
27:19		Reserved
18	RW	Enable Auto Drain feature
17	W	Drains buffer to memory
16	R	Parity Error
15	RW	Enables SBus parity checking
14	R	Interrupt Summary
13	RW	Enable interrupt upon terminal transfer count
12	R	Transfer count has expired; clears on load of counter
11	RW	DVMA burst size: 0 = 32 byte, 1 = 16 byte
10	R	Do not assert FLUSH or RESET when this bit is '1'
9	RW	Allow DMA between ESP and Interface
8	RW	Direction of DVMA transfer
7	RW	1 = Reset ESP and Interface
6	R	Slave access size error or access to ESP while reset is asserted
5	W	Resets DVMA state machine
4	RW	Enables bit 14 5o issue an interrupt to the system
3	R	Buffer 1 has data
2	R	Buffer 0 has data
1	R	SCSI DVMA received an SBus ERR ack
0	R	ESO interrupt is asserted

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11.2.24 SCSI DMA Count Control Register

Table 11-25. **SCSI DMA Count Control Register Bit Definitions**

Bits	Type	Function
31:24		Reserved
23:0	RW	SCSI DMA transfer count

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12.1 Architecture and Implementation

The SEC ASIC provides the interface between the SBus and the EBus. The EBus connects together the following devices:

- Two 85C30 serial port chips
- The 4MB boot EPROM
- The TOD/NVRAM chip
- The interface to the LED

One 85C30 chip provides Serial Ports A/B on the SPARC 20MP; ports A & B. The other 85C30 chip provides the Keyboard / Mouse port. UC5170 and UC5180 line drivers provide the serial port interface from the 85C30 chips to the serial ports.

The SEC has two operation modes: SPARC server mode and SPARC 20MP mode, selected by the mode pin SEC_MODE. In SPARC 20MP mode, the EBus is 8 bits of data and 16 bits of address.

12.1.1 Auxiliary Registers 1 and 2

The SEC has two Auxiliary Registers. The low order four-bits of each register are writable, and the high order four-bits of each register are readable. Bits 0-1 of each Auxiliary Register are inputs to the SEC, and bits 4-7 of Auxiliary Register 1 and bits 4-5 of Auxiliary Register 2 are outputs from the SEC.

Table 12-1. **Auxiliary Registers 1 and 2 Bit Definitions**

Bit	Type	Auxiliary Register 1	Auxiliary Register 2
7		Reserved	Reserved
6		Reserved	Reserved
5	R	Floppy double density	Reserved
4	R	Test Edge Jump In	Reserved
3	W	Link Test Enable	Reserved
2	W	Monitor Mux	Reserved

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Table 12-1. **Auxiliary Registers 1 and 2 Bit Definitions**

Bit	Type	Auxiliary Register 1	Auxiliary Register 2
1	W	Floppy Terminal Count	Reserved
0	W	LED	Power Off

Link Test Enable is active high. Set low for use with AT&T TPE Ethernet hubs. Set high to enable Link Test (default setting in the Boot PROM). Link Test is an input to monitor the 7213 Link Test Status. If Link_Test is low, Link Test is enabled at both 20MP and the hub. If Link_Test is high or fluctuates, then either Link_Test is not enabled correctly on both ends or the cable is not connected.

Monitor Mux is active high and muxes the monitor serial port in the 53C90 and disables the mouse serial port.

12.1.2 Data and Control Paths

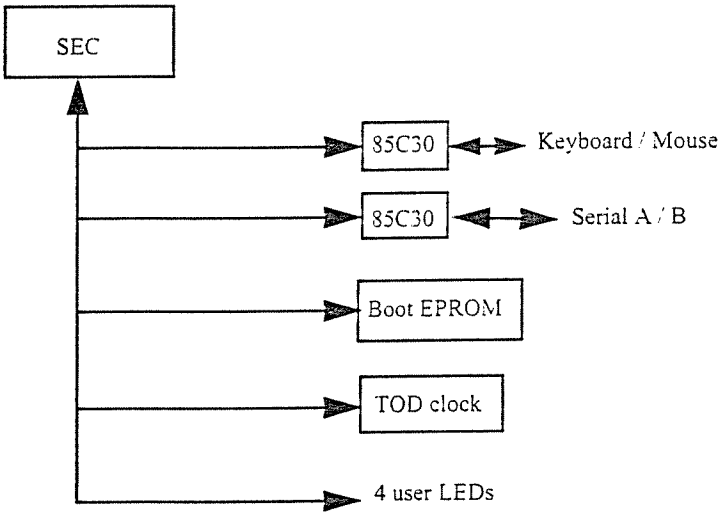


Figure 12-1. **SEC Data & Control Paths**

12.2 SEC Register Maps

Table 12-2. **SEC Register Map Overview**

Address	Register
0xF F000 0000	PROM (4MBits)
0xF F010 0000 - 0xF F0F0 0000	Reserved
0xF F100 0000	Keyboard/Mouse
0xF F110 0000	Serial Ports
0xF F120 0000	RTC

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Table 12-2. **SEC Register Map Overview** (Continued)

Address	Register
0xF F130 0000	Counter/Timer
0xF F140 0000	Interrupt
0xF F150 0000	Audio Port
0xF F160 0000	Reserved
0xF F170 0000	Floppy
0xF F180 0000	AUX1
0xF F190 0000	Reserved
0xF F1A0 0000	Generic & AUX2
0xF F1B0 0000 - 0xF F1E0 0000	Reserved
0xF F1F0 0000	System Status

12.2.1 SEC Internal Address Map

Table 12-3. **SEC Internal Address Map Bit Definitions**

PA[35:0]	Description
Counter/Timer	
0xF F130 0000	Processor 0 Counter Limit Reg/user TimerMSW
0xF F130 0004	Processor 0 Counter Reg/User Timer LSW
0xF F130 0008	Processor 0 Counter Limit Reg
0xF F130 000C	Processor 0 User Timer Start/Stop Register
0xF F130 1000	Processor 1 Counter Limit Reg/User Timer MSW
0xF F130 1004	Processor 1 Counter Reg/User Timer LSW
0xF F130 1008	Processor 1 Counter Limit Reg
0xF F130 100C	Processor 1 User Timer Start/Stop Register
0xF F130 2000	Processor 2 Counter Limit Reg/User Timer MSW
0xF F130 2004	Processor 2 Counter Reg/User Timer LSW
0xF F130 2008	Processor 2 Counter Limit Reg
0xF F130 200C	Processor 2 User Timer Start/Stop Register
0xF F130 3000	Processor 3 Counter Limit Reg/User Timer MSW
0xF F130 3004	Processor 3 Counter Reg/User Timer LSW
0xF F130 3008	Processor 3 Counter Limit Reg
0xF F130 300C	Processor 3 User Timer Start/Stop Register
0xF F131 0000	System Counter Register

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Table 12-3. **SEC Internal Address Map Bit Definitions** (Continued)

PA[35:0]	Description
0xF F131 0004	System Counter Limit Register
0xF F131 0008	System Counter Limit Reg
0xF F131 000C	Reserved
0xF F131 0010	Timer Configuration Register
Interrupt	
0xF F140 0000	Processor 0 Interrupt Pending Register
0xF F140 0004	Processor 0 Interrupt Pending Clear Register
0xF F140 0008	Processor 0 Soft Interrupt Set Register
0xF F140 1000	Processor 1 Interrupt Pending Register
0xF F140 1004	Processor 1 Interrupt Pending Clear Register
0xF F140 1008	Processor 1 Soft Interrupt Set Register
0xF F140 2000	Processor 2 Interrupt Pending Register
0xF F140 2004	Processor 2 Interrupt Pending Clear Register
0xF F140 2008	Processor 2 Soft Interrupt Set Register
0xF F140 3000	Processor 3 Interrupt Pending Register
0xF F140 3004	Processor 3 Interrupt Pending Clear Register
0xF F140 3008	Processor 3 Soft Interrupt Set Register
0xF F141 0000	System Interrupt Pending Register
0xF F141 0004	System Interrupt Mask Register
0xF F141 0008	System Interrupt Clear Mask Register
0xF F141 000C	System Interrupt Mask Set Register
0xF F141 0010	System Soft Target Register

12.2.2 SEC External Bus Address Map

Table 12-4. **SEC External Bus Address Map Bit Definitions**

PA[35:0]	Description
Keyboard / Mouse	
0xF F100 0000	Mouse Control Port
0xF F100 0002	Mouse Transmit (W) / Receive (R) Data Port
0xF F100 0004	Keyboard Control Port
0xF F100 0006	Keyboard Transmit (W) / Receive (R) Data Port
Serial Ports A/B	

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Table 12-4. **SEC External Bus Address Map Bit Definitions** (Continued)

PA[35:0]	Description
0xF F110 0000	Serial Port B Control Port
0xF F110 0002	Serial Port B Transmit (W) / Receive (R) Data Port
0xF F110 0004	Serial Port A Control Port
0xF F110 0006	Serial Port A Transmit (W) / Receive (R) Data Port
Audio / ISDN	
0xF F150 0000	Command (CR, Write) Interrupt (IR, Read) Register
0xF F150 0001	Data Register (DR)
0xF F150 0002	D-channel Status Register 1 (DSR1)
0xF F150 0003	D-channel Error Register (DER)
0xF F150 0004	D-channel Transmit/Receive Buffer
0xF F150 0005	Bb channel Transmit/Receive Buffer
0xF F150 0006	Bc channel Transmit/Receive Buffer
0xF F150 0007	D-channel Status Register 2
Floppy Disk Controller	
0xF F170 0000	Not used
0xF F170 0001	Not used
0xF F170 0002	Digital Output Register
0xF F170 0003	Not used
0xF F170 0004	Main Status Register (Read)
0xF F170 0004	Data Rate Select Register (Write)
0xF F170 0005	FIFO Data Port
0xF F170 0006	Reserved
0xF F170 0007	Digital Input Register (Read)
0xF F170 0007	Configuration Control Register (Write)
TOD Clock / NVRAM (EEPROM)	
0xF F120 0000 - 0xF F120 1FD7	NVRAM
0xF F120 1FD8 - 0xF F120 1FF7	IDPROM
0xF F120 1FD8	Format Code
0xF F120 1FD9	Machine Type
0xF F120 1FDA - 0xF F120 1FDF	Ethernet Address
0xF F120 1FE0	Date of Manufacture
0xF F120 1FE1 - 0xF F120 1FE3	Serial Number
0xF F120 1FE4 - 0xF F120 1FE7	CheckSum
0xF F120 1FF8	TOD Control Register

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Table 12-4. **SEC External Bus Address Map Bit Definitions** (Continued)

PA[35:0]	Description
0xF F120 1FF9	Seconds
0xF F120 1FFA	Minutes
0xF F120 1FFB	Hours
0xF F120 1FFC	Day
0xF F120 1FFD	Date
0xF F120 1FFE	Month
0xF F120 1FFF	Year
0xF F120 2000 - 0xF F12F FFFF	Reserved

12.3 SEC Registers

There are five sets of counter timers with one set for each processor generating a level 14 interrupt, and one set dedicated to the system generating level 10 interrupts. Only the Processor timer counters can be configured as user counters by writing to the configuration register. Three addresses are associated with each counter, a LIMIT register, a COUNT register and a load-Limit-without-affecting Count address. The COUNT and LIMIT registers all look alike.

12.3.1 Count and Limit Registers

Table 12-5. **Count and Limit Registers Bit Definitions**

Bits	Type	Function
31	R	Limit Bit
30:9	W	21 bit value
8:0		0000 0000

12.3.2 User Timer Register

Table 12-6. **User Timer Register Bit Definitions**

Bits	Type	Function
63	R	Limit bit
62:8	W	Count value
8:0		0000 0000

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12.3.3 Timer Configuration Register

Table 12-7. **Timer Configuration Register Bit Definitions**

Bits	Type	Function
31:4		Reserved
3	RW	Timer / Counter 3 0 = Counter / Timer 1 = User Timer
2	RW	Timer / Counter 2 0 = Counter / Timer 1 = User Timer
1	RW	Timer / Counter 1 0 = Counter / Timer 1 = User Timer
0	RW	Timer / Counter 0 0 = Counter / Timer 1 = User Timer

12.3.4 User Timer Start / Stop Register

Table 12-8. **User Timer Start / Stop Register Bit Definitions**

Bits	Type	Function
31:1		Reserved
0	RW	0 = Start Counter 1 = Stop Counter

12.3.5 Interrupt Target Register

Table 12-9. **Interrupt Target Register Bit Definitions**

Bits	Type	Function
31:2		Reserved
1:0	RW	Target Processor ID

12.3.6 System Interrupt Pending Register

Table 12-10. **System Interrupt Pending Register Bit Definitions**

Bits	Type	Function
31		Reserved
30	R	Module Error

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Table 12-10. **System Interrupt Pending Register Bit Definitions** (Continued)

Bits	Type	Function
29	R	IOMMU Error on M -to - S write buffer error
28	R	ECC Memory Error
27:22		Reserved
21	R	Module Interrupt
20		Reserved
19	R	Level 10 System Timer Interrupt
18	R	SCSI
17		Reserved
16	R	Ethernet
15	R	Serial Ports
14	R	Keyboard/Mouse
13:7	R	SBus Interrupts <7:1> or VME Interrupts <7:1>
6:0		Reserved

12.3.7 Mask Register

- Current Target Mask Register (R)
- Set Mask Register (W)
- Clear Mask Register (W)

Table 12-11. **Mask Register Bit Definitions**

Bits	Type	Function
31	R	Mask All Interrupts
30	R	Module Error
29	R	IOMMU Error on M -to- S write buffer error
28	R	ECC Memory Error
27		Reserved
26	R	Moonshine Interrupt 1: Expansion Memory Error
25:22		Reserved
21	R	Module Interrupt
20		Reserved
19	R	Level 10 System Timer Interrupt
18	R	SCSI
17		Reserved
16	R	Ethernet

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Table 12-11. **Mask Register Bit Definitions** (Continued)

Bits	Type	Function
15	R	Serial Ports
14	R	Keyboard/Mouse
13:7	R	SBus Interrupts <7:1> or VME Interrupts <7:1>
6:0		Reserved

12.3.8 Processor Interrupt Pending Register

Table 12-12. **Processor Interrupt Pending Register Bit Definitions**

Bits	Type	Function
31:17	R	SOFTINT<15:1>
16	R	0
15:1	R	HARDINT<15:1>
0	R	0

12.3.9 Processor Interrupt Clear Register

Table 12-13. **System Interrupt Pending Register Bit Definitions**

Bits	Type	Function
31:17	W	SOFTINT<15:1> Clear
16	W	0
15	W	HARDINT<15> Clear
14:0	W	0

12.3.10 Processor Soft Interrupt Set Register

Table 12-14. **Processor Soft Interrupt Set Register Bit Definitions**

Bits	Type	Function
31:17	W	SOFTINT<15:1> Set
16:0		Reserved

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12.3.11 System Control Status Register

Table 12-15. **System Control Status Register Bit Definitions**

Bits	Type	Function
31:4		Reserved
3	RW	Reset Switch
2	R	Diagnostics Mode Switch
1	RW	Set on soft SYS_RESET, clear on PowerOnReset
0	RW	Generates equivalent of a PowerOnReset

12.3.12 Auxiliary I/O Register 1

Table 12-16. **Auxiliary I/O Register 1 Bit Definitions**

Bits	Type	Function
7:6		Reserved
5	R	Floppy Density
4	R	Test Edge Connector Jumper are in
3	W	Link Test Enable
2	W	Monitory Mux
1	W	Floppy Terminal Count
0	W	LED 1 = On 0 = Off

12.3.13 Auxiliary I/O Register 2

Table 12-17. **Auxiliary I/O Register 2 Bit Definitions**

Bits	Type	Function
7:6		Reserved
5	R	Power Fail Detect (Not implemented in Power Supply, pulled high)
4	R	KeyBoard Power Interrupt (Not used, function performed in SW)
3:2		Reserved
1	W	Clear Power On Interrupt (Not needed since function is in SW)
0	W	Power Off

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13

MBus to VMEbus to SBus Interface Controller (MVSIC)

13.1 Overview

The MVSIC daughterboard provides the interface between the MBus, VMEbus, and the SBus for the SPARC 20MP. Its primary function is to provide:

- master access from the CPU to VMEbus slave devices
- slave access from the VMEbus master to local memory
- high speed DMA engine to transfer data
- bus requester
- interrupt requester for VMEbus

The MVSIC utilizes both MBus and SBus to connect SPARC 20MP to the VMEbus. The MBus is used for master access to VMEbus slave devices because its small latency time and large address space (full 32-bit address space). The SBus is used for slave access initiated by VMEbus master because the IOMMU inside the MSI chip for the SBus can protect the local memory through the DVMA function. Both master and slave accesses are implemented by FPGAs to enhance overall performance.

Other functions are implemented by SCV64 from Tundra Semiconductor Corporation (former Newbridge Microsystems) to provide system controller function, interrupt handler function, mailbox interrupt function and DMA engine. Due to performance issues on master and slave access, the master and slave access capability of SCV64 is not used. For detailed descriptions of MVSIC registers, please see *§ 4.4 On-Board SPARC 20MP Registers* on page 4-7.

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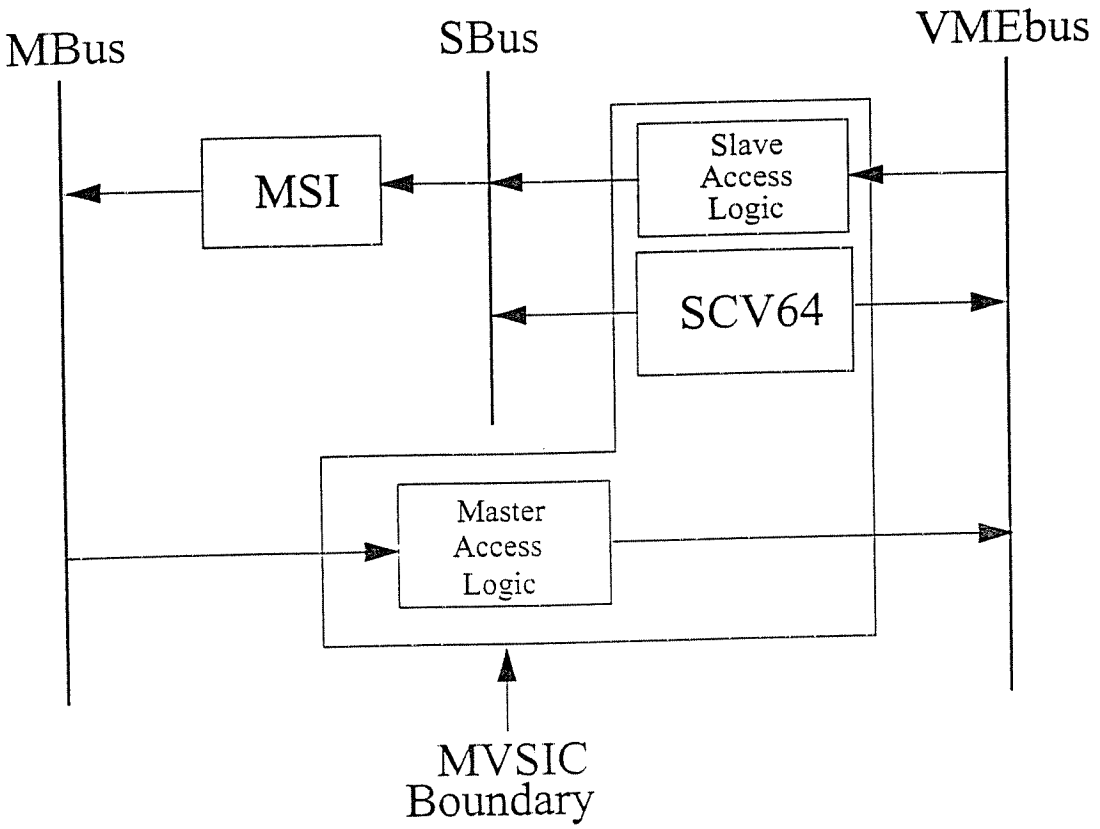


Figure 13-1. **MVSIC Block Diagram**

13.2 Features

13.2.1 MBus

- High performance 50 MHz clock MBus operation
- Fully supports Level I MBus slave interface
- Capable of setting supervisor bit when accessed by a VMEbus supervisory cycle
- Supports no MBus wrapping
- Supports 64-bit Read and Write cycles
- Supports Atomic Cycles (Read-Modify-Write cycles)
- Conforms to SPARC MBus Interface Specifications, Revision 1.2

13.2.2 SBus

- MVSIC uses standard SBus signals and is fully compliant with SBus Rev. B specification
- Does not support SBus-64

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13.2.3 VMEbus

- Supports VME64 master access when DMA engine is used
- Completely asynchronous VMEbus operation
- Fully supports VMEbus master and slave interfaces
- Capable of generating RMW cycle as a VME master
- Supports A32, A24 and A16 normal accesses
- Supports A32 and A24 block mode accesses
- Doesn't support unaligned transfers
- Features a round robin/fixed priority VMEbus arbiter
- Supports all 7 levels of Interrupt requests
- Conforms to the VMEbus specification version C.1

13.3 Functional Description of Major Building Blocks

13.3.1 MBus Interface

The MVSIC daughterboard only supports level 1 slave accesses listed in Table 13-1. Other slave access type will cause an MBus time-out.

Table 13-1. MBus Slave Operation Cycles

Type[3:0]				Size[2:0]			MBus Slave Operation
MAD[39]	MAD[38]	MAD[37]	MAD[36]	MAD[42]	MAD[41]	MAD[40]	
L	L	L	L	L	L	L	1 byte Write
L	L	L	L	L	L	H	2 byte Write
L	L	L	L	L	H	L	4 byte write
L	L	L	L	L	H	H	8 byte Write
L	L	L	L	L	L	L	1 byte Read
L	L	L	L	L	L	H	2 byte Read
L	L	L	L	L	H	L	4 byte Read
L	L	L	L	L	H	H	8 byte Read
L	L	L	L	H	L	L	16 byte Read

Three signals on the MBus are used to send acknowledgments back to the current MBus master when the MVSIC is acting as a MBus slave. The three remaining types of acknowledgment: Time-out, Uncorrectable Error and Retry are not used. In addition, MBus Wrapping is not currently supported.

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Table 13-2. **MBus Slave Acknowledgments**

MERR_	MRDY_	MRTY_	Meaning
H	H	H	Idle
H	H	L	Relinquish and Retry
H	L	H	Valid Data Transfer
L	H	H	Bus Error

13.3.1.1 Relinquish and Retry

A Relinquish and Retry (R&R) is issued whenever the MVSIC chip is busy attempting to acquire the VMEbus and cannot respond immediately to the master's VME transfer request. Deadlocks are resolved by issuing a R&R when the MBus is trying to access the VMEbus at the same time a VME master is trying to access the MBus.

13.3.1.2 Valid Data Transfer

For bus read operations, this acknowledgment means that the MVSIC has placed valid data onto the MBus. For write operations, this indicates that the MVSIC has accepted the data on the Mbus.

13.3.1.3 Bus Error

A Bus Error status is returned to the master if any Illegal Operations are attempted to the MVSIC address space by a MBus master. A Bus Error is also returned if the MVSIC was unable to obtain master-ship of the VMEbus or if the VME slave failed to respond in the specified time-out period.

13.3.2 VMEbus Arbiter

The MVSIC has the ability to act as the central arbiter for the VMEbus, which is configured by the system controller jumper. It supports all 4 bus request levels in either a fixed priority or round robin fashion. VMEbus Clear is asserted when a higher level of bus request is presented. This arbiter is implemented by SCV64 from Tundra Semiconductor Corporation.

13.3.3 VMEbus Bus Requester

MVSIC has the ability to request the VMEbus at any of the four Bus Request levels.

13.3.4 VMEbus Interrupt Handler

MVSIC supports the Interrupt Handler function by allowing the MBus processor to generate Interrupt Acknowledge cycles on the VMEbus. This is done through the SCVISR and IACK registers.

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13.3.5 VMEbus Interrupt Generator

A VMEbus Interrupt on any level can be generated by SCV64. It is controlled through the VMEbus Interrupt Requester at 0x8C offset of SCV64.

13.3.6 VMEbus Interface

The MVSIC has the ability to respond to, and generate, all combinations of A32, A24 and A16 address spaces with data widths of 32, 16 or 8 bits in either slave or master mode. The following table summarizes the accesses that the MVSIC is capable:

Table 13-3. **VME Master/Slave Transfer Cycle**

Transfer Cycle	VME Master	VME Slave
A32/D32	Normal & Block	Normal & Block
A32/D16	Normal	Normal
A32/D8	Normal	Normal
A24/D32	Normal & Block	Normal & Block
A24/D16	Normal	Normal
A24/D8	Normal	Normal
A16/D32	Normal	Normal
A16/D24	Normal	Normal
A16/D8	Normal	Normal

13.3.7 VMEbus A16 Slave Accesses

Currently, VMEbus A16 slave access is not supported on MVSIC.

13.3.8 VMEbus A24 Slave Accesses

A24 slave is controlled by the following registers:

- VME slave base address register at 0xE.FC00.0001.
- VME slave window size register at 0xE.FC00.0006.
- VME A24 DVMA slave base address configuration register at 0xE.FC00.0002.

The slave base address register controls the base address of A24 slave window. The VME slave window size register controls the size of the slave window. It also controls whether A24 slave is enabled or not. In addition to the above two registers, VME A24 DVMA slave base address configuration register also needs to be programmed to the DVMA window assigned by MSI IOMMU module, so that the A24 VME slave access can be channelled through MSI chip to MBus memory.

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13.3.9 VMEbus A32 Slave Accesses

A32 slave is controlled by the following registers:

- VME slave base address register at 0xE.FC00.0001.
- VME slave window size register at 0xE.FC00.0006.
- VME A32 DVMA slave base address configuration register at 0xE.FC00.0004.

The slave base address register controls the base address of A32 slave window. The VME slave window size register controls the size of the slave window. It also controls whether A32 slave is enabled or not. In addition to above two registers, VME A32 DVMA slave base address configuration register also needs to be programmed to the DVMA window assigned by MSI IOMMU module, so that the A32 VME slave access can be channelled through MSI chip to MBus memory.

13.3.10 VMEbus Master Accesses

MVSIC supports both D32 and D16 space. When D16 space is accessed, packing and unpacking is done automatically, so that the software does not need to be concerned about the port size of the slave VME devices.

A complete 32-bit space starting from 0x6.0000.0000 is allocated for VME D32 ports. Another 32-bit space starting from 0x7.0000.0000 is allocated for VME D16 ports.

In both D32 and D16 32-bit address space, the full 32-bit address space is split in the following way to allow all the A32, A24 and A16 slave VME devices to be accessible:

- In A32 address space, accesses are limited to the bottom 4GB - 16MB. The top 16 Mbytes are used for A24 slave devices.
- In A24 address space, accesses are limited to the bottom 16MB - 64KB. The top 64KBytes are used for A16 slave devices.
- In A16 address space, all the 64Kbyte space is accessible.

13.3.11 VMEbus Master Address Modifiers

The MBus Supervisor Access bit MAD[59] is also passed on as either Supervisory or Non-privileged accesses on the VMEbus.

13.3.12 VMEbus Master RMW Cycles

RMW cycles are supported when the Lock bit on the MBus transaction is asserted by preventing the VMEbus Arbiter from releasing the VME bus between the read and write cycles.

13.3.13 Interleaved Accesses

Since the MVSIC supports both master and slave accesses, interleaved accesses are also supported. For example, if the MVSIC is performing a DMA operation on the DMA bus, another VMEbus master is free to get onto the VMEbus and transfer data into the MBus memory. The DMA controller will suspend an ongoing transfer and resume the transfer as soon as the other VMEbus master releases the bus.

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14 SCV64

14.1 Overview

This chapter contains an abbreviated version of the specifications for the Tundra Semiconductor Corporation SCV64 VME Controller Chip. It is used in the SPARC 20MP to provide the following functions:

- system controller
- interrupt requester
- interrupt handler
- DMA engine.

Optionally, the mailbox can be used by the SPARC 20MP. If used, it will be at the top of allocated VMEbus A24 or A32 space for SCV64, i.e. these allocated VMEbus spaces will not be used by MVSIC A32 or A24 VMEbus slave access.

Note — This chapter describes the complete SCV64 chip. However, the master and slave access capability of this chip is not used in SCV64 due to its poor performance in these two areas.

14.2 Features

- VMEbus Rev. D compliant
- A32, A24, D32, D16, D08 (EO) Master capabilities and A64 capability when using DMA
- A16/D16, D08 master capabilities
- A32, A24 Slave capabilities with configurable slave window sizes (8/32/64/128MB) generating DVMA accesses
- Full VMEbus system controller functionality
- Automatic VMEbus SCON identification
- Interrupter and interrupt handling for all 7 VMEbus interrupt levels
- VME slave access protection
- Multiple VMEbus request and release options
- Multiple VMEbus arbitration schemes
- Integrated DMA controller

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14.3 General Description

The SCV64 is a single chip implementation of the 64-bit VMEbus interface compliant with IEEE Rev. D. The controller encompasses a rich set of programmable features and operational modes that make it ideally suited to CPU board implementations with both master and slave capabilities.



Warning — Not all features of the SCV64 controller are applicable to the SPARC 20MP design and certain capabilities and elements of the SCV64 have been superseded by custom implementations.

14.4 SCV64 Registers

Table 14-1. **SCV64 Registers**

Register	Address	Name
DMA Local Address	0xFD00 0000	DMALAR
DMA VMEbus Address	0xFD00 0004	DMAVAR
DMA Transfer Count	0xFD00 0008	DMATC
Control and Status	0xFD00 000C	DCSR
Rx FIFO Data	0xFD00 0014	RXDATA
Rx FIFO Address Register	0xFD00 0018	RXADDR
Rx FIFO Control Register	0xFD00 001C	RSCTL
VMEbus Interrupt Vector	0xFD00 0024	IVECT
Tx FIFO Data	0xFD00 002C	TXDATA
Tx FIFO Address Register	0xFD00 0030	TXADDR
Tx FIFO Control Register	0xFD00 0034	TXCTL
Location Monitor FIFO Read Port	0xFD00 0038	LMFIFO
SCV64 Mode Control	0xFD00 003C	MODE
DMA VMEbus Transfer Count	0xFD00 004C	DMAVTC
VMEbus Interrupter Requester	0xFD00 008C	VINT
VMEbus Requester Register	0xFD00 0090	VREQ
VMEbus Arbiter Register	0xFD00 0094	VARB
ID Register	0xFD00 0098	ID
Delay Line Status Register 1	0xFD00 00C8	DLST1

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14.5 VMEbus System Controller

14.5.1 Bus Arbitration

The arbiter is enabled whenever the SCV64 is configured as system controller. The SCV64 provides all arbitration modes defined in the VMEbus specification. The arbitration module provides four programmable arbitration modes:

- Full Round Robin
- Priority 3; Round Robin 2, 1, 0
- Priority 3, 2; Round Robin 1, 0
- Full Priority

14.5.1.1 Arbitration Modes

All arbitration modes are determined by the ARB1 and ARB0 bits in the VARB register. Since the arbiter logic continuously samples the VARB register, any changes to these bits will immediately be reflected in the current arbitration mode. The default mode after reset is full Round Robin.

Table 14-2. **Arbitration Mode Settings**

Arbitration Mode	ARB1, ARB0 Setting
Full Round Robin	00
Priority 3, Round Robin 2,1,0	01
Priority 3 2; Round Robin 1,0	10
Full Priority	11

14.5.1.2 Arbitration Time-out

Arbitration time-out ensures that bus arbitration will resume if BBSY* is not asserted within 16µs of a bus grant signal. The time-out returns the arbiter to its previous mode and outstanding requests. Arbitration time-out is enabled by default and is deactivated by clearing the ATEN bit in the VARB register.

14.5.2 Bus Timer

The SCV64 uses BERR* to terminate VMEbus data transfers if a slave does not respond within a specific programmed time. The time-out period before BERR* is driven low can be 16 µs, 32 µs, 64 µs (the default setting), or Never, depending upon the value of the VXL1 and VXL0 bits in the VARB register. The Never setting should only be used during system debugging, since the VMEbus cannot recover from errors (such as incorrect addressing) in this mode. Note also that the Auto-ID function depends on bus time-out.

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The timer is held reset while DS1* and DS0* are high, and begins running when either data strobe becomes asserted. At time-out, the SCV64 asserts and maintains BERR* until both DS1* and DS0* are high. Note that a race condition can occur if a slave takes a long time to respond and asserts DTACK* coincidentally with the SCV64 assertion of BERR*. Under these conditions, the master may see DTACK* and BERR* simultaneously. On-board logic may be required to resolve this conflict.

Table 14-3. **VMEbus Time-out Setting**

Time-out Period	VXL1, VXL0 Setting
Never	00
16µs	01
32µs	10
64µs (default)	11

14.6 VME Interrupter

The SCV64 can generate VMEbus interrupts on any of the seven VMEbus interrupt levels. VMEbus interrupt level and interrupt generation are controlled by the VMEbus Interrupter Requester (VINT) Register.

Table 14-4. **VMEbus Interrupter Requester - VINT (0x FD00 008C)**

Bit	Type	Function
7:4		Reserved
3	R	0 = No interrupt pending 1 = Interrupt is presently asserted
	W	0 = No effect 1 = Assert interrupt
2:0	RW	0 = Interrupter clears itself 1 = VMEbus Interrupt Level 1 2 = VMEbus Interrupt Level 2 3 = VMEbus Interrupt Level 3 4 = VMEbus Interrupt Level 4 5 = VMEbus Interrupt Level 5 6 = VMEbus Interrupt Level 6 7 = VMEbus Interrupt Level 7

The corresponding interrupt vector supplied upon IACK is programmed into the lower 8-bits of the VMEbus Interrupter Vector (IVECT) Register. (0xFD00 0024). Any reset will return the SCV64 registers to their default values. Thus all VMEbus interrupts will be deasserted.

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14.7 Location Monitor

The Location Monitor resides at the top longword (32 bits) of each A32 and A24 slave image and is accessible from both the local and VMEbus. The bottom (even) word of the Location Monitor is used for 16-bit messages. Since the Location Monitor replaces the long word of memory which otherwise exists at that address, writes to the Location Monitor are not turned into local cycles or entered into the RXFIFO. In addition, read accesses to the Location Monitor result in a bus error.

Writes to the Location Monitor are queued in the LMFIFO (32 bits wide and 31 stages deep) and read from the LMFIFO register. While there are entries in the LMFIFO, the SCV64 asserts LMINT and sets the LMHD bit in the DCSR register. Since LMINT is only asserted while there are entries in the LMFIFO, an interrupt service routine or polling of the LMINT signal can be used to test for entries in the LMFIFO and support various Location Monitor functions.

The CPU may write to its own Location Monitor through its slave image as it would any address on the VMEbus. The SCV64 address decoder responds by redirecting the message to the LMFIFO. From there the message is handled in the same manner as a write from the VMEbus side. If the condition occurs in which the local CPU and VMEbus write to the Location Monitor at the same time, the race condition is resolved and the writes queued without loss of either of the message providing space is available in the LMFIFO.

One function of the Location Monitor is as a command to exit BI-mode. When there is a write to the Location Monitor, the SCV64 is removed from BI-mode and the BIMODE signal is cleared.

Table 14-5. **Location Monitor FIFO Read Port - LMFIFO (0xFD00 0038)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Location Monitor FIFO Output Stage - Byte 3								Location Monitor FIFO Output Stage - Byte 2							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Location Monitor FIFO Output Stage - Byte 1								Location Monitor FIFO Output Stage - Byte 0							

14.8 DMA Transfers

The SCV64 performs all BLT and MBLT cycles through the DMA controller. During DMA transfers, the SCV64 is both the VME and local master. In case of a DMA write operation, the source address is contained in the DMA Local Address Register (DMALAR).

Table 14-6. **DMA Local Address Register - DMALAR (0xFD00 0000)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Not Used					DLA - Byte 3			DLA (DMA Local Address) - Byte 2							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DLA (DMA Local Address) - Byte 1								DLA (DMA Local Address) - Byte 0							0

DMA reads use the DMA VME Address Register (DMAVAR) for the source address.

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Table 14-7. **DMA VMEbus Address Register - DMAVAR (0xFD00 0004)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DVA (DMA VME Address) - Byte 3								DVA (DMA VME Address) - Byte 2							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DVA (DMA VME Address) - Byte 1								DVA (DMA VME Address) - Byte 0							

Data from the source address is transferred to the RXFIFO or TXFIFO for DMA read and write operations respectively.

The various addressing and data transfer modes applicable to the DMA operation are selected using the MODE register. The required bit settings for the supported addressing (A64, A32, A24) and data modes (D32, D16) are indicated below.

For A64 transfers, the MA64BAR register is used for the upper 32-bits of the source or destination address.

The size of the DMA transfer is controlled by both the DMATC register and the DTCSIZ bit in the MODE register. With the DTCSIZ bit cleared (default), the DMATC register will count up to 4096 32-bit transfers (16KB). If the DTCSIZ bit is set, the DMATC register will count up to 1,048,576 transfer (4MB).

Note — D16 transfer is not supported.

Table 14-8. **DMA Transfer Count Register - DMATC (0xFD00 0008)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Not Used								Not Used				DTC			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DTC (DMA Transfer Count)								DTC (DMA Transfer Count)							

The transfer count for VMEbus cycles is recorded in the DMAVTC register. The difference between the value in the DMATC register and the DMAVTC is equal to the number of entries in the RXFIFO or TXFIFO.

Table 14-9. **DMA VMEbus Transfer Count Register - DMAVTC (0xFD00 004C)**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Not Used								Not Used				DMA VME Xfer Count			
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DMA VME Transfer Count								DMA VME Transfer Count							

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14.9 SCV64 as VME Slave

in Decoupled Mode

14.9.1 Coupled Mode

Reads from a slave SCV64 are always coupled, although writes may be either coupled or decoupled. Coupled mode for VME slave write cycles is programmed by settings the RXATOM bit in the MODE register. If the bit is set while entries still exist in the RXFIFO, then the SCV64 completes all pending cycles in the RXFIFO before entering coupled mode. Clearing this bit returns the SCV64 to decoupled mode (its default settings).

While in coupled mode, the local bus is released after each local cycle. The exception is during MBLT slave reads in which the local bus is released every two local cycles. The SCV64 samples KDSACKn and KBERR on the falling edge of the local clock and ends the cycle when KDSACKm or KBERR are double sampled low. When the local cycle is terminated, the SCV64 asserts DTACK* to end the VMEbus cycle.

If a slave read is initiated while there are entries in its RXFIFO, the cycles in the RXFIFO will be completed before the coupled read is allowed. Similarly, the SCV64 will complete all entries in this TXFIFO before initiating a coupled master read cycle. In both cases the master CPU will execute wait states until the FIFO is empty. Completing pending write cycles before allowing reads ensures sequential consistency: this is, the data being read is the most current.

14.9.2 Decoupled Mode

Writes to a slave SCV64 may be either coupled or decoupled. The SCV64 is programmed for decoupled mode by clearing the RXATOM bit in the MODE register. The SCV64 defaults to decoupled mode.

After the slave address decoder and protection logic validate the access, write cycles from the VMEbus are loaded into the RXFIFO and acknowledged with DTACK on the VMEbus. If the access is protected, the SCV64 asserts BERR.

If the RXFIFO is full, the SCV64 does not accept writes until at least one is cleared from the RXFIFO, making space available. Note that the VMEbus data transfer rate is limited by the rate at which the slave local bus completes its cycles. Therefore, a full RXFIFO effectively couples the buses. If the RXFIFO cannot perform its writes on the local bus, the VMEbus transfer times out with a BERR signal.

Each 72-bit entry in the RXFIFO is made up of 3 components: - control, address, and data. The 3 components for the most current or last completed cycle (the oldest entry in the RXFIFO) are read from the - RXFIFO Control register, RXFIFO Address register, or the RXFIFO Data register.

The RXCTL register contains 6 control bits which qualify the RXFIFO entry. These control bits will:

- identify the entry as the beginning of a block transfer,
- indicate whether the entry is a BLT or MBLT cycle,
- provide the size of the cycle (longword, byte, word, or triple byte), and
- give the local function code for non-privileged or supervisory program and data space.

The RXADDR register is 32 bits and gives the RXFIFO output address. During MBLT cycles, this register provides the top 32 bits of the 64-bit data transfer. The RXDATA register is also 32 bits wide and provides the RXFIFO output data.

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The local bus is requested by the RXFIFO whenever entries appear. Arbitration of the local bus follows these priorities:

- **LBRQ1 (if SCV64 is not in default fair mode)**
- **the RXFIFO**
- **the DMA controller**

The RXFIFO is given priority over the DMA controller to ensure sequential consistency (the most current data is available). Entries in the RXFIFO are transferred to their indicated address by single local cycles or burst mode. Using zero wait state memory on the local bus, the SCV64 can transfer one longword every 3 clock cycles.

The SCV64 can be programmed to perform burst double clock write cycles. With a 33 MHz local clock, burst writes allow data transfer rates up to 62 MBytes/sec. Burst writes are enabled by setting the FIFOBEN bit in the MODE register. The BLEN1 and BLEN0 bits in the MODE register set the maximum burst length (4, 8, 16, or 32 longwords). The default setting for maximum burst length is 4 longwords.

If the FIFOBEN bit is set, then the SCV64 will initiate burst writes when there are 2 sequential MBLT entries or 4 sequential BLT entries in the RXFIFO. If a sufficient number of BLT or MBLT entries are queued, the SVC64 initiates a burst write. The burst write is terminated if the SCV64:

- encounters a different entry type (e.g., a BLT entry after a series of MBLT entries)
- completes its maximum burst length
- empties the RXFIFO

Unlike the TXFIFO, which is disabled by a VMEbus error, the RXFIFO is not disabled if a local bus error occurs. However, the RXFIFO can be disabled by setting the DISRX bit in the MODE register, (by default, the RXFIFO is enabled). If the RXFIFO is disabled, then it can only be emptied by using the RXSHFT bit in the DSCR register. Writing 1 to the RXSHFT bit discards the oldest entry and shifts the RXFIFO queue forward by one step. The VMEbus can still write to the RXFIFO if it is disabled, but doing so will set the LBERR bit in the DSCR register and cause VMEINT to be asserted. If the RXFIFO fills while it is disabled, then the pending VME cycles will time out.

14.10 SCV64 as VME Master

14.10.1 Coupled Mode

Master read cycles are always coupled, although writes may be either coupled or decoupled. Coupled mode for VME master cycles is programmed by setting TXATOM bit in the MODE register. If the bit is set while entries still exist in the TXFIFO, then the SCV64 completes all pending cycles in the TXFIFO before entering coupled mode. Clearing this bit returns the SCV64 to decoupled mode (its default setting).

In coupled mode, the CPU transfer is not queued by the TXFIFO but is directly linked to the VMEbus. The CPU enters wait states until a DTACK or BERR signal is generated by the VMEbus slave. The SCV64 copies the cycle termination through to the local master, which then ends the master local cycle. If BERR is received during the coupled cycle, the VBERR flag is set in the DCSR register, and VMEINT is asserted.

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If the SCV64 initiates a coupled slave read while there are still entries in its TXFIFO, the cycles in the TXFIFO will be completed before the coupled read is allowed. Similarly, the SCV64 will complete all entries in its RXFIFO initiating a coupled master write cycle. In both cases the master CPU must execute wait states until the FIFO is empty. Completing pending cycles before allowing subsequent coupled cycles ensures sequential consistency; that is, the data being read is the most current.

14.10.2 Decoupled Mode

Writes from a master SCV64 to a slave may be either coupled or decoupled. The SCV64 is programmed for decoupled write cycles by clearing the TXATOM bit in the MODE register. The SCV64 defaults to decoupled mode. In decoupled mode, writes to the VMEbus are loaded into the TXFIFO. The TXFIFO queues the entries and asserts KDSACK1 and KDSACK0 to terminate the master local cycle. In normal operation, the SCV64 requests the VMEbus as soon as entries appear in the TXFIFO. However, while the device is in DMA mode, the SCV64 can be programmed to request the VMEbus only when the TXFIFO is filled. This option is programmed by setting the FILL bit in the MODE register.

If the TXFIFO is full, the SCV64 does not accept writes until an entry is unloaded to the VMEbus, making space available. Note that the master local bus data transfer rate is limited by the rate at which the slave bus completes its cycles. Therefore, a full TXFIFO effectively couples the buses. If the TXFIFO cannot perform its writes on the VMEbus, the master local bus transfer times out with a KBEER signal. The user should consider the capabilities of slave buses and alternate between cycles for slower and faster buses.

Each 72-bit entry in the TXFIFO is made up of three components - control, address, and data. The three components for the most current or last completed cycle are read form the TXFIFO Control register, TXFIFO Address register, and TXFIFO Data register.

The TXCTL register contains 8 control bits which qualify the TXFIFO entry. These control bits:

- identify the cycle as MBLT or BLT
- provide information about transfer size (longword, byte, word, or triple byte)
- identify the address space (A32, A24, A16)
- distinguish whether the cycle is supervisory or non-privileged
- identify the data type as program or data

The TXADDR register is 32 bits and gives the TXFIFO output address. During MBLT cycle, this register provides the top 32 lines of the 64-bit data transfer. The TXDATA register is also 32 bits wide and provides the TXFIFO output data.

When a VMEbus BERR signal is received by the SCV64, it releases the bus, sets the VBERR bit in the DCSR register, asserts VMEINT and negates BRn.

While the VBERR flag is set, entries may still be queued in the TXFIFO until it reaches a full condition. After the TXFIFO is full, any local cycles will time out on the local bus. The TXFIFO is unable to dequeue cycles to the VMEbus until the VBERR flag is cleared. The TXCTL, TXADDR and TXDATA registers in the SCV64 record the values that were present at the output stage of the TXFIFO when the error occurred. They may be read by the CPU to obtain the address, data and control codes in the failed write cycle. This information can be examined by software to determine the fault, or used to rerun the cycle. The failed cycle will not remain in the TXFIFO when the VBERR bit is cleared, and must be regenerated in order for it to be retried.

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15.1 Architecture and Implementation

The 20MP clock chip provides the MBus and SBus clocks for the 20MP. There are 14 MBus clocks generated by the clock chip, one for each receiver. The MBus clock receivers are.

- 4 per MBus module (2 modules)
- EMC
- MSI
- 4 more for future expansion

There are also 5 SBus clocks:

- MSI
- SEC
- MACIO
- SBus slots 0 & 1
- SBus slots 2 & 3

The skew between MBus clocks at their receivers must be less than 1.5ns, the skew between SBus clocks at their receivers must be less than 2.5ns and the skew between MBus and SBus clocks at the MSI must be less than 2.5ns. The clock chip matches the trace lengths inside the die for the MBus clocks and the SBus clocks such that MBus clocks at the output pads of the die will have less than 50ps of skew. The same is true for SBus clocks. Since all MBus or SBus clock receivers (except for the SBus slots) have a separate clock driver pin per receiver, it is possible to match the trace lengths; taking into account the capacitive loading variation of the receivers, to guarantee that the MBus and SBus clocks at the receivers are within the specs for the respective clocks.

The clock chip provides a JTAG interface between the external Service Processor and JTAG circuitry on each of the ASICs that support JTAG. The clock chip contains a JTAG Tap Controller with a data register (no instruction register). The clock chip contains circuitry to decode the address sent to it by the Service Processor to send TMS to the appropriately selected ASIC or system. TMS provides the data for the selected JTAG receiver to transition through the states of its internal tap controller. The C2 tap controller is used to load data into the C2 Clock Control/Status register to start and stop the MBus and SBus clocks. JTAG data is sent out in series to each JTAG receiver and JTAG data is returned in series from all JTAG receivers. The same TMS is sent to all JTAG receives, i.e., there is one single JTAG scan ring, instead of multiple separate rings.

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15.1.1 System Reset Description

There are a number of different resets that are generated in the SPARC 20MP. There are two sources for these resets: POK (Power OK) and SV_RESET*. The POK is generated by the reset monitor (7705) in response to either the front panel reset or a VME sysreset and is disabled by removing the reset enable switch, solder bead (see *§ 3.12.2.1 Front Panel Reset Solder Bead* on page 3-21) or switch settings (see *§ 3.12.1.3 VMEbus Reset and NVRAM Write Protect Switch* on page 3-17). The SV_RESET* is generated by an optional, external, service processor (and is qualified by SV_MP* = Service Processor Present).

Note — POK is low for 100 ms after DC power from the power supply has stabilized, and then goes high (or True) and stays high.

Both POK* and SV_RESET* are inputs to the clock chip. These two resets are OR'ed together and produce the system reset output from the clock chip, called Board_Reset*. Since POK is asserted for about 100 ms., Board_Reset* is used as the reset for the MBus scan TMS2 pin. Board_Reset* is also an input to the SEC chip. The SEC chip sends out two resets, mem_rst* and sys_rst*. Sys_rst* has an active low duration of about 500ms and mem_rst* has an active low duration of about 70ms. Sys_rst* is then driven by a buffer, as "mrst", to Mbus reset, MSI chip, VME interrupt mask register, MVSIC, VME reset PAL, and the front panel LED driver/register. It is also driven by another buffer to the SBus module reset and to the MACIO chip SBus reset input, as signal "sbreset*".

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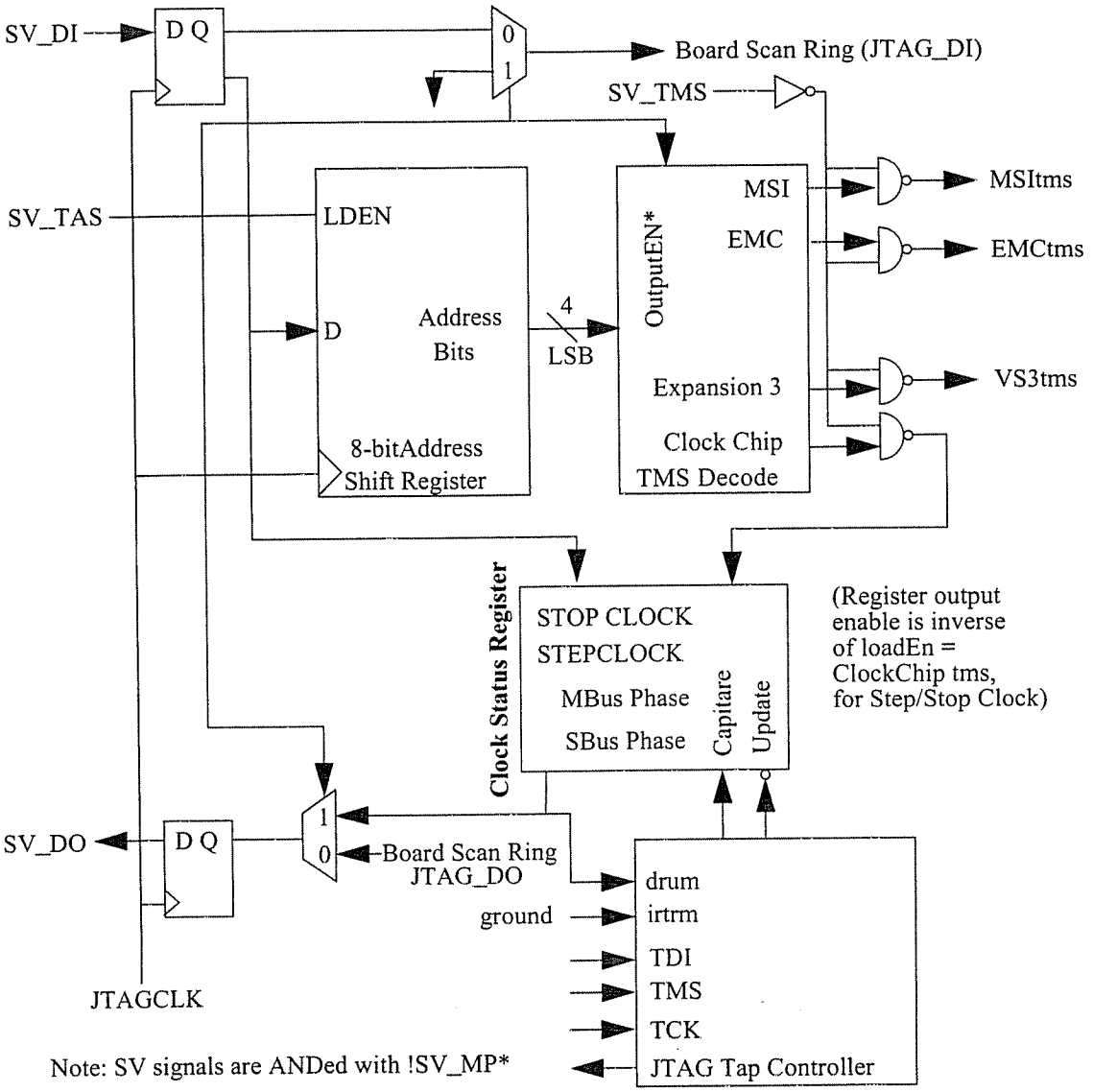


Figure 15-1. **Clock Chip Diagram**

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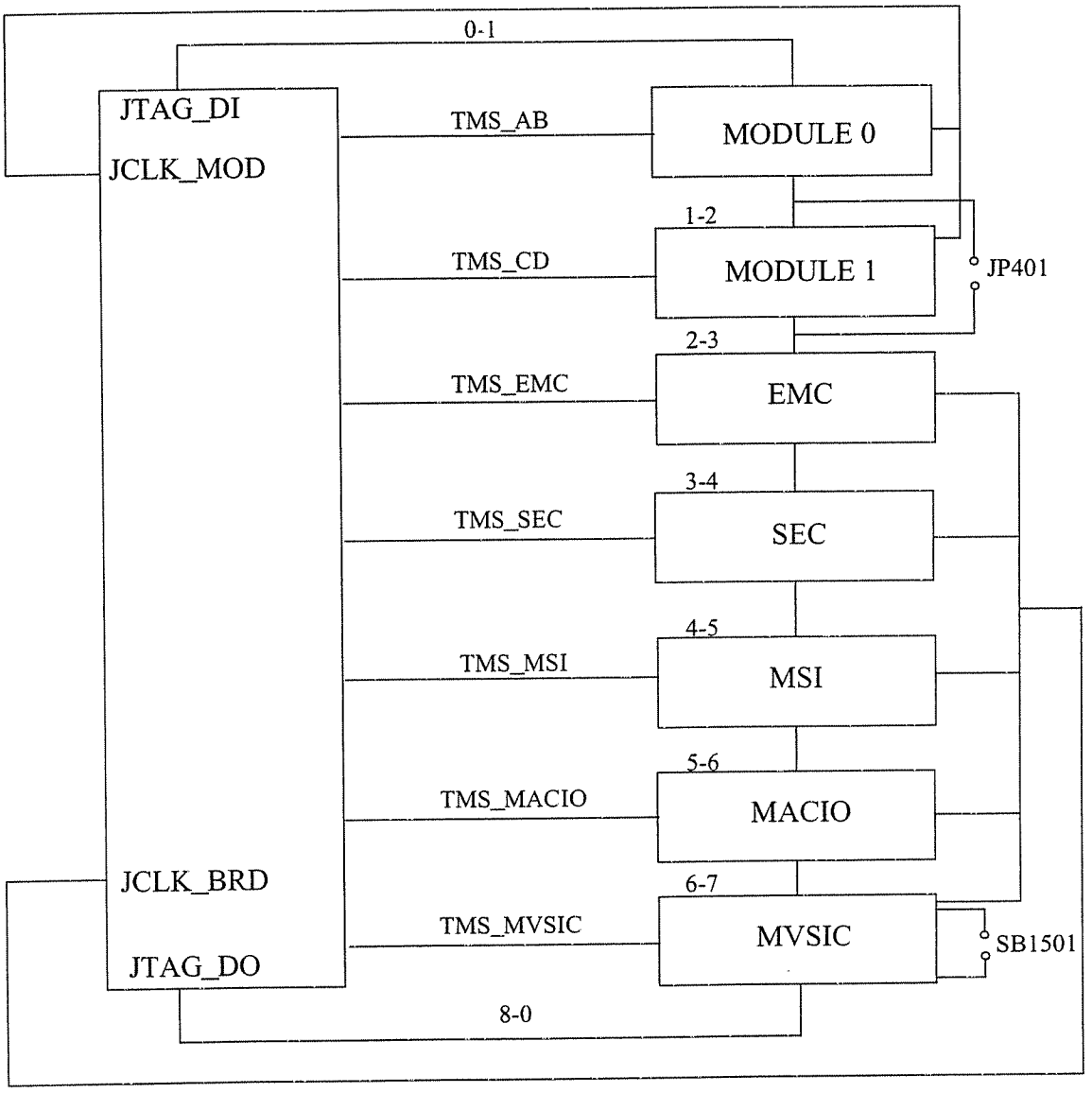


Figure 15-2. **JTAG Interface Diagram**

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16.1 Directed vs. Undirected Interrupts

There are two types of interrupts in the SPARC 20MP Architecture: directed and undirected. Directed interrupts must always be sent to a particular processor. The level-14 timer interrupt is directed. Undirected interrupts come from system devices and can be serviced by any processor.

16.2 Definitions of the Interrupts

Table 16-1. **Interrupt Definitions**

SPARC Level	MP20 SBus IRQ	SPARC 20MP
15		Asynchronous Error (broadcast), VMEERR, VME AC Fail,VME SysFail, and Abort Switch
14		Per Processor Counter/Timer
13	SBus IRQ7/VME IRQ7	
12		Keyboard/Mouse, Serial
11	SBus IRQ6/VME IRQ6	
10		System Counter/Timer
9	SBus IRQ5/VME IRQ5	Module Interrupt
8		
7	SBus IRQ4/VME IRQ4	
6		On-Board Ethernet
5	SBus IRQ3/VME IRQ3	
4		On-Board SCSI
3	SBus IRQ2/VME IRQ2	
2	SBus IRQ1/VME IRQ1	
1		

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17.1 Register Window Architecture

The SPARC (Scalable Processor Architecture Reduced Instruction Set Computer) CPU design provides an instruction set, memory model, register definitions and trap definitions from which to implement CPU processors.

The SPARC architecture defines a CPU register file consisting of 32-bit registers that are broken up into register windows. There is a set of registers called Global registers that are always accessible regardless of the value of the Current Window Pointer (CWP, i.e., regardless of which register window is currently active). Global register #0 has all of its 32-bits set to zero. In each register "window" there are three sets of 8 registers, called In, Local and Out registers. The Out register sets of CWP+1 are the same registers as the In register set of CWP. The boundary conditions of the register windows is cyclic, i.e., if there are enough registers in a given implementation of the SPARC architecture for a maximum of 7 register windows, then the In registers of CWP = 7 are the same registers as the Outs of CWP = 0.

The reasoning for register windows is that when procedures call another procedure and want to pass parameters to the called procedure, the call would produce another register window, where the in-registers are equal to the out-calling procedure's registers to the called procedure's registers.

For more details, see the *SPARC Architecture Manual, Version 8.*

17.2 CPU Registers

17.2.1 Control Transfer Instructions

There are five basic Control Transfer Instructions (CTIs)

1. Conditional Branch (Bicc, FBfcc, CBcc)
2. Call and Link (CALL)
3. Jump and Link (JMPL)
4. Return from Trap (RETT)
5. Trap (Ticc)

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Table 17-1 below categorizes these Control Transfer Instructions.

Table 17-1. **Control Transfer Instructions**

CTI	Target Address Calc	Transfer Time
Bicc, FBcc, CBcc	PC-relative	Conditional-delayed
CALL	PC-relative	Delayed
JMPL, RETT	Register-indirect	Delayed
Ticc	Register-Indirect-vectored	Non-Delayed

A delayed control transfer changes control to the instruction at the target address after a 1-instruction delay. A conditional-delayed control transfer causes either a delayed or non-delayed control transfer depending on the value of the instruction's annul "a"-bit, and whether the transfer is conditional or not according to *Table 17-2* below.

Table 17-2. **Delayed Control Transfer Instructions**

a-bit	Type of branch	Description
0	Unconditional	Yes
0	Conditional, taken	Yes
0	Conditional, un-taken	Yes
1	Unconditional	No (annulled)
1	Conditional	Yes
1	conditional, un-taken	No (annulled)Process

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17.2.2 Window Registers

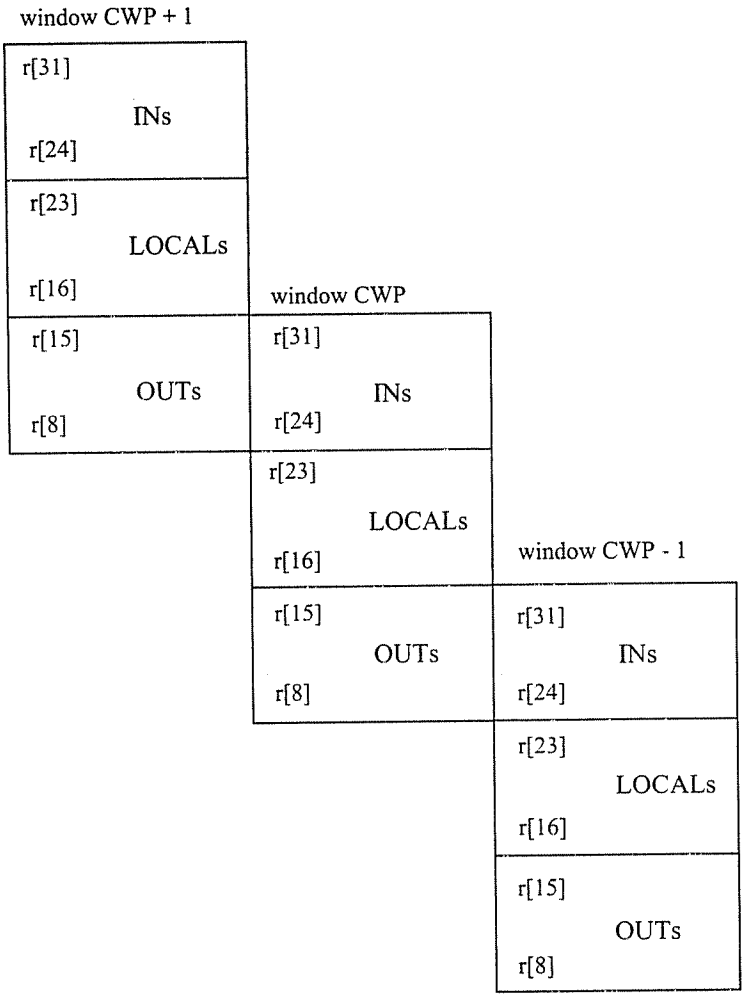


Figure 17-1. **Window Registers**

17.2.3 Processor State Register (PSR)

Table 17-3. **Processor State Register Bit Definitions**

Bits	Type	Function
31:28	R	Implementation class of architecture
27:24	R	Implementation Version
23:20	RW	Integer Condition Codes (icc) 23 = Negative 22 = Zero 21 = V = Overflow 20 = Carry
19:14		Reserved
13	RW	Enable Co-processor

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Table 17-3. **Processor State Register Bit Definitions** (Continued)

Bits	Type	Function
12	RW	Enable Floating Point
11:8	RW	Interrupt Level
7	RW	Supervisor Mode
6	RW	Value of Supervisor-bit at time of most recent trap
5	RW	Enable Traps
4:0	RW	Current Window Pointer

17.2.4 Window Invalid Mask Register (WIM)

Table 17-4. **Window Invalid Register Bit Definitions**

Bits	Type	Function
31	RW	Window 31
30	RW	Window 30
29	RW	Window 29
28:3	RW	Window 3 to 28
2	RW	Window 2
1	RW	Window 1
0	RW	Window 0

17.2.5 Trap Register (TBR)

Table 17-5. **Trap Register Bit Definitions**

Bits	Type	Function
31:12	RW	Trap Base Address
11:4	R	Trap Type
3:0	R	Zeros

17.2.6 Multiply/Divide Register (Y)

Table 17-6. **Multiply/Divide Register Bit Definitions**

Bits	Type	Function
31:0	RW	Contains the most significant word of the double precision product (dividend) of an integer multiply (divide). The Y register can be read and written with the RDY/WRY instructions.

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17.2.7 Program Counter (PC, nPC) Register

Table 17-7. **Program Counter (PC, nPC) Register Bit Definitions**

Bits	Type	Function
31:0	R	(Next) Program Counter. Read by a CALL or JMPL
		instruction. Written to two local registers during a trap.

17.2.8 Ancillary State Register (ASR)

There are 31 Ancillary State Registers allowed in SPARC. ASRs 1 to 15 are reserved for future use, ASRs 16-31 are available for timers, counters, diagnostic registers, and trap control registers. An ASR is read (written) with the RDASR (WRASR) instructions.

Table 17-8. **Ancillary State Register Bit Definitions**

Bits	Type	Function
31:0	RW	Whatever you'd like.

17.2.9 Format 1 Instruction Set Summary

Table 17-9. **Format 1 Instruction Set Summary**

Mnemonic	Opcode[31:30]	Instruction
CALL	01	CALL

17.2.10 Format 2

Table 17-10. **Format 2**

Mnemonic	Opcode[31:30]	Opcode[24:22]	Instruction
SETHI	00	100	Set High Order 22-bits
NOP	00	100	Operation (rd field = 00000)
UMIMP	00	000	Un-implemented

Table 17-11. **Format 2**

Mnemonic	Opcode [31:30]	Opcode [28:25]	Opcode [24:22]	icc Test	Instruction
BA	00	1000	010	1	Branch Always
BN	00	0000	010	0	Branch Never
BNE	00	1001	010	not Z	Branch on Not Equal

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Table 17-11. **Format 2** (Continued)

Mnemonic	Opcode [31:30]	Opcode [28:25]	Opcode [24:22]	icc Test	Instruction
BE	00	0001	010	Z	Branch on Equal
BG	00	1010	010	not (Z | (N ^ V))	Branch on Greater
BLE	00	0010	010	Z | (N ^ V)	Branch on Less or Equal
BGE	00	1011	010	!(N ^ V)	Branch on Greater or Equal
BL	00	0011	010	N ^ V	Branch on Less
BGU	00	1100	010	!(C | Z)	Branch on Greater Unsigned
BLEU	00	0100	010	C | Z	Branch on Less or Equal Unsigned
BCC	00	1101	010	!C	Branch on Carry Clear (Greater than or Equal, Unsigned)
BCS	00	0101	010	C	Branch on Carry Set (Less than, Unsigned)
BPOS	00	1110	010	!N	Branch on Positive
BNEG	00	0110	010	N	Branch on Negative
BVC	00	1111	010	!V	Branch on Overflow Clear
BVS	00	0111	010	V	Branch on Overflow Set
TA	00	1000	010	1	Trap Always
TN	00	0000	010	0	Trap Never
TNE	00	1001	010	not Z	Trap on Not Equal
TE	00	0001	010	Z	Trap on Equal
TG	00	1010	010	not (Z | (N ^ V))	Trap on Greater
TLE	00	0010	010	Z | (N ^ V)	Trap on Less or Equal
TGE	00	1011	010	!(N ^ V)	Trap on Greater or Equal
TL	00	0011	010	N ^ V	Trap on Less
TGU	00	1100	010	!(C | Z)	Trap on Greater Unsigned
TLEU	00	0100	010	C | Z	Trap on Less or Equal Unsigned
TCC	00	1101	010	!C	Trap on Carry Clear (Greater than or Equal, unsigned)
TCS	00	0101	010	C	Trap on Carry Set (Less than, Unsigned)
TPOS	00	1110	010	!N	Trap on Positive
INEG	00	0110	010	N	Trap on Negative
TVC	00	1111	010	!V	Trap on Overflow Clear
TVS	00	0111	010	V	Trap on Overflow Set
Floating Point Branches					
FBA	00	1000	110	1	Branch Always
FBN	00	0000	110	0	Branch Never

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Table 17-11. **Format 2** (Continued)

Mnemonic	Opcode [31:30]	Opcode [28:25]	Opcode [24:22]	icc Test	Instruction
FBU	00	0111	110	U	Branch on Unordered
FBG	00	0110	110	G	Branch on Greater
FBUG	00	0101	110	G | U	Branch on Unordered or Greater
FBL	00	0100	110	L	Branch on Less
FBUL	00	0011	110	L | U	Branch on Unordered or Less
FBLG	00	0010	110	L | G	Branch on Less or Greater
FBNE	00	0001	110	L | G | U	Branch on Not Equal
FBE	00	1001	110	E	Branch on Equal
FBUE	00	1010	110	E | U	Branch on Equal or Unordered
FBGE	00	1011	110	E | G	Branch on Greater or Equal
FBUGE	00	1100	110	E | G | U	Branch on Unordered or Greater or Equal
FBLE	00	1101	110	E | L	Branch on Less or Equal
FBULE	00	1110	110	E | L | U	Branch on Unordered or Less or Equal
FBO	00	1111	110	E | L | G	Branch on Ordered
Co-Processor Branches				**bp_CP_cc[1:0] test**	
CBA	00	1000	110	Always	
CBN	00	0000	110	Never	
CBNE	00	0111	110	3	
CBE	00	0110	110	2	
CBG	00	0101	110	2 or 3	
CBLE	00	0100	110	1	
CBGE	00	0011	110	1 or 3	
CBL	00	0010	110	1 or 2	
CBGU	00	0001	110	1 or 2 or 3	
CBLEU	00	1001	110	0	
CBCC	00	1010	110	0 or 3	
CBCS	00	1011	110	0 or 2	
CBPOS	00	1100	110	0 or 2 or 3	
CBNEG	00	1101	110	0 or 1	
CBVC	00	1110	110	0 or 1 or 3	
CBVS	00	1111	110	0 or 1 or 2	

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17.2.11 Format 3 Instruction Set Summary

Table 17-12. **Format 3 Instruction Set Summary**

Mnemonic	Opcode[24:19]	Instruction
LDSB	001001	Load Signed Byte
LDSH	001010	Load Signed Halfword
LDUB	000001	Load Unsigned Byte
LDUH	000010	Load Unsigned Halfword
LD	000000	Load Word
LDD	000011	Load Doubleword
LDSBA	011001	Load Signed Byte from Alternate Space
LDSHA	011010	Load Signed Halfword from Alternate Space
LDUBA	010001	Load Unsigned Byte from Alternate Space
LDUHA	010010	Load Unsigned Halfword from Alternate Space
LDA	010000	Load Word from Alternate Space
LDDA	010011	Load Doubleword from Alternate Space
LDF	100000	Load Floating Point Register
LDDF	100011	Load Double Floating Point Register
LDFSR	100001	Load Floating Point State Register
LDC	110000	Load Co-processor Register
LDDC	110011	Load Double Co-processor
LDCSR	110001	Load Co-processor State Register
STB	000101	Store Byte
STH	000110	Store Halfword
ST	000100	Store Word
STD	000111	Store Doubleword
STBA	010101	Store Byte into Alternate Space
STHA	010110	Store Halfword into Alternate Space
STA	010100	Store Word into Alternate Space
STDA	010111	Store Doubleword into Alternate Space
STF	100100	Store Floating Point
STDF	100111	Store Double Floating Point
STFSR	100101	Store Floating Point State Register
STDFQ	100110	Store Double Floating Point Deferred Trap Queue
STC	110100	Store Co-processor
STDC	110111	Store Double Co-processor

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Table 17-12. **Format 3 Instruction Set Summary** (Continued)

Mnemonic	Opcode[24:19]	Instruction
STCSR	110101	Store Co-processor State Register
STDCQ	110110	Store Double Co-processor Queue
LDSTUB	001101	Atomic Load Store Unsigned Byte
LDSTUBA	011101	Atomic Load Store Unsigned Byte into Alternate Space
SWAP	001111	SWAP register with memory
SWAPA	011111	SWAP register with Alternate Space memory
AND	000001	And
ANDcc	010001	And and modify icc
ANDN	000101	And Not
ANDNcc	010101	And Not and modify icc
OR	000010	Inclusive Or
ORcc	010010	Inclusive Or and modify icc
ORN	000110	Inclusive Or Not
ORNcc	010110	Inclusive Or Not and modify icc
XOR	000011	Exclusive Or
XORcc	010011	Exclusive Or and modify icc
XNOR	000111	Exclusive Nor
XNORcc	010111	Exclusive Nor and modify icc
SHLL	100101	Shift Left Logical
SRL	100110	Shift Right Logical
SRA	100111	Shift Right Arithmetic
ADD	000000	Add
ADDcc	010000	Add and modify icc
ADDX	001000	Add with Carry
ADDXcc	011000	Add with Carry and modify icc
TADDcc	100000	Tagged Add and modify icc
TADDccTV	100010	Tagged Add, modify icc and Trap on Overflow
STC	110100	Store Co-processor
STDC	110111	Store Double Co-processor
STCSR	110101	Store Co-processor State Register
STDCQ	110110	Store Double Co-processor Queue
SUB	000100	Subtract
SUBcc	010100	Subtract and modify icc

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Table 17-12. **Format 3 Instruction Set Summary** (Continued)

Mnemonic	Opcode[24:19]	Instruction
SUBX	001100	Subtract with Carry
SUBXcc	011100	Subtract with Carry and modify icc
TSUBcc	100001	Tagged Subtract and modify icc
TSUBccTV	100011	Tagged Subtract, modify icc and Trap on Overflow
MULScc	100100	Multiply Step and modify icc
UMUL	100100	Unsigned Integer Multiply
SMUL	001011	Signed Integer Multiply
UMULcc	011010	Unsigned Integer Multiply and modify icc
SMULcc	011011	Signed Integer Multiply and modify icc
UDIV	001110	Unsigned Integer Divide
SDIV	001111	Signed Integer Divide
UDIVcc	011110	Unsigned Integer Divide and modify icc
SDIVccc	011111	Signed Integer Divide and modify icc
SAVE	111100	Save caller's window
RESTORE	111101	Restore caller's window
JMPL	111000	Jump and Link
RETT	111001	Return from Trap
RDASR	101000	Read Ancillary State Register
RDY	101000	Read Y Register
RDPSR	101001	Read Processor State Register
RDWIM	101010	Read Window Invalid Mask Register
RDTBR	101011	Read Trap Base Register
WRASR	101000	Write Ancillary State Register
WRY	101000	Write Y Register
WRPSR	101001	Write Processor State Register
WRWLM	101010	Write Window Invalid Mask Register
WRTBR	101011	Write Trap BAse Register
STBAR	101000	Store Barrier
FLUSH	111011	Flush Instruction Memory
FOPs1	110100	Floating Point Operate - see-bits 13-5 for type
FOPs1	110101	Floating Point Operate - see-bits 13-5 for type

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17.3 SPARC Traps

There are three categories of SPARC Traps: precise traps, deferred traps and interrupting traps. A precise trap is induced by a particular instruction and occurs before any program-visible state has changed by the trap-inducing instruction. After a precise trap, the PC saved in r[17] points to the instruction which issued the trap, and nPC points to the next instruction to be executed. Also after a precise trap, the instructions before the trap causing instruction have executed and instructions after have not executed. A deferred trap may occur after program visible state has changed. An interrupting trap is neither a precise or deferred trap and is controlled by the Processor Interrupt Level (PIL) field of the PSR.

The default SPARC trap model is that all traps are precise, except for floating point and co-processor exceptions, implementation dependent "machine-check" exceptions, and an exception cause by the second access of a two-memory-access load/store instruction.

The Enable Trap (ET)-bit in the PSR must be 1 for traps to occur normally. The IU compares the interrupt request level (bp_IRL) against the processor interrupt field (PIL) of the PSR. If bp_IRL is greater than PIL, or if bp_IRL = 15 (unmaskable) then the IU takes the trap. When ET = 0, all interrupting traps are ignored even bp_IRL = 15. If a precise or a deferred trap occurs, the processor halts execution and enters the error_mode state.

When a trap occurs, ET is set to 0, the existing S-bit in the PSR is saved into PS in the PSR, S is changed to 1, the register window is advanced to the next window, i.e., CWP <- ((CWP-1) modulo NWINDOWS), the trapped program counters are saved in local registers 1 and 2 of the new window, i.e., r[17]←PC, r[18]←nPC, the tt field of the TBR is written with the trap identifier number, and if the trap is a reset trap, execution control is transferred to address 0, i.e.,PC←0, nPC←4. If the trap is not a reset trap, control is transferred into the trap table, i.e., PC←TBR, nPC←TBR+4. The following tables list the traps and priorities.

Table 17-13. **Trap Priorities**

Exception	Priority	tt
reset	1	(see text)
data_store_error	2	0x2B
instruction_access_MMU_miss	2	0x3C
instruction_access_error	3	0x21
r_register_access_error	4	0x20
instruction_access_exception	5	0x01
privileged_instruction	6	0x03
illegal-instruction	7	0x02
fp_disabled	8	0x04
cp_disabled	8	0x24
unimplemented_FLUSH	8	0x25
watchpoint_detected	8	0x0B
window_overflow	9	0x05

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Table 17-13. **Trap Priorities** (Continued)

Exception	Priority	tt
window_underflow	9	0x06
mem_address_not_aligned	10	0x07
fp_exception	11	0x08
cp_exception	11	0x28
data_access_error	12	0x29
data_access_MMU-miss	12	0x2C
data_access_exception	13	0x09
tag_overflow	14	0x0A
division_by_zero	15	0x2A
trap_instruction	16	0x80-FF
interrupt_level-15	17	0x1F
interrupt_level_14	18	0x1E
interrupt_level_13	19	0x1D
interrupt_level_12	20	0x1C
interrupt_level_11	21	0x1B
interrupt_level_10	22	0x1A
interrupt_level_9	23	0x19
interrupt_level_8	42	0x18
interrupt_level_7	25	0x17
interrupt_level_6	26	0x16
interrupt_level_5	27	0x15
interrupt_level_4	28	0x14
interrupt_level_3	29	0x13
interrupt_level_2	30	0x12
interrupt_level_1	31	0x11

17.4 SPARC Memory Model

The SPARC memory model defines real memory to have an ASI of 8, 9, 0xA or 0xB, or when the SPARC Reference MMU (SRMMU) is used 0x20-2F refers to real memory. I/O locations are those memory locations that do not have ASI fields of 8, 9, 0xA, 0xB or 0x20-2F, and those memory locations accessed with a cacheable-bit set in the SRMMU.

The standard memory model is called Total Store Ordering (TSO), while an additional model called Partial Store Ordering (PSO) may be used for higher performance memory systems. One of the two are enabled by the PSO-bit in the MMU Control Register of the SPARC Reference MMU. Strong Consistency memory

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models support both TSO and PSO. In Strong Consistency, loads, stores and atomic load-stores of all processors are executed by memory serially in the order that these instructions were issued by the individual processors. A given SPARC implementation must provide TSO but does not have to provide PSO.

Total Store Ordering guarantees that the store, FLUSH, and atomic load-store instructions of all processors appear to be executed by memory serially in the order that the instructions were issued by the processor. In Partial Store Ordering, store, FLUSH, and atomic load store are executed in memory serially, but that order may not be the same order that they were issued by the processor. The STBAR instruction provides conformance between issuing order and memory order. If two instructions are separated by a STBAR, then the issuing order and the memory order are the same.

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18.1 SBus IOMMU Control Space

Table 18-1. **SBus IOMMU Control Space Addresses**

PA[35:0]	Description
0xF E000 0000	IOMMU Control Register
0xF E000 0004	IOMMU Base Address Register
0xF E000 0008 - 0xF E000 0010	Reserved
0xF E000 0014	Flush All TLB entries
0xF E000 0018	Address Flush Register
0xF E000 0100	IOMMU tags Diagnostic Access
0xF E000 0200	IOMMU Translation Cache Diagnostic
0xF E000 0300 - 0xF E000 0FFF	Reserved
0xF E000 1000	M-to-S Asynchronous Fault Status Register
0xF E000 1004	M-to-S Asynchronous Fault Status Register
0xF E000 1008	Arbiter Enable Register
0xF E000 100C	Reserved
0xF E000 1010	SBus slot #0 Configuration Register
0xF E000 1014	SBus slot #1 Configuration Register
0xF E000 1018	SBus slot #2 Configuration Register
0xF E000 101C	SBus slot #3 Configuration Register
0xF E000 2000 - 0xF E000 2004	MID Register

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18.2 Processor Core Register Definitions

– (ASI = 0x4)

18.2.1 Module Control Register

Table 18-2. **Module Control Register Bit Definitions**

Bits		Type
31:28	R	SRMMU Implementation number
27:24	R	SRMMU version number
23:15	RW	Reserved
14	RW	Boot Mode (= 1)
13	RW	Cacheable-bit for second level caches
12:11	RO	Cache Parameters
10	RW	1 = write-back cache, 0 = write through cache
9		Reserved
8	RW	Cache Enable
7:2		Reserved
1	RW	No fault if S = 1, access exceptions are not reported to IU
0	RW	MMU Enable

18.2.2 Context Table Pointer Register

Table 18-3. **Context Table Pointer Register**

Bit	Function
31:8	DCTP<35:12>

18.2.3 Context Register

Table 18-4. **Context Register**

Bit	Function
N = 15	64K contexts supported

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18.2.4 Synchronous Fault Status Register

Table 18-5. **Synchronous Fault Status Register**

Bit	Function
13	Undefined Error set by MXCC signals a Retry and asserts Data Ready
14	Control Space Access Error

18.2.5 Synchronous Fault Address Register

Table 18-6. **Synchronous Fault Address Register Bit Definitions**

Bits	Type	Function
31:0	R	Address of where fault occurred

18.2.6 Asynchronous Fault Status Register

Table 18-7. **Asynchronous Fault Status Register Bit Definitions**

Bits	Type	Function
31:13		Reserved
12	R	Un-correctable Error on MBus
11	R	Time-out response from MBus
10	R	Bus Error response from MBus
9:8		Reserved
7:4	R	Asynchronous Fault Address-bits PA<35:32>
3:1	R	Reserved
0	R	Asynchronous Fault Occurred

18.2.7 Asynchronous Fault Address Register

Table 18-8. **Asynchronous Fault Address Register Bit Definitions**

Bits	Type	Function
31:0	R	Address of where fault occurred

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18.2.8 Reset Register

Table 18-9. **Reset Register Bit Definitions**

Bits	Type	Function
31:3		Reserved
2	R	Watchdog Reset
1	RW	Software Internal Reset
0		Reserved

18.2.9 MBus Port Address Register

Table 18-10. **MBus Port Address Register Bit Definitions**

Bits	Type	Function
31:16	R	Implementation specific
15:8	R	MBus device number
7:4	R	Device revision number
3:0	R	MBus vendor number

18.2.10 System Control Status Register

Table 18-11. **System Control Status Register Bit Definitions**

Bits	Type	Function
31:4		Reserved
3	RW	Reset Switch
2	R	Diagnostics Mode Switch
1	RW	Set on soft SYS_RESET, clear on PowerOnReset
0	RW	Generates equivalent of a PowerOnReset

18.2.11 Arbiter Enable Register

Table 18-12. **Arbiter Enable Register Bit Definitions**

Bits	Type	Function
31	RW	Enables S-to-M asynchronous writes
30:21		Reserved
20	RW	Enables arbitration for on-board SCSI/Ethernet masters
19	RW	Enables arbitration for SBus slot 3

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Table 18-12. **Arbiter Enable Register Bit Definitions** (Continued)

Bits	Type	Function
18	RW	Enables arbitration for SBus slot 3
17	RW	Enables arbitration for SBus slot 3
16	RW	Enables arbitration for SBus slot 3
15:4		Reserved
3	RW	Enables arbitration for MBus master 0xB
2	RW	Enables arbitration for MBus master 0xA
1	RW	Enables arbitration for MBus master 0x9
0	R	Reads as '1'

18.2.12 M-to-S Asynchronous Fault Status Register

Table 18-13. **M-to-S Asynchronous Fault Status Register Bit Definitions**

Bits	Type	Function
31	R	Summary Error-bit
30	R	Late Error SBus
29	R	Write Access timed out in PA<35:32> = 0xE range
28	R	E Bus received an error ack or a SBus write access received a BERR
27:25	R	Size of error transaction
24	R	Error access had Supervisor-bit set in the MBus address phase
23:20	R	Module ID number
19	R	Multiple error
18	R	Direction of error access
17		Reserved
16:12	R	Actual address <4:0>
11:9	R	Actual size of error transaction
8:4		Reserved
3:0	R	PA<35:32> of the fault address

18.2.13 Timer Configuration Register

Table 18-14. **Timer Configuration Register Bit Definitions**

Bits	Type	Function
31:4		Reserved

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Table 18-14. **Timer Configuration Register Bit Definitions** (Continued)

Bits	Type	Function
3	RW	Timer / Counter 3 0 = Counter / Timer 1 = User Timer
2	RW	Timer / Counter 2 0 = Counter / Timer 1 = User Timer
1	RW	Timer / Counter 1 0 = Counter / Timer 1 = User Timer
0	RW	Timer / Counter 0 0 = Counter / Timer 1 = User Timer

18.2.14 Count and Limit Registers

Table 18-15. **Count and Limit Registers Bit Definitions**

Bits	Type	Function
31	R	Limit Bit
30:9	W	21 bit value
8:0		0000 0000

18.2.15 User Timer Register

Table 18-16. **User Timer Register Bit Definitions**

Bits	Type	Function
63	R	Limit bit
62:8	W	Count value
8:0		0000 0000

18.2.16 User Timer Start / Stop Register

Table 18-17. **User Timer Start / Stop Register Bit Definitions**

Bits	Type	Function
31:1		Reserved
0	RW	0 = Start Counter 1 = Stop Counter

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18.2.17 Module Identification (MID) Register

Table 18-18. **Module Identification Register Bit Definitions**

Bits	Type	Function
31:4		Reserved
3:0	R	MID

18.2.18 Memory Enable Register

Table 18-19. **Memory Enable Register Bit Definitions**

Bits	Type	Function
31:28	R	Implementation Number 0 = SPARCserver 10 1 = EMC 2 = SMC
27:24	R	Version Number
23:12		Reserved
11	RW	CI 0 = Normal 1 = Inhibit
10	R	Memory Controller address map specifies EMC0 (=0) or EMC1 (=1) type of memory controller
9:2	RW	Memory Row Refresh. Specifies DRAM MMBs that need to be EMC refreshed
1	RW	Enable Correctable Error Interrupt
0	RW	Enable ECC defect and Correct

18.2.19 Memory Fault Status Register

Table 18-20. **Memory Fault Status Register Bit Definitions**

Bits	Type	Function
31:18		Reserved
17	R	Transfer induced memory error. Set when DE or UE occurs during a graphics access
16	R	Multiple error. Multiple error occurring before clearing FAR sets this bit.
15:8	R	Syndrome code for bit in error or stored check bits. This field contains syndrome code of memory fault
7:4	R	Double Word in a block with CE or UE. Pointer to double word in error
3	R	Un-correctable ECC error

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Table 18-20. **Memory Fault Status Register Bit Definitions** (Continued)

Bits	Type	Function
2		Reserved
1	R	Mis-referenced slot error.
0	R	Correctable ECC error

18.2.20 Fault Address Register 0

Table 18-21. **Fault Address Register 0 Bit Definitions**

Bits	Type	Function
31:28	R	Module identifier of transaction's origin
27	R	Supervisor access indicator
26:22		Reserved
21:14	R	MBus virtual address VA[19:12]
13	R	Boot mode/local bus
12	R	Bus lock Indicator
11	R	Data cacheable
10:8	R	MBus transaction size-same encoding as MAD [42:40}
7:4	R	Transaction type - same encoding as MAD[39:36]
3:0	R	Higher 4 bits of Physical Address

18.2.21 Fault Address Register 1

Table 18-22. **Fault Address Register 1 Bit Definitions**

Bits	Type	Function
31:0	R	Lower 32 bits of the faulty Physical Address

18.2.22 Processor Interrupt Pending Register

Table 18-23. **Processor Interrupt Pending Register Bit Definitions**

Bits	Type	Function
31:17	R	SOFTINT<15:1>
16	R	0
15:1	R	HARDINT<15:1>
0	R	0

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18.2.23 Processor Interrupt Clear Register

Table 18-24. **System Interrupt Pending Register Bit Definitions**

Bits	Type	Function
31:17	W	SOFTINT<15:1> Clear
16	W	0
15	W	HARDINT<15> Clear
14:0	W	0

18.2.24 Processor Soft Interrupt Set Register

Table 18-25. **Processor Soft Interrupt Set Register Bit Definitions**

Bits	Type	Function
31:17	W	SOFTINT<15:1> Set
16:0		Reserved

18.2.25 Interrupt Target Register

Table 18-26. **Interrupt Target Register Bit Definitions**

Bits	Type	Function
31:2		Reserved
1:0	RW	Target Processor ID

18.2.26 System Interrupt Pending Register

Table 18-27. **System Interrupt Pending Register Bit Definitions**

Bits	Type	Function
31		Reserved
30	R	Module Error
29	R	IOMMU Error on M -to - S write buffer error
28	R	ECC Memory Error
27:22		Reserved
21	R	Module Interrupt
20		Reserved
19	R	Level 10 System Timer Interrupt
18	R	SCSI

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Table 18-27. **System Interrupt Pending Register Bit Definitions** (Continued)

Bits	Type	Function
17		Reserved
16	R	Ethernet
15	R	Serial Ports
14	R	Keyboard/Mouse
13:7	R	SBus Interrupts <7:1> or VME Interrupts <7:1>
6:0		Reserved

18.2.27 Mask Register

- **Current Target Mask Register (R)**
- **Set Mask Register (W)**
- **Clear Mask Register (W)**

Table 18-28. **Mask Register Bit Definitions**

Bits	Type	Function
31	R	Mask All Interrupts
30	R	Module Error
29	R	IOMMU Error on M -to- S write buffer error
28	R	ECC Memory Error
27		Reserved
26	R	Moonshine Interrupt 1: Expansion Memory Error
25:22		Reserved
21	R	Module Interrupt
20		Reserved
19	R	Level 10 System Timer Interrupt
18	R	SCSI
17		Reserved
16	R	Ethernet
15	R	Serial Ports
14	R	Keyboard/Mouse
13:7	R	SBus Interrupts <7:1> or VME Interrupts <7:1>
6:0		Reserved

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18.2.28 IOMMU Page Table Entry

Table 18-29. **IOMMU Page Table Entry Bit Definitions**

Bits	Type	Function
31:8	RW	Physical Page Number
7	RW	Cacheable
6:3		Reserved
2	RW	Writable
1	RW	Valid-bit
0	RW	Write as '0' always

18.2.29 IOMMU Control Register

Table 18-30. **IOMMU Control Register Bit Definitions**

Bits	Type	Function
31:28	R	Implementation
27:24	R	Version
23:5		Reserved
4:2	RW	IOMMU translation range = 16MB * 2** <RANGE>
1	RW	Diagnostic Enable = 1 allows direct access to TLB and tags
0	RW	IOMMU Enable 0 = pass through mode 1 = translation is enabled

18.2.30 IOMMU Base Address Register

Table 18-31. **IOMMU Base Address Register Bit Definitions**

Bits	Type	Function
31:10	RW	IOMMU Base Address for Page Table
9:0		Reserved

18.2.31 SBus Slot Configuration Register

Table 18-32. **SBus Slot Configuration Register Bit Definitions**

Bits	Type	Function
31:22		Reserved

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Table 18-32. **SBus Slot Configuration Register Bit Definitions** (Continued)

Bits	Type	Function
21:16	RW	Segment
15	RW	Cacheable-bit
14:5		Reserved
4	RW	Slave supports 64 byte bursts
3	RW	Slave supports 32 byte bursts
2	RW	Slave supports 16 byte bursts
1	RW	Slave supports 8 byte bursts
0	RW	Bypass Enabled

18.2.32 Address Base Flush Register

Table 18-33. **Address Base Flush Register Bit Definitions**

Bits	Type	Function
31		Reserved
30:12	W	Flush Address - 32 bit virtual address of TLB flush
11:0		Reserved

18.2.33 Translation Cache (TLB) Entry Register

Table 18-34. **Translation Cache (TLB) Entry Register Bit Definitions**

Bits	Type	Function
31:8	RW	Physical Page Number
7	RW	Cacheable
6:3		Reserved
2	RW	Writable = 1, Read only = 0
1	RW	Valid = 1
0		Reserved

18.2.34 Translation Cache Tag Format

Table 18-35. **Translation Cache Tag Format Bit Definitions**

Bits	Type	Function
31		1

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Table 18-35. **Translation Cache Tag Format Bit Definitions** (Continued)

Bits	Type	Function
30:12	RW	Tag<30:12> is compared to VA<30:12> on DVMA access
11:4		Reserved
3:0	R	LRUQ TLB number in the Least Recently Used Queue The lowest (highest) address has the number of the LRU (MRU) TLB

18.2.35 Translation Cache Tag Format

Table 18-36. **Translation Cache Tag Format Bit Definitions**

Bits	Type	Function
31:24	RW	Tag identifies block within 8K page compared to VA<12:5>
23	RW	Valid
22	RW	Modified
21	RW	IOC-cacheable - set by the kernel during mapping independent of the system cachability of the data
20	RW	Write-allowed - set by the kernel during mapping
19:0		Reserved

18.2.36 I/O Cache Data Format

Table 18-37. **I/O Cache Data Format Bit Definitions**

Bits	Type	Function
31:0	RW	Cache Data - PA<14:5> addresses the cache line and PA<4:2> addresses the word within the 32 byte line

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19

Reference Documentation

19.1 Other References

Below is a list of reference documentation specific to the SPARC 20MP design and layout. We suggest that you obtain this information to help you with the SPARC 20MP product implementation.

1. SPARC MBus Interface Specification, SPARC International
2. Sun 4M architecture, Sun P/N 950-1373-10
3. Writing Fcode Programs for SBus cards, Sun P/N 800-4456-10
4. The SBus Specification, Revision B, Sun P/N 800-5922-10
5. Open Boot PROM Toolkit User's Guide, Sun P/N 800-4251-10
6. SPARC Assembly Language Specification, Sun P/N 800-1595-10
7. The SuperSPARC Microprocessor User Documentation, Sun P/N 800-5072-10
8. SPARC Architecture Manual, Version 8, SPARC International
9. NCR SBus I/O Chipset Data Manual, NCR Corporation, February, 1993

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A

Temperature Measurement for MBus Modules

A.1 Purpose

To provide a method for our customers to determine whether they have provided adequate cooling of MBus modules in their application.

A.2 Recommended Equipment

Equipment Source (For Written Orders and Quotations)

Omega Engineering
P.O. Box 4047
Stamford, CT 06907-0047
800-826-6342

- Thermocouple
  - Teflon Insulation Thermocouple, CHROMEGA-ALOMEGA Calibration, 36 AWG, 36" Long, Stripped Lead Termination (Omega Engineering Part Number 5TC-TT-K-36-36)
- Digital Panel Thermometer (or Temperature Meter with type K Thermocouple)
  - Input Type K Thermocouple (Omega Engineering Part Number DP371-KC2))

A.3 Test Conditions

Place the unit under test in the highest temperature environment expected to occur in the application or assure air temperature surrounding the unit does not exceed 50 degrees C at any time. At 50 degrees C, minimum 300 LFM air flow must be provided to the MBus module.

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A.4 Procedure

1. Furnish power to the panel thermometer/temperature meter.
2. Attach thermocouple(s) to the meter.
3. Locate heat sink of MBus module. Attach other end of thermocouple to the surface of the heat sink, between fins, directly opposite and on the centerline of MDP (Multi Die Package). See *Figure A-1* below. One thermocouple should be used per MDP.
4. Hold thermocouple(s) in place using appropriate temperature resistant polymer (or equivalent materials).
5. Run unit under test in hot environment. Assure cooling mechanism functions correctly.
6. Adequate cooling has been provided if temperature of heatsink does not exceed 80 degrees C.

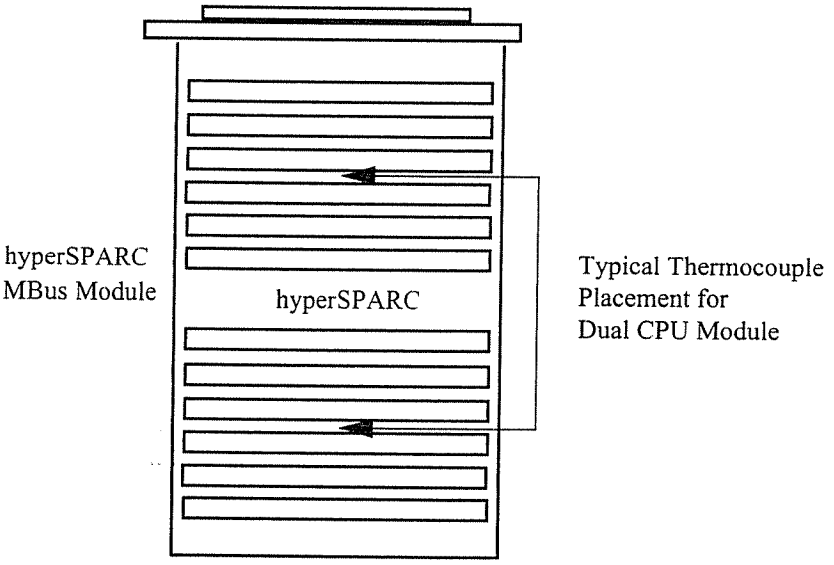


Figure A-1. **Thermocouple Placement for MBus Module Temperature Testing**

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Reader Comment Card

We welcome your comments and suggestions to help improve the *Themis Sparc 20MP Users Manual*. Please take time to let us know what you think about these manuals.

- The information provided in the maunal was complete.

  Agree___ Disagree___ Not Applicable___

- The information was well documented and easy to follow.

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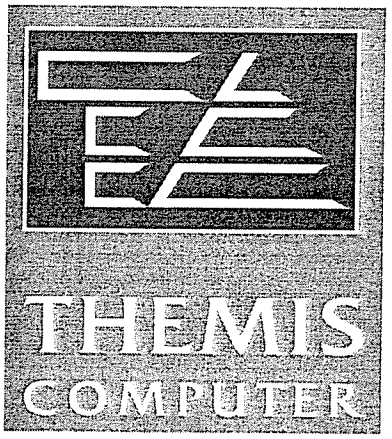
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