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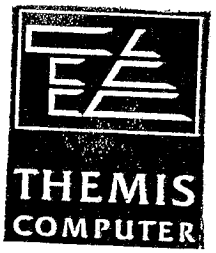
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Themis SPARC LXE User's Manual

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How to Use This Manual



This manual describes the Themis LXE, a SPARCclassic compatible computer with VMEbus interface.

7.1 Intended Audience

It is written for end-users, integrators and programmers and contains all relevant information to install and configure the LXE board. It primarily assumes that the SUN Open Boot PROM (OBP) is installed. If you intend to operate the LXE with an operating system other than Solaris or use a real-time kernel such as VxWorks, please consult the appropriate documentation supplements accompanying your OS or kernel software.

Although all Themis LXE specific hardware and software features are described in detail in this manual, programmers wishing to code for the LXE without the benefit of an operating system or real-time kernel will require additional date sheets and documentation for the NCR chip-set, the Tsunami processor and other systems components comprising the SPARCclassic design. A complete reference list of available supplemental documentation is available in (APPDX X).

The reader is assumed to be familiar with and have working knowledge of the VMEbus C.1/ANSI/IEEE Std 1014-1987 specifications, SPARC processor architecture, NCR SPARCclassic chip-set, SBus C.0 specifications, Ethernet and SCSI (ANSI X3.131-1986).

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For easy reference, all pertinent board information such as jumper layout and configuration, address maps, VMEbus accessing, etc. is available in the appendices.

7.2 *Organization*

The features and building blocks of the Themis LXE are listed in Themis SPARC LXE Features on page 2. the chapter titled Introduction to the Themis SPARC LXE also covers aspects of software compatibility and should be consulted to gain basic knowledge

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Introduction to the Themis SPARC LXE



The Themis SPARC LXE board is a SPARC [1]-based single-board VME computer, based on the new Texas Instruments microSPARC® (Tsunami), a highly integrated microprocessor with a wide array of on-chip features.

The LXE comes standard with two SBus slots, SCSI-2, Ethernet, Centronics, mouse/keyboard interface, 2 RS232 ports, VMEbus interface and JTAG testability for the major ASICs. The hardware chip set is composed of the microSPARC, two NCR ASICs (SLAVIO and MACIO) and the SUN S4 VME controller.

Use of the same chip set found in Sun's new SPARCclassic product line and standard Solaris 2.x CD-ROM binary distribution media assures compatibility with Sun Microsystems products on both hardware and software levels.

The Themis LXE SPARCclassic compatible CPU is a high performance, low cost VMEbus CPU board supporting Solaris 1.1 and Solaris 2.3 UNIX operating systems. For demanding real-time applications, a wide variety of real-time kernels including VxWorks and LynxOS are supported.

The highly integrated Texas Instruments Tsunami processor was designed as a building block for cost effective computer systems with very low component counts. Themis has build a powerful, simple and reliable CPU engine around this MicroSPARC.

---

1. Scalable Processor Architecture Reduced-instruction-set Computer

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1.1 *Themis SPARC LXE Features*

Performance

- CPU: 37 MIPS/18 SPECmarks @ 40 MHz
- FPU: 3.7 Linpack Double-performance MFLOPS @ 40 MHz

Sun custom low-power CMOS integrated ASICs for high reliability:

- Tsunami (SPARC Version 8 compatible RISC microprocessor)
  - SPARC IU
  - SPARC FPU
  - Cache controller
  - Instruction cache (4 KB)
  - Data cache (2 KB)
  - Reference MMU
  - I/O MMU
  - DRAM controller (main memory)
  - SBus controller
  - JTAG internal/boundary scan controller
- MACIO (master I/O controller)
  - DMA2 controller
  - SCSI-2 (ESP) controller
  - Ethernet controller (LANCE-compatible)
  - Parallel port controller (Centronics compatible)
  - JTAG internal/boundary scan controller
- SLAVIO (slave I/O controller)
  - Serial A and B controller (synchronous/asynchronous)
  - Interrupt controller
  - Reset controller
  - Power on/off controller
  - Counter/timer controls
  - EPROM/NVRAM controller
  - JTAG internal/boundary scan controller
- S4 VMEbus Controller
  - A32/24/16 master capabilities
  - A32/24 slave
  - Single level and round-robin bus arbiter
  - Block mode transfer support
  - Mailbox interrupts

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- Full read-modify-write

Components from other vendors:

- 4Mbit (512x8) boot PROM (OBP)
- 8K TOD/NVRAM (with battery backup)
- DBRI (ISDN) controller for 8-bit audio

Connectors

- Two or four SIMM connectors
  - supports 4 and 16 MB SIMMs at 70 ns
  - up to 96 MB of on-board main memory expansion (16 MB SIMMS and 4 socket configuration)
  - one parity bit per 32-bit word
  - 64-bit memory bus
- Two SBus master/slave connectors
  - 32-bit data path
  - 32-bit virtual address for master, 28-bit physical slave address
  - Maximum 16 byte burst
- High density SCSI connector
- Sun keyboard/mouse connector
- 10BaseT Ethernet connector
- Serial port A/B connector

1.2 *Themis SPARC LXE Supported Standards*

- Fully compatible with SunOS 5.2 and Solaris 2.1 (or higher)
  - Binary compatible with SPARCware applications (Solaris 1.0 or later)
  - Disk I/O read and write clustering
- Complete implementation of SunOS 4.1.3 and Solaris 1.1
  - Binary compatible with sun4m architecture
  - Runs all Solaris 1.1 applications
- Hardware standards compliant:
  - SPARC International SPARC Compliance Definition 1.0
- Software standards compliant:
  - IEEE POSIX standard 1003.1 (1988)

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- X/Open-XPG3 component branded
- XPG2 BASE branded
- System V Interface Definition Issue II

- Supports standards in application software:
  - SPARC standards
  - OpenLook standards
  - Sun UNIX standards

- 3000+ SPARCware applications

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Themis SPARC LXE Description



2.1 Themis SPARC LXE Board

The Themis SPARC LXE is a SPARC RISC (Reduced Instruction Set Computer) based VMEbus board.

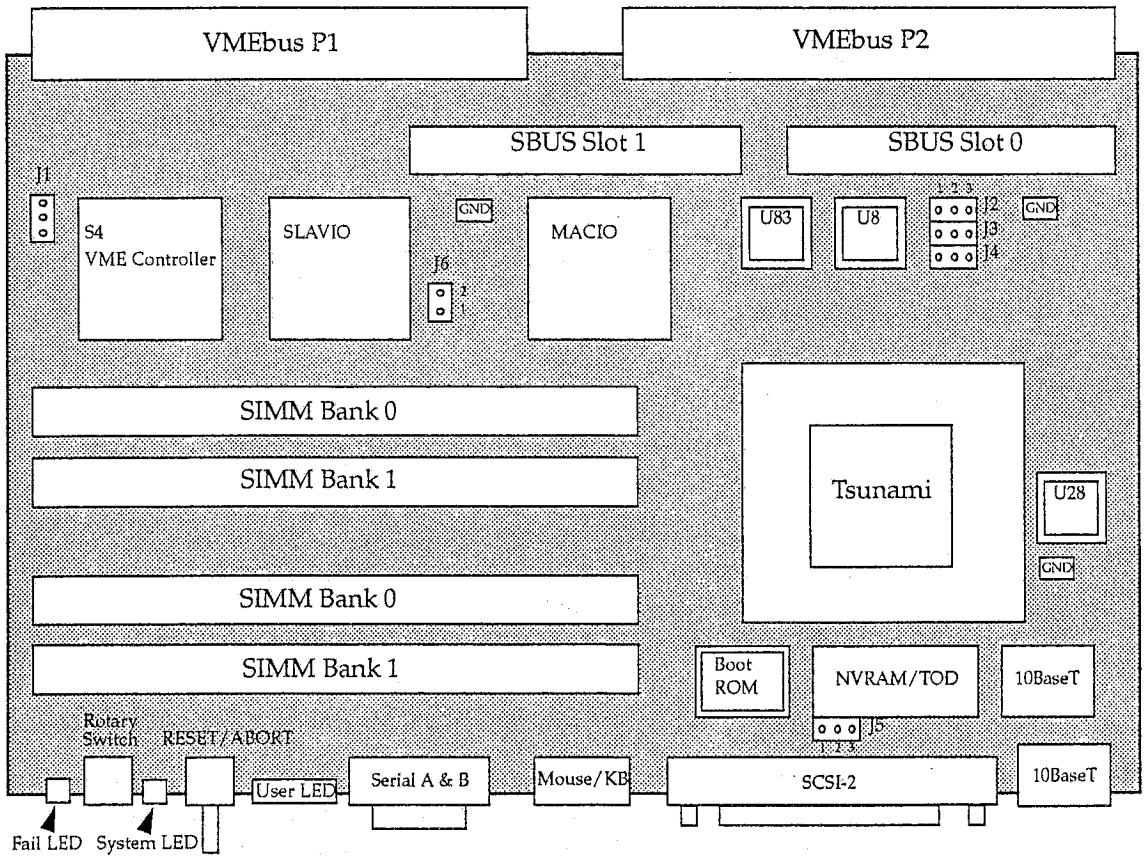
Fully compatible with the SUN SPARCclassic designs, the LXE SBC (Single Board Computer) features the Texas Instruments Tsunami microprocessor, a master I/O (MACIO) controller, a slave I/O (SLVIO) controller, an audio controller, SIMM DRAM (main memory) and the S4 VMEbus controller.

On-board peripheral connectors include a full VME A32D32 interface, two SBus slots, SCSI-2, 10BaseT Ethernet, keyboard/mouse and 2 RS232 ports.

All signals are also available on the user pins of the VME P2 connector. A paddle board provides industry standard connectors for AUI Ethernet, Centronics parallel, SCSI and 2 RS-232, to the P2 I/O interfaces.

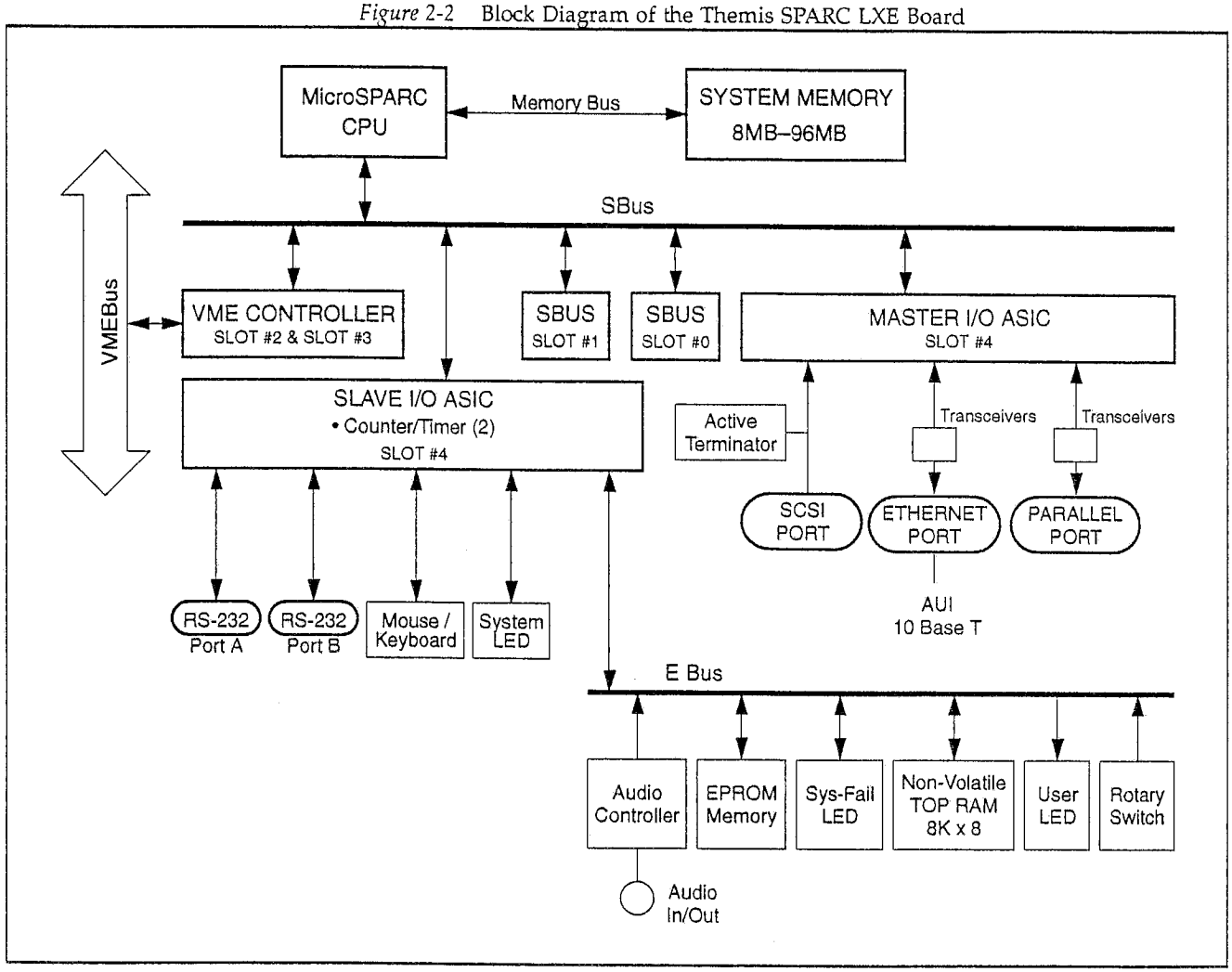
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Figure 2-1 Layout of the Themis SPARC LXE Board



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Figure 2-2 Block Diagram of the Themis SPARC LXE Board



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2.2 *Themis SPARC LXE Main Components*

2.2.1 *Tsunami Microprocessor*

Tsunami is a single-chip microprocessor that contains an Integer Unit (IU), a Floating Point Unit (FPU), data and instruction caches, and controllers for Main Memory Cache, Random-Access Memory (RAM), Direct-Memory Access (DMA), and Memory Management Unit (MMU).

The Tsunami processor runs at 40 MHz, with a processing capability of 39 million instructions per second (MIPS). The FPU runs at 3.7 million floating-point operations per second (MFLOPS)[1].

Integer Unit (IU) and Floating-Point Unit (FPU)

The core of the Tsunami is the combined SPARC Integer Unit/Floating-Point Unit (IU/FPU).

The IU includes a 32-bit external bus interface with separate data and address buses, a five-stage instruction pipeline, a barrel shifter, two data aligners, and a three-port register file consisting of 128 registers. These registers are configured into overlapping sets that facilitate the passing of parameters. All instructions with the exception of double loads, stores, and floating-point operations are executed in one machine cycle.

Main Memory Cache

Cache memory included on the Tsunami chip provides high-speed local memory for the IU. The 2 KB data cache is a direct-mapped physical-address write-through cache with no write allocate, organized as 128 lines of 16 bytes. The 4 KB instruction cache is a physically-addressed cache, organized as 128 lines of 32 bytes.

1. Performance measurement specifications are defined in chapter 3

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Reference Memory Management Unit (MMU)

Translation of 32-bit virtual addresses from the CPU is performed by a SPARC Reference MMU as defined in the SPARC Architecture Manual Version 8. The Tsunami MMU also functions as an I/O MMU. It controls arbitration between I/O, data cache, instruction cache and TLB references to memory.

The SBus is the basic communication mechanism between the processing core (CPU), the MMU, main memory and various I/O devices. The MMU translates the virtual address output of the CPU and drives the resulting physical address on the SBus. It also decodes this physical address into a set of select signals used to enable main memory or I/O devices on the SBus.

Translation Lookaside Buffer (TLB)

The TLB is 32-entry fully-associative reference translation-lookaside buffer that uses a pseudo-random algorithm for the replacement of TLB entries, all contained within the MMU.

RAM Controller

The Dynamic Random Access Memory (DRAM) controller provides all control signals to support up to 96MB of onboard DRAM. It supports 70 ns DRAMs to give burst reads and writes at one word per clock. It also provides parity generation and checking. It has a 2-word write buffer to provide quick response to cache write-through operations. The DRAM controller includes a private RAM data bus, isolating the DRAM data from the SBus data. This lowers the load on the SBus data lines, in addition to allowing the RAM controller to do buffered writes while releasing the SBus.

SBus Controller

The Tsunami ASIC controls the 20 MHz SBus and all SBus devices, including devices in the three virtual SBus slots, and in the two physical single-height SBus slots.

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Table 2-1 Themis SPARC LXE SBus Slots

SBus Slot Number	Function of SBus Slot
Slot 0	Physical SBus slot 0 for an SBus Card
Slot 1	Physical SBus slot 1 for an SBus Card
Slot 2	VME port
Slot 3	
Slot 4	SLAVIO and MACIO I/O controllers

2.2.2 *Input/Output Controllers and 8-Bit Devices*

MACIO (Master I/O Controller)

The MACIO ASIC implements DMA driven input/output interfaces on the Themis LXE. It's functionality is divided into a set of macrocell based sections dedicated to a particular device

Ethernet Controller Macrocell

Ethernet is supported via a LANCE compatible controller. A 10BaseT interface is available at the front panel and a standard AUI interface is routed to the P2 connector and accessible via the paddle board.

SCSI-2 Controller Macrocell

SCSI device operations are handled through a SCSI-2 controller macrocell. All SCSI bus transfers are performed by the on-chip DMA controller. The controller provides transfer speeds of up to 10MB/s

DMA Controller Macrocell

Direct-Memory Access (DMA) is handled through the DMA2 controller macrocell. It includes three external interfaces designed to provide DMA access to Ethernet, SCSI, and the bi-directional Centronics parallel port.

To minimize SBus usage, the DMA2 controller has internal line buffers and performs SBus burst operations of 16 bytes where possible.

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The DVMA (Direct Virtual Memory Access) function of the DMA2 controller provides two channels of direct memory access between the main memory on the SBus and the SCSI and Ethernet interfaces.

DVMA also provides the data path between the SBus and the SCSI and Ethernet interface devices required for the IU to initialize and configure these interfaces.

Printer Port Controller Macrocell

Centronics-compatible bi-directional parallel port operations are handled through the DMA2 macrocell.

SLVIO (Slave I/O Controller)

All non-DMA and 8-bit interface connections are implemented by the SLVIO ASIC controller.

Serial Port A Controller

Asynchronous only RS-232 interface with baud rates up to 38400.

Serial Port B Controller

Synchronous or asynchronous RS-232 interface with modem control and baud rates up to 38400.

Keyboard/Mouse Controller

Standard Sun Microsystems keyboard/mouse ports are provided to connect a keyboard and a mouse through the standard 8-pin connector located on the front panel or via the serial C&D ports on the P2.

EBus Controller

The EBUS is a SLVIO 8-bit sub-bus for controlling low speed peripherals.

The OBP PROM and NVRAM/TOD components are attached to the SLVIO ASIC through the external EBUS 8-bit interface.

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JTAG Internal & Boundary Scan Controller

Signal paths and circuitry are provided to perform a ASIC-level diagnostic examination of SLVIO.

Interrupt Controls

SLVIO contains a uni-processor subset of the Sun-4M interrupt controller. It includes all system logic to support 15 levels of software and/or externally generated interrupts. Assignment and prioritizing of these interrupts is performed by the interrupt logic.

System Reset Controls

Three reset sources are recognized by the system reset controller: power-on reset (POR), software reset (SWR) and the front panel reset switch. Either of these sources will cause SLVIO to assert a reset signal, returning the Themis SPARC LXE board to a known state.

Counter/Timer Controls

SLVIO features two programmable counter/timer channels.

S4 VMEbus Controller

Designed by SUN Microsystems, the S4 is a SBus to VMEbus interface controller offering a full master/slave A32D32 VME interface with burst mode capabilities. The VME interface is mapped into Sbus slots 2+3 (see Appendix X)

Audio Controller (DBRI)

The Themis SPARC LXE audio function is implemented with the AT&T T5900 DBRI. The DBRI ASIC is a DVMA capable SBus master. The Concentration Highway Interface (CHI) is utilized to support an external audio speaker.

Audio Controller (CODEC)

A CODEC (Crystal C54215 and/or Analog Devices 1849) is used with the AT&T T5900 DBRI (see above) to provide the Themis SPARC LXE audio.

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Slot 0: Extension SBus Slot

Standard SBUS slot with master/slave capability

Slot 1: Extension SBus Slot

Standard SBUS slot with master/slave capabilities. This slot is unavailable in LXE systems equipped with 4 SIMM sockets.

Single Inline Memory Modules (DRAM SIMMs)

4 MB or 16 MB SIMMs can be used in the two or four[1] LXE SIMM sockets. Main memory can be expanded up to 96 MB[2]. The two SIMM socket configuration allows physical access to both SBUS connectors, while the four SIMM socket version prevents mechanical access to the SBUS 1 connector.

The LXE is designed to use 4MB or 16 MB 70 ns Sun Microsystems 33 bit SIMMs that support a single parity bit per 32 bit word.

Standard SIMMs can also be used with the LXE; three of the four parity bits remain unused.

Open Boot PROM (OBP)

The Open Boot PROM is connected to the Sun Microsystems Expansion Bus (EBus). OBP is contained in a 512Kx8 PROM providing the following functionality:

- Runs start-up diagnostic tests.
- Initializes the host machine.
- Reads non-volatile RAM (NVRAM) and executes the boot sequence, typically booting SunOS. The Diagnostic Executive or standalone programs can also be executed.

---

1. Factory configuration required

---

2. 64MB for the 2 SIMM socket version

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- Includes the abbreviated system monitor. Entry into the system monitor is signified by the > prompt. If a boot attempt fails, the Open Boot PROM tries to start the abbreviated system monitor.
- Supplies program code for the FORTH Toolkit; the on-board diagnostics containing the FORTH Toolkit and the FORTH language interpreter. Entry into the FORTH Toolkit is signified by the ok prompt.
- VMEbus related board settings are controlled by a number of environment variables.

Non-volatile RAM (NVRAM)

8 KB of Non-Volatile Random Access Memory (NVRAM) are provided by the TOC chip connected to the SLVIO EBus. A single lithium battery within the NVRAM module provides battery backup for approximately 10 years.

The NVRAM stores the default system configuration parameters. You can modify these parameters using the FORTH Toolkit in the OBP.

Time-of-Day Clock (TOD)

The NVRAM chip contains the time-of-day clock (TOD). A lithium battery within the NVRAM module provides battery backup for the TOD.

2.2.3 *LXE Board Connectors*

SBus Slot (SBus Devices) Connectors

Two physical SBus 96-pin high-density connectors are located on the Themis SPARC LXE board supporting either 2 single slot or one dual slot SBUS card(s)[1].

The SBus is an open systems 32-bit synchronous bus with a 28-bit address space and support any available SBus board. The physical slots have full master/slave capabilities. Additional mechanical support must be provided in your enclosure design for the SBus cards, as defined in the SBus specifications.

1. Single slot SBus card only on 4 SIMM socket version.

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Main Memory DRAM SIMM Female Connectors

Two or four SIMM sockets allow memory expansion by up to 64MB in addition to the 8 or 32MB of onboard DRAM. The physical characteristics of the four socket design prevents access to the second SBus slot (SBUS 1).

SCSI Female Connector

This front panel, 50-pin dual-row high density SCSI-2 connector can be used to attach any SCSI/SCSI-2 device. All SCSI signals are also provided on the backplane P2 connector and are accessible through the paddle adapter.

Speaker/LED Male Connector

A 4-pin connector providing monophonic sound output to a external speaker.

10base-T Ethernet

Supplies Ethernet connectivity to a hub or router.

Mouse/Keyboard Connector

Support for a standard SUN Type-4 or Type-5 keyboard and mouse.

2.3 *System Considerations*

2.3.1 *Required Initial Power-Up System Components*

A VME system rack with power supply

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Themis SPARC LXE Specifications



3.1 Themis SPARC LXE Board

Physical Dimensions	
CPU Board Size:	6U VME form factor
Height	233.35 mm (9.187 in.)
Depth	160 mm (6.299 in.)

Microprocessor Performance Figures (50MHz)	
IU Performance	47.3 MIPS
FPU Performance	4.6 Linpack MFLOPS Double Precision
SPECint92	26.4
SPECfp92	21.0

RISC Microprocessor	
Microprocessor	Tsunami @ 40 MHz
FPU	Meiko Design FPU
Cache Controller	Cache
Memory Controller	Reference MMU
Testing Support	JTAG scan support, built-in self-testing

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RISC Microprocessor (Continued)	
Packaging	288 pin 10 mil pitch TAB
Integer Unit	Sun Microsystems SPARC IU
IU Performance	59.1 MIPS @ 50 MHz
Architecture	Harvard
Cache Streaming Support	Instruction and Data
Floating Point Unit	Meiko Design FPU
FPU Performance	3.7 MFLOPS @ 40 MHz
Instructions	Single and double precision
Cache Instruction	4 KB direct-mapped write-through, virtual
Cache Data	2 KB direct-mapped write-through, virtual
Cache Write Buffering	Two double-word
Cache Recovery	Complete write-fault recovery supported
Cache Linesize	32-byte

Input/Output	
SBus Devices	5 master/slave devices
SBus Slots	2 physical slots
SBus Standard	SBus specifications, Revision A.2
SBus Data Size	32-bit full master/slave (all slots)
SBus Clock Rate	20 MHz
SBus Write Sizes	Maximum 16 byte burst
SBus Writes	Quad/doubleword burst mode supported
SCSI Port	One 50-pin connector and signals to backplane P2 connector
SCSI Standard	ANSI X3.133
SCSI Types	synchronous/asynchronous (host)
SCSI Performance	Up to 10 MB per second (synchronous) (fast)
Ethernet Port	Twisted-pair signals to RJ45 front connector; AUI signals to backplane P2 connector
Ethernet Standard	IEEE 802.3
Parallel Port	Signals to backplane P2 connector
Parallel Port Standards	Bi-directional 8-bit Centronics-compatible

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Input/Output (Continued)	
Serial A/B Ports	Signals to DB 26-pin front connector
Serial Standard	RS232C
Serial Types	synchronous/asynchronous
Serial Configuration	DCE (channel A)
Serial Performance	19200 (19.2 Kbit) bauds
Serial C/D Ports*	Signals to backplane P2 connector
Serial Standard	RS232
Serial Types	asynchronous
Serial Performance	38400 baud
K/M Port*	Signals to 8-pin DIN front connector
K/M Type	asynchronous
K/M Configuration	DTE
K/M Performance	38400 baud
Audio Speaker Port	Signals to VME P2 connector†
Audio Microphone Port	Signals to VME P2 connector (Mono)
Audio CHI Port	Signals to VME P2 connector
Audio Performance	Voice standard (8-bit) and CD quality (16-bit)
Audio Speaker	32 Ohms

* Keyboard/Mouse ports and serial ports C/D cannot be used simultaneously.
† Accessable through paddle board

On-board Main Memory	
Type of memory	Parity memory (1 parity bit per 32 bits)
On-card DRAM Banks	2 or 4
SIMMs per Bank	2
DRAM SIMM Specs	72-pin (x 33 or x 36)
DRAM Speed	70 nsec fast-page mode
DRAM Expansion Range	8 MB to 96 MB (16 MB minimum for Solaris 2.2)

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SBus	
SBus Controller Chip	microSPARC
SBus Physical Ports	Two female SBus 96-pin connectors

VMEbus	
VME Interface Controller	Sun Microsystems S4
VME Master Capabilites	A32/A24/A16 D32/D16/D8 RMW
VME Slave Capabilities	A32/A24 D32
Arbiter Options	Single Level or Round Robin
Requester Options	ROR with fair request option
Interrupter Options	None
Interrupt Handler	IRQ1-7, fixed VME-MMU mapping

3.2 *Themis SPARC LXE Electrical Specifications*

Power Requirements For This Product	
Power Dissipation	< 33 Watts (not including SBus cards)

+5VDC 0-5%
maximum5 Amperes
(no SBus card, no hard disk drive, and no optional memory)

RS232/Ethernet Power Supply
+12VDC +8%/-10%
-12VDC 1 10%
maximum 0.0–0.1 Amperes
(no hard disk drive)

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Power Dissipation	
For a system with 40 MB of DRAM and no SBus cards:	
Typical	24 Watts
Maximum	33 Watts

3.3 *Themis SPARC LXE Environmental Specifications*

The following environmental specifications for the Themis SPARC LXE board are presented for your information only. NOTE: The testing was performed using a standard Sun Microsystems workstation enclosure.

Operating Environmental Requirements For This Product		
Values	*Minimum*	*Maximum*
Temperature Range	32° F (0° C)	122° F (50° C)
Humidity Range relative non-condensing at 104° F (40° C):	5%	95%
Altitude Range	0 feet (0 m)	30,000 feet (9,144 m)

Non-Operating Environmental Requirements For This Product		
Temperature Range	-4° F (-20° C)	167° F (75° C)
Humidity Range relative non-condensing at 104° F (40° C):	5%	95%
Altitude Range	0 feet (0 m)	40,000 feet (12,192 m)

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Themis SPARC LXE Installation



4.1 Registering Your SPARC LXE

Please review the Themis Computer warranty and complete the product registration card delivered with your LXE board(s). Return of the registration card is not required to activate your product warranty, but by registering your LXE, Themis Computer will be able provide you with timely update information and product enhancement notifications.

For your convenience a product response card and problem report form have been included at the end of this manual should you have any comments or encounter a problem.

Themis Computer values its customers and listens to them. Our marketing department is eager to know what you think of our products and our customer support department is committed to providing the best product support in the industry.

Customer support is available 8AM to 5PM PST, Monday through Friday via telephone, fax or email.

Customer Support:
Phone: 510-734-0870
Fax: 510-734-0873
Email: support@themis.com

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4.2 *Unpacking The SPARC LXE*

Caution – The SPARC LXE contains statically sensitive components. Industry standard anti-static measures should be observed when removing the LXE from its shipping container and during any subsequent handling

A *wrist strap* (or *grounding strap*) provides grounding for static electricity between your body and the chassis of the system unit. Electric current and voltage do not pass through the wrist strap.

Before handling the LXE, attach the wrist strap to your wrist and to the metal casing of your grounded chassis.

Caution – Boards and modules can be damaged by harmful electrical charges if you do not wear a wrist strap.

To attach the wrist strap:

1. **Wrap the grounding strap twice around your wrist.**
   Make sure the adhesive side is against your skin
2. **Attach the grounding wire to a chassis or other ground connection**

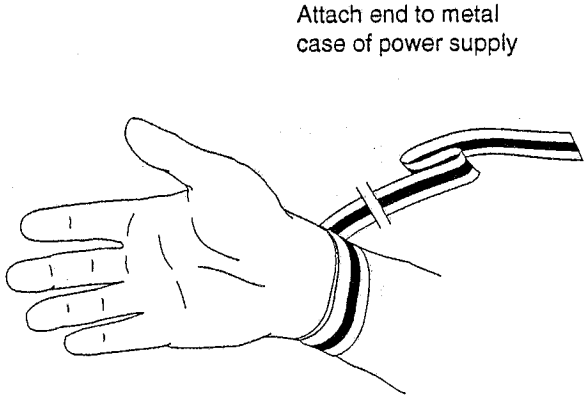


Figure 0-1 Attaching a Wrist Strap

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Remove the LXE and accessories from its shipping container and check the contents against the packing list. The package should include:

1. SPARC LXE
2. Dual serial null-modem cable
3. SCSI cables (2)
4. LXE paddle board
5. This manual

Report any discrepancies to Themis customer support immediately.

Remove the SPARC LXE CPU board from its anti-static wrapping. If you have ordered your LXE with more than 32MB DRAM, 2 or 4 SIMM sockets will be occupied by SIMM modules.

4.3 *Configuring the SPARC LXE*

Confirm installation of all factory default jumpers (see diagram below and *LXE Jumper Location and Settings on page 46*). The default configuration supports the following:

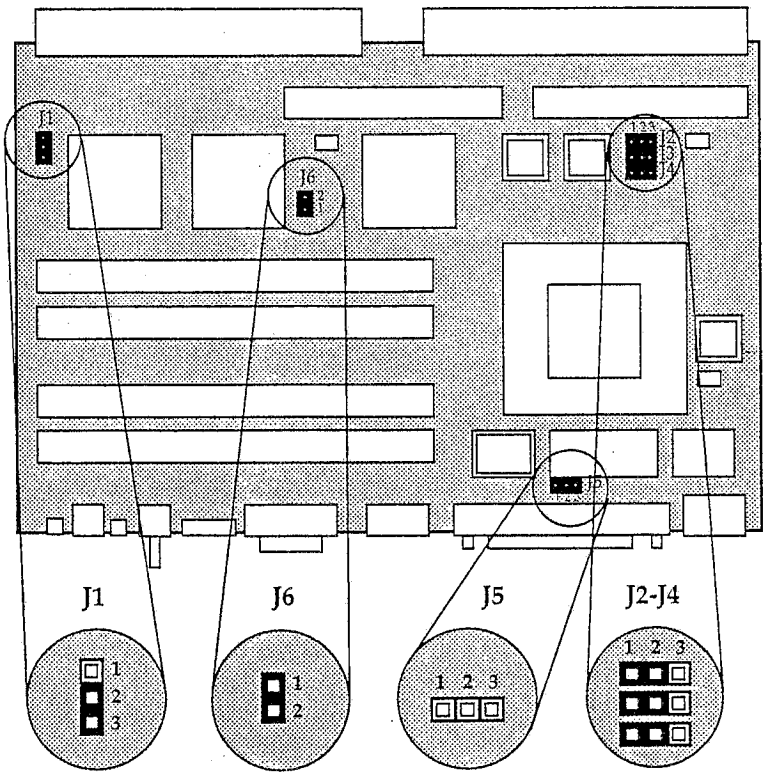
- LXE as Slot 1 System Controller
- Keyboard/Mouse ports connect to front panel
- SCSI termination active
- Front panel RESET switch enabled

If the default jumper settings meet your requirements you are now ready to install the LXE in a standard VME chassis. If re-configuration is required, follow the instructions in *LXE Jumper Location and Settings on page 46* for setting board jumpers to match your application.

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Caution – If you are not installing the LXE as a slot 1 system controller, jumper J1 must be set to 1-2.

Figure 4-1 LXE default jumper settings



In addition to the LXE hardware a standard VME chassis with P1/P2 backplane is required. If you intend to use the LXE in a workstation configuration instead of as an embedded controller, you will also need a hard disk and graphics frame buffer or serial terminal.

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4.4 *Configuring The VME Interface*

Only the slot-1/system controller capability of the LXE board is configured via a hardware jumper. All other VMEbus interface related options are configured using extensions to the Sun OpenBoot PROM monitor program. OBP stores system configuration parameters in non-volatile storage (NVRAM) using a `setenv` mechanism familiar to UNIX shell users.

The default configuration upon delivery of the LXE (or after restoring the factory default values via `L1-N`) is:

- VME slave accesses disabled
- VME slave base address at 0x00
- VME master accesses map to offset 0x00
- Mailbox interrupts disabled
- Mailbox interrupt at level 1

This configuration is typically sufficient for simple VME configurations with a limited number of I/O boards present. For complex configurations and implementations requiring slave accesses to the LXE DVMA space, this default configuration may require changes. Themis has implemented the following environment variables for this purpose (see also *OpenBoot PROM Extension Commands on page 79*):

- `vme-slave-address` sets the slave base address for the LXE.
- `vme-master-address` determines the offset of the 512MB VME window in the VMEbus address space.
- `vme-mailbox-interrupt-level` sets the local interrupt level for mailbox interrupts.
- `vme-mailbox-address` sets the address in A16 space at which the mailbox will be located.
- `vme-slave-enable?` enables slaves access to the LXE if set to `true`.
- `vme-mailbox-interrupt-enable?` enables mailbox interrupts if set to `true`.

The OBP command **`setenv`** must be used to set the values of these environment variables. The **`printenv`** command will list all supported environment variables and can be used to verify proper setting. You must be at the OpenBoot command prompt to enter and execute OpenBoot commands.

If autoboot is enabled, interrupt the boot sequence by pressing `L1-A` (`STOP-A`); on an serial terminal press `BREAK`.

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If BOOTMON compatibility mode is enabled, you will initially see the BOOTMON prompt. Enter n to start OpenBoot:

```
Type b (boot), c (continue), or n (new command mode)
>n
ok>
```

At the ok> prompt you are now able to enter OBP commands. Use setenv to modify the environment variables necessary to configure the LXE for your VMEbus configurations.

The following example moves the 512MB VME master access window of the LXE to 0x10000000 in the A32 address space, the slave window to 0x80000000 and enables slave accesses:

```
ok> setenv vme-master-address 0x1000.0000
ok> setenv vme-slave-address 0x8000.0000
ok> setenv vme-slave-enable? true
```

The OBP automatically programs the S4 VME interface chip with the correct register values and retains your settings in NVRAM.



Caution – Unless you are familiar with the Forth Monitor and are experienced in interacting with your system PROM, restrict yourself to the most basic Forth Monitor operations. That is, to syncing your disks, ejecting floppies from the diskette drive, booting your system and configuring the VME interface. More advanced commands can do damage to your system's operation.

4.5 *Installing The LXE Paddle Board*

The paddle delivered with the LXE attaches to the rear of the P2 backplane and provides industry standard connectors for serial ports C&D, Ethernet, SCSI, printer and speaker.

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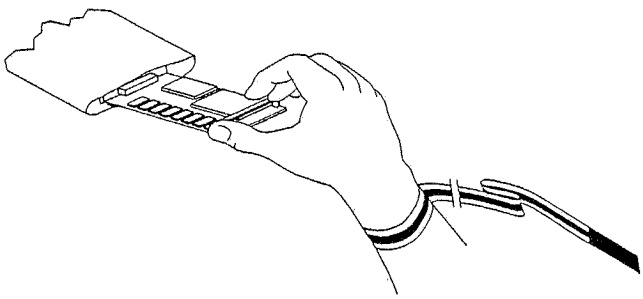
The board contains no statically sensitive components but should be handled with care to avoid bending pins on the connectors.

Two P2 connectors allow secure installation of the paddle at the rear of the P2 backplane.

4.6 *Installing An SBus Card*

Two single slot SBus cards or one dual-slot SBus card can be attached to the LXE via the SBus connectors[1].

Remove the SBus card from its anti-static packaging.

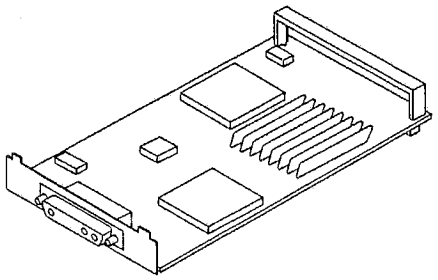


Typically an SBus card includes a metal front panel and a plastic handle on the component side to facilitate easy installation and removal of the card.

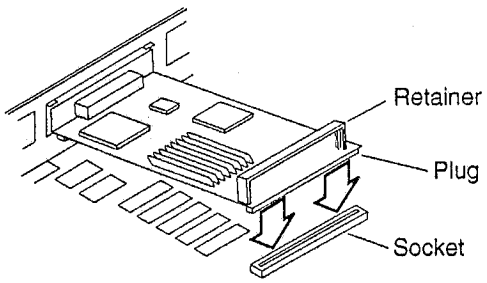
Remove the filler plate in the front panel of the LXE corresponding to the SBus slot(s) you wish to install your card in. Retain the mounting screws as you will need them to secure the card you are installing.

1. LXE version with 4 SIMM sockets support a one single-slot SBus card only

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To install the SBus card, insert its front panel into the LXE front panel cutout and insert the SBus plug into the SBus socket on the LXE while holding the card by its plastic retainer. Secure the card to the front panel with the mounting screws supplied with the SBus card.

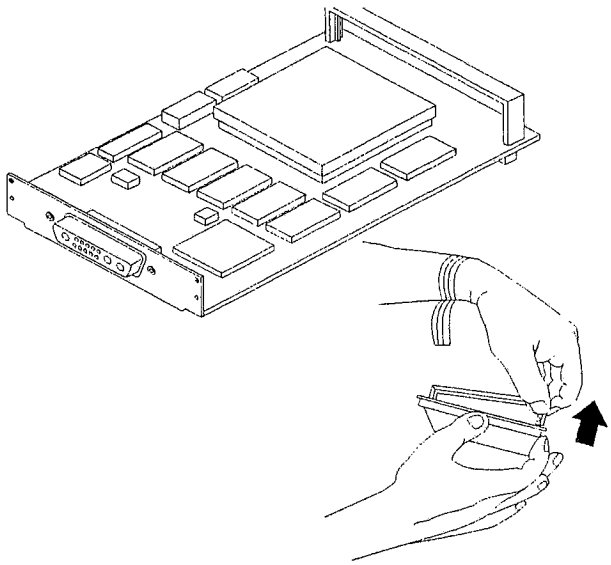




Caution – Observe all necessary anti-static measures to prevent damage to the LXE and the SBus card being installed.

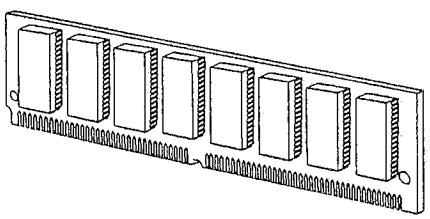
In a full populated VME chassis, with slot space at a premium, the plastic retainer of certain SBus cards may prevent additional VME boards from properly inserting in the adjacent slot. Should this occur, simply remove the plastic retainer from the SBus card by pulling each end of the retainer from its mounting hole.

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4.7 *Installing SIMM Memory*

The on-board memory capacity of the LXE can be expanded by installing two or four SIMM modules (4MB or 16MB per module).



The LXE utilizes standard 33-bit Sun SIMM modules (also available from 3rd party sources).

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4.8 Attaching the LXE To A Network

The LXE features both a 10Base-T front panel connector as well as a AUI interface connector on the paddle board. An auto-select circuitry determines the active interface upon power-up. The default interface is 10Base-T and the AUI interface is only selected if a drop cable and media attachment unit (MAU) are connected to the paddle board.

After attaching the LXE to the network, you can verify proper physical connection by executing the Forth monitor network selftest function:

```
ok> test net

Using AUI Ethernet Interface
Lance Register test -- succeeded
Internal loopback test -- succeeded
External loopback test -- Lost Carrier (transceiver cable problem?)
send failed

Using TP Ethernet Interface
Lance Register test -- succeeded
Internal loopback test -- succeeded
External loopback test -- succeeded
send ok
net selftest succeeded
```

This test will indicate external loopback failure on the selected network interface if no proper physical connection exists. As only one interface can be active, the unattached network interface will always return an external loopback error.

4.9 Attaching a Keyboard and Mouse

A standard SUN type 4 or type keyboard/mouse combination can be attached to the front panel keyboard connector.

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5.1 Introduction

This guide is intended to provide helpful information and tips to those wanting to program the Themis LXE board without the aid of an operating system or real-time kernel.

Detailed information concerning on-board device interfaces, memory maps and device accesses are contained in the appendices and should be consulted while reading this guide.

The Themis LXE microSPARC processor board implements a SPARC LX/SPARCclassic compatible workstation on a single- or double-width 6U VMEbus board. A full VME master/slave interface is included, using the Sun S4 Sbus-VMEbus controller. This guide is primarily concerned with the implementation and programming of LXE specific features not those common to the microSPARC family of workstations (SPARC LX/SPARCclassic). A comprehensive list of additional reference literature and data sheets is included at the end of this guide.

Because of the flexibility and power of the OpenBoot PROM (OPB) it is recommended that developers retain the OPB if possible.

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5.2 LXE VME Interface

5.2.1 System Controller

The LXE features a slot one system controller including SYSCLK, SYSRESET, bus time-out and four level arbiter. System controller capabilities are enabled by installing jumper J1 1-2 (see *LXE Jumper Locations and Configuration* on page 72)

Both single arbitration or round-robin arbiters are support

5.2.2 VMEbus Master Interface

The master interface of the LXE supports 8, 16 and 32-bit data transfer cycles in A32, A24 and A16 addressing modes. Unaligned data transfers, block mode transfers and longword accesses to word-wide slaves are not support.

The VMEbus is made accessible to the Tsunami processor by mapping the 256MB address spaces of SBus slots 2 and 3 to the VMEbus. This mapping yields a total VME address range of 512MB.

Because of the limited local address space compared to the 4GB space of the A32 VME address space and the fact that the VMEbus supports multiple addressing modes, a flexible mapping scheme has been developed to allow mapping of varying portions and combinations of the 3 primary VME addressing modes (A32, A24, A16) and their sub-modes.

Four pre-defined addressing maps are available and selectable through the VMEREG VME control register. These maps are described in detail in *Master VME and SBus Slot 2&3 Address Mapping* on page 62. Each individual map divides the available SBus slot address space into combinations of A32, A24 and A16 modes and maps local accesses to the corresponding VME accesses. The address maps are static and limited to the four maps listed but provide considerable flexibility for systems configuration. Complex VMEbus systems with a large mix of boards will required careful analysis to determine the most appropriate map selection.

Note – Under the Solaris operating system, the VME driver automatically loads the VMEREG master address bits based on the VME devices configured into the kernel.

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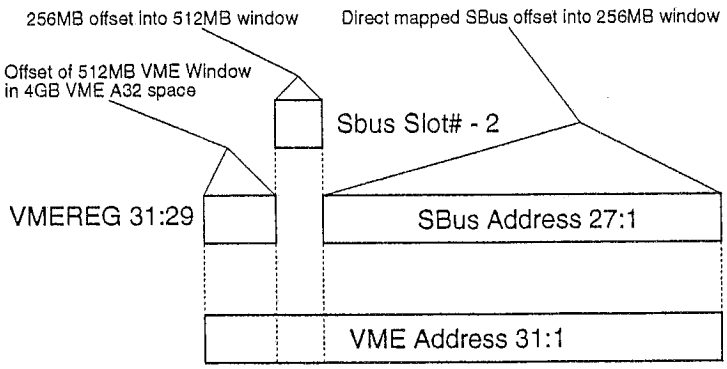
Map selection is done through bits 1:0 of the VME control register (see *VME Control Register* on page 69).

The mapping bits in the VME Control Register are pre-loaded upon power-up by the Openboot Prom, initialized from a set of environment variables described in *OpenBoot PROM Extension Commands* on page 75. Use of the OBP variable `vme-master-address` allows transparent setting of the correct VME Control Register bits.

Note – The VME Address bits in the S4VME A32 MAP Register are not used.

The VME addresses is derived as follows:

Figure 5-1 VME Master Address Generation



Explicit control of address modifier bits AM0 and AM2 are provided through bits 27:26 of the VMEREG register.

5.2.3 *VMEbus Slave Interface*

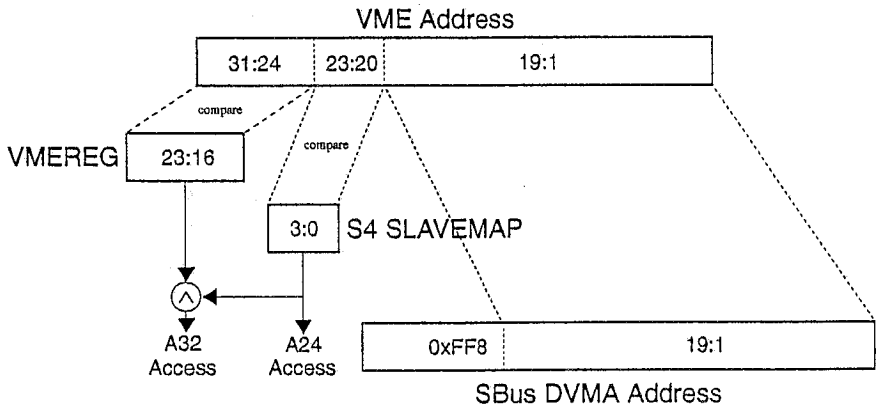
The VME slave interface implemented on the Themis LXE supports A32 and A24 slave accesses. A limited block mode transfer capability is also supported.

The S4VME controller limits the slave address window accessible from the VMEbus to 1MB. VME slave accesses generate local Sbus DVMA accesses. The slave base address is set in the VMEREG control register (see *Slave VME and SBus DVMA Address Generation* on page 63).

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All slave accesses generate SBus DVMA addresses of 0xFF8X.XXXX. For A24 accesses VME address bits 23:20 are compared to S4 SLAVEMAP register bits 3:0. For A32 accesses VME address bits 31:24 are also compared to VMEREG bits 23:16 as shown in Figure 5-2.

Figure 5-2 VME Slave Access Address Generation



The LXE supports block mode slave accesses. Block mode accesses are limited to 4 longword transfers - any other length or word size transfers are ignored.

Use of the OBP variables `vme-slave-address` and `vme-slave-enable?` (described in *OpenBoot PROM Extension Commands* on page 75) allows transparent setting of the correct VMEREG and S4 SLAVEREG bits.

5.2.4 *VMEbus Interrupt Sources*

The VMEbus interface of the LXE supports all 7 VME interrupt levels. The S4 chip implements a mask register to selectively enable/disable specific VMEbus interrupt levels. A set of 7 VMEIACK interrupt acknowledge register allow retrieval of the interrupt vector for each interrupt level. Reading a VMEIACK register performs an interrupt acknowledge cycle on the VMEbus and returns the interrupt vector of the interrupting device (see *VME IACK Cycles* on page 50 for details).

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5.2.5 *VMEbus Inter-Process Communication Registers/Mailboxes*

To facilitate inter-process communications in multi-processor VME environments, the LXE implements a set of mailbox registers. These registers are located in the A16 address space and programmed through the S4VME controller chip.

The Mailbox Control Register (see *Mailbox Interface* on page 49) defines a location in the A16 address space that, when accessed in byte or word mode, generates a local interrupt defined in the Mailbox Interrupt Register.

Configuration on power-up/reset initialization of the mailbox control registers are performed by the OpenBoot PROM. The environment variables vme-mailbox-interrupt-enable?, vme-mailbox-address and vme-mailbox-interrupt-level are used to configure the required S4VME chip registers. Please refer to *OpenBoot PROM Extension Commands* on page 79 for further details.

Note – Mailbox registers are not supported under Solaris 1.1 or 2.X for compatibility with existing Sun VME interface implementations.

5.3 *VME Interface And Solaris 1.1/2.X*

Great effort has been expended to achieve complete compatibility between Sun VME implementations and the device driver interface implemented for the LXE board under Solaris.

The VMEbus interface of the LXE is transparently implemented under Solaris 1.1 (SunOS 4.1.3) and Solaris 2.3, compatible with generic Sun4 VME architecture systems.

A VME device driver provides the standard `/dev` devices for accessing the VMEbus from user processes:

```
/dev/vme32d32

/dev/vme32d16

/dev/vme32

/dev/vme24d32

/dev/vme24d16
```


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```
/dev/vme24

/dev/vme16d32

/dev/vme16d16

/dev/vme16
```

Read(), write() and mmap() calls are support and no special ioctl() calls are required to configure the interface. VME interface configuration is performed under OBP and should not be modified while the operating system is running.

The OpenBoot PROM has been enhanced with a set of environment variables that configure slave and master access windows and mailbox interrupts and maintain these values in NVRAM. The kernel uses these OBP variables to initalize the VME interface. Address maps and base address are typically configured and finalized during system integration and after all VMEbus board base addresses have been configured. Run-time mapping and address changes are not required. Please see *OpenBoot PROM Extension Commands* on page 79 for details on the available OBP configuration commands. OBP retains your configuration in NVRAM.

Note – TheVME driver only uses VME map 0. Maps 1-3 are not supported.

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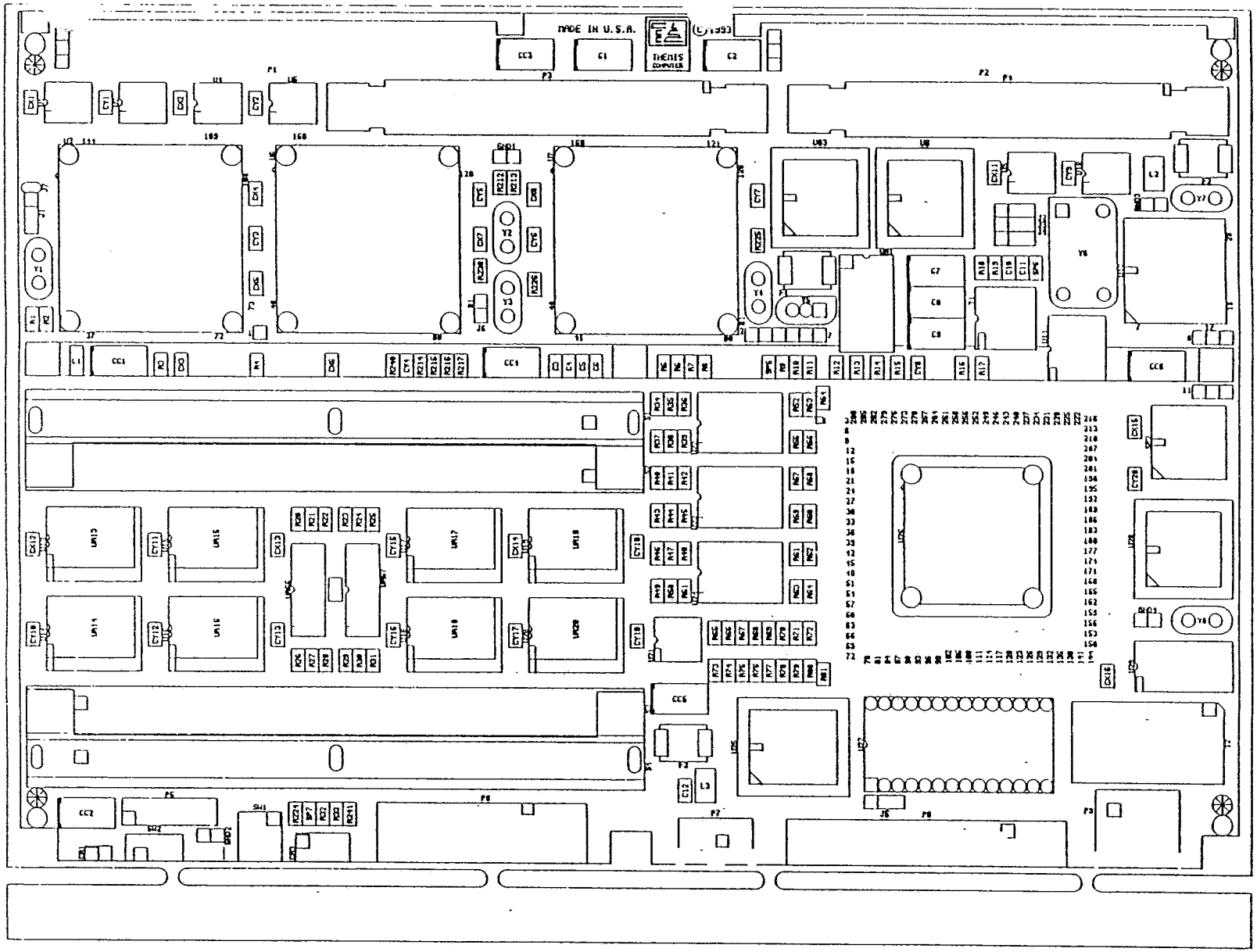
Themis SPARC LXE Board Drawings



This appendix contains the assembly drawings for the Themis SPARC LXE board.

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QTY REQD	FSCM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION
			PARTS LIST	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.XX ±
.XXX ±

MATERIAL

FINISH

NEXT ASSY | USED ON

APPLICATION

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN Q Cooley	06/93
CHECKED	
ISSUED	

THEMIS COMPUTER

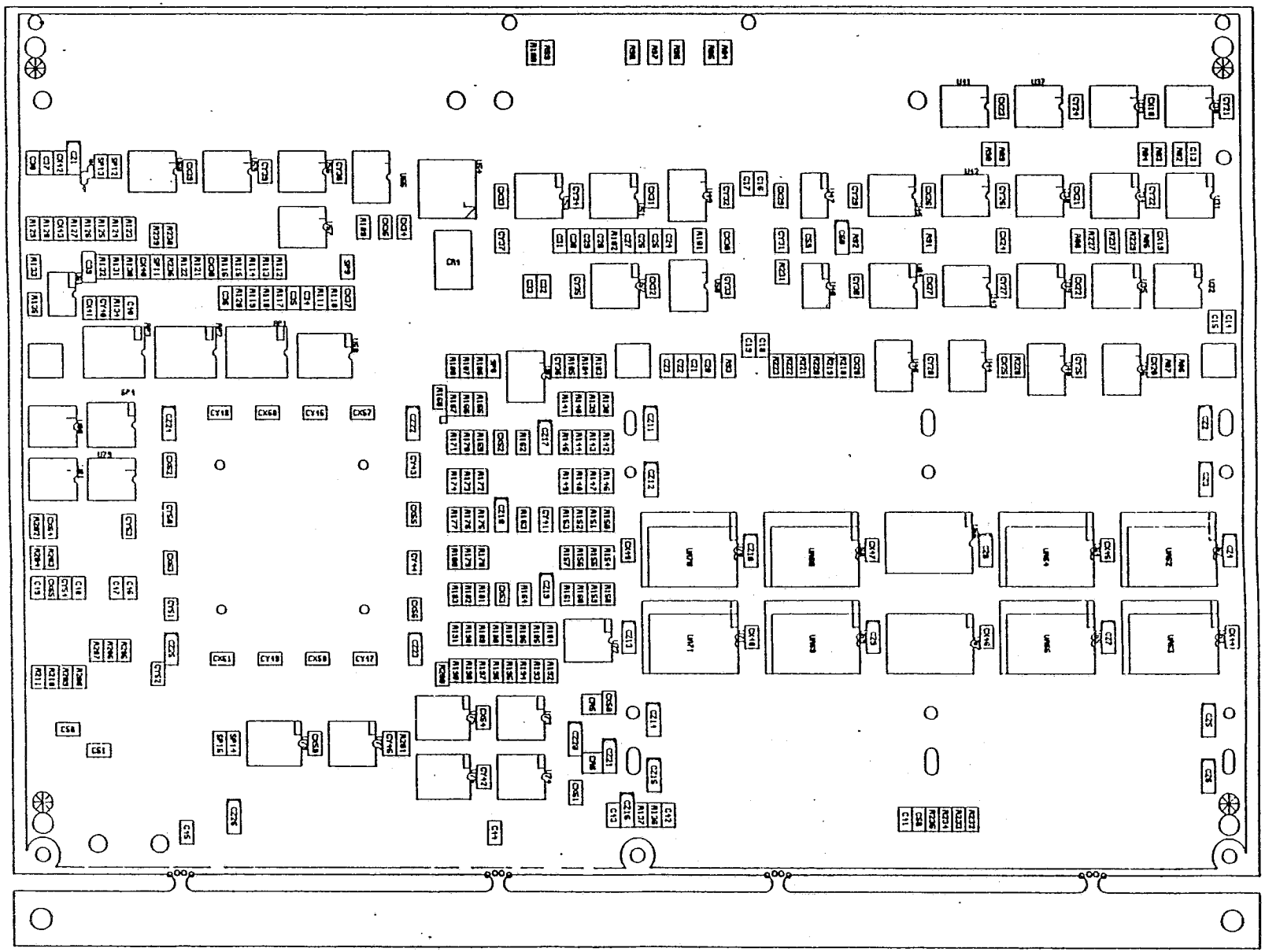
ASSEMBLY DRAWING
SPARC LXE

SIZE	FSCM NO.	DWG. NO.	REV
D		101758	02A

SCALE 2/1 SHEET 1 OF 2

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BACK



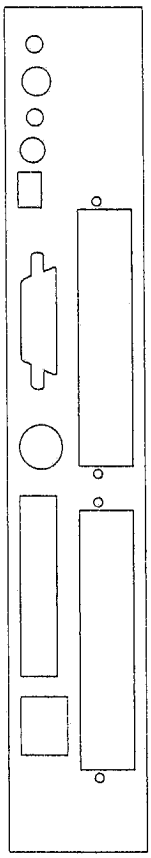
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ISSUED	SCALE 2/1		SHEET 2 OF

2 1

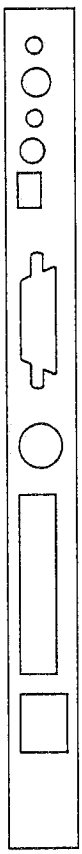
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Themis SPARC LXE Front Panels

Double Width Panel



Single Width Panel

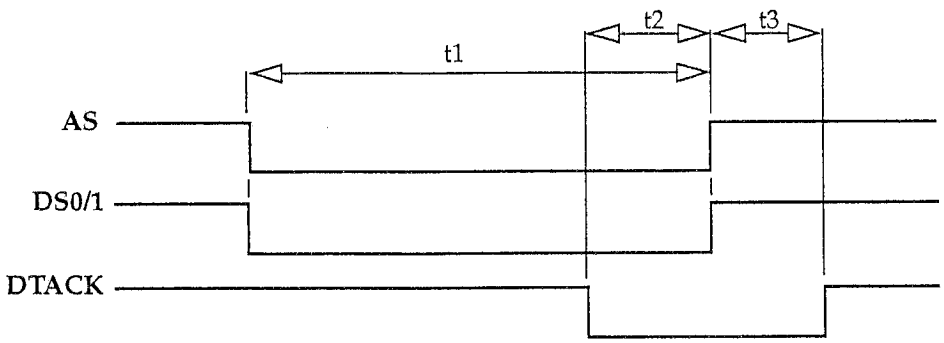


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VME Access Speed

VMEbus transfer speeds measured with an LXE in slave mode and no SBus modules installed using a digital storagae oscillosacope.



	Write Access			Read Access			
	Min	Typ	Max	Min	Typ	Max	
t1	0.62	0.75	0.87	0.75	1.1	1.4	us
t2	0.11		0.12	0.11		0.12	us
t3	0.12		0.14	0.12		0.14	us
Throughput	3.96	4.54	5.4	2.6	3.25	4.6	MB/s

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Sun S4-VME (R5) Chip Set Specifications

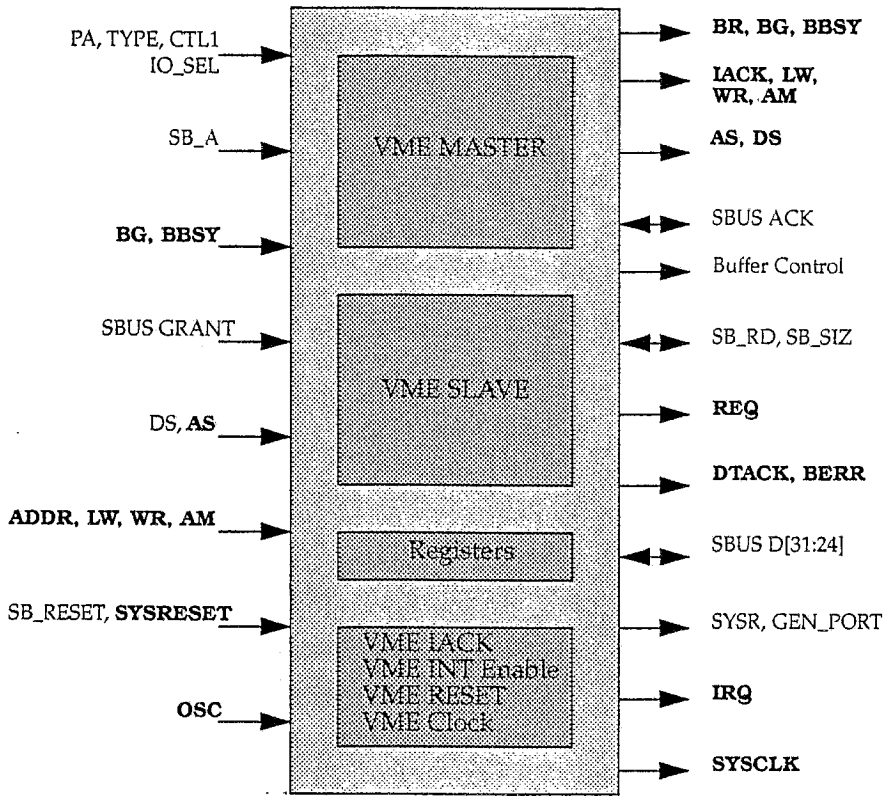


The appendix contains an abbreviated version of the specifications for the Sun Microsystems S4 Chip Set (Sun SPARC™ Support System).

D.1 Features

- A32/A24/A16 Master (Sun-4 VME Device) and A24/A32 Slave DVMA device as SBus DMA device.
- Offers both Single level and Round Robin arbitration with bus arbiter timer.
- VME Interrupt Handler, IACK Daisy Chain Driver, Clock Driver.
- Supports Block Mode transfers and SBus burst cycles on slave accesses for fast DMA.
- Fast bus arbitration by supporting early release enabling bus arbitration concurrent with data accesses.
- Includes multiprocessing support with mail box interrupts, programmable slave base address ranges, true Read Modify Write (Master), and VMEbus locker (Slave).
- Full 4GByte VME addressing with mapping register.

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D.2 *Functional Description*

The S4-VME controller interfaces the Sbus to the VMEbus. When acting as a Sbus Slave, i.e., VMEbus Master, the VMEbus is a physical device in type 2 or 3 space. During Sbus Master cycles, i.e., VME Slave cycles, it will appear as an Sbus slot device. Refer to the Sbus specification for further explanation.

The S4-VME chip contains all functionality to implement a full VME interface.

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D.3 Registers

Following is a list of the VME Interface Registers:

Name	Physical Base	Size
Bus Locker	0xEFE00000	byte
IACK cycle (Interrupt Level 1)	0xEFE00003	byte
ACK cycle (Interrupt Level 2)	0xEFE00005	byte
ACK cycle (Interrupt Level 3)	0xEFE00007	byte
ACK cycle (Interrupt Level 4)	0xEFE00009	byte
ACK cycle (Interrupt Level 5)	0xEFE0000B	byte
ACK cycle (Interrupt Level 6)	0xEFE0000D	byte
ACK cycle (Interrupt Level 7)	0xEFE0000F	byte
Interrupt Monitor	0xEFE00004	byte
MB Interrupt Level	0xEFE00008	byte
Mail Box register	0xEFE00010	byte
Interrupt Enable Register	0xEFE00014	byte
Slave Map Register	0xEFE0001C	byte

D.4 Master Interface:

A full 32-bit Master Interface is provided. Direct VME access is provided to a 512 MByte window located and adjustable within the 4 GByte A32 address space through a VME mapping register.

A32, A24, A16 address modes and D32, D16, D8(EO) data sizes are supported.

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Master RMW[1], i.e., atomic load-store cycles are implemented according to the VME specification. The VME data strobe will be asserted two times as the VME address strobe is asserted. Block mode transfers are only supported in slave mode.

Unaligned transfers (UAT) are not supported and will result in a bus time-out.

D.4.1 A32 Map Register

31	30	29	28	27	26	25	24
VME Master Addr			0	0	0	0	LoopB

This register is not used.

D.5 Slave Interface

Slave Map Register

31	30	29	28	27	26	25	24
BLM	DVMA	0	0	VME Slave Base Address			

The slave map register is a byte accessible register that controls VME slave accesses. The DVMA bit enables slave accesses when set. Slave block mode transfers are enabled by setting the BLM bit.

Note – Block mode transfers are limited in length to 4 32-byte words

In adherence to the Sun-4 architecture, the system DVMA space is limited to 1MB and normally mapped to the lowest Megabyte in the address space. Under SunOS, this lowest Megabyte is mapped to the highest Megabyte in the virtual address space. Register bits 27:24 can be used to move the base of the 1MB DVMA space within a 16MB window:

1. Read-Modify-Write

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Bits 27:24	Address Range	MB Offset
0x0	0x00000000-0x000FFFFF	0-1MB
0x1	0x00100000-0x001FFFFF	1-2MB
0x2	0x00200000-0x002FFFFF	2-3MB
0x3	0x00300000-0x003FFFFF	3-4MB
0x4	0x00400000-0x004FFFFF	4-5MB
0x5	0x00500000-0x005FFFFF	5-6MB
0x6	0x00600000-0x006FFFFF	6-7MB
0x7	0x00700000-0x007FFFFF	7-8MB
0x8	0x00800000-0x008FFFFF	8-9MB
0x9	0x00900000-0x009FFFFF	9-10MB
0xA	0x00A00000-0x00AFFFFF	10-11MB
0xB	0x00B00000-0x00BFFFFF	11-12MB
0xC	0x00C00000-0x00CFFFFF	12-13MB
0xD	0x00D00000-0x00DFFFFF	13-14MB
0xE	0x00E00000-0x00EFFFFF	14-15MB
0xF	0x00F00000-0x00FFFFFF	15-16MB

Together with the VMEREG control register, this allows mapping of the 1MB DVMA space anywhere within the 4GB VME address space.

This register is initialized to 0x0.

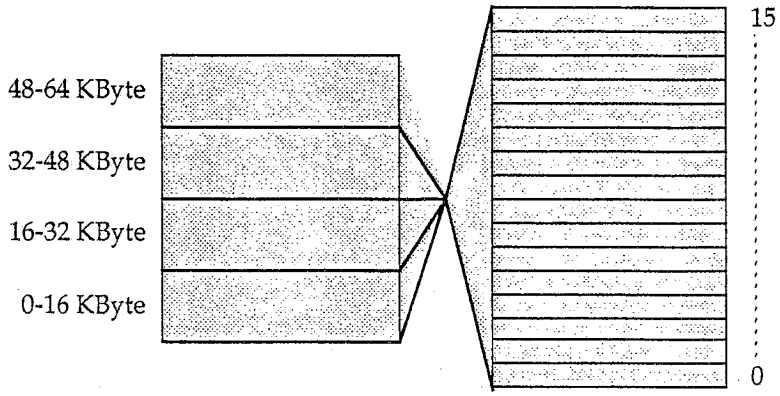
D.6 *Mailbox Interface*

Mailbox Control Register

31	30	29	28	27	26	25	24
I-FLG	EN I	0	A15:14		A3:1		

The mailbox interrupt control register is used to program a location in A16 address space that, when accessed from the VMEbus in A16 address space as using 8-bit or 16-bit access, will generate a local interrupt. Address bits 15:14,3:1 are compared to the corresponding values in the mailbox control register and a local interrupt is generated if the ENI bit is set. The I-FLG bit indicates a pending mailbox interrupt. Address bits A15:14 and A3:1 correspond to one of the first 16 words in one of four 16KB blocks respectively.

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Mailbox Interrupt Level and Rerun Length Register

31	30	29	28	27	26	25	24
MB2	MB1	MB0	RER4	RER3	RER2	RER1	RER0

This register sets the mailbox interrupt level. By default, the MB_IRQ pin is used, but by setting MB2:MB0, any of the VME interrupt lines may be selected:

BM2:MB0	Mailbox Interrupt Pin
0	MB_IRQ
1	B_IRQ1
2	B_IRQ2
3	B_IRQ3
4	B_IRQ4
5	B_IRQ5
6	B_IRQ6
7	B_IRQ7

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It also controls the number of SBUS rerun cycles before freezing a VME slave access cycle:

RER4:RER0	SBUS Rerun Cycles
0	16
1	17
2	18
...	...
31	47

D.7 VMEbus Locker

VME Bus Locker Register

31	30	29	28	27	26	25	24
OWN	0	0	0	0	0	BR	LCK

In support of multi-processor applications, a bus locker function is provided to enable the CPU to perform atomic read-modify-write (RMW) cycles to onboard memory without interrupting VME slave RMW accesses. This register is only applicable for multi-processor configurations. In a single processor implementation, this register should be left undisturbed. When used, the LCK bit must be set.

To use the bus locker properly, follow this sequence:

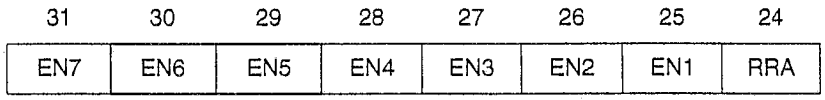
1. Disable VME interrupts (the IRQ acknowledge cycle needs to acquire the bus).
2. Request the VMEbus by setting BR (write 0x03).
3. Read the bus locker register until OWN is set indicating that the bus is owned and locked.
4. Perform RMW cycle to onboard memory.
5. Unlock the VMEbus by clearing BR (write 0x01)

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Note – If the VMEbus is not unlocked quickly, other accesses may time out, causing a system crash. Always unlock the VMEbus immediately after the RMW has completed

D.8 Interrupt Handler

Interrupt Enable/Bus Arbiter Mode Register

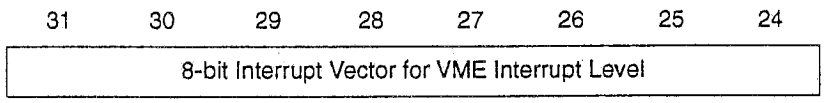


The interrupt handler can selectively handle all VMEbus interrupt levels. Specific interrupt levels are enabled in the interrupt enable register by setting the corresponding enable bits.

By default, the S4 arbiter operates in single level arbitration mode. Setting the RRA bit enables round-robin arbitration mode.

The bus arbiter function of the S4 is actually enabled via a jumper (see section E.8 on page 46).

D.9 VME IACK Cycles



Vectored VMEbus interrupts require an interrupt acknowledge cycle to be performed to retrieve the interrupt vector from the interrupting device. A set of 7 registers, corresponding to their respective VME interrupt levels, are implemented. Reading an IACK register performs a VME IACK cycle, acquires and returns the interrupt vector for the corresponding interrupt level.

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D.10 VME Interrupt Monitor Register

31	30	29	28	27	26	25	24
IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	FAIR

To avoid the necessity of performing a lengthy interrupt acknowledge cycle for a device that has removed its interrupt (spurious interrupt), the interrupt monitor register is provided. This register is a direct status representation of the VMEbus interrupt request lines. Interrupt lines are not latched and each IRQ bit in the register indicates the current status of the corresponding VMEbus IRQ line.

The FAIR bit determines the bus request mode. If set, the bus requestor will request the bus according to VMEbus specifications, namely attempting a request only when no other requestor is requesting the bus.

D.11 Bus Arbitration

Bus Requester

The implemented bus requester is an ROR requester. The bus is released whenever another master/requestor requests the bus. in FAIR (see *VME Interrupt Monitor Register*) mode, the requester will not request the bus until no other requests are active.

Bus Arbiter

Arbitration mode can be selected between single level arbiter or round robin select arbiter. The arbiter is only enabled if the S4 is configured as slot 1 system controller.

Bus Time-out

Two additional timers are used by the arbitration circuitry; an internal bus cycle timer and a VMEbus timer.

The internal timer is included in the SBus controller. To provide enough SBus bandwidth, SBus slaves must generate reruns if their cycles are too long. Two time-out parameters apply to VME master cycles (i.e. SBus slave cycles): Rerun time-out and abort.

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- Rerun Time-out. On a VME master cycle, if the slave delays DTACK for more than 1.6us, the cycle will be rerun by the IU to allow high priority SBus devices to use the bus. In the meantime, the master cycle and all output signals are frozen and any DTACK is ignored. The cycle will complete when it is rerun.
- Abort. A master VME access will time out after 300us (including the time for acquiring the VMEbus).

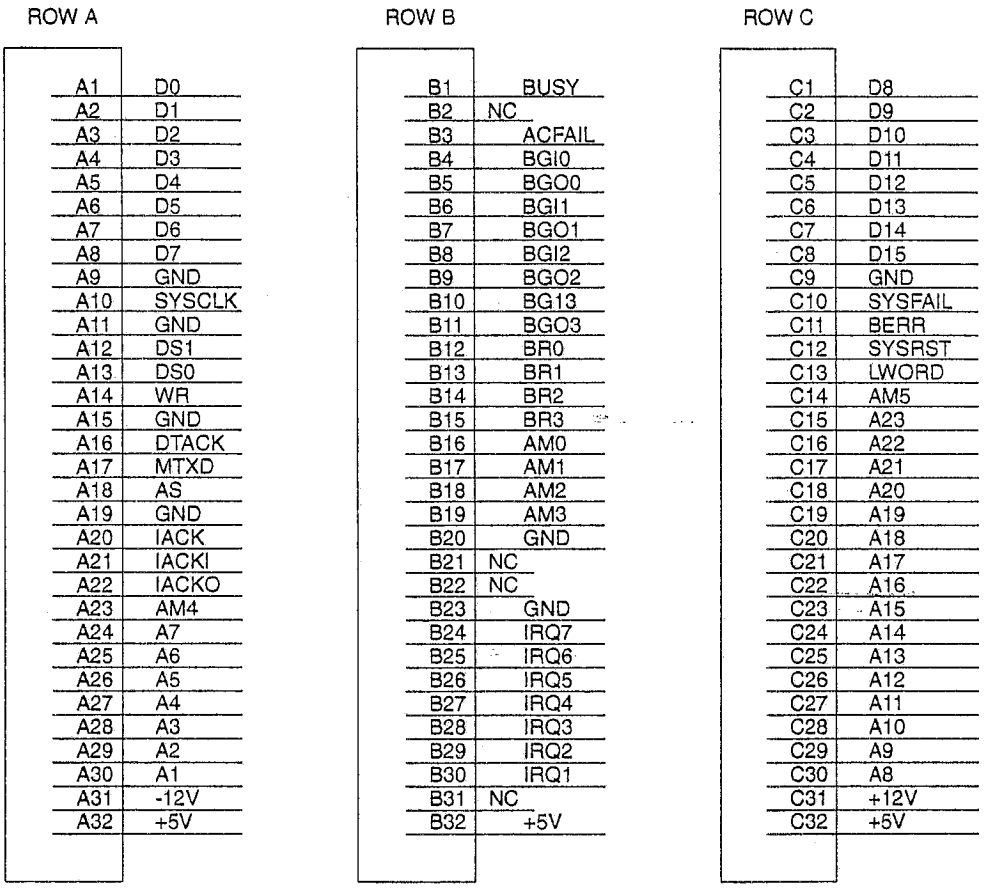
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LXE Connector Specifications



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E.1 VME Bus Connectors (P1)

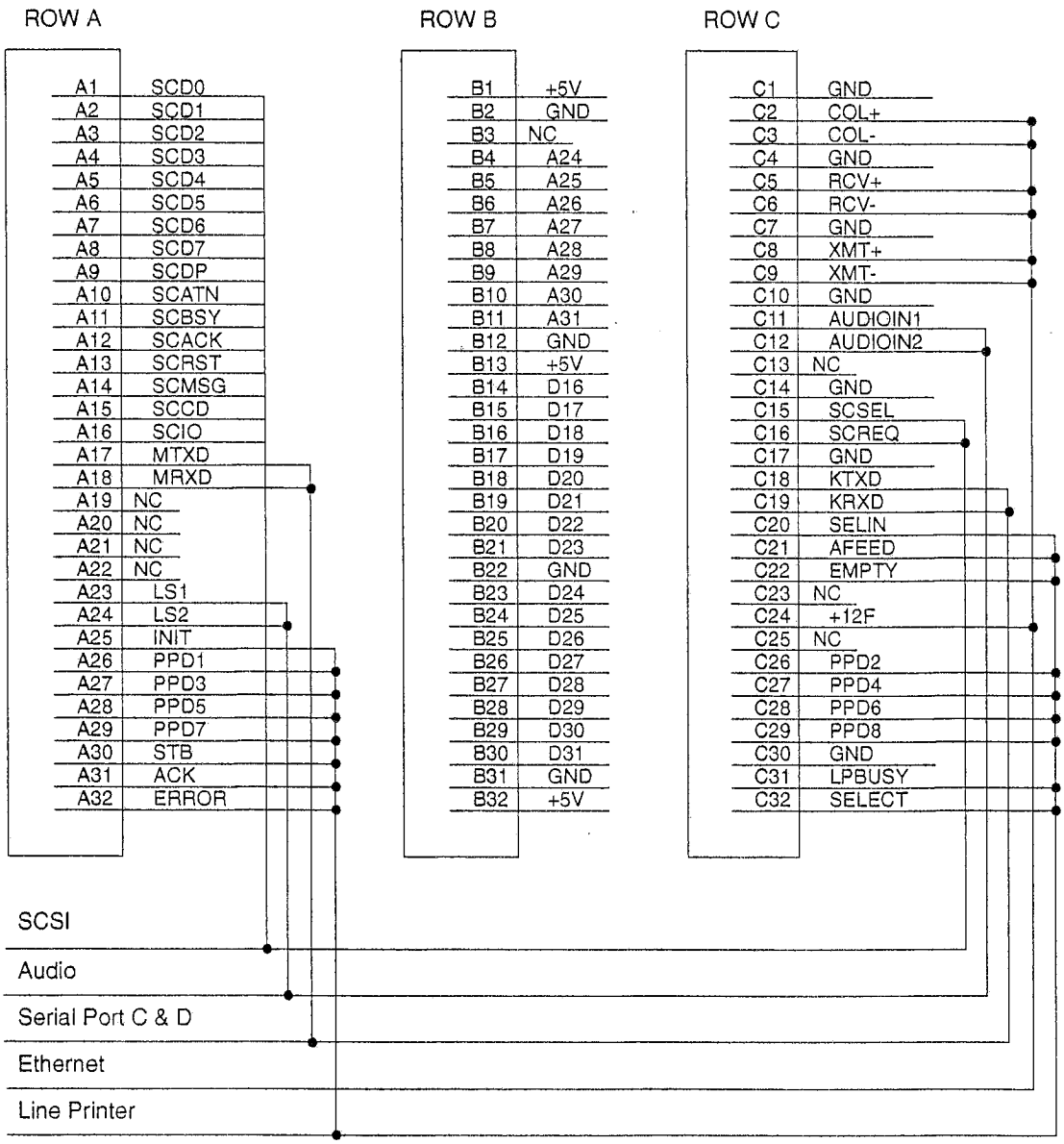


ROW A		ROW B		ROW C	
A1	D0	B1	BUSY	C1	D8
A2	D1	B2	NC	C2	D9
A3	D2	B3	ACFAIL	C3	D10
A4	D3	B4	BGI0	C4	D11
A5	D4	B5	BGO0	C5	D12
A6	D5	B6	BGI1	C6	D13
A7	D6	B7	BGO1	C7	D14
A8	D7	B8	BGI2	C8	D15
A9	GND	B9	BGO2	C9	GND
A10	SYSCLK	B10	BG13	C10	SYSFAIL
A11	GND	B11	BGO3	C11	BERR
A12	DS1	B12	BR0	C12	SYSRST
A13	DS0	B13	BR1	C13	LWORD
A14	WR	B14	BR2	C14	AM5
A15	GND	B15	BR3	C15	A23
A16	DTACK	B16	AM0	C16	A22
A17	MTXD	B17	AM1	C17	A21
A18	AS	B18	AM2	C18	A20
A19	GND	B19	AM3	C19	A19
A20	IACK	B20	GND	C20	A18
A21	IACKI	B21	NC	C21	A17
A22	IACKO	B22	NC	C22	A16
A23	AM4	B23	GND	C23	A15
A24	A7	B24	IRQ7	C24	A14
A25	A6	B25	IRQ6	C25	A13
A26	A5	B26	IRQ5	C26	A12
A27	A4	B27	IRQ4	C27	A11
A28	A3	B28	IRQ3	C28	A10
A29	A2	B29	IRQ2	C29	A9
A30	A1	B30	IRQ1	C30	A8
A31	-12V	B31	NC	C31	+12V
A32	+5V	B32	+5V	C32	+5V

"NC" stands for "Not Connected"

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E.2 VME Bus Connectors Continued (P2)



+12V is protected by a 12A polyswitch
"NC" stands for "Not Connected"

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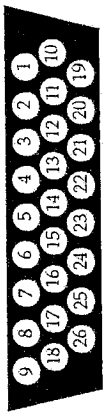
E.3 SBus Connectors Pinout: P3 (Slot 1) and P4 (Slot 0)

GND	1		49	SCLK
BR	2		50	B6
SEL	3		51	SBAS
SINT1	4		52	GND
SD0	5		53	SD1
SD2	6		54	SD3
SD4	7		55	SD5
SINT2	8		56	+5V
SD6	9		57	SD7
SD8	10		58	SD9
SD10	11		59	SD11
SINT3	12		60	GND
SD12	13		61	SD13
SD14	14		62	SD15
SD16	15		63	SD17
SINT4	16		64	+5V
SD19	17		65	SD18
SD21	18		66	SD20
SD23	19		67	SD22
SINT5	20		68	GND
SD25	21		69	SD24
SD27	22		70	SD26
SD29	23		71	SD28
SINT6	24		72	+5V
SD31	25		73	SD30
SZ0	26		74	SZ1
SZ2	27		75	SBRD
SINT7	28		76	GND
SA0	29		77	SA1
SA2	30		78	SA3
SA4	31		79	SA5
LERR	32		80	+5V
SA6	33		81	SA7
SA8	34		82	SA9
SA10	35		83	SA11
ACK0	36		84	GND
SA12	37		85	SA13
SA14	38		86	SA15
SA16	39		87	SA17
ACK1	40		88	+5V
SA18	41		89	SA19
SA20	42		90	SA21
SA22	43		91	SA23
ACK2	44		92	GND
SA24	45		93	SA25
SA26	46		94	SA27
NC	47		95	SBRST*
-12V	48		96	+12V

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E.4 Serial Ports A and B: 26-pin Connector (P6)

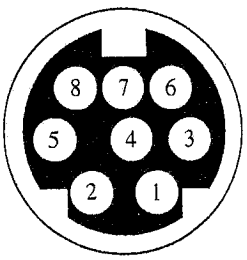
GND	1
TXDBP	2
TXDBN	3
RTSBP	4
RTSBN	5
TXCBP	6
TXCBN	7
DTRBP	8
DTRBN	9
RXDBP	10
RXDBN	11
DCDBP	12
DCDBN	13
RXCBP	14
RXCBN	15
CTSBP	16
CTSBN	17
GND	18
TDA	19
RTSA	20
TXCA	21
DTRA	22
RDA	23
CDA	24
RXCA	25
CTSA	26



Pin	Name	DB25 Pin	Port	Dir	Description
2	TXD	3	B	In	Transmitted Data from Terminal
23			A		
10	RXD	2	B	Out	Received Data to by Terminal
19			A		
16	CTS	4	B	In	Clear To Send - ON if DCE is ready to accept data
26			A		
4	RTS	5	B	Out	Request To Send - ON if DTE is ready to transmit
20			A		
1	GND	7	B	-	Signal Ground
18			A		
8	DTR	8	B	In	Data Terminal Ready - ON if DCE ready
22			A		
12	DCD	20	B	In	Data Carrier Detect
24			A		
6	Transmit Clk	24	B	In	Transmit Clock (synchronous mode)
14	Receive Clk	25	B	Out	Receive Clock (synchronous mode)

E.5 Keyboard/Mouse: 8-Pin DIN Connector (P7)

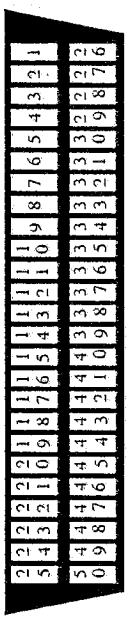
GND	1
GND	2
+5V F	3
M_RD	4
K_WR	5
K_RD	6
GND	7
+5V F	8



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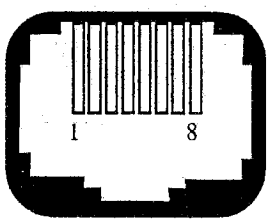
E.6 SCSI Connector: High-Density 50-pin (P8)

SCD0	26	1	GND
SCD1	27	2	GND
SCD2	28	3	GND
SCD3	29	4	GND
SCD4	30	5	GND
SCD5	31	6	GND
SCD6	32	7	GND
SCD7	33	8	GND
SCDP	34	9	GND
GND	35	10	GND
GND	36	11	GND
NC	37	12	GND
TRMPWR	38	13	GND
NC	39	14	GND
GND	40	15	GND
SCATN	41	16	GND
NC	42	17	GND
SCBSY	43	18	GND
SCACK	44	19	GND
SCRST	45	20	GND
SCMSG	46	21	GND
SCSEL	47	22	GND
SCCD	48	23	GND
SCREQ	49	24	GND
SCIO	50	25	GND



E.7 10 Base T: RJ45 Twisted-Pair Connector (P9)

TP_OUT+	1
TP_OUT-	2
TP_IN+	3
TP_IN-	6
NC	4
NC	5
NC	7
NC	8



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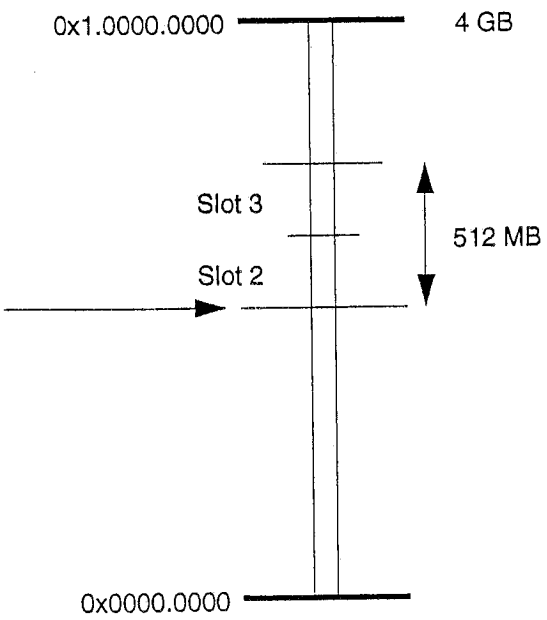
F.1 Master VME Address Generation

512MB page defined by VMEREG[31:29].

All VME boards accessed by SPARC LXE must be mapped into a single 512MB page.

Address modifier AM2 and AM0 are defined by VMEREG[27:26].

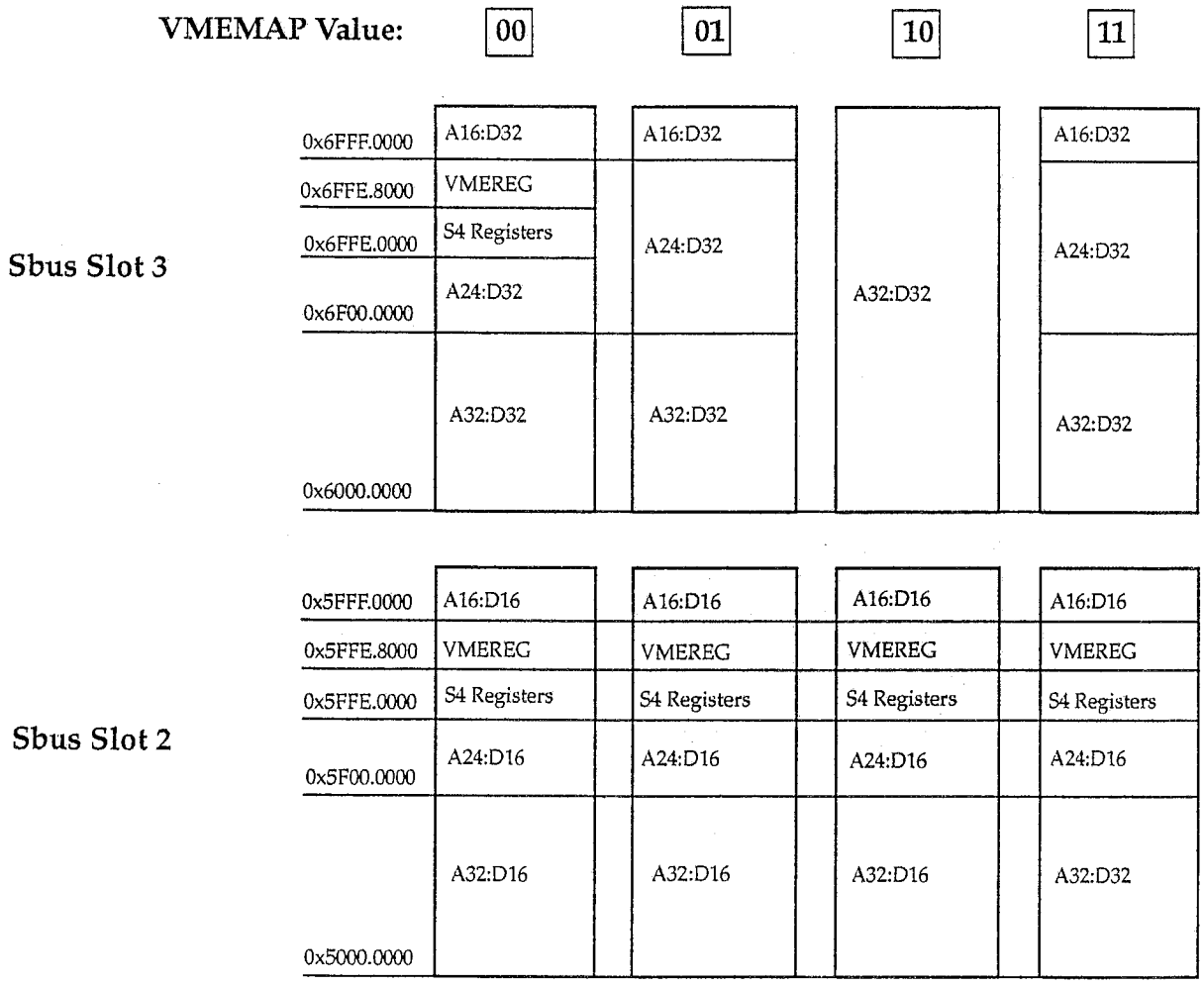
Master VMEA31 = VMEREG[31]
VMEA30 = VMEREG[30]
VMEA29 = VMEREG[29]
VMEA28 = 0 (if CPU to Slot 2)
= 1 (if CPU to slot 3)
VMEA[27:1] = SBUSA[27:1]



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F.2 *Master VME and SBus Slot 2&3 Address Mapping*

SBus slots 2 and 3 are mapped to provide master access to the VMEbus. Depending on the setting of the *VMEMAP* bits in the *VME Control Register*, one of four possible address maps may be selected and are show in the diagram below.



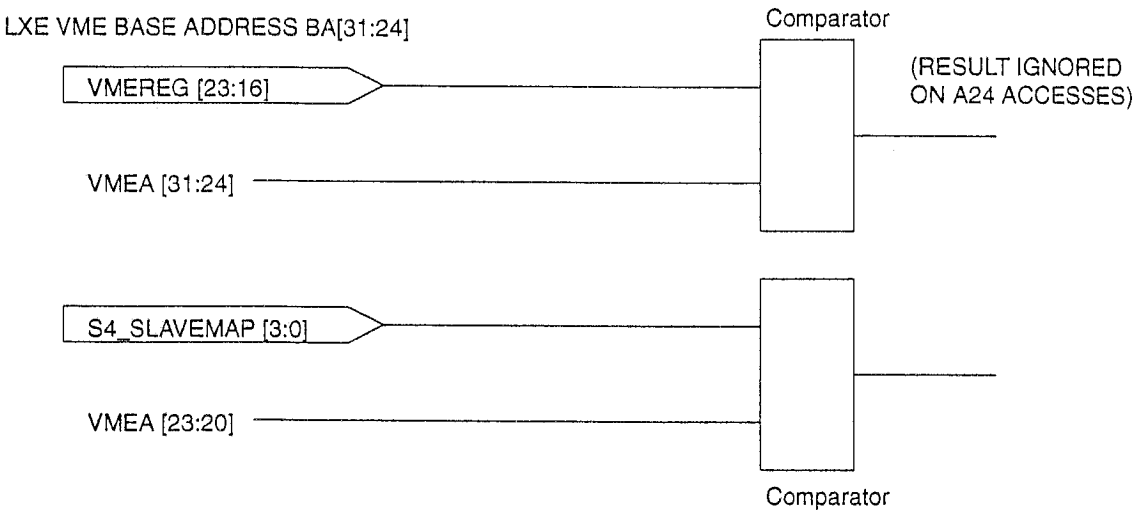
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F.3 *Slave VME and SBus DVMA Address Generation*

VMEREG = Programmable Register (addr 0x5FFE.8000)

S4 = VME Controller (addr 0x5FFE.00XX)

S4_SLAVEMAP = Register (addr 0x5FFE.001C)



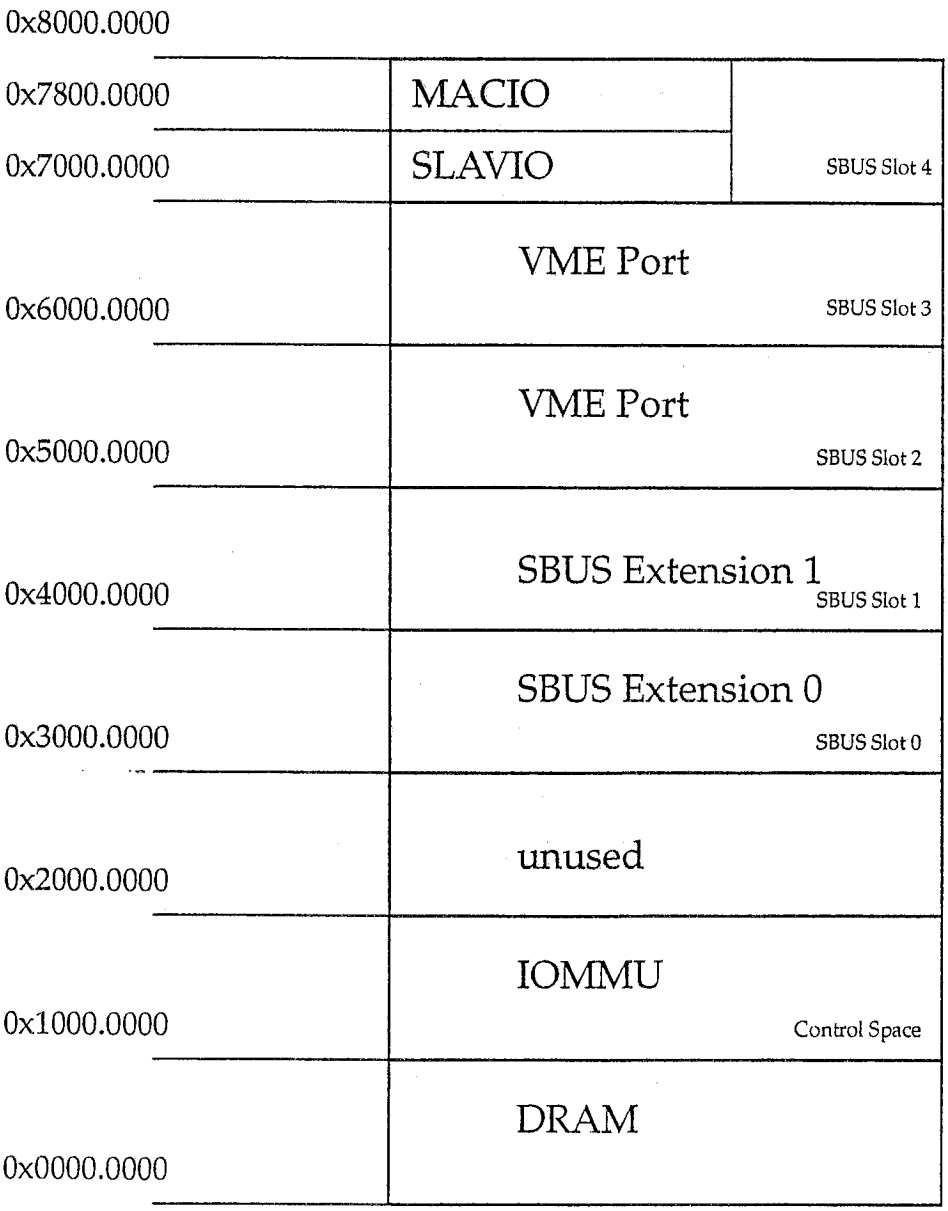
SBUS VIRTUAL ADDRESS SDVMA GENERATION

SDVMA [31:20] = 0xFF8 (constant value)
SDVMA [19:1] = VMEA [19:1]

SLAVE VME ACCESSES USE BUS REQUEST #3 TO ACQUIRE SBUS MASTERSHIP.

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F.4 *Tsunami Mapping*



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F.5 S4 VME Controller Register Map

Access Mode: BYTE R/W

Data Bus: 31..24

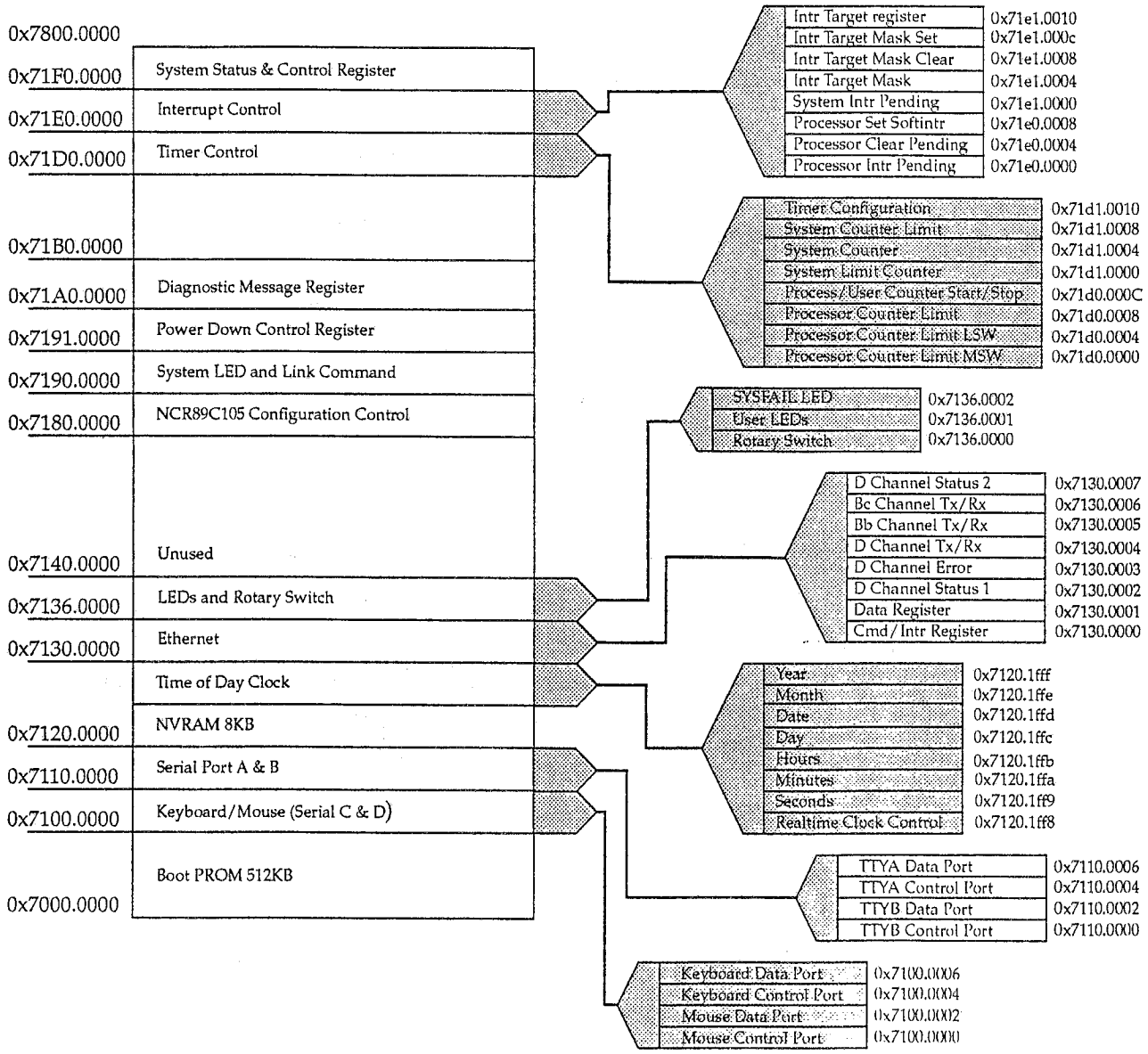
Base Address: 0x5ffe.0000

0x5ffe.001c	Slave Base Address
0x5ffe.0018	Master A32 Map
0x5ffe.0014	VME Interrupt Enable
0x5ffe.0010	Mailbox Register
0x5ffe.000f	VME IACK 6
0x5ffe.000d	VME IACK 5
0x5ffe.000b	VME IACK 5
0x5ffe.0009	VME IACK 4
0x5ffe.0008	Mailbox Interrupt Level
0x5ffe.0007	VME IACK 3
0x5ffe.0005	VME IACK 2
0x5ffe.0004	VME Interrupt Status
0x5ffe.0003	VME IACK 1
0x5ffe.0000	Bus Locker

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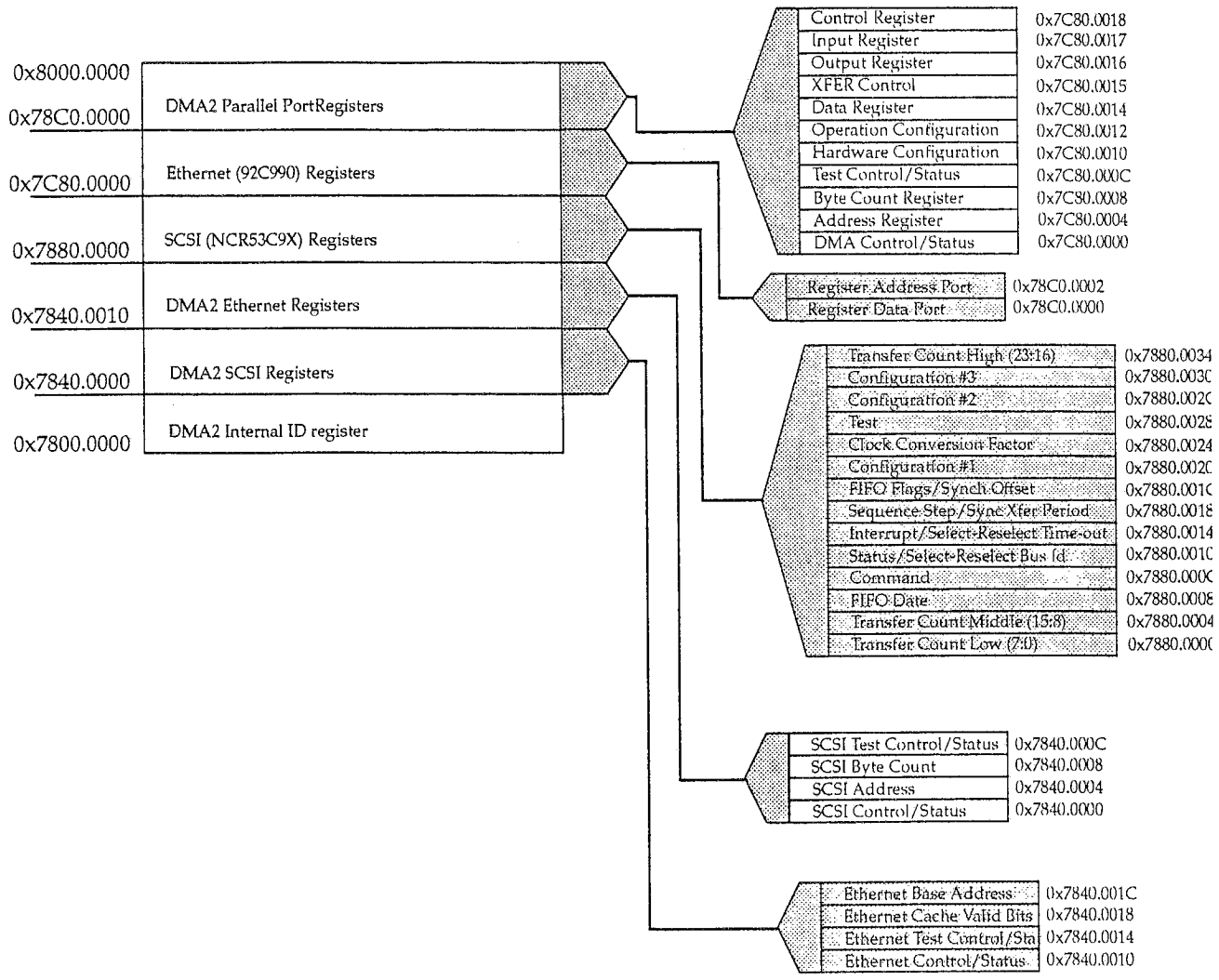
F.6 EBus Mapping

The SLVIO controlled EBus connects all non-DMA 8-bit peripheral devices



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F.7 MACIO Mapping



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F.8 LED And Rotary Switch Register

Access Mode: BYTE Read

Base Address: 0x7136.0000

Bit #	Description
3-0	Rotary Switch Value
4	Always 0
5	Abort Switch Status: 0 = Abort Asserted 1 = Abort Inactive
6	VME ACFAIL Status: 0 = ACFAIL Asserted 1 = ACFAIL Inactive
7	VME SYSFAIL Status: 0 = SYSFAIL Asserted 1 = SYSFAIL Inactive

F.9 User LED Register

Access Mode: BYTE Write

Base Address: 0x7136.0001

Bit #	Description
3-0	LED Control Bits (per LED): 0 = LED ON 1 = LED OFF
7-4	No Effect

F.10 SYSFAIL Control Register

Access Mode: BYTE Write

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Base Address: 0x7136.0002

Offset	Description
0	A WRITE access to this register asserts SYSFAIL on the VMEbus and turns on the SYSFAIL LED
1	A WRITE access to this register de-asserts SYSFAIL on the VMEbus and turns off the SYSFAIL LED

F.11 VME Control Register

Access Mode: 32bit WORD R/W

Base Address: 0x5ffe.8000

Bit #	Description
1-0	VME MAP Select: 0 0 = MAP 0 0 1 = MAP 1 1 0 = MAP 2 1 1 = MAP 3
15-2	Must be written as 0. Undefined on read
23-16	VME Slave Base Address (Bits 31-24)
24	Read-Modify-Write VME Cycle: 0 = Normal Transfers 1 = RMW Transfer
25	Unused
27-26	Master VME Address Modifiers (AM0 & AM2)
28	Unused
31-29	Master VME Access (bits 31-29)

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LXE Jumper Settings



G.1 Factory Default Settings

Jumper	Default	Description
1	2-3	VME system controller enabled
2	1-2	Keyboard connected to front panel P7
3	1-2	Mouse connected to front panel P7
4	1-2	On-board SCSI termination active
5	OPEN	Reserved - must be open
6	CLOSE	Enable front panel RESET switch

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G.2 *LXE Jumper Locations and Configuration*

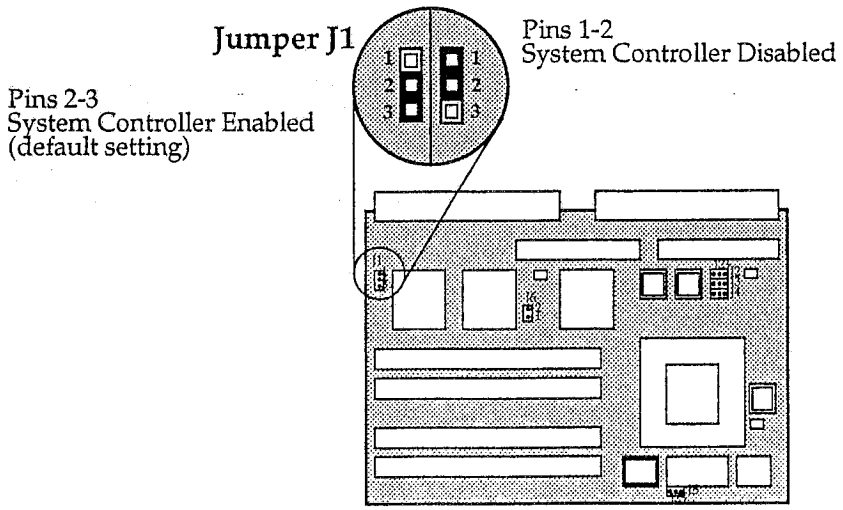
The LXE includes 6 user configurable jumpers that control various aspects of the SBCs behavior.

The S4 VMEbus interface chip can be configured to provide VME system controller functions. When enabled, the S4 supports a single level Round Robin arbiter and SYSRESET output.

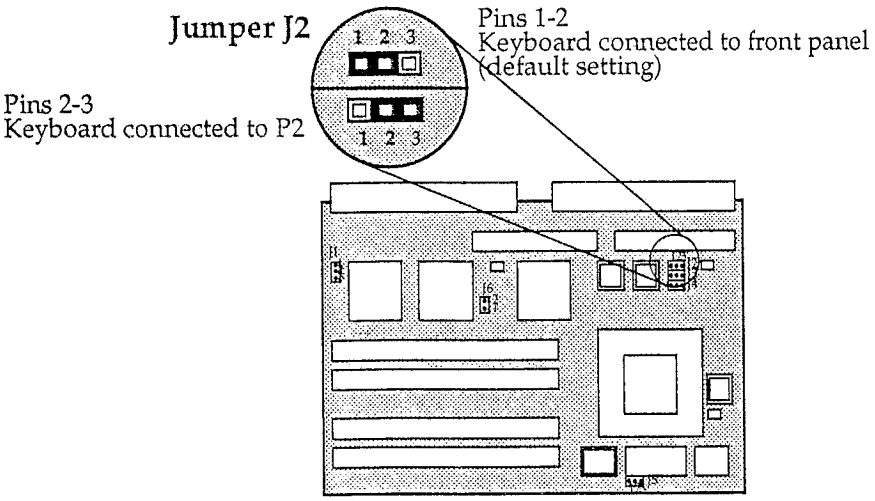
Serial ports C & D (keyboard and mouse) can be routed to the front panel or the paddle board via the P2 connector.

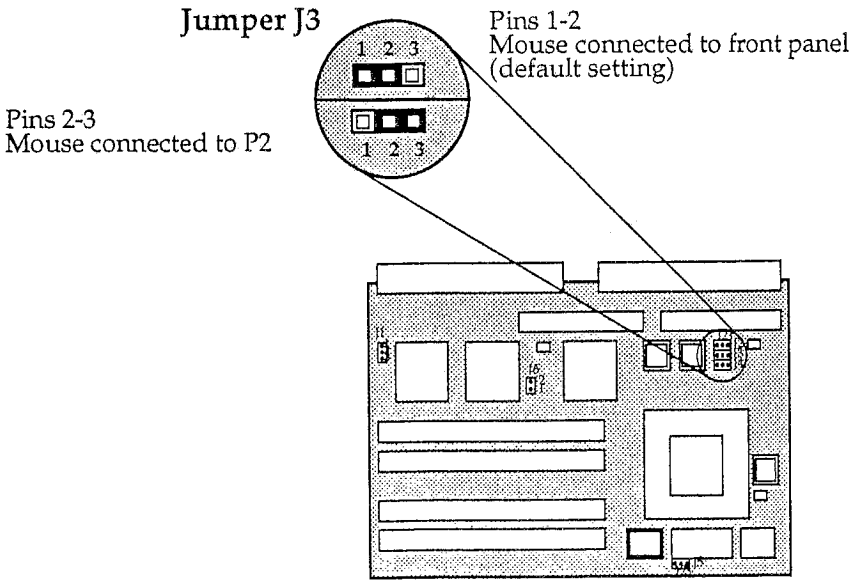
With SCSI-2 interfaces provided at both the front panel and P2, the LXE may be located within a SCSI chain. A jumper is provided to disable SCSI termination if the LXE is not a terminal node on the SCSI bus.

The front panel RESET switch may be disabled to prevent accidental or intentional hardware reset.

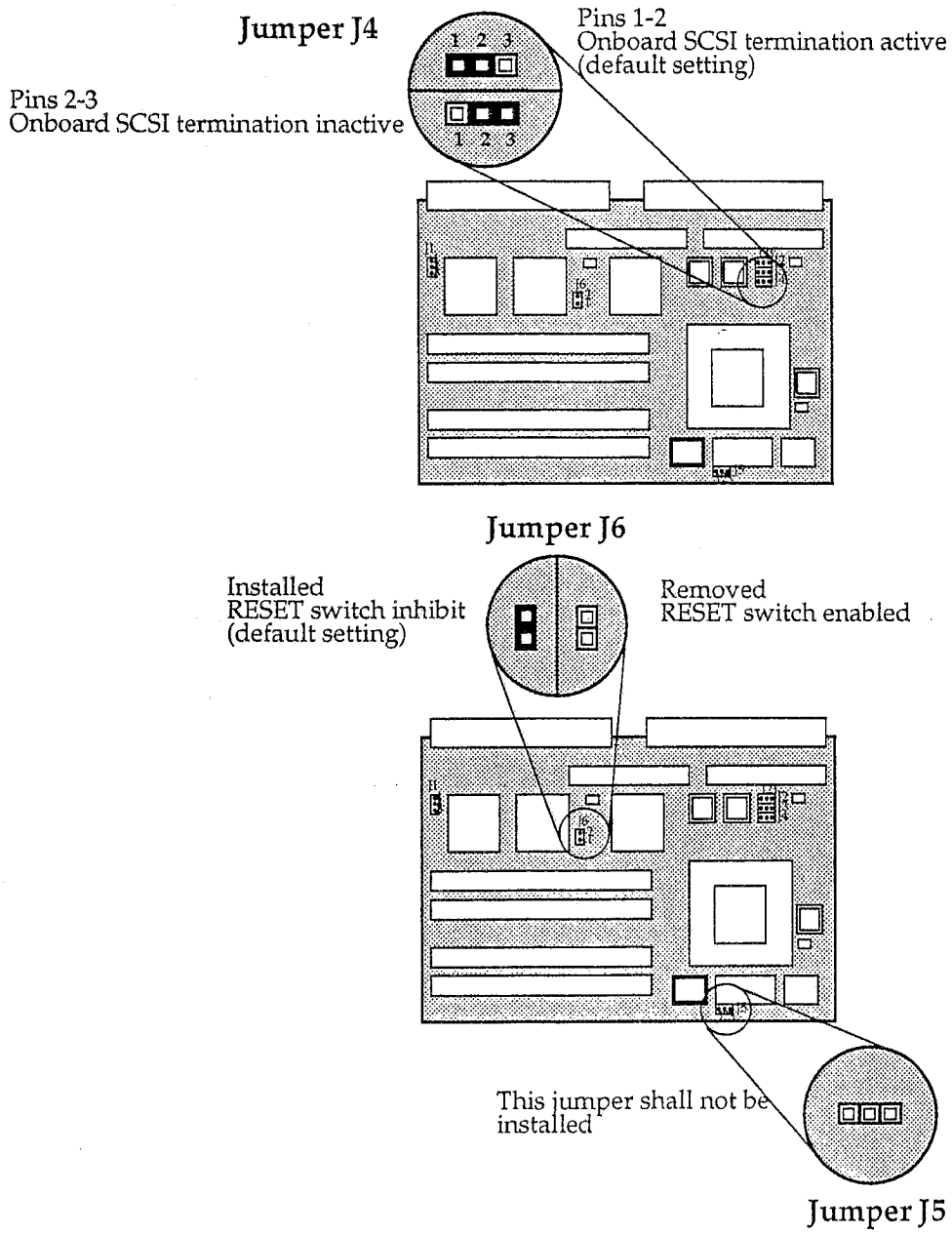


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Themis SPARC LXE Paddle Board

The paddle board for the Themis LXE is an adapter board that provides industry standard connectors for accessing the interface signals available on the user pins of the P2 VMEbus connector.

The board attaches to the rear of the P2 backplane and occupies three slots

Connectors for the following interfaces are provided on the paddle board:

Interface	Id	Connector Type
AUI Ethernet	J6	DB-15
Centronics Parallel	J4	IBM Compatible Female DB-25
SCSI-2	J1	50-pin IDC
Audio Speaker	J5	8-pin Header Row
Serial Port C	J2	14-pin IDC
Serial Port D	J3	14-pin IDC

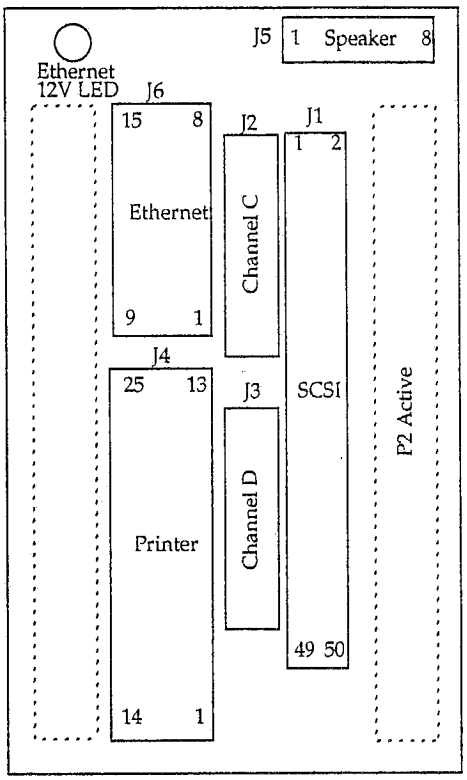
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J6 Ethernet Connector

Pin	Name	Dir	Description
1	GND	-	Ground
2	CP	In	Collision+
3	TP	Out	Transmit Data+
4	GND	-	Ground
5	RP	In	Receive Data+
6	GND	-	Ground
7			
8			
9	CN	In	Collision-
10	TN	Out	Transmit Data-
11	GND	-	Ground
12	RN	In	Receive Data-
13	+12V	Out	12V Ethernet Power
14		-	N/C
15		-	N/C

J5 Speaker Connector

Pin	Name	Dir
1	Speaker A	Out
2	Speaker B	Out
3	GND	-
4	GND	-
5	Microphone A	In
6	Microphone B	In
7	+5V (fused)	-
8	+5V (fused)	-



J2/3 Serial Ports C&D

Pin	Name	Dir	Pin	Name	Dir
1			8		
2	Receive Data	In	9		
3	Transmit Data	Out	10		
4			11		
5	Ground	-	12		
6			13	Ground	-
7			14	5V (fused)	-

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SCSI-2 Connector

Pin	Name	Dir	Pin	Name	Dir
1	Ground	-	2	SCDB0	In/Out
3	Ground	-	4	SCDB1	In/Out
5	Ground	-	6	SCDB2	In/Out
7	Ground	-	8	SCDB3	In/Out
9	Ground	-	10	SCDB4	In/Out
11	Ground	-	12	SCDB5	In/Out
13	Ground	-	14	SCDB6	In/Out
15	Ground	-	16	SCDB7	In/Out
17	Ground	-	18	SCDBP	In/Out
19	Ground	-	20		
21	Ground	-	22		
23	Ground	-	24		
25	Ground	-	26		
27	Ground	-	28		
29	Ground	-	30		
31	Ground	-	32	SCATN	Out
33	Ground	-	34		
35	Ground	-	36	SCBSY	In/Out
37	Ground	-	38	SCACK	Out
39	Ground	-	40	SCRST	In/Out
41	Ground	-	42	SCMSG	In
43	Ground	-	44	SCSEL	In/Out
45	Ground	-	46	SCCD	In
47	Ground	-	48	SCREQ	In
49	Ground	-	50	SCIO	In

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OpenBoot PROM Extension Commands



The Themis LXE implements a full VMEbus interface using the SUN S4 SBus to VMEbus controller. To control the VMEbus related systems settings, a number of environment variables have been added to the Sun OpenBoot PROM (OPB).

Variable	Default	Description
`vme-slave-address`	0	Set VME slave base address. Bits 31-24 are programmed into VMEREG bits 23-16 and bits 23-20 are programmed into S4 XXX register
`vme-master-address`	0	Set VME master access bits 31-29
`vme-mailbox-interrupt-level`	1	Interrupt level to use on mailbox interrupts
`vme-mailbox-address`	0	A16 mailbox register base address
`vme-slave-enable?`	`false`	Enable DVMA bit in slave map register
`vme-mailbox-interrupt-enable?`	`false`	Enable mailbox interrupts

These variables may be setup at the **ok** OBP prompt using:

```
setenv variable_name value
```

or when running Solaris with the command:

```
eeprom variable_name=value
```

A RESET is required for the new values to take effect.

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Solaris 2.x Installation On The LXE



To install a Sun Microsystems CD-ROM release of Solaris 2.x you will need:

- Solaris 2.x CD-ROM for the Sun4m-c architecture.

Note – This CD-ROM is not yet available. Substitute the SunSoft Solaris 2.x release for the SPARCclassic (The Themis LXE is fully SPARCclassic compatible). With the SPARCclassic CD-ROM you will require a patch tape containing the VMEbus interface drivers for the LXE

- A Themis LXE OBP EPROM version 2.10 or greater
- A SBus graphics card
- A Sun compatible keyboard and mouse

Note – The Solaris 2.x installation procedure cannot be performed from a terminal connected to the LXE serial port. Both a graphics board as well as a keyboard and mouse are required.

Installation Procedure

- Assure that the OBP PROM version you have installed on the LXE is version 2.10 or greater (you will be able to install using version 2.9, but won't be able to access the VMEbus).
- Follow the standard Sun CD-ROM installation instructions

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- If you are using the SunSoft Solaris CD-ROM for SPARC LX machines, you will have to install the VME patch tape after completing the CD-ROM installation:

```
# cd /
# tar xvf /dev/rmt/0
```

Note – If the tape drive was not attached or powered up when the disk was generated, you must use the `boot -r` option to configure the kernel to recognize the tape drive.

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