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THEMIS COMPUTER

TSVME110

Multi-function 68000 CPU board

USER'S MANUAL

TSVME110

Multi-function 68000 CPU board

85125-A0

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PRODUCT : TSVME110 - 85125 - A0

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I - PREPARATION FOR USE

1.1 - INCOMING GOODS INSPECTION

- Check that the packaging shows no signs of having been damaged in transit.

- Open the packaging and make sure that none of the items figuring on the Product Inventory Sheet are missing.

- The packaging should be kept for storing the board when not in use and for returning the board for servicing if necessary.

- As soon as the board has been unpacked, inspect the printed circuit, front panel, connectors, modules and components for signs of damage.

1.2 - POWER UP

- Both serial links come configured in asynchronous mode, as follows:

  - Channel 1 : terminal link
  - Channel 2 : "system" link (see § 3.8.2 for details on changing these settings)

- The user must configure the following to suit his particular application:

(1) - Type of chips fitted in JEDEC banks (see § 3.2)

SW5	- Bank 3	EPROMs
SW9	- Bank 2	SRAM/EEPROM/EPROM
SW10	- Bank 1	SRAM/EEPROM/EPROM
SW11	- Bank 0	SRAM/EEPROM/EPROM

SW6 - Battery backup

(2) - JEDEC socket dynamic RAM configuration - SW12 (see § 3.1, 3.2, 3.3)

(3) - VME arbiter/requester - F12 (see § 3.7)

(4) - Requester level, bus grant chaining - SW16, 17, 18 (see § 3.7)

(5) - VME SYSCLK, RESET*, SYSFAIL* - F16, SW15, F15 (see § 3.6.1/3; § 3.7)

- Pushbutton reset - SW3 (see § 3.6.1)

(6) - Local IT levels and watchdog operation - SW14 (see § 3.4, 3.6.4)

(7) - Watchdog reset source and watchdog trigger times - F20, SW1, SW2 (see § 3.6.4)

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(8) - Peripheral devices:

- Timer 3 and timer 2 input - SW8 (§ 3.8.1)

- Parallel ports (§ 3.8.3)

  - Non-buffered mode: board configured for straight-through 68230-P2 link F17, F18 and F19 wired

  - Buffered mode:
    F17, F18 and F19 not wired;
    SN75160 chips fitted at IC79 and IC80; MC3448A chip fitted at IC81

- SCSI / Floppy option:

  - Enable incoming reset from SCSI bus - F14 (§ 3.8.4)

  - P2/SO0055 configuration (§ 3.8.4.4)

    F24/SW1 on SO0055 (§ 3.12)

  - Floppy interface configuration:
    enable DISK CHANGE, set DRV polarity - SW13, F13 and F21 (§ 3.8.5)

- Insert the board into a non-powered chassis, making sure that the VMEbus signals IACKIN*/OUT* and BGxIN*/OUT* are correctly daisy-chained up to the slot occupied by the TSVME110 board.

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II - INTRODUCTION

2.1 - PRELIMINARIES

The TSVME110 is a multi-function 16-bit CPU board on the VMEbus. In its basic version, it provides the following application CPU functions on the VMEbus.

- Master access to VMEbus
- Two-way 16-bit parallel port
- Two serial ports (one configurable for synchronous or asynchronous operation)
- Watchdog
- Three programmable timers
- Four banks of two 32-pin JEDEC sockets each
- Five LEDs plus decimal display on front panel

- On option, the board may incorporate SCSI and floppy controllers.

- Further options increase the on-board memory with 512K, 1M or 2M bytes of dynamic RAM.

- The board includes connection facilities for adding a user module.

The TSVME110 is available in a number of different versions, as set out below:

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	TSVME110-1	TSVME110-2	TSVME110-3	TSVME110-4	TSVME110-5
CPU	68000-8MHz	68010-10MHz	68010-12.5MHz	68010-12.5MHz	68010-12.5MHz
Jedec bank 0	64 Kbytes 100ns SRAM	64 Kbytes 100ns SRAM	64 Kbytes 80ns SRAM	Empty	64 Kbytes 80ns SRAM
Jedec bank 1	Empty	Empty	Empty	Empty	64 Kbytes 80ns SRAM
Jedec bank 2	Empty	Empty	Empty	Empty	Empty
Jedec bank 3	Vbug EPROMS LP5282,5283	Vbug EPROMS LP5288,5289	Vbug EPROMS LP5340,5341	Vbug EPROMS LP5336,5337	Vbug EPROMS LP5338,5339
DYNAMIC RAM	NONE	1Mbytes	1Mbytes	512Kbytes	2Mbytes
Serial ports	RS232C	RS232C	RS232C	RS232C	RS232C
Parallel I/Os	Various 75160, MC3448A	Various 75160, MC3448A	Various 75160, MC3448A	Various 75160, MC3448A	Various 75160, MC3448A
SCSI controller	NO	YES	YES	NO	YES
Floppy controller	NO	YES	YES	NO	YES
Timekeeper	YES	YES	YES	YES	YES

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2.2 - DESCRIPTION OF TSVME110 BOARD

2.2.1 - Specifications

FUNCTION	SPECIFICATIONS
CPU	
MICROPROCESSOR	68000 at 8 MHz 68010 at 10 MHz or 12.5 MHz on option
MEMORY	
RAM, EEPROM, EPROM	Four banks of two 32-pin JEDEC sockets: - three banks with solder-bead configuration for different memory chips
EPROM	- one bank reserved for EPROMs All memory banks mounted on 16-bit data bus Memory chips have programmable access times, as follows:

CPU		68000 8MHz	68010 10MHz	68010 12.5MHz
Ram, Eeprom	0wst	150ns	100ns	80ns
	1wst	300ns	200ns	150ns
Eprom	0wst	250ns	200ns	150ns
	1wst	400ns	300ns	250ns

DYNAMIC RAM OPTION	512K, 1M or 2M bytes with parity check maximum of 1 wait state excluding refresh
INTERRUPT HANDLING	
	7 VME levels and 7 local levels Software-controlled interrupt masking Local IT levels set by jumper or wrapping All local ITs autovectored

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FUNCTION	SPECIFICATIONS
WATCHDOG	
	- Timer reset either by external signal on P2 or by internal software access - Watchdog output accessible externally on P2 and internally for generation of local IT or board reset - 2 trigger modes: 1) trigger if counter not reset within TIMEmax 2) trigger if counter not reset within TIMEmax or if reset attempted before TIMEmax/2 - TIMEmax set by wrapping: 0,25, 0,5, 1, or 2 seconds
BUS TIME OUT	
	Bus time out with software disable capability

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FUNCTION	SPECIFICATIONS
ON-BOARD PERIPHERAL DEVICES	
Serial ports	One RS232C asynchronous port One RS232C or TTL synchronous/asynchronous port (Z8530 controller) Serial ports accessible from 9-pin front-panel connectors and on P2 connector
Timer	68B40 triple timer: three programmable timers operating individually or in cascade; one timer accessible from P2 connector
Parallel ports	- two 8-bit ports and four control signals from 68230 PIT - direct output onto P2 or two-way interface with 75160 and MC3448A drivers
Option : SCSI controller	SCSI bus on P2, to ANSI SCSI X3T9.2 specs. WD33C93 controller On-board terminating resistors
Option : Floppy controller	Floppy disk interface on P2 WD37C65 controller - up to four floppies or microfloppy-disks (TM) - data transfer rates of 125, 250, 500K bit/s
User module	Provision for mounting customized user module on TSVME110 board - 2x35-pin J5 connector carrying local CPU bus (address, data, control), clock signals, one CSMOD* line and one interrupt line - 12-pin J3 connector connecting to eight pins on the P2 connector and carrying +12V and -12V power supplies

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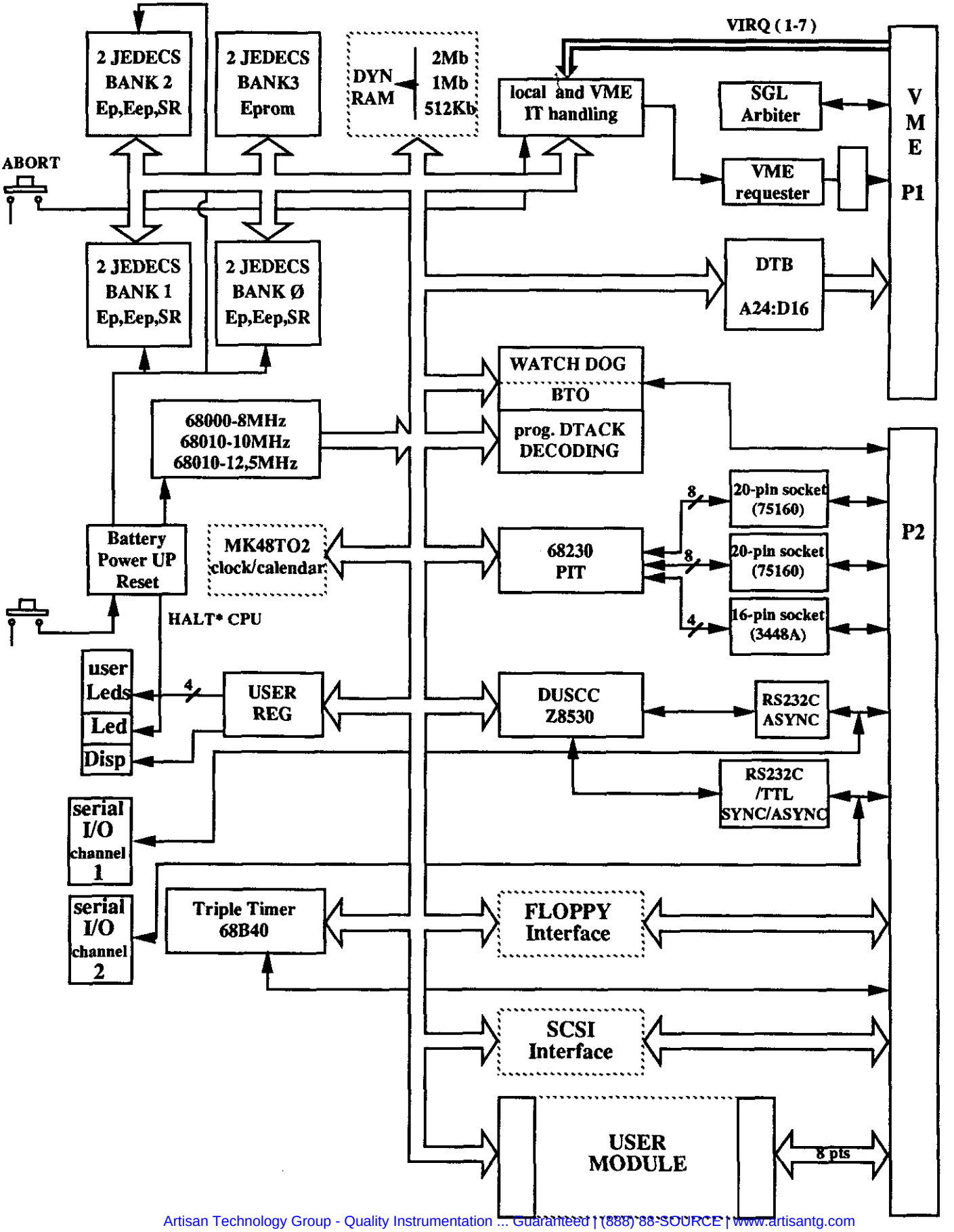
FUNCTION	SPECIFICATIONS
VME INTERFACE	
Compatibility	ANSI/IEEE STD1014 - 1987
Type of board	Master
VME arbiter	Single level Set from selector
VME requester	Release on Request (ROR) Level set by wrapping
Data transfer	A24:D08 (EO) Read/Write RMW A24:D16 Read/Write
Bus time out	Bus Time Out with software disable capability
Interrupt handler	7 VME levels
System clock	Outgoing SYSCLK (switchable)e
System reset	Outgoing or incoming SYSRESET* (switchable)
System failure	Outgoing SYSFAIL* (software-generated) Incoming SYSFAIL* (switchable by solder bead)
Mains failure	Incoming ACFAIL*
VME connectors used	P1 All three rows on the P2 connector are used for on-board peripheral interfaces. A TSVME110 board with SCSI and floppy controller options cannot be mounted in a VME slot with a 32-bit VME extension backplane on P2.

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FUNCTION	SPECIFICATIONS
FRONT PANEL	
LEDS Display Pushbuttons 9-pin SUB-D connectors	HALT and FAIL LEDs, plus three user LEDs 7-segment display with decimal point Reset, Abort Two serial port connectors
ELECTRICAL ENVIRONMENT	
Power supplies Power consumptions	+5Vdc -2,5% +5% +12Vdc -3% +5% -12Vdc -3% +5% 5V : 3.5A max. with DRAM, FLOPPY, SCSI +12V : 50mA max. -12V : 50mA max.
CLIMATIC ENVIRONMENT	
TEMPERATURE : - operating - storage Relative humidity	 0 à 60° C - 40 à +85° C 0 to 95% non condensing
MECHANICAL SPECIFICATIONS	
FORMAT Occupation	Double EUROCARD 160 x 233.3 mm (6,29 x 9,18 inches) One VME slot

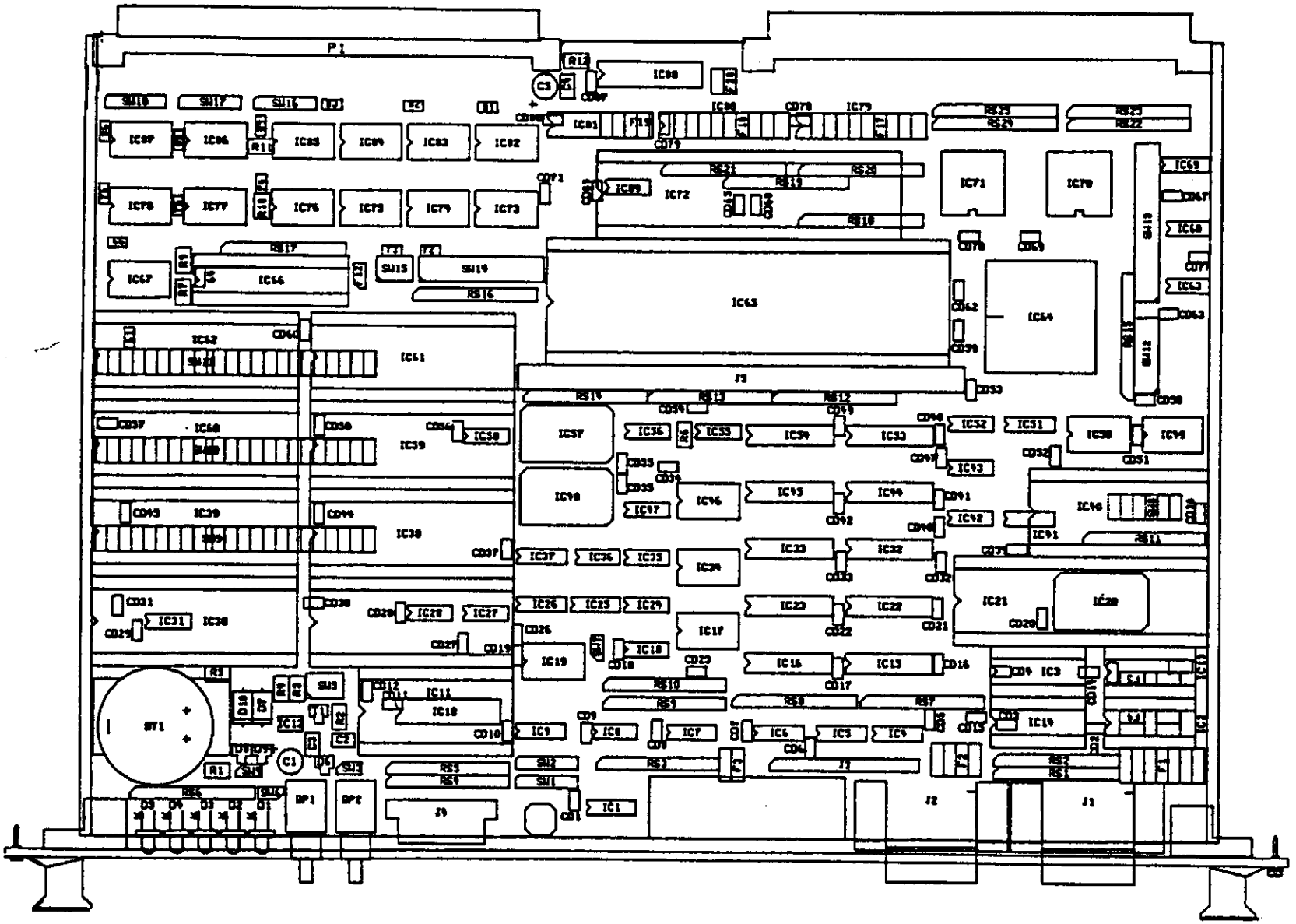
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2.2.2 - Block diagram



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2.2.3 - Component layout



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2.2.4 - Connectors and selectors

CONNECTORS

Name	Purpose	Notes	Section
J1	Serial port channel 2 RS232C/TTL synchronous/asynchronous	9-pin female SUB-D	3.8.2
J2	Serial port channel 1 RS232C asynchronous	9-pin female SUB-D	3.8.2
J3	User module connector	1x 12-pin, I/O onto P2	3.9.2
J5	User module connector	2x 25-pin, CPU bus + control	3.9.2
P1	VMEbus connector		3.7
P2	Peripheral I/O connector	Serial ports, channels 1 & 2 Parallel I/Os Timer Watchdog SCSI bus Floppy interface User module General	3.8.2 3.8.3 3.8.1 3.6.4 3.8.4 3.8.5 3.9 3.10

SELECTORS

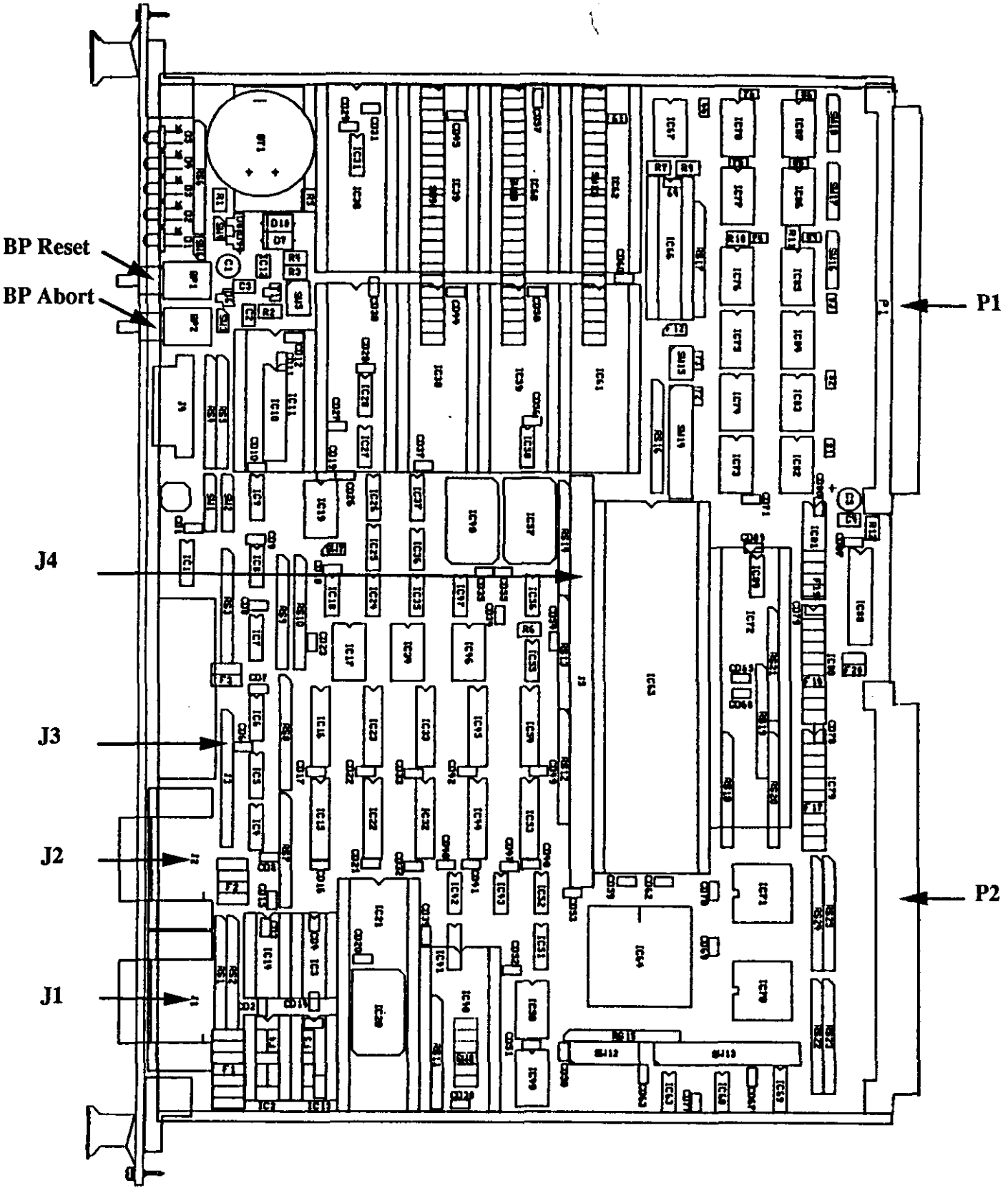
Name	Purpose	Notes	Section
SW1,2	Set watchdog trigger times		3.6.4
SW3	Enable pushbutton RESET*	jumper	3.6
SW4	Set battery or lithium cell	enable battery charge	3.2.4
SW5	Configure JEDEC bank 3	EPROMs	3.2.2.2
SW6	Enable battery backup		3.2.4
SW7	Set self-test mode		3.5.2
SW8	Configure Timer 3		3.8.1
SW9	Configure JEDEC bank 2	static RAM / EEPROM / EPROM	
SW10	Configure JEDEC bank 1	static RAM / EEPROM / EPROM	
SW11	Configure JEDEC bank 0	static RAM / EEPROM / EPROM	3.2.2.1
SW12	Configure memory		3.1 3.2 and 3.3
SW13	Configure floppy interface		3.8.5
SW14	Set local IT levels and watchdog operation	2x9-pin - jumper or wrapping	3.4 3.6.4

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Name	Purpose	Notes	Section
SW15	Enable incoming/outgoing VME reset		3.6.1
SW16 SW17 SW18	\ > Set VME request/arbiter level /		3.7.2
F1	Configure serial port channel 2	modem/terminal	3.8.2
F2	Configure serial port channel 1	modem/terminal	3.8.2
F4,F5	Set channel 2 for RS232C or TTL		3.8.2
F7	Set channel 2 DUART clock		3.8.2
F12	Set VME arbiter or requester		3.7.2
F13	Enable "DISK Change"		3.8.5
F14	Enable incoming reset from SCSI bus		3.8.4
F15	Enable incoming SYSFAIL*		3.6.3
F16	Enable SYSCLK on VME		3.7.4
F17 F18 F19	\ Set parallel I/Os > for direct or buffered / configuration		3.8.3
F20	Set watchdog reset mode		3.6.4
F21	Set DRV (0/1)		3.8.5.3
F22 F23	\ Configure S2TXC signal /		3.8.2.1
F24	SCSI : REQ connection on P2		3.8.4.4
F25	Grounding the housing of serial I/O connectors		3.8.2
F3	Set dynamic RAM type (256K/1Mx4)	factory set	
F6	Test/normal - channel 1 DUART clock	factory set	
F8, F9	68010 option	factory set	
F10,F11	Test/normal - clocks	factory set	

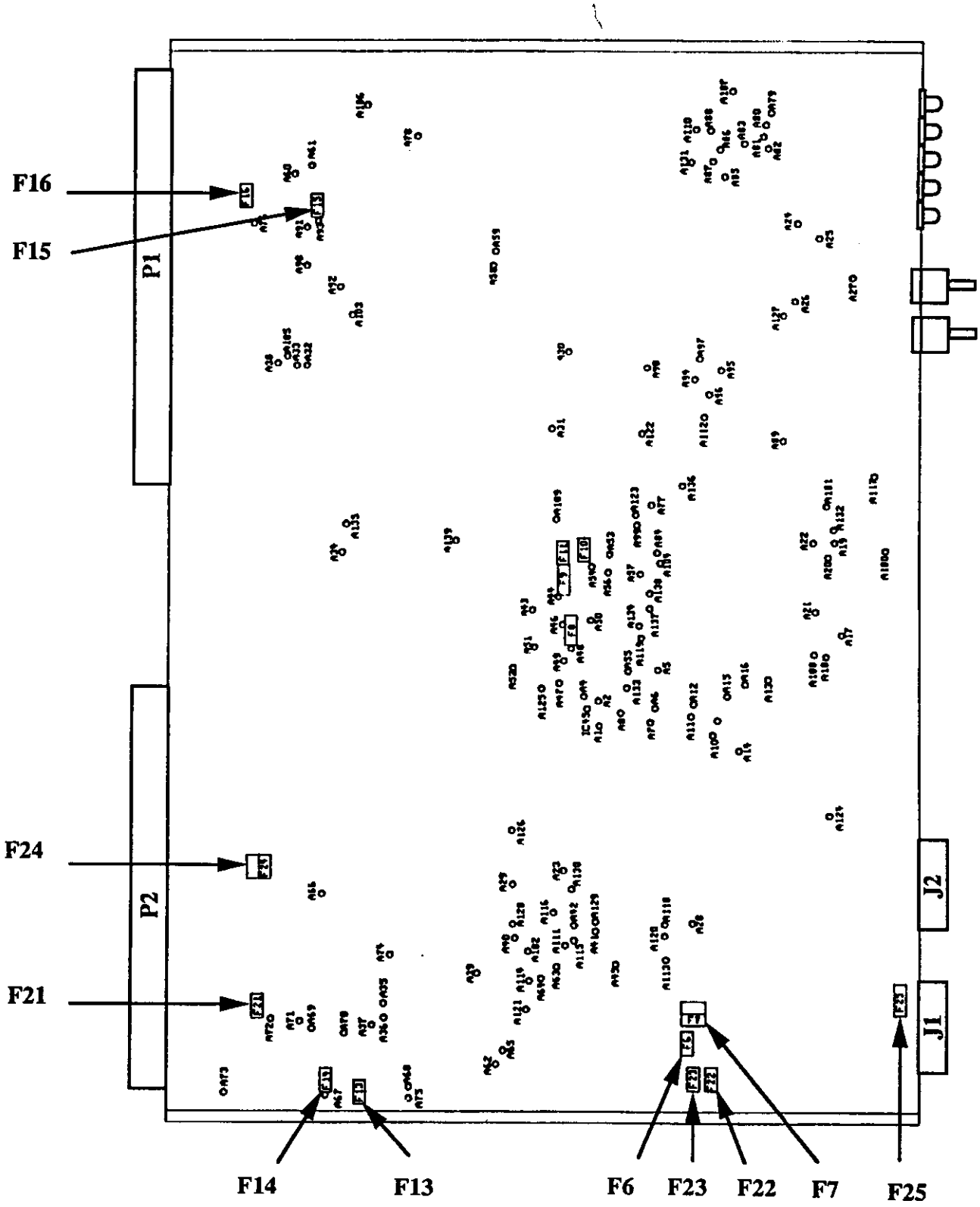
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Fig. 2.1 : Location of connectors



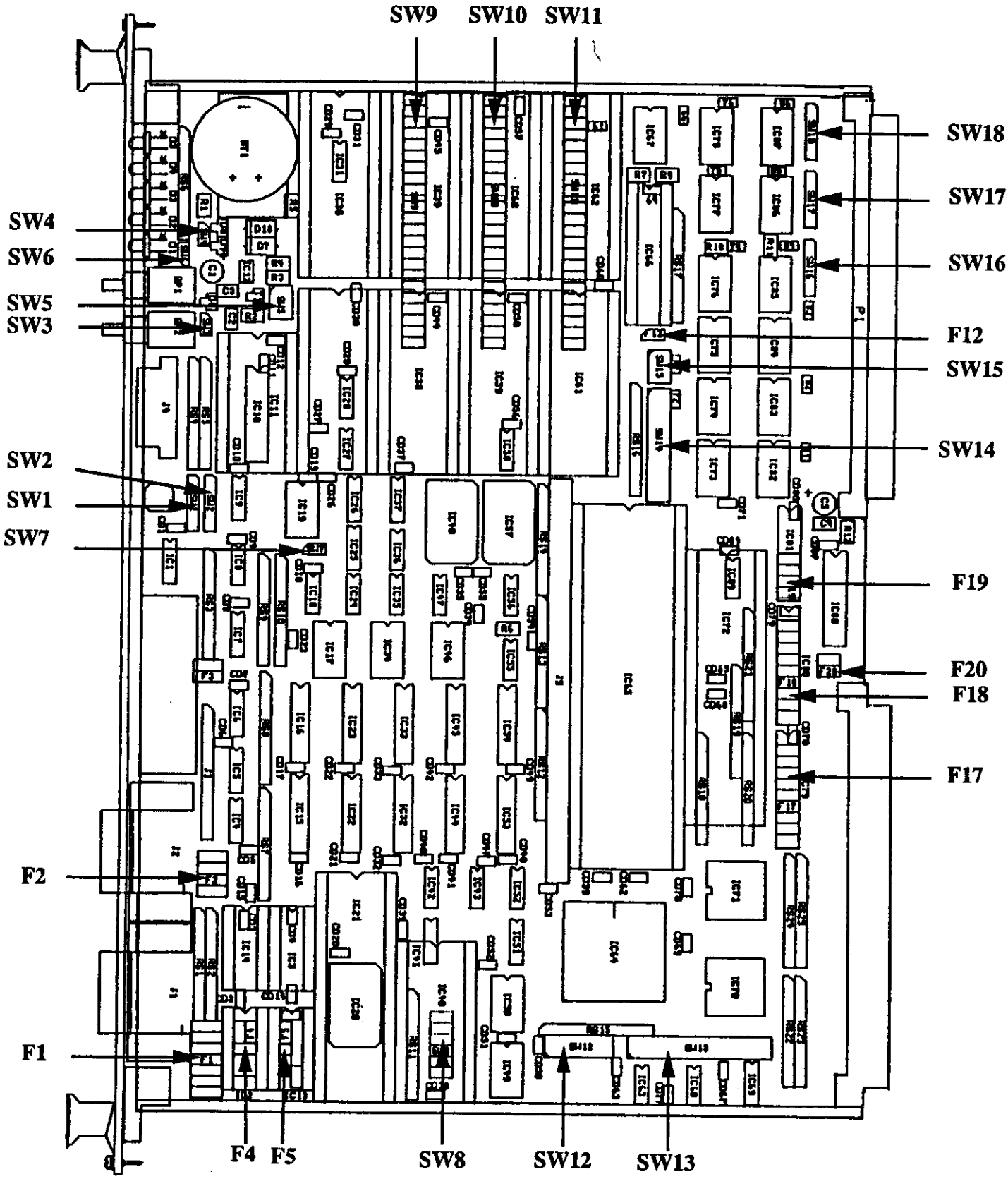
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Fig. 2.2 : Location of solder beads - soldered side



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Fig. 2.3 : Location of selectors and solder beads - component side



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III - TECHNICAL DESCRIPTION

3.1 - MAPPING

The TSVME110 board CPU mapping is configured to match the memory options chosen by the user, i.e.:

- 0, 512K, 1M or 2M bytes of dynamic RAM
- RAM, EEPROM or EPROM chips installed in JEDEC banks 0-2

For the present purposes, EEPROM memory is assimilated to RAM memory.

- The following notes refer to the mapping table overleaf:

  - $FFFFFF to $F00000:

    VME short addressing - peripheral devices and internal registers. Optional peripheral devices (floppy and SCSI) are always decoded, i.e. there will be no "bus time out" for access to these address areas if the components in question are not fitted.

  - $EFFFFF to $E00000:

    JEDEC banks. The result of an access to this area will depend on the configuration set on SW12.

  - $DFFFFF to $C00000:

    User module. The user module must supply the CPU DTACK* and BERR* signals when this area is accessed.

  - $BFFFFF to $010000:

    Standard VME access or dynamic RAM access, depending on the configuration

  - $FFFF to 0:

    Dynamic RAM access or JEDEC bank 0 access, depending on the configuration.

- The decoding logic determines the user configuration from the SW12 selector.

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Fig. 3.1 : Mapping

ADDRESS	FUNCTION
$FFFFFF $FF0000	VME short addressing 64 Kb
$FE0000	Parity register
$FD0000	SCSI
$FC0000	Floppy
$FB0000	User registers
$FA0000	TIMER
$F90000	PIT
$F80000	DUART
$F70000	JEDEC DTACK setting : bank 3 access time
$F60000	JEDEC DTACK setting : bank 2 access time
$F50000	JEDEC DTACK setting : bank 1 access time
$F40000	JEDEC DTACK setting : bank 0 access time
$F30000	VME IT mask
$F20000	Local IT mask
$F10000	Bus time out register
$F00000	Clock / calendar
$EFFFFF $E00000	Four banks of two JEDEC sockets each
$DFFFFF $C00000	User module
$BFFFFF $200000 $100000 $080000 $010000	S T A N D A R D V M E 512Kb DRAM 1Mb DRAM 2Mb DRAM
000000	JEDEC bank 0

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- Lines CF1 and CF0 determine the dynamic RAM configuration, as follows:

	CF (1-0)	DYNAMIC RAM	STANDARD VME
CF0 o---o CF1 o---o	0	None	$010000 to $BFFFFF
CF0 o o CF1 o---o	1	512Kb 0 to $07FFFF	$080000 to $BFFFFF
CF0 o---o CF1 o o	2	1Mb 0 to $0FFFFF	$100000 to $BFFFFF
CF0 o o CF1 o o	3	2 Mb 0 to $1FFFFF	$200000 to $BFFFFF

- Lines CF2 to CF4 determine the type of chips fitted in the JEDEC sockets, as discussed below.

3.2 - BANKS OF 32-PIN JEDEC SOCKETS

The TSVME110 board has four banks of two 32-pin JEDEC sockets each. These are mapped from addresses $E00000 to $EFFFFF. The address of each bank within this area will depend on the type of memory chip fitted, i.e.:

- EPROMs: 27256 to 27010 \
- EEPROMs: 8K x 8, 32K x 8, 128K x 8 > Access time see 3.5.1.3
- static RAMs: 8K x 8, 32K x 8, 128K x 8 /

Decoding is such that EPROM banks (0 to 3) containing 64-kbyte or 128-kbyte EPROMs (27512 and 27010) will be mapped to consecutive addresses. The same applies to static RAM or EEPROM chips of 32-kbyte or 128-kbyte capacity.

JEDEC bank 3 is exclusively reserved for EPROMs.

Write accesses to EPROMs will be inoperative, terminating in a "bus time out" provided the bus time out feature is enabled (bus time out applies to CPU accesses globally).

Three operations are required to configure the JEDEC banks:

1. Configure selector SW12:
This informs the decoding system as to the type of chip installed on each JEDEC bank (see 3.2.1).

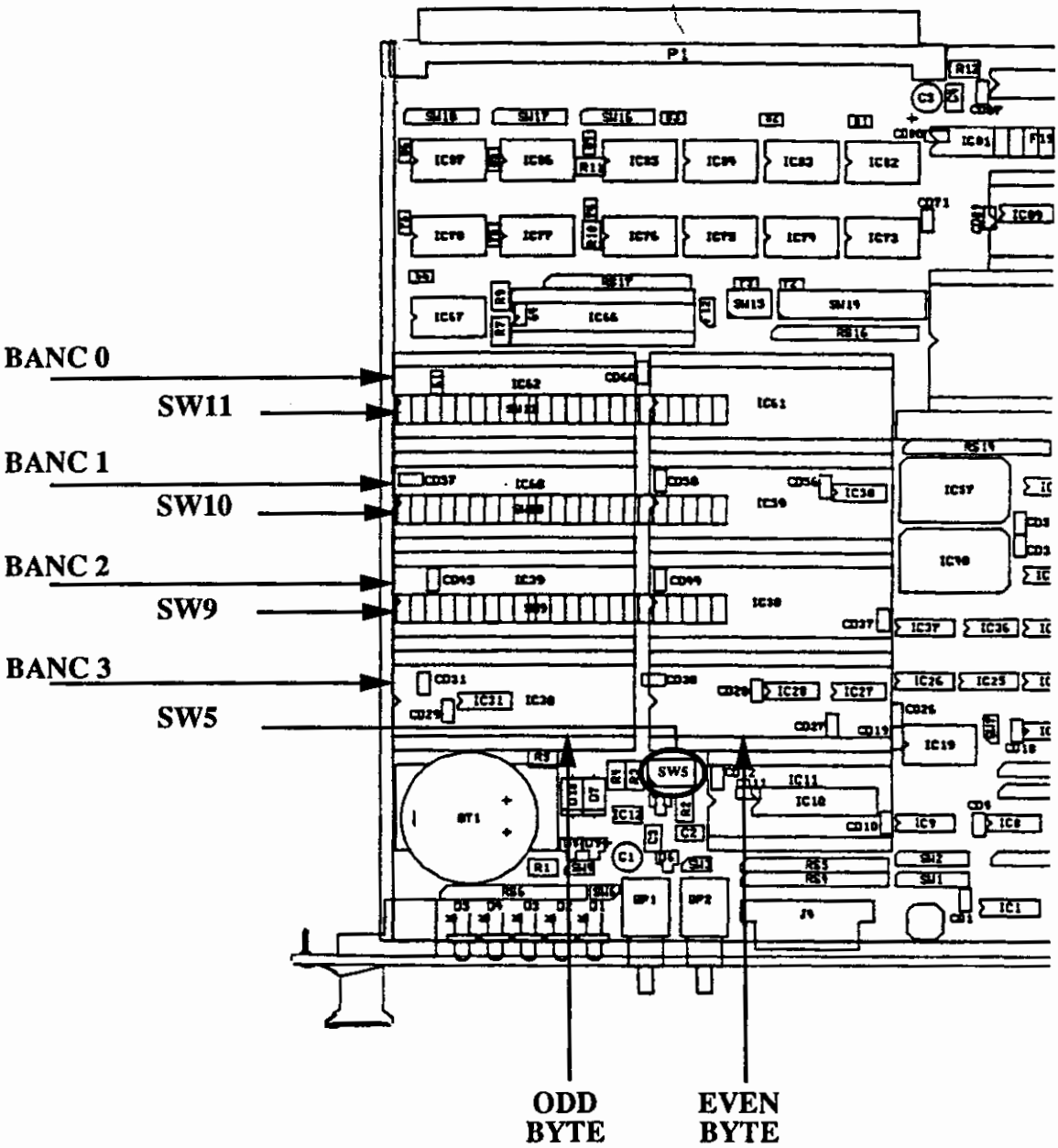
2. Configure selectors SW11, 10, 9 and 5:
This configures the individual JEDEC banks to match the type of chip fitted (see 3.2.2).

3. Define the access times to each bank:
This is performed by software. Possible access times are 0 and 1 wait state ; the 1 wait state value is taken as default after a reset (see 3.5.1.3).

A final note concerns battery backup of the chips installed in the JEDEC sockets. Selector S6 takes the battery voltage Vbb onto selectors SW11, 10 and 9, where battery backup can be enabled/disabled for each bank. The SW4 selector sets whether a lithium cell or a battery is used (see 3.2.4).

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Fig. 3.2 : Location of JEDEC banks and associated selectors



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3.2.1 - Mapping of the four banks of JEDEC sockets - configuration of SW12 selector

The SW12 selector consists of five links: CF0 to CF4.
CF0 and CF1 set the dynamic RAM configuration.
CF2, CF3 and CF4 configure the individual JEDEC sockets.

(see § 3.1 for location of SW12)

CF4	CF3	CF2	CF1	CF0	CF(H) CODE	BANK 0 TYPE/ BANK SIZE	BANK 1 TYPE/ BANK SIZE	BANK 2 TYPE/ BANK SIZE	BANK 3 TYPE/ BANK SIZE
0	0	0	X	X	0 to 3	EPROM 128Kb	EPROM 128 Kb	EPROM 128 Kb	EPROM 128/256 Kb
0	0	1	X	X	4 to 7	EPROM 256Kb	EPROM 256 Kb	EPROM 256 Kb	EPROM 128/256 Kb
0	1	0	X	X	8 to B	static RAM EEPROM 64/256Kb	EPROM 128 Kb	EPROM 128 Kb	EPROM 128/256 Kb
0	1	1	X	X	C to F	static RAM EEPROM 64/256Kb	EPROM 256 Kb	EPROM 256 Kb	EPROM 128/256 Kb
1	0	0	X	X	10to13	static RAM EEPROM 64 Kb	static RAM EEPROM 64 Kb	EPROM 128/256 Kb	EPROM 128/256 Kb
1	0	1	X	X	14to17	static RAM EEPROM 256 Kb	static RAM EEPROM 256 Kb	EPROM 128/256 Kb	EPROM 128/256 Kb
1	1	0	X	X	18to1B	static RAM EEPROM 64 Kb	static RAM EEPROM 64 Kb	static RAM EEPROM 64 Kb	EPROM 128/256 Kb
1	1	1	X	X	1Cto1D	static RAM EEPROM 256 Kb	static RAM EEPROM 256 Kb	static RAM EEPROM 256 Kb	EPROM 128/256 Kb

- The bank sizes shown above are maximum bank sizes; with this bank size, three or four banks holding the same type of chip will be addressed contiguously. The sizes shown represent the total capacity of the two chips, i.e.:

64 Kb = two 32-kbyte static RAM chips
256 Kb = two 128-kbyte chips

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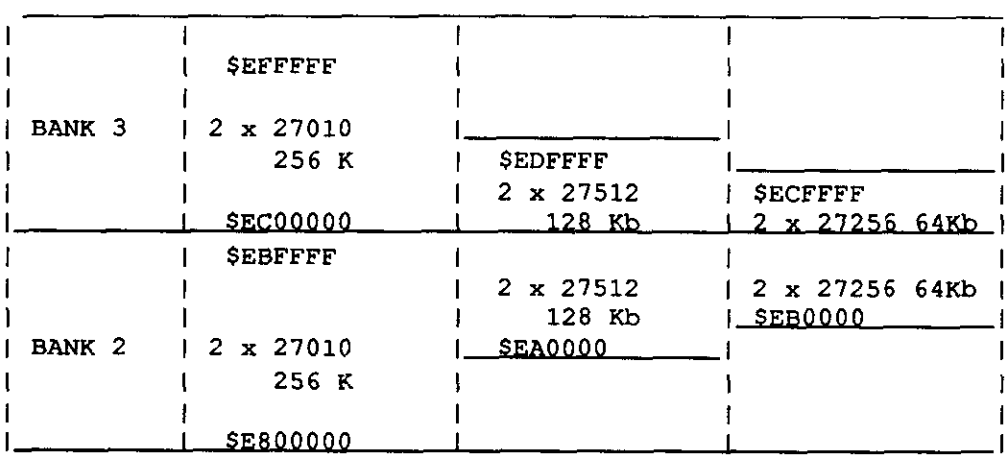
- If the chips fitted on the board give a lower capacity than that set for the JEDEC bank in question, the chips will be multiple-mapped over the area in question. By way of example, if two 8Kx8 RAM chips are fitted in bank 1 (minimum bank size 64 kbytes), these will be mapped four times within the bank 1 area, at the addresses below:

- $E10000 to $E13FFF
- $E14000 to $E17FFF
- $E18000 to $E1BFFF

and - $E1C000 to $E1FFFF

- If the same type of chip is fitted in two consecutive banks only, continuous addressing will still be possible even though the maximum bank capacity is not reached, as the chips can be mapped at contiguous locations across the boundary between the two bank areas in question.

Example : Configuration codes from 10 to 17



In the above example, contiguity between banks 2 and 3 is simply a question of starting the bank 2 mapping at the appropriate location within the available bank 2 area.

The table overleaf gives JEDEC bank, dynamic RAM and VMEbus mappings for configuration codes 0 to $1F on CF0-CF4.

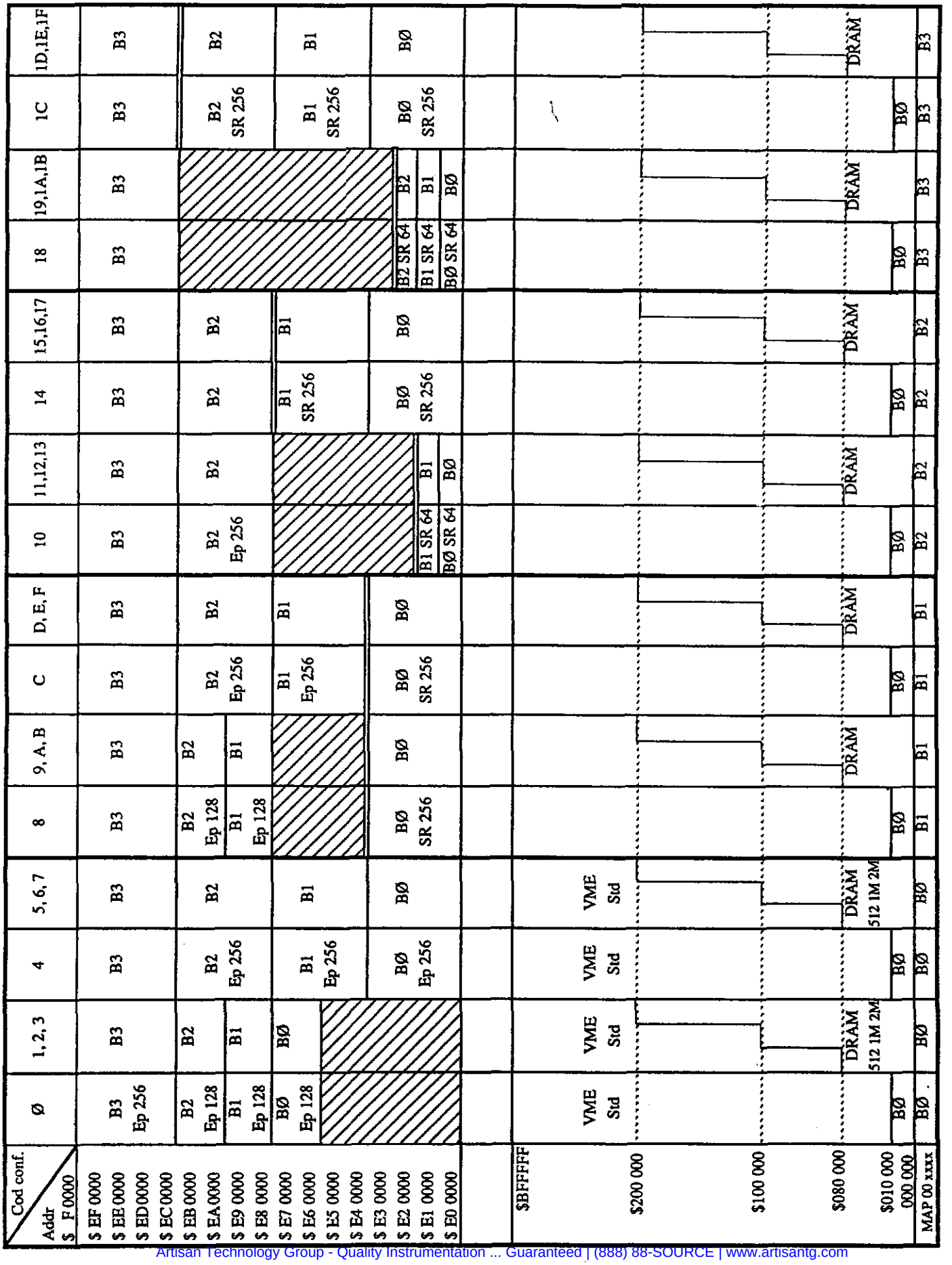
The line "MAP 00XXXX" indicates the JEDEC bank to which CPU accesses will be routed after a reset. This will be the first bank configured for EPROMs. CPU accesses to page 0 (00XXXX) will be routed to this JEDEC bank until an access to the JEDEC area ($EXXXXX) has been made.

In the absence of dynamic RAM, JEDEC bank 0 will always be seen at page 0.

```
SR64        static RAM (or EEPROM)        64 Kbytes (maximum bank size)
SR128       static RAM (or EEPROM)        128 Kbytes
Ep128       EPROM                         128 Kbytes
Ep256       EPROM                         256 Kbytes
```

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Fig. 3.3 : Mapping of the four JEDEC banks



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3.2.2 - Configuration of individual JEDEC banks

Both of the JEDEC sockets in each bank must be fitted with the same type of chip. These should have the same access times or else the whole bank will be bound by the longest access time of the two.

3.2.2.1 - JEDEC banks 0, 1 and 2

The following chips can be fitted in JEDEC banks 0, 1 and 2:

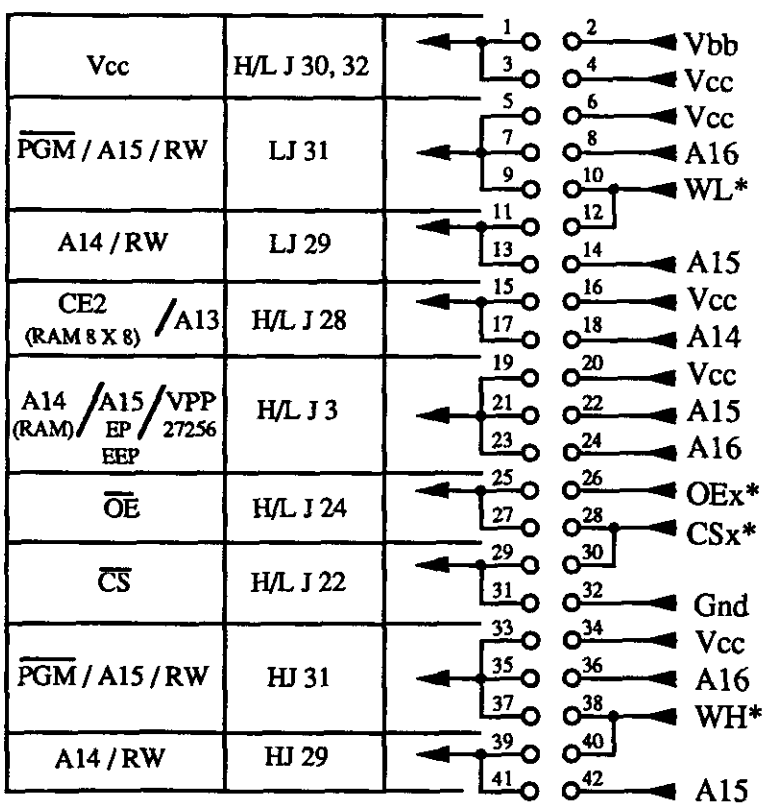
- EPROMs :
  27256; 27512; 27010.

- EEPROMs :
  8K x 8; 32K x 8; 128K x 8; 28C256; 28C010 (with "DATA polling" system)

- Static RAMs :
  8K x 8, 32K x 8, 128K x 8.

  Battery back-up for RAM contents may be wired from the Vbb battery voltage line. Specifications for batteries and lithium cells for this purpose are given in 3.2.4.

For each of banks 0, 1 and 2, the type of chip fitted is configured from one of the 2x21-pin solder-bead selectors as shown below:



J30, 32 : JEDEC socket pin 30

H : JEDEC socket high-end, i . e. even address D8 - D15

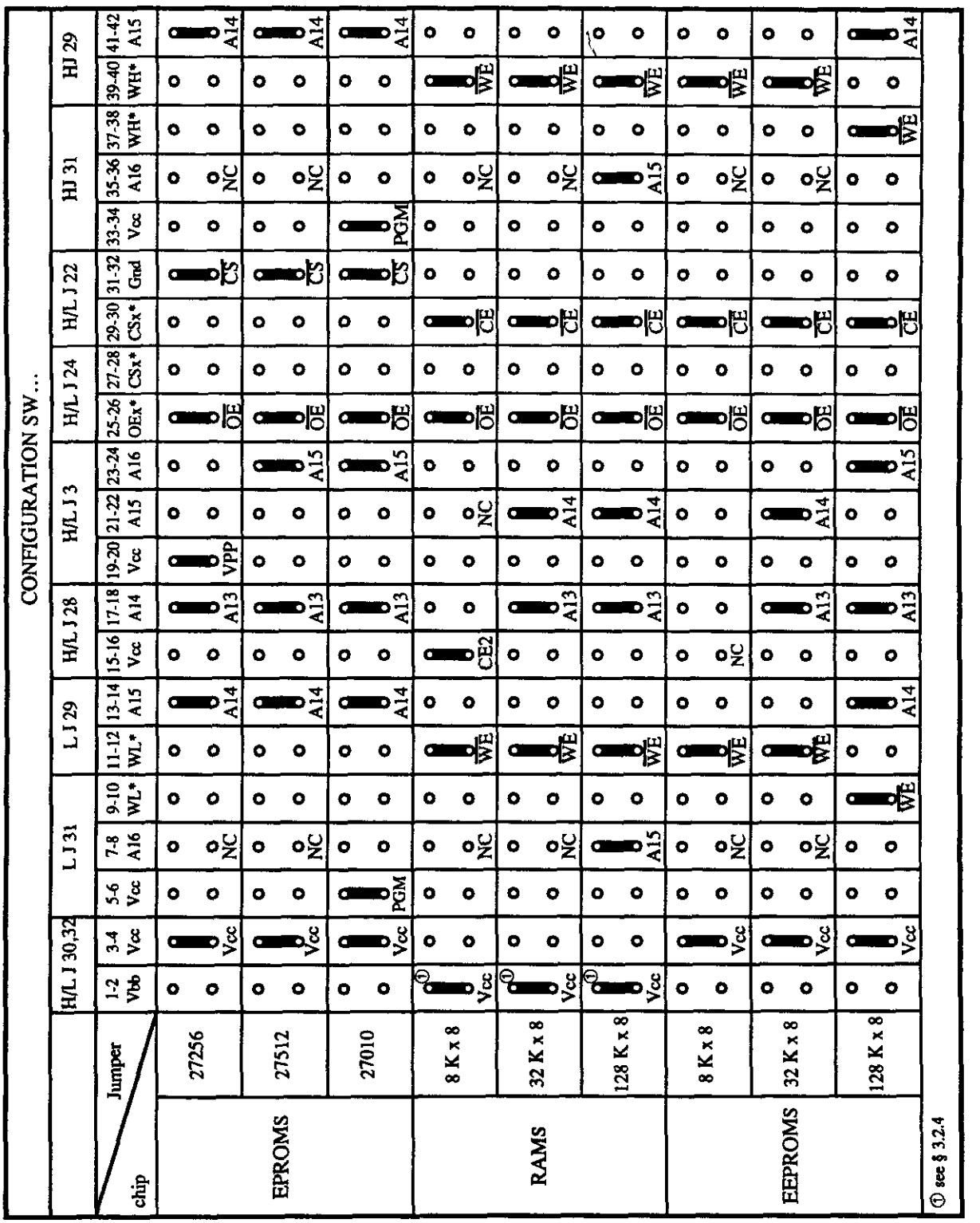
L : JEDEC socket low-end, i . e. odd address DØ - D7

H/LJx signal common to both chips in JEDEC bank

The table below shows SW11, 10 and 9 settings for different types of chip.

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Fig. 3.4 : SW11, 10 and 9 settings



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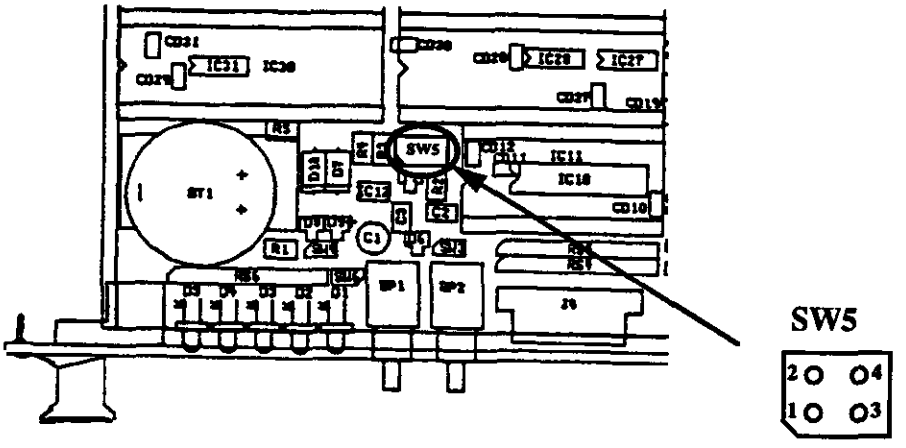
Selector SW11 configures JEDEC bank 0: IC61, IC62 (even, odd)
Selector SW10 configures JEDEC bank 1: IC59, IC60 (even, odd)
Selector SW9 configures JEDEC bank 2: IC38, IC39 (even, odd)

3.2.2.2 - JEDEC bank 3

JEDEC bank 3 (IC29 and IC30) can only take 27256, 27512 and 27010 EPROM chips. The SW5 selector configures bank 3 to match the type of EPROM chip fitted. IC29 takes the EVEN byte chip and IC30 the ODD byte chip.

JEDEC bank 3 - SW5 selector

CHIP		1-2	3-4
EEPROM	27256	o | o	o o
	27512	o o	o | o
	27010	o o	o | o



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3.2.3 - Access time settings on the four banks of Jedec sockets

The four banks of Jedec sockets have software-programmable access times. The default setting, adopted after a board reset, is one wait state. Zero wait states for Jedec banks 0 to 3 are set via registers B0DEL, B1DEL, B2DEL and B3DEL respectively.

These 1-bit write only registers are accessed through CPU data bit D7 as follows:

D7 statns	Wait states	Chip	Maximum permissible access time with :		
			68000 8MHz	68010 10MHz	68010 12.5MHZ
1	1	RAM EEPROM	300ns	200ns	150ns
		EPROM	400ns	300ns	250ns
0	0	RAM EEPROM	150ns	100ns	80ns
		EPROM	250ns	200ns	150ns

Addresses of access time registers :

- B0DEL $F40001 bank 0 access time register
- B1DEL $F50001 bank 1 access time register
- B2DEL $F60001 bank 2 access time register
- B3DEL $F70001 bank 3 access time register

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3.2.4 - Battery backup

The TSVME110 board is fitted as standard with a 3.6 V 110 mAh Dielh battery (NCM 3.6 R7). Battery charging is enabled with the SW4 link made. The SW6 link enables battery backup at the SW11, 10 and 9 selectors (see 3.2.2 - fig. 3.4) and at the control logic governing access to banks 0, 1 and 2.

Battery backup can be enabled/disabled for each bank individually from selectors SW11, SW10 and SW9:

link 1-2 made — battery backup enabled
link 3-4 not made

link 1-2 not made — battery backup disabled
link 3-4 made

Figure 3.2 (see § 3.2) shows the location of pins 1 and 2 on selectors SW11, 10 and 9.

The maximum battery backup duration will vary with the type of static RAM used.

Example:

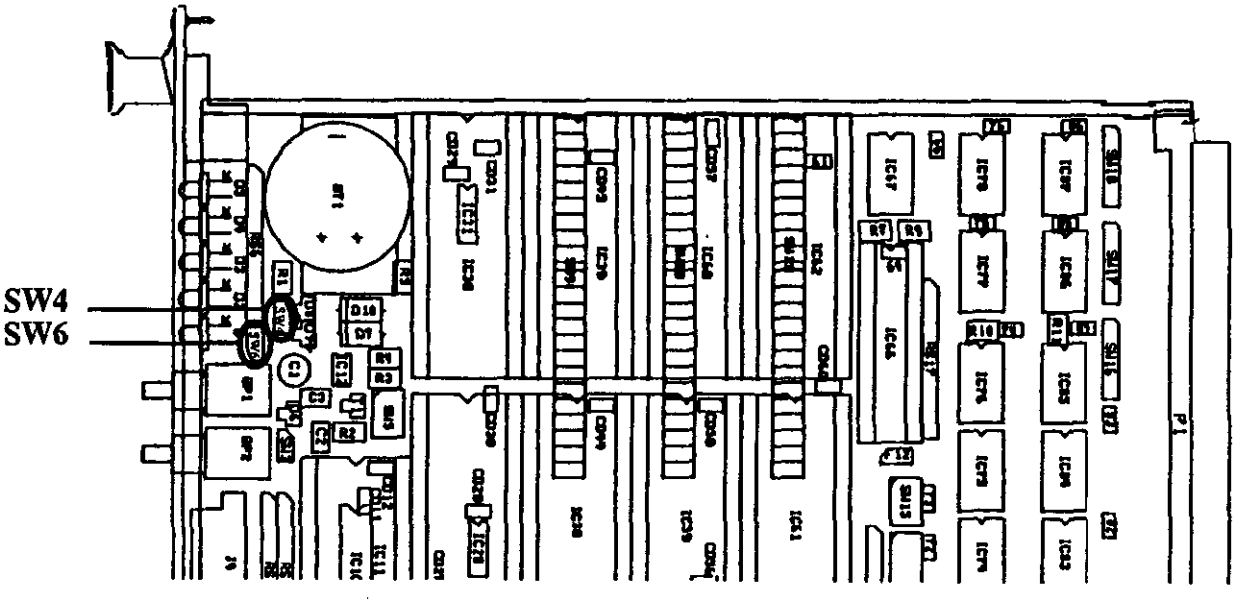
six static RAMs with standby current of 1uA
total current = 6uA => backup duration = 2 years

six static RAMs with standby current of 100uA
total current = 0.6 mA => backup duration = 180 hours

OPTIONS: The battery may be replaced by a 3.6V 850 mAh lithium cell of the SAFT LSL3 CN type if required. If this is done, the SW4 link should be removed.

- The backup voltage may also be taken from the VMEbus VMEVBB line. A system of diodes prevents conflicts with the on-board battery or cell, and SW6 continues to operate in the same way.

Location of SW4 and SW6



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3.3 - DYNAMIC RAM OPTION

The TSVME110 board may be fitted with 512K, 1M or 2M bytes of dynamic RAM. The 2-Mb version uses 1Mx4 chips.

Composition of different dynamic RAM configurations:

512 Kb	256 K x 4 chips fitted at F3 1-2 4-5	IC15, 22, 32, 44
1 Mb	256 K x 4 chips fitted at F3 1-2 4-5	IC15, 16, 22, 23, 32, 33, 44, 45
2 Mb	1 Mb x 4 chips fitted at F3 2-3 5-6	IC15, 22, 32, 44

- One wait state.

- Parity checking operates for all dynamic RAM read accesses. The parity error signal (PARERR*) is taken onto the local interrupt selector SW14.15 (§ 3.4.2). This signal is deasserted by a board hardware reset. It is also deasserted by a read access to address $FEXXX1 of the parity register (§ 3.5.1.1), upon which bit D7 gives the PARERR* status as follows:

d7 = 0 parity error detected
d7 = 1 no parity error

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3.4 - INTERRUPT HANDLING

The TSVME110 board logic handles 7 local interrupt levels and 7 VME interrupt levels.

To service a VMEbus interrupt the system asserts the VIACK* signal. This generates a VMEbus request and gives rise to an interrupt acknowledge cycle on the VMEbus.

To service a local interrupt, the CPU VPA* signal is asserted. All local interrupt acknowledgements are autovectored (vectors $19 to $1F).

3.4.1 - VMEbus interrupt requests

The TSVME110 board handles the 7 VME interrupt lines. VME interrupts are software-enabled, with all VME interrupt requests masked after a board hardware reset.

A write access to the 1-bit VME IT registers has the following effect:

with D7 at 1: enable IT at this level
with D7 at 0: mask IT at this level

Address

```
$F3XXX3  VMEbus level 1 IT mask register
$F3XXX5  VMEbus level 2 IT mask register
$F3XXX7  VMEbus level 3 IT mask register
$F3XXX9  VMEbus level 4 IT mask register
$F3XXXB  VMEbus level 5 IT mask register
$F3XXXD  VMEbus level 6 IT mask register
$F3XXXF  VMEbus level 7 IT mask register
```

These registers are write only.

3.4.2 - Local interrupt requests

The various local IT sources are taken onto selector SW14, where they can be wired, by jumper or wrapping, onto the seven local IT lines handled by the TSVME110 board logic. Local interrupts may also be software-masked, and all local IT lines are masked after a board hardware reset. A write access to the 1-bit VME IT registers has the following effect:

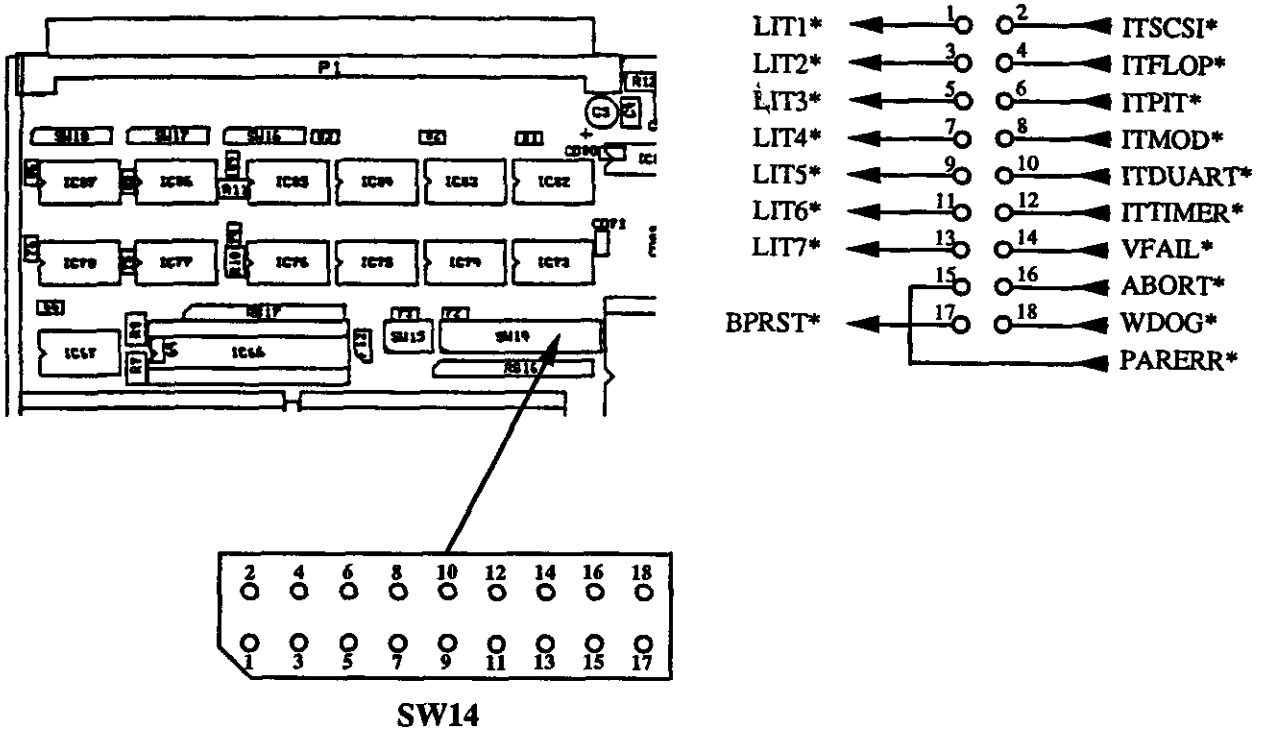
with D7 at 1: enable IT at this level
with D7 at 0: mask IT at this level

Address:

```
$F2XXX3  local level 1 IT mask register
$F2XXX5  local level 2 IT mask register
$F2XXX7  local level 3 IT mask register
$F2XXX9  local level 4 IT mask register
$F2XXXB  local level 5 IT mask register
$F2XXXD  local level 6 IT mask register
$F2XXXF  local level 7 IT mask register
```

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Fig. 3.5 : Local interrupt configuration



The SW14 selector configures the seven local IT lines LIT1* to LIT7*.

BPRST* wires the watchdog output WDOG* in a logical "OR" with the pushbutton for a board hardware reset.

Local interrupt sources are all of the open collector type and active at 0:

- ITSCSI* :

  Interrupt request from SCSI bus controller (WD33C93)

- ITFLOP* :

  Interrupt request from floppy interface controller (WD35C67)

- ITPIT* :

  Interrupt request from parallel port (68230 PIT)

- ITMOD* :

  Interrupt request from user module

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- ITDUART* :

  Interrupt request from dual serial link controller (Z8530)

- ITTIMER* :

  Interrupt request from triple timer (68B40)

- VFAIL* :

  Interrupt request from wired logical "OR" between VMEbus ACFAIL* and SYSFAIL* signals (provided F15 solder bead is set)

- ABORT* :

  Interrupt request from front panel "ABORT" pushbutton

- PARERR* :

  Interrupt request on dynamic memory parity error

- WDOG* :
  Watchdog output (open collector): may be wired either to an IT line or to a board hardware reset.

3.5 - CONTROL AND STATUS REGISTERS

There are several types of control and status registers on the TSVME110 board:

- Board control function registers:
  - Parity register
  - Local and VME IT mask registers
  - Bus time out control registers
  - JEDEC bank access time registers (see 3.2.3)
- Overall board control and status register
- Watchdog reset register
- Decimal display register
- SCSI/floppy interface control and status register (optional)

3.5.1 - Board control function registers

The board control function registers are all 1-bit registers operating on CPU bit D7. This bit determines the effect of writing 1s to the various register addresses and yields the results of read operations to these addresses.

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3.5.1.1 - Parity register - read only

Address : $FEXXX1

Reading bit D7 gives the status of the parity error signal (PARERR*).

D7 = 1 no parity error
D7 = 0 parity error detected on read access to dynamic RAM

A read to this register resets the PARERR* signal.

3.5.1.2 - Local and VME interrupt mask registers - write only

The IT mask registers behave as follows:

- loaded with 0 by board hardware reset or write access with D7 = 0
- loaded with 1 by write access with D7 = 1

Interrupts are masked with registers at 0 and enabled with registers at 1.

Address	IT mask	Level
$F2XXX3	local	1
$F2XXX5	"	2
$F2XXX7	"	3
$F2XXX9	"	4
$F2XXXB	"	5
$F2XXXD	"	6
$F2XXXF	"	7
$F3XXX3	VME	1
$F3XXX5	"	2
$F3XXX7	"	3
$F3XXX9	"	4
$F3XXXB	"	5
$F3XXXD	"	6
$F3XXXF	"	7

3.5.1.3 - Bus time out control registers

The bus time out controller has two 1-bit write-only registers: BTODIS and BTOMOD. These are loaded with 0 by a write access with D7 = 0 or by a board hardware reset. They are loaded with 1 by a write access with D7 = 1.

Read operations to the addresses corresponding to these registers yield, on D7, the status of the BTOUT signal. The BTOUT signal is discussed in § 3.6.2.

Address	Write	Read
$F10XX1	BTOMOD	BTOUT
$F18XX1	BTODIS	BTOUT

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Bus time out control with BTODIS, BTOMOD:

BTODIS	BTOMOD		
0	X	Bus time out	inoperative
1	0	Bus time out	active for accesses to VMEbus only, counting from TSVME110 board being granted the bus.
1	1	Bus time out	active for all CPU cycles, counting from high-to-low transition on AS*

3.5.1.4 - JEDEC bank access time registers - write only

The four 1-bit JEDEC bank access time registers also operate on bit D7. They are loaded with 1 by a board hardware reset or a write access to the corresponding address with D7 = 1. They are loaded with 0 by a write access with D7 = 0.

Address	Register	JEDEC bank
$F4XXX1	B0DEL	0
$F5XXX1	B1DEL	1
$F6XXX1	B2DEL	2
$F7XXX1	B3DEL	3

With the register at 1, CPU access cycles to the Jedec bank in question will have one wait state.

With the register at 0, CPU access cycles to the Jedec bank in question will have zero wait states.

The table in section 3.2.3 shows the maximum permissible access times for chips installed in the Jedec sockets for one-wait-state and zero-wait-state operation.

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3.5.2 - Overall board control/status register

This is a read/write register.

Access address : $FBXXX1

Write :

D7	D6	D5	D4	D3	D2	D1	D0
NU	OVFAIL*	NU	MWDOG	Led3	Led2	Led1	Fail

This register is cleared by a TSVME110 board hardware reset.

bits 0-3 :
- FAIL, LED1, LED2, LED3 : front panel LED control

= 0 LED on
= 1 LED off

The three user LEDS 1 to 3 and the FAIL LED are turned off on successful completion of all self-tests phases (see § 3.11 - FRONT PANEL).

bit 4 - MWDOG : watchdog operating mode

= 0 watchdog triggers if timer not reset within maximum time threshold

= 1 watchdog triggers on either of the following:

. timer reset attempt before minimum time threshold
. timer not reset before maximum time threshold

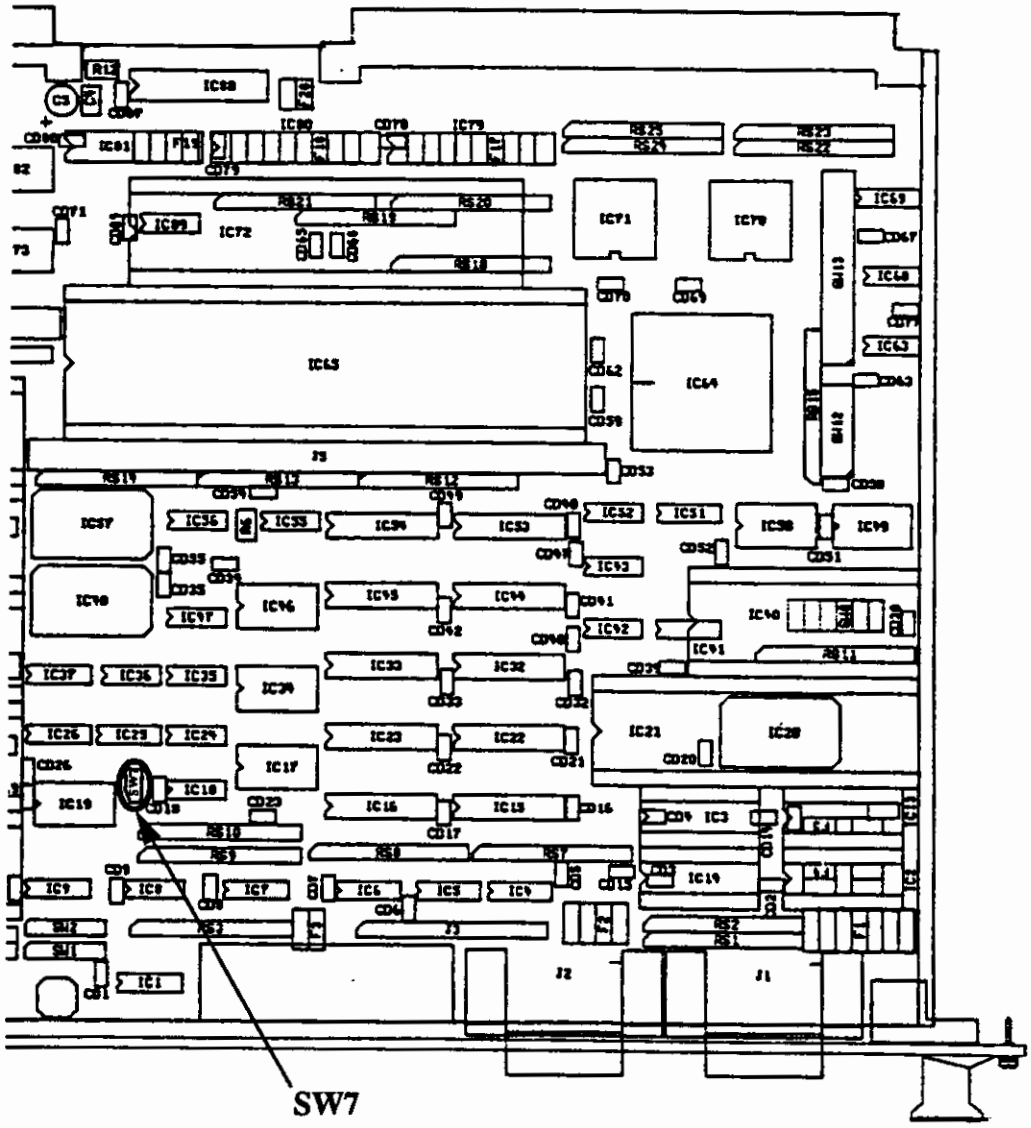
For further details, see 3.6.4.

bit 6 - OVFAIL* : VMEbus SYSFAIL* enable (with bit at 0)

The TSVME110 board releases the VMEbus SYSFAIL* signal when this bit is loaded with a 1.

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Location of SW7 selector



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Read :

D7	D6	D5	D4	D3	D2	D1	D0
ABORT*	SYSFAIL*	ACFAIL*	MODHCK	Led3	Led2	Led1	FAIL

bits 0-3 : status of FAIL, LED1, LED2 and LED3 signals

These bits are set by writing to the same register.

bit 4 : MODHCK - status of SW7 selector

0 = jumper set
1 = jumper not set

The standard version of the TSVBUG debugger polls this bit and will loop the self-test function on power up if it finds a jumper set on SW7.

bit 5 : status of VMEbus ACFAIL* signal

bit 6 : status of VMEbus SYSFAIL* signal

bit 7 : status of TSVME110 board ABORT* signal
(asserted by pressing BP2, the front panel ABORT pushbutton)

ACFAIL*, SYSFAIL* and ABORT* are active at 0.

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3.5.3 - Watchdog reset register

Address : $FBXXX7

Write :

A write access to this address resets the watchdog timer (provided the F20 selector is set for "internal reset" - see 3.6.4).

Read :

4-bit register

D3	D2	D1	D0
IWDOG*	CPTM	CPTH	CPTH2

BIT 0 : CPTH2
Fixed output signal from watchdog timer: period = 0.262144 s

BIT 1 : CPTH
Watchdog timer output selected as minimum reset threshold from SW2 selector: period variable from 2.097152 s to 0.262144 s

BIT 2 : CPTM
Watchdog timer output selected as maximum reset threshold from SW1 selector: period variable from 4.194304 s to 0.524288 s

BIT 3 : IWDOG*
Watchdog logic control signal: active at 0

CPTH2 and CPTH in this register are read for the purpose of monitoring watchdog operation without necessarily triggering it.

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3.5.4 - Decimal display register

This register controls the 7-segment BCD display.

Write-only access to address : $FBXXX3

Bits 0-3 control the decimal value displayed (bit 0 = LSB, bit 3 = MSB).

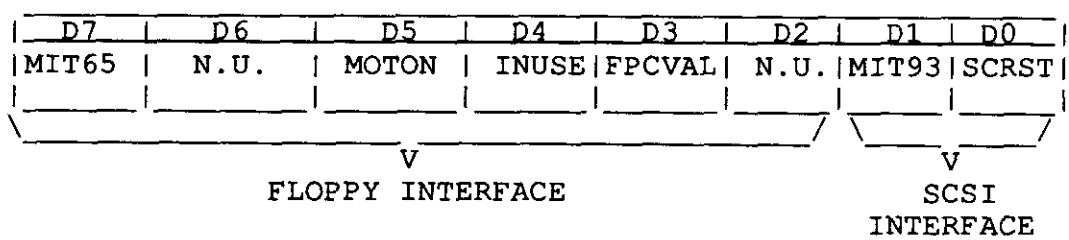
Bit 4 controls the decimal point:
= 0 point lit
= 1 point off

After a board hardware reset, the display shows a value of 0 with the decimal point lit.

3.5.5 - Optional register : SCSI and floppy control/status register

Write and read, address : $FBXXX5

Write :



This register is cleared by a board hardware reset and by a CPU RESET instruction.

bit 0 : SCRST

This bit asserts the SCSI bus reset line. It is active at 1, which means that the SCSI bus reset line will not be asserted when the register is cleared.

bit 1 : MIT93

This bit masks the IT line from the WD33C93 SCSI bus controller. It is active at 0 (IT masked).

bit 2 : not used

bit 3 : FPCVAL

Precompensation used by floppy controller:
= 0 : 187 ns
= 1 : 125 ns.

bit 4 : INUSE

This signal is wired via the SW13 selector to the floppy interface INUSE line, which is managed by the control register and not by the floppy controller.

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bit 5 : MOTON

This signal is wired to the floppy interface MOTON line, which is managed by the control register and not by the floppy controller.

bit 6 : not used

bit 7 : MIT65

This bit masks the IT line from the WD37C65 floppy controller (interrupt masked with bit at 0).

- Read :

D7	D6	D5	D4	D3	D2	D1	D0
MIT65	RDY	MOTON	INUSE	FPCVAL	IRQ65	MIT93	RSTSC

Apart from bits 0, 2 and 6, we have here a readback of the control register.

bit 0 : RSTSC

This bit is not a readback of bit SCRST in the control register. Rather, it gives the inverse of the SCSI bus reset line, which may be asserted by another user of the SCSI bus.
=1 SCSI reset asserted
=0 SCSI reset deasserted

bit 2 : IRQ65

Status of WD37C65 floppy controller IRQ line before MIT65 masking logic
=1 floppy controller IRQ line asserted
=0 floppy controller IRQ line deasserted

bit 6 : RDY

Status of floppy interface READY line via SW13 selector

3.6 - TSVME110 BOARD CONTROL FUNCTIONS

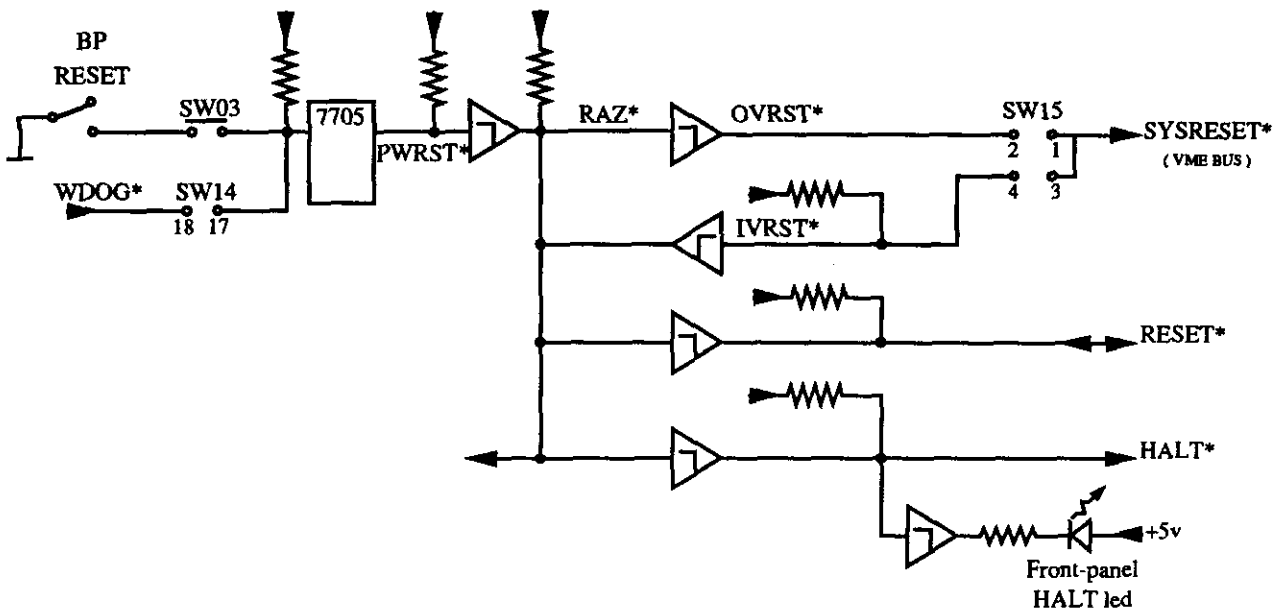
This section discusses the following internal and VMEbus-related control functions found on the TSVME110 board.

- reset
- bus time out
- SYSFAIL, ACFAIL
- watchdog

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3.6.1 - Reset function

Fig. 3.6 : Block diagram



The RAZ* signal can be asserted by any of the following:

- front panel pushbutton (with SW3 link set)
- board power up or 7705 voltage drop (+5V)
- VMEbus (with SW15 link 3-4 set)
- watchdog triggering (with SW14 link 17-18 set)

The RESET* signal can be asserted by either of the following:

- RAZ* signal as above
- CPU (in particular, the RESET instruction for the RESET* signal)

Assertion of the RAZ* signal corresponds to a board hardware reset.

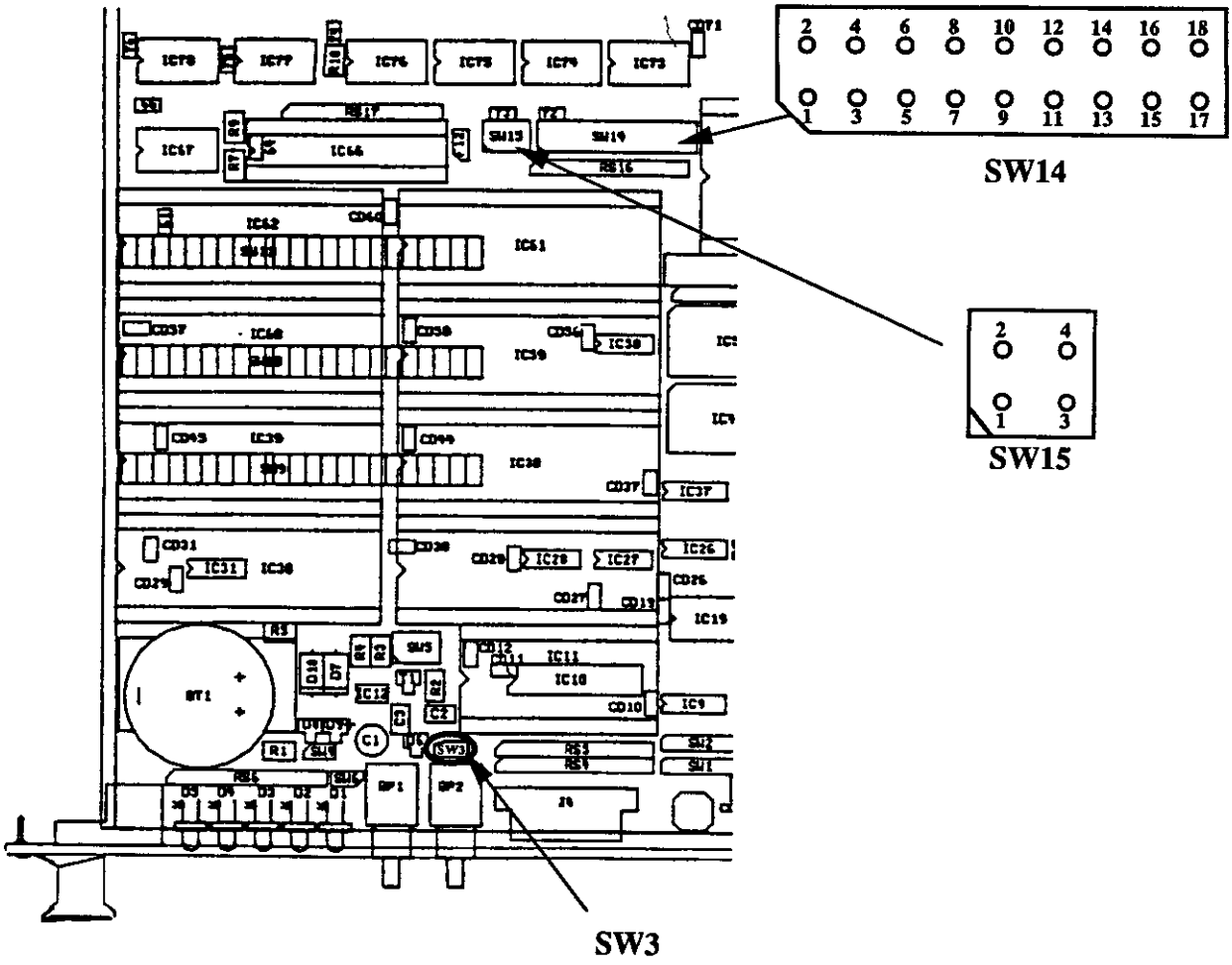
The following are affected by a board hardware reset:

- CPU RESET* and HALT* lines
- interrupt handling system (masks)

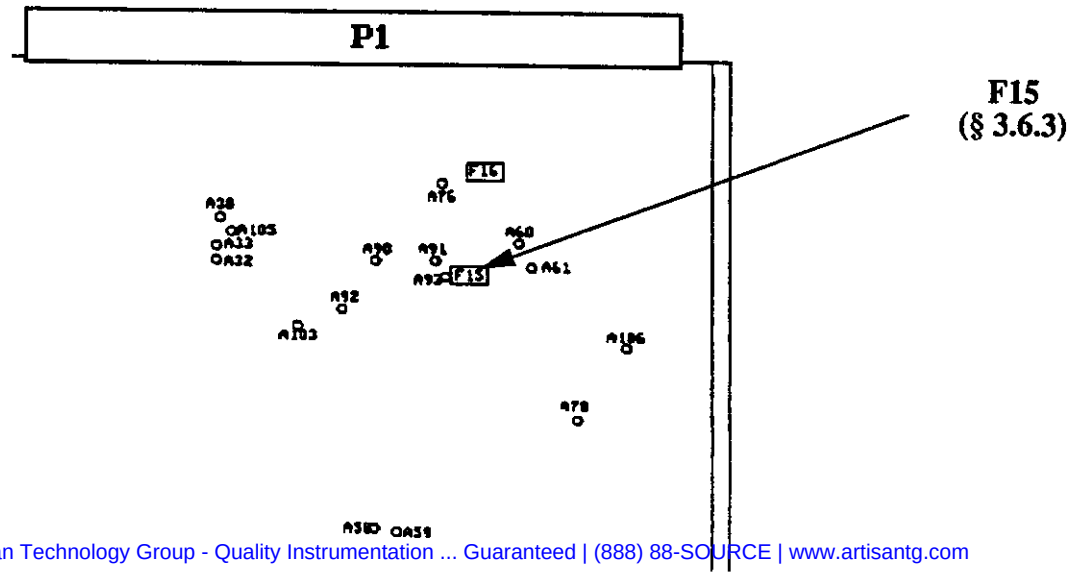
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Location of SW3, SW14, SW15 and F15

Components Side



Solder beads Side



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- the registers below:

  . bus time out
  . JEDEC bank access times
  . overall board control/status
  . decimal display

- watchdog timer

- VMEbus arbiter/requester

- VMEbus (with SW15 link 1-2 set)

- Z8530 DUART via RD* and WR* signal logic

SW15 links 1-2 and 3-4 are mutually exclusive; otherwise, RAZ* would be looped back via IVRST*.

The following are wired to the RESET* signal:

- CPU
- the peripheral devices below:

  . 68B40 timer
  . 68230 PIT
  . WD33C93 SCSI bus controller
  . WD37C65 floppy controller

3.6.2 - Bus time out function

The bus time out function, disabled by a board hardware reset, is operated by two 1-bit registers:

BTODIS	$F18XX1
BTOMOD	$F10XX1

These two registers are cleared after a reset. They are programmed by writing to the above addresses, upon which they will take the value of data bit D7.

BTODIS	BTOMOD	BUS TIME OUT FUNCTION	
0	X	Bus time out	inoperative
1	0	Bus time out	active for accesses to VMEbus only, counting from TSVME110 board being granted the bus.
1	1	Bus time out	active for all CPU cycles, counting from high-to-low transition on AS*

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The bus error will be generated between 263 us and 279 us after the bus time out has been triggered, provided AS* remains asserted.

For accesses to the VMEbus, a bus time out will assert the VMEbus BERR* signal.

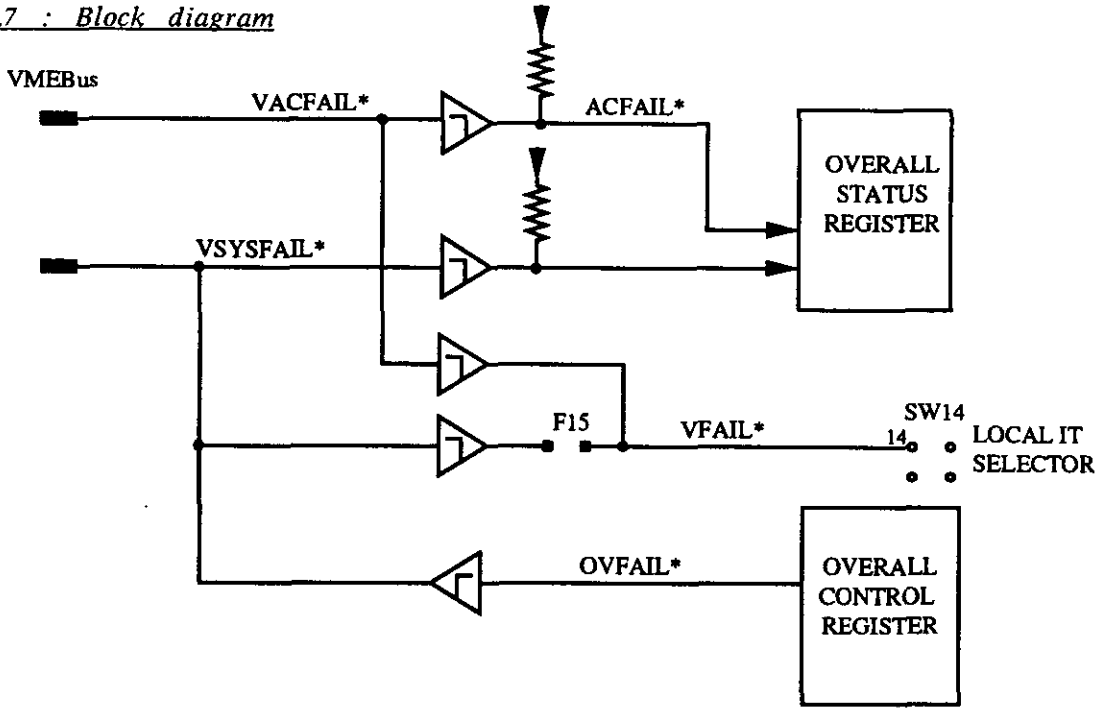
Triggering of the bus time out function sets the BTOUT register, the value of which can be read back (on bit D7) from address $F1XXX1.

D7 = 1 bus time out has been triggered
D7 = 0 bus time out has not been triggered since the last board hardware reset nor since the last read to this register

BTOUT is cleared by a board hardware reset and on completion of a read cycle to this register at $F1XXX1.

3.6.3 - VMEbus SYSFAIL* and ACFAIL* signals

Fig. 3.7 : Block diagram



The VMEbus ACFAIL* signal is permanently received by TSVME110 board. The status of this signal can be read back at any time from bit D5 of the overall board status register.

ACFAIL* may also be used to generate a local IT on the TSVME110 board, wired as a logical "OR" with the SYSFAIL* signal on pin 14 of the SW14 selector.

The status of the VMEbus SYSFAIL* signal can be read back at any time from bit D6 of the overall board status register.

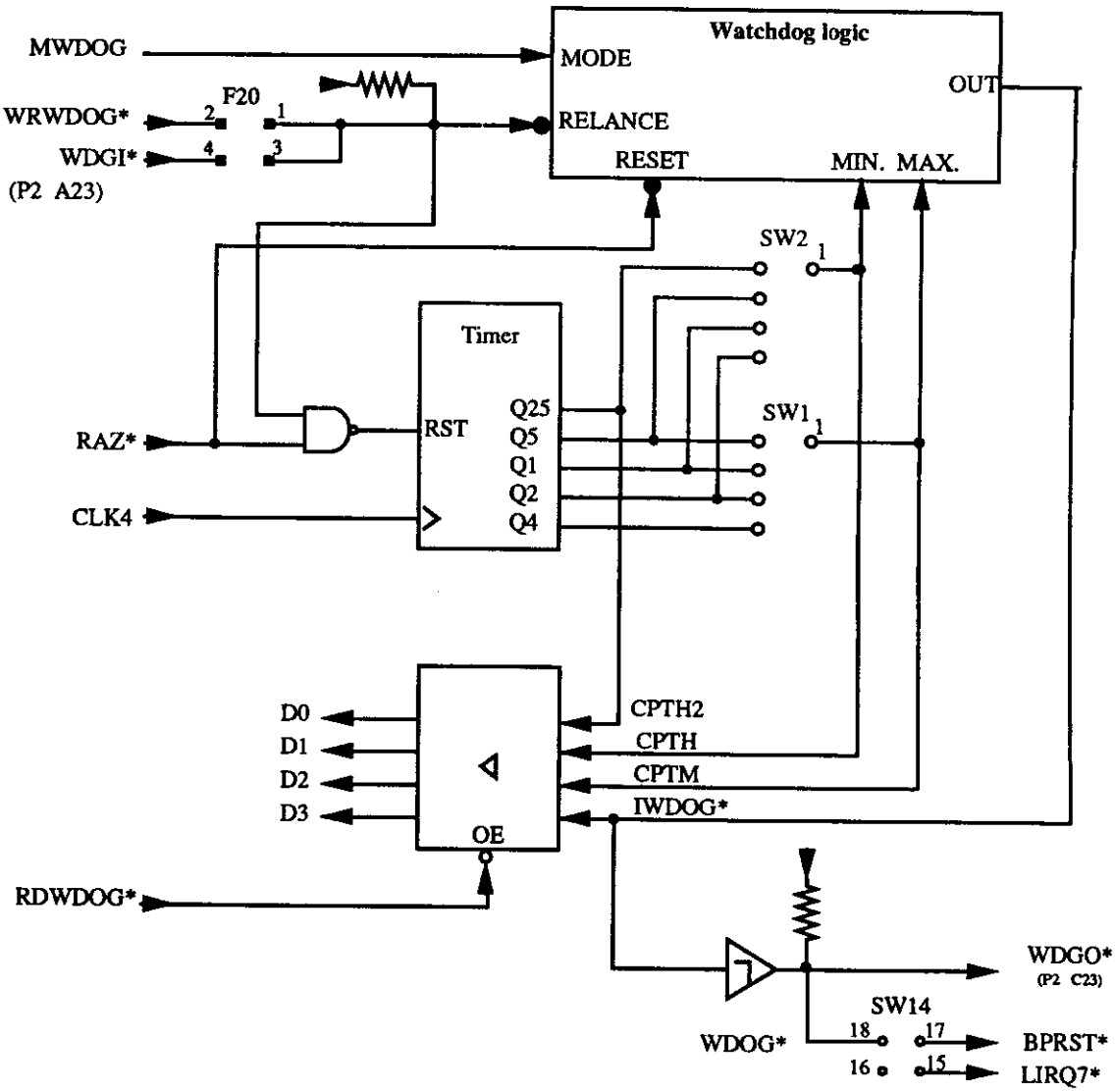
Provided the F15 link is set, SYSFAIL* may also be used to generate a local IT on the TSVME110 board, wired as a logical "OR" with the ACFAIL* signal on pin 14 of the SW14 selector.

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The TSVME110 board is able to assert the SYSFAIL* signal on the VMEbus from bit D6 in the overall board control register. SYSFAIL* is asserted on the VMEbus when this bit is at 0, i.e. after a board hardware reset or a write access to the register with D6 at 0. SYSFAIL* is released by writing to the overall control register with D6 at 1 (see § 2.6.2 for locations of F15 and SW14).

3.6.4 - Watchdog function

Fig. 3.8 : Block diagram



Description of watchdog function:

The watchdog can be triggered in one of two ways:

1. Conventional mode:

   Watchdog triggered if reset signal is not asserted within upper time limit.

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2. MIN/MAX mode:

Watchdog triggered either if the reset signal is asserted before a minimum time limit, or (as in conventional mode) if the reset signal is not asserted before a maximum time limit.

In compliance with the recommendations of the French *Institut National de Recherche sur la Sécurité*, Min/Max mode provides a means for increasing the safety of applications; over-short loop times are just as indicative of hitches in application programs as over-long ones.

- Watchdog reset :

In either of the above two operating modes, the watchdog reset signal may be taken from one of two possible sources. This is set from the F20 selector:

- F20 link 1-2 set: watchdog reset by write to watchdog reset register ($FBXXX7)

- F20 link 3-4 set: watchdog reset by low-level external TTL or open collector signal on WDGI (A23 on P2 connector) (zero-level pulse of at least 40 ns duration)

Note:

With both links set on F20, watchdog reset will operate by writing to the watchdog reset register and the user will be able to monitor the internal reset proceedings from an external device via the WDGI line. However, the signal output on P2 under these circumstances is generated by a 74LS138, which means that monitoring must be performed in the proximity of the P2 connector. The duration of the low-level pulses output from P2 is at least 250 ns.

- Watchdog outputs:

The WDOG* signal, active at 0, is accessible from pin C23 of the P2 connector. It is also taken onto the SW14 selector, where it can be wired so as to produce either a board hardware reset (SW14 link 18-17) or a local IT.

If it is taken as a local IT, the corresponding IT service sub-routine is able to check that the IT was in fact triggered by the watchdog by reading the watchdog register at $FBXXX7. Here, bit D3 (active at 0) gives the WDOG* status; bit D1 gives the CPTH status (when at 0 indicates lower time limit has not yet been reached); bit D2 gives the CPTM status (when at 1 indicates upper time limit has been exceeded).

- Watchdog reset after triggering:

In conventional mode (MAX), the watchdog timer is reset by simply asserting the reset signal.

In MIN/MAX mode, it is necessary to first switch over to conventional mode, then assert the reset signal, and then switch back to MIN/MAX mode by reloading a 1 in the MWDOG* bit of the overall control register.

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- Watchdog monitoring:

Operation of the watchdog timer can be monitored by reading the watchdog register; the status of the timer output (period = 262.144 ms) is given on bit D0.

MAXIMUM time limit:

The upper time limit is set from selector SW1 (wrapping) as follows:

```
SW1
1 o------>  CPTM
2 o<-----   Q .5    Period:    524.288 ms
3 o<-----   Q 1     Period:  1 048.576 ms
4 o<-----   Q 2     Period:  2 097.152 ms
5 o<-----   Q 4     Period:  4 194.304 ms
```

Triggering takes places when the signal selected here goes low-to-high, i.e. at half-period:

```
Link SW1  1-5   trigger:  2 097.152 ms
          1-4   trigger:  1 048.576 ms
          1-3   trigger:    524.288 ms
          1-2   trigger:    262.144 ms
```

MINIMUM time limit (enabled if MWDOG* = 1):

The lower time limit is set from selector SW2 (wrapping) as follows:

```
SW2
1 o------>  CPTH
2 o<-----   Q .25   Period:    262.144 ms
3 o<-----   Q .5    Period:    524.288 ms
4 o<-----   Q 1     Period:  1 048.576 ms
5 o<-----   Q 2     Period:  2 097.152 ms
```

Triggering takes place if the watchdog reset signal is asserted before the signal selected here goes low-to-high; this gives the following minimum thresholds:

```
Link SW2  1-5   trigger:  1 048.576 ms
          1-4   trigger:    524.288 ms
          1-3   trigger:    262.144 ms
          1-2   trigger:    131.072 ms
```

Connections on P2:

WDGI*	P2. a23
WDGO*	P2. c23

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3.7 - VMEBUS INTERFACE

The TSVME110 board acts exclusively as a master on the VMEbus. Interfacing with the VMEbus involves the following functions:

- DTB
- bus arbiter / requester
- interrupt handling
- management of VME control signals

3.7.1 - Data transfer (DTB)

Accesses from the TSVME110 board CPU to the VMEbus have the following formats:

- A24 : D16/D08
- A16 : D16/D08

- TSVME110 board mapping on VMEbus:

. Standard addressing (A24:D16): start of VME mapping varies with size of on-board dynamic memory:

DYNAMIC RAM:	none	: standard VME	$10000 - $BFFFFF
	512K	: " "	$80000 - $BFFFFF
	1Mb	: " "	$100000 - $BFFFFF
	2Mb	: " "	$200000 - $BFFFFF

. Short addressing (A16:D16): $FF0000 - $FFFFFF

- Address modifiers used:

CODE	FUNCTION ON VMEBUS
$29	Short, user, I/O access
$2D	Short, supervisor, I/O access
$39	Standard, user, data access
$3A	Standard, user, program access
$3D	Standard, supervisor, data access
$3E	Standard, supervisor, program access

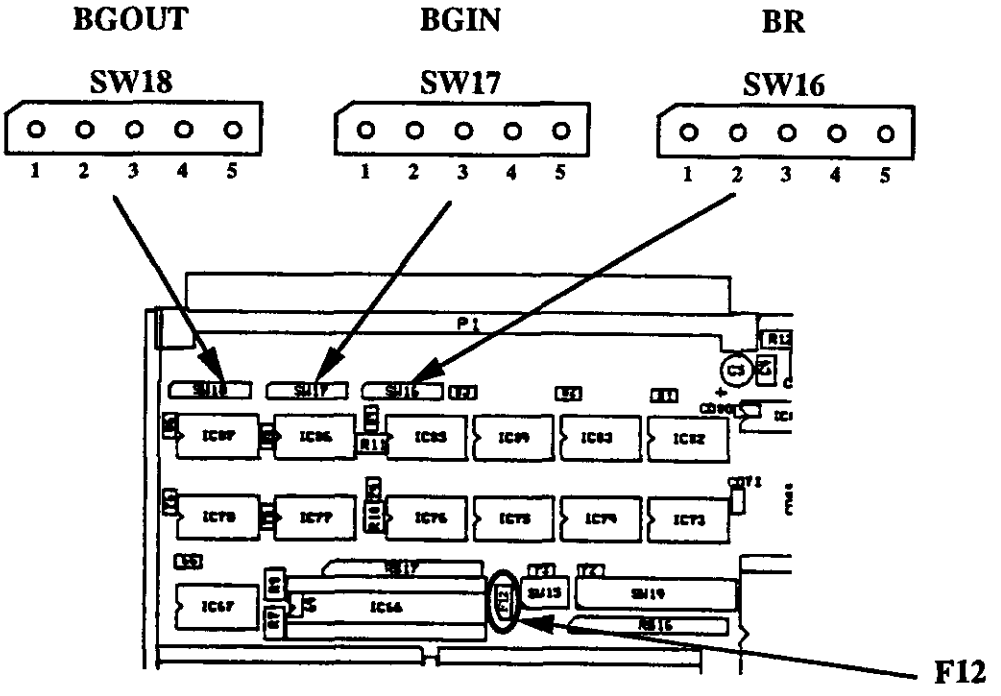
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3.7.2 - VMEbus arbiter / requester

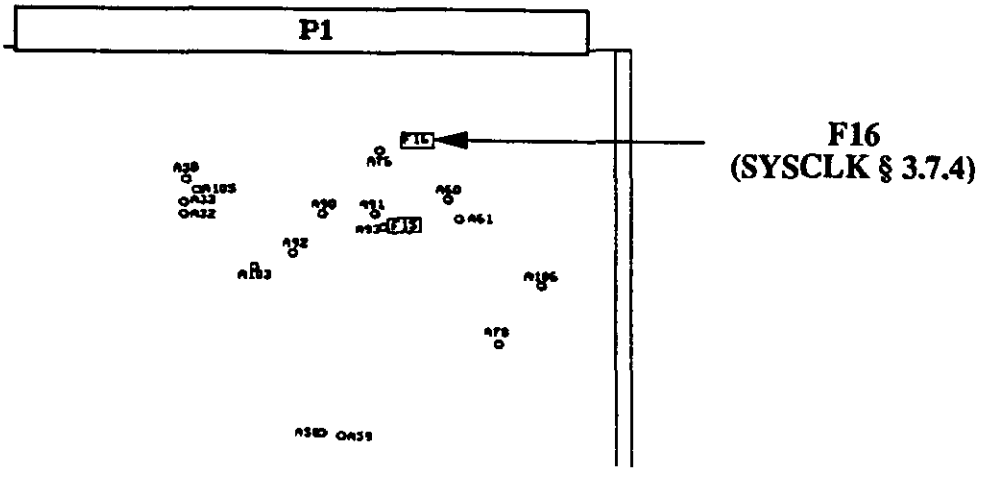
The TSVME110 board incorporates a single-level VME arbiter, enabled/disabled from selector F12. The arbiter function is enabled with the F12 jumper set and disabled with the F12 jumper absent, in which case the board acts as a simple requester on the VMEbus.

The requester operates in RELEASE ON REQUEST mode. The VME bus request / bus grant level required for the TSVME110 board is set from selectors SW16, SW17 and S18.

Location of F12, SW16, SW17 and SW18



Location of F16 - Soldered side



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The TSVME110 board must provide chaining for those BGIN and BGOUT signals which it does not handle itself. For example, if request / grant level 3 is selected for the TSVME110 board, BG2IN* must be linked straight through to BG2OUT*, BG1IN* to BG1OUT*, and BG0IN* to BG0OUT*.

SW17.2	BG3IN*	SW18.2	BG3OUT*
SW17.3	BG2IN*	SW18.3	BG2OUT*
SW17.4	BG1IN*	SW18.4	BG1OUT*
SW17.5	BG0IN*	SW18.5	BG0OUT*

These links are made by wrapping:

Link on SW16, SW17 and SW18	Bus request / bus grant level
1 - 2	3
1 - 3	2
1 - 4	1
1 - 5	0

3.7.3 - VMEbus interrupt handling

The TSVME110 board is able to simultaneously handle the seven VMEbus interrupt levels.

Interrupts from the VMEbus are masked/enabled from the board's seven VME IT mask registers.

All VME interrupts are masked after a board hardware reset. They can be individually enabled by writing to the appropriate VME IT mask register with D7 at 1 and they can be remasked by writing with D7 = 0.

Addresses $F3XXX3,5,7,9,B,D,F, for levels 1 to 7

See 3.5.1.1.

The TSVME110 board does not have a VME interrupt generator function.

3.7.4 - VMEbus control signals: SYSRESET*, SYSFAIL*, ACFAIL*, SYSCLK

- SYSRESET*

The TSVME110 board reset function is dealt with in 3.6.1.

Handling of the SYSRESET* signal is set from the SW15 selector as follows:

. Neither link set: TSVME110 board isolated from VMEbus SYSRESET*

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. SW15 link 3-4 set: TSVME110 board receives SYSRESET* for asserting RAZ* and RESET*

. SW15 link 1-2 set: TSVME110 board generates SYSRESET* signal on VMEbus under the following circumstances:

- power up or mains failure
- operation of front panel RESET pushbutton (with SW3 link set)
- watchdog triggering (with SW14 link 17-18 is set)

Links 1-2 and 3-4 on SW15 must not both be set at the same time.

See § 3.6.1 for locations of SW15, 14 and 3.

- SYSFAIL*

See § 3.6.3 and selector location in § 3.6.1.

Incoming SYSFAIL*:

- SYSFAIL* is permanently accessible on bit 6 of the overall board status register.

- With the F15 link set, SYSFAIL* may be used for generating a local IT, wired as a logical "OR" with ACFAIL* on pin 14 of SW14.

Outgoing SYSFAIL*:

- SYSFAIL* is controlled from bit 6 of the overall board control register. It is generated by a board hardware reset and can also be disabled or re-enabled by writing to the register (SYSFAIL* asserted with bit 6 = 0).

- ACFAIL*

See § 3.6.3

ACFAIL* is incoming only:

ACFAIL* can be read from bit 5 of the overall board register.
It is wired as a logical "OR" with SYSFAIL* on pin 14 of SW14 (local interrupt selector).

- SYSCLK*

With the F16 link set, the TSVME110 board generates a 16 MHz clock signal as the SYSCLK* signal on the VMEbus. See 3.7.2 for location of F16.

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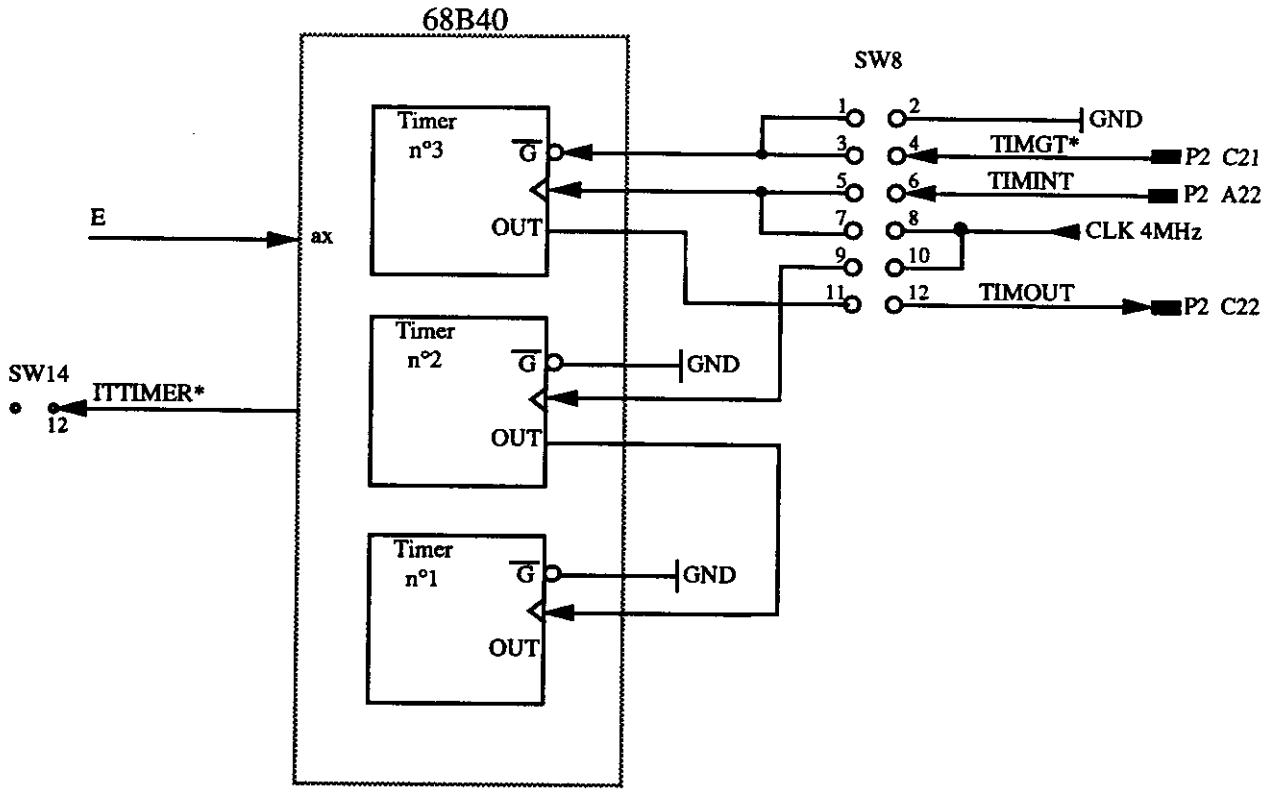
3.8 - TSVME110 BOARD PERIPHERAL DEVICES

3.8.1 - 68B40 triple timer

The TSVME110 board is fitted as standard with a 68B40 triple timer capable of generating variable time intervals.

The 68B40 chip possesses three 16-bit binary timers with their associated control registers, plus an overall status register. The timers are software-controlled and may be wired to a local IT line from pin 12 on SW14.

Fig. 3.9 : 68B40 triple timer



- Timer 3 can operate either internally or from signals entering on P2. It is also able to supply outgoing signals to P2.

. Enable:
- always enabled : SW8 link 1-2 set
- enabled from TIMGT* (P2.C21) : SW8 link 3-4 set

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These two links are mutually exclusive.

. Clock:

- internal CPU clock E: frequency = CPU clock / 10 = 0.8 MHz
  (or 1MHz with 10 MHz 68010 option)
  (or 1,25MHz with 12,5 MHz 68010 option)

- one of the following external clocks:

  . on-board 4 MHz clock : SW8 link 7-8 set
  . TIMINT clock from P2 pin A22 : SW8 link 5-6 set

  These two links are mutually exclusive.

. Output:

- P2 pin C22 - TIMOUT : SW8 link 11-12 set
- timer 2 clock input : SW8 link 9-11 set

- Timer 2 is permanently enabled and its output is permanently wired to the clock input of timer 1.

The timer 2 clock may be internal or external as follows:

- internal CPU clock E: 0.8 MHz
  (or 1 MHz with 10 MHz 68010 option)
  (or 1,25 MHz with 12,5 MHz 68010 option)

- external:
  . timer 3 output : SW8 link 9-11 set

- Timer 1 is permanently enabled.

The timer 1 clock may be taken from either of the following:

- internal 0.8 MHz clock (1 MHz or 1.25 MHz options)
- timer 2 output

The three timers may operate either independently (in which case timer 1 must be set to "internal clock") or in cascade.

68B40 base address : $FAXXX1

P2 connections :

TIMGT*	P2.c21	timer 3 enable
TIMINT	P2.a22	timer 3 input
TIMOUT	P2.c22	timer 3 output

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68B40 TIMER - PROGRAMMING EXAMPLE

Timer 3 is initialized to generate an external 25 KHz clock signal on output 03, using an external clock input taken from the TSVME110 board 4MHz clock (SW8 link 7-8 set).

Timer 2 is initialized to program an external 0.5 KHz clock signal on output 02, using an external clock input taken from the timer 3 output (SW8 link 9-11 set).

Timer 1 is initialized to generate an interrupt on its IRQ line at an interval of 100 ms, using an external clock input taken from the timer 2 output.

The example program only covers timer initialization; the user must therefore add the program for initializing the interrupt service logic, the vector table (autovectored) and the service routine for the incoming interrupt.

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```
Sep  2 03:43 1989  timer.s Page 1


timer    equ $fa0001      ; timer 68b40.
* write registers.  offsets / timer .
tmcr1    equ     0        ; control register 1 if tmcr20 = 0.
tmcr3    equ     0        ; control register 3 if tmcr20 = 1.
tmcr2    equ     2        ; control register 2.
tmsbr1   equ     4        ; msb buffer register.
tml1     equ     6        ; lsb timer 1 latches.
tmsbr2   equ     8        ; msb buffer register.
tml2     equ     $a       ; lsb timer 2 latches.
tmsbr3   equ     $c       ; msb buffer register.
tml3     equ     $e       ; lsb timer 3 latches.
* read registers.  offsets / timer .
tmsta    equ     2        ; status register.
tmcnt1   equ     4        ; msb timer 1 counter.
tmlsb1   equ     6        ; lsb buffer .
tmcnt2   equ     8        ; msb timer 2 counter.
tmlsb2   equ     $a       ; lsb buffer .
tmcnt3   equ     $c       ; msb timer 3 counter.
tmlsb3   equ     $e       ; lsb buffer .
*
* control registers bits.
tmcoe    equ %10000000 ; timer x counter output enable.
tmie     equ %01000000 ; timer x interrupt enable.
tmcmc    equ %00000100 ; timer x dual-8bits counter mode /16b mode.
tmeclk   equ %00000010 ; timer x uses Enable clock / ext.cx* clock.
tmirb    equ %00000001 ; TMCR1 ONLY : all timers in preset state.
tmwcr1   equ %00000001 ; TMCR2 ONLY : write to tmcr1 in 0/else tmcr3.
tm3psc   equ %00000001 ; TMCR3 ONLY : t3 clock is prescaled (/8).
tmcogwr  equ %00000000 ; continuous mode, init on Gv,wr.latch,rst.
tmfreqm  equ %00001000 ; freq.comp.mode, it on G!_!-! < count time out.
tmcogr   equ %00010000 ; continuous mode, init on Gv or rst.
tmpulwm  equ %00011000 ; pulse comp.mode, it on G!__! < count time out.
tmshgwr  equ %00100000 ; single shot mode, init on Gv,wr.latch,rst.
tmfreqp  equ %00101000 ; freq.comp.mode, it on G!_!-! > count time out.
tmshgr   equ %00110000 ; single shot mode, init on Gv or rst.
tmpulwp  equ %00111000 ; pulse comp.mode, it on G!__! > count time out.
*
timerst  equ     *
 lea     timer,a3
 move.b  #tmwcr1,tmcr2(a3)          ; cr1 access
 move.b  #tmirb,tmcr1(a3)           ; all timers in preset state.
*
 clr.b   tmcr2(a3)                  ; cr3 access.
 move.b  #tmcoe+tm3psc,tmcr3(a3)    ; c3 in cont.mode - ext clk prescaled.
 clr.b   tmsbr3(a3)                 ; 0 -> msb cr3.
 move.b  #5,tml3(a3)                ; 4 -> lsb cr3 : 25khz clock.
 move.b  #tmcoe+tmcmc+tmwcr1,tmcr2(a3) ; c2 in cont.,ext.clk,out en.
 move.b  #3,tmsbr2(a3)              ; 3 -> msb cr2.
 move.b  #$a,tml2(a3)               ; $a -> lsb cr2 : 500hz clock.
 move.b  #tmshgwr+tmie+tmirb,tmcr1(a3) ; c1 in single sh.- ext clk
 clr.b   tmsbr1(a3)                 ; 0 -> msb cr1
 move.b  #$32,tml1(a3)              ; 32 -> lsb cr1 : 100ms delay.
 move.b  #tmshgwr+tmie,tmcr1(a3)    ; start count.
 end
```

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3.8.2 - Serial ports

The TSVME110 board has two serial ports, accessible from two 9-pin SUBD connectors on the front panel (J2, J1) and from the P2 connector. One of the uses of these ports consists in connecting a terminal onto one channel and a development system onto the other, thus allowing the user to download and debug application programs independently of other boards on the bus.

Channel 1:

Channel 1 is an asynchronous RS232C channel carrying the four lines below:

TxD	Transmit data
RxD	Receive data
RTS	Request to send
CTS	Clear to send

Selector F2 configures channel 1 for modem or terminal.

Channel 2:

Channel 2 may be configured either for RS232C operation or to take TTL-level signals. It can also be set to operate in synchronous or asynchronous mode. It carries the seven lines below:

TxD	Transmit data
RxD	Receive data
RTS	Request to send
CTS	Clear to send
TxC	Transmit clock
RxC	Receive clock
DCD	Data carrier detect

Whether channel 2 acts as an RS232C or a TTL port depends on the settings of selectors F4, F5 and F22 and whether or not chips are fitted at IC2 and IC13.

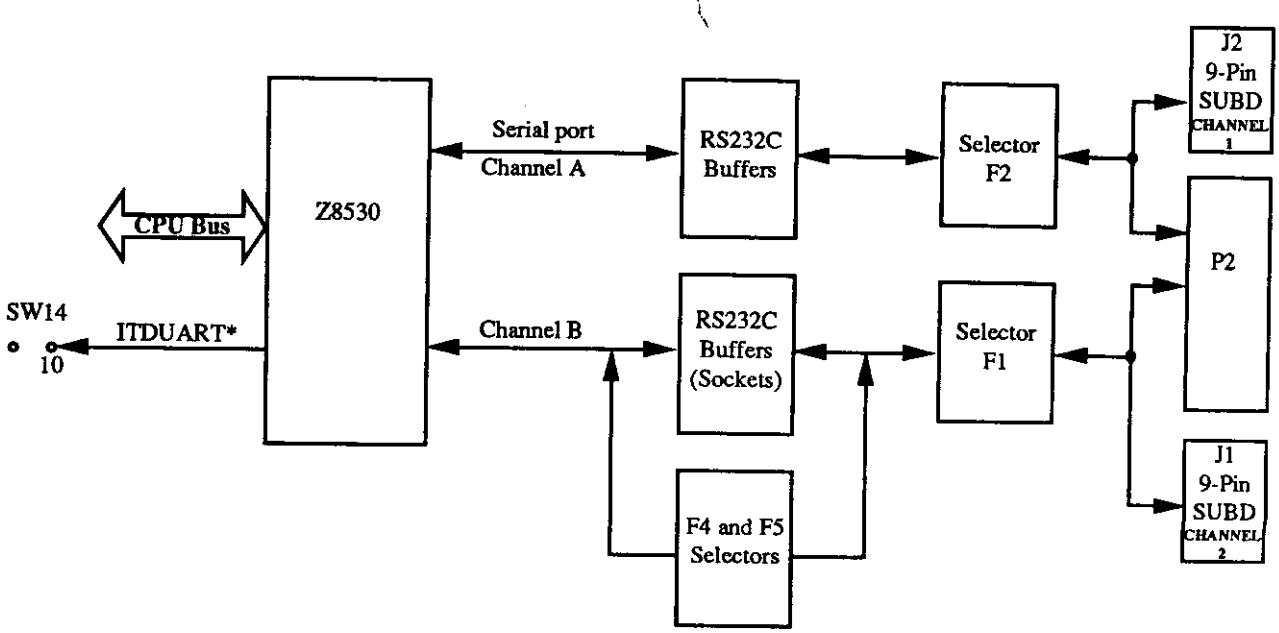
Selector F1 configures channel 2 as modem or terminal.

Selector F7 selects the channel 2 clock: "on-board 2.4576 MHz" or "external clock".

Selectors F22 and F23 configure the TRXCB pin on the Z8530 chip as input or output.

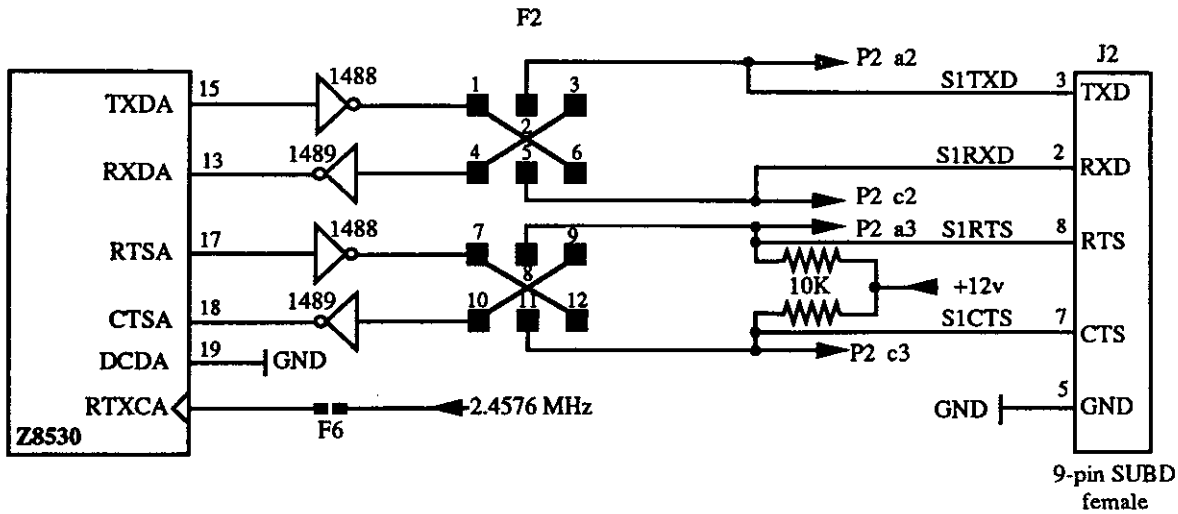
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Fig. 3.10 : Serial ports - block diagram



3.8.2.1 - Configuration of serial port channels

Fig. 3.11 : Configuration of channel 1

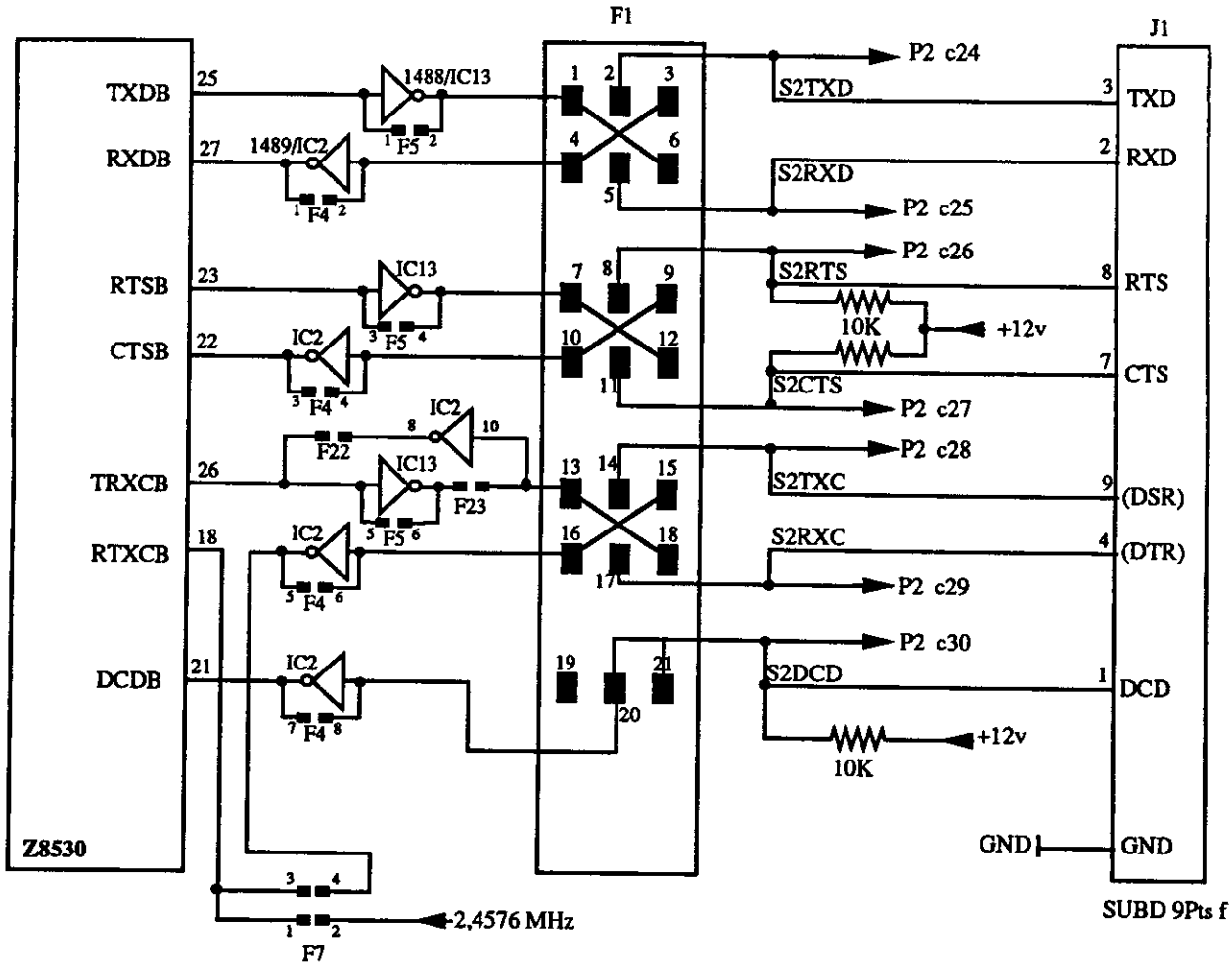


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Signal	Pin J2	Pin P2	TX	RX
S1TXD	3	a2	F2 : 1-2	F2 : 2-3
S1RXD	2	c2	F2 : 5-6	F2 : 4-5
S1RTS	8	a3	F2 : 7-8	F2 : 8-9
S1CTS	7	c3	F2 : 11-12	F2 : 10-11

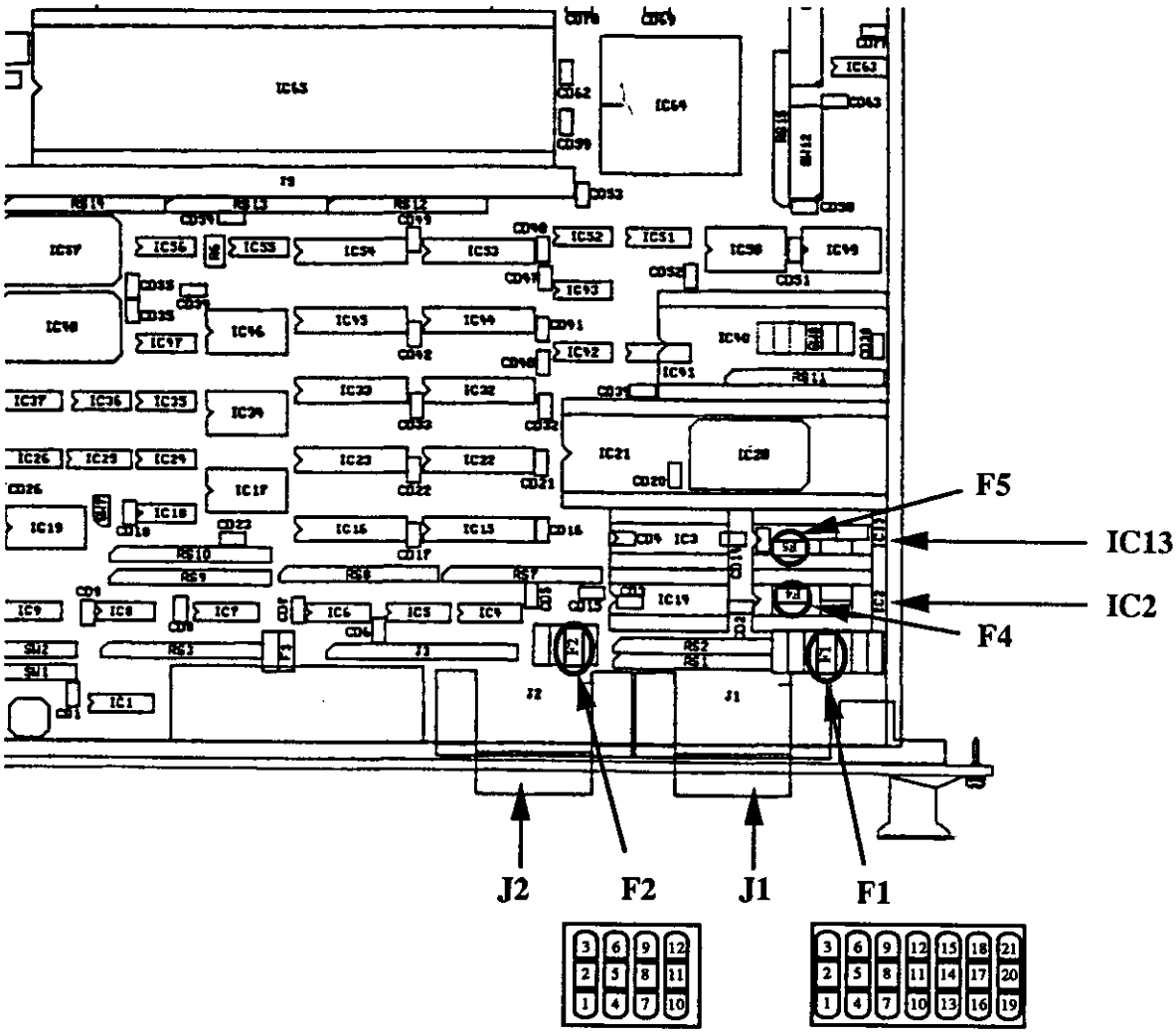
Solder bead F6, used for automatic testing purposes, is factory set with the link made. Channel A receives a basic clock frequency of 2.4576 MHz on RTXCA. This hardware configuration must be taken into account during initialization of channel A.

Fig. 3.12 : Configuration of channel 2

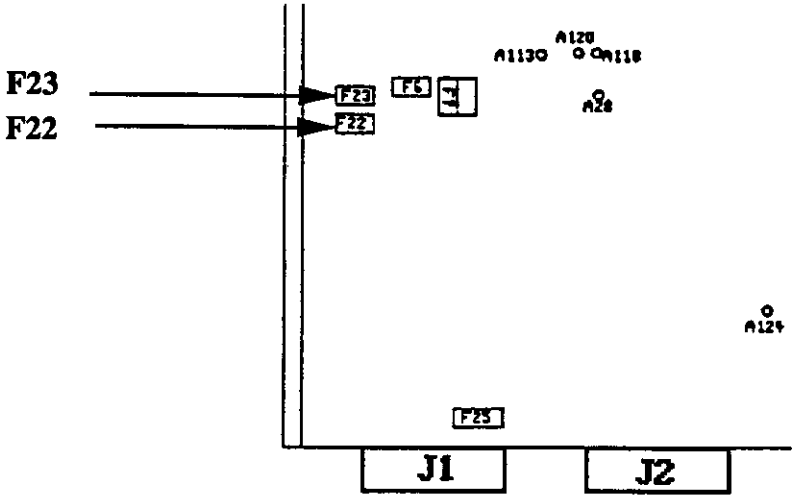


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Location of J1, J2, F1, F2, F4, F5, IC13 and IC2



Location of F22 and F23



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- Signal directions on J1 and P2 - F1 selector

Output signal	J1 pin	P2 pin	TRANSMISSION F1 link	TRANSMISSION Z8530 signal	RECEPTION F1 link	RECEPTION Z8530 signal
S2TXD	3	C24	1-2	TXDB	2-3	RXDB
S2RXD	2	C25	5-6	TXDB	4-5	RXDB
S2RTS	8	C26	7-8	RTSB	8-9	CTSB
S2CTS	7	C27	11-12	RTSB	10-11	CTSB
* S2TXC	9	C28	13-14	TRXCB	14-15	RTXCB
* S2RXC	4	C29	17-18	TRXCB	16-17	RTXCB
S2DCD	1	C30			20-21	DCDB

(*) With F22 solder bead open circuit and F23 solder bead closed circuit, for either RS232C or TTL port.

It is also possible to wire S2RXC to RTXCB incoming and S2TXC to TRXCB also incoming. This is done using the same F1 configuration, with S2TXC to TRXCB (F1 link 13-14) and S2RXC to RTXCB (F1 link 16-17), but with F22/F23 settings as follows:

RS232C:
-> unwire F23 solder bead and wire F22

TTL:
-> leave F23 wired and F22 unwired

Note: TRANSMISSION/RECEPTION links are mutually exclusive.

- RS232C / TTL signal levels (IC2, IC13, F4 , F5 and F22)

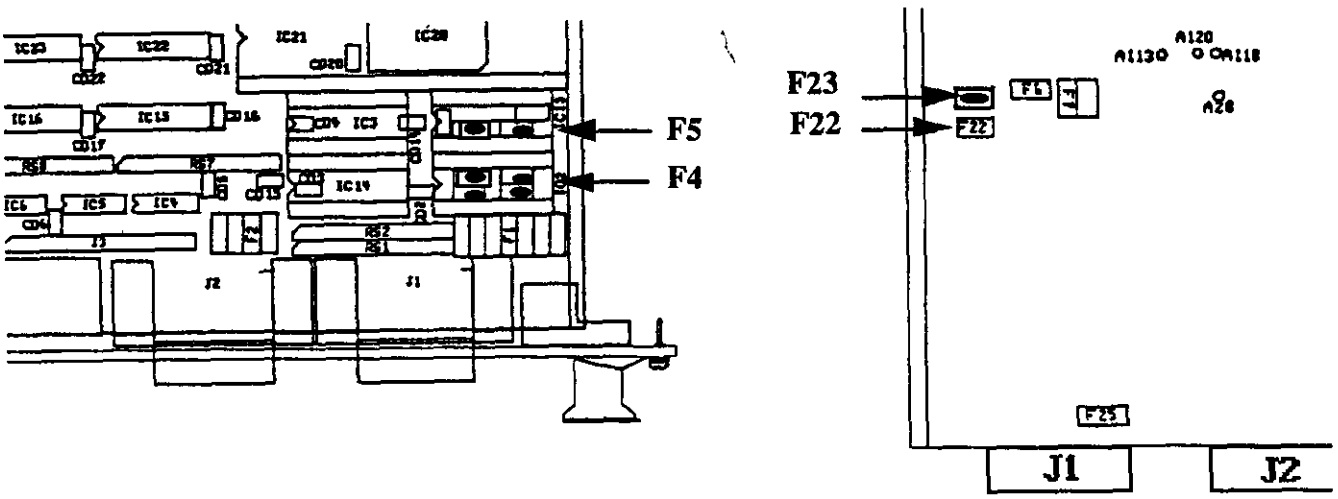
The channel 2 RS232C drivers are socket-mounted, with solder beads located below the sockets: F4 under IC2; F5 under IC13.

As standard, channel 2 is configured as a RS232C port, i.e. with a 1488 chip fitted at IC13, a 1489 chip at IC2, and no links made on solder beads F4 and F5.

However, the user may wish to install a different type of serial port on channel 2, by adding an external differential module, say. In this case the channel 2 input and output signals should be configured for TTL levels.

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TTL configuration is obtained with the 1488 and 1489 chips absent from sockets IC13 and IC2, the F22 solder bead unwired, and solder beads F4, F5 and F23 wired as follows:



- Channel B clock - F7 selector

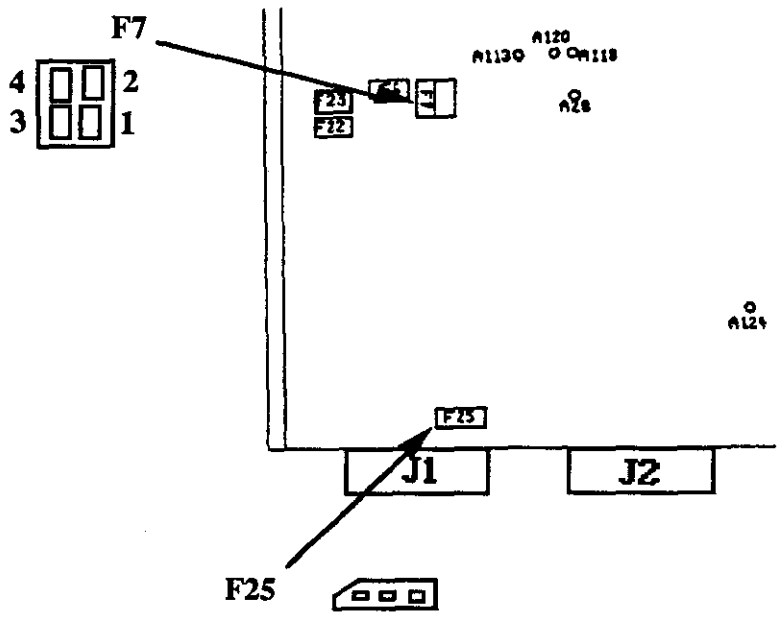
The channel B clock may be chosen from the following:

. on-board 2.4576 MHz clock (asynchronous mode): F7 link 1-2 set

. external clock from P2 pin c29 or J1.4 (synchronous mode): F7 link 3-4 set.

Solder bead F7 is located on the soldered side of the board beneath IC21 (Z8530).

Location of F7 and F25 :



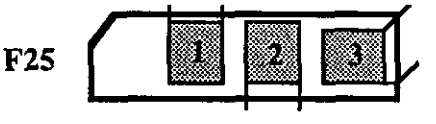
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Grounding the housing of serial I/O connectors

The TSVME110 board circuity includes a screening line that is connected through to the housing and the fixations for the serial I/O connectors. You can wire this screening line either to the signal ground or to the frame ground (via the front panel, provided the board is fitted with the required metallic grounding eyelets).

You wire the screening line to the required ground by simply making solder bridges between the appropriate contacts on the W2 selector, located on the soldered side of the board.

1. Connected through to front panel fixing eyelets (frame ground)
2. Connected through to screening line (housing and fixations of serial I/O connectors)
3. Connected through to signal ground.



- Connections on P2

Channel 1		Channel 2	
S1TXD	P2.a2	S2TXD	P2.c24
S1RxD	P2.c2	S2RXD	P2.c25
S1RTS	P2.a3	S2RTS	P2.c26
S1CTS	P2.c3	S2CTS	P2.c27
		S2TXC	P2.c28
		S2RXC	P2.c29
		S2DCD	P2.c30

Z8530 - PROGRAMMING EXAMPLE

The programming example below first sets out the Z8530 programming model used. The program resembles that which is executed during the board self-test. Both serial ports are reinitialized before returning to TSVBUG.

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```
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**********************************
* Duscc z8530 programming model
*       on tsvme 110.
**********************************
*
duart   equ     $f80001 ; z8530 base addr.
*    duscc registers :
*
*       offsets / duart - base addr.
*
scca    equ     4       ; channel a.
sccb    equ     0       ; channel b.
sccd    equ     2       ; offset cmd/data registers in 2 channels.
*
* write registers :
*
*wr0    equ     0       ; command register
*
R0      equ %00000000
R1      equ %00000001
R2      equ %00000010
R3      equ %00000011
R4      equ %00000100
R5      equ %00000101
R6      equ %00000110
R7      equ %00000111
R8      equ %00001000
R9      equ %00001001
R10     equ %00001010
R11     equ %00001011
R12     equ %00001100
R13     equ %00001101
R14     equ %00001110
R15     equ %00001111
*
* wr1 :
*
wdmarqen equ %10000000  ; wait/dma request enable.
wdmarqfn equ %00000001  ; wait/dma request function.
wdmarqrt equ %00000010  ; wait/dma request on rec or trans.
rxid    equ  %00000000  ; receive interrupt disable.
rxiof   equ  %00001000  ; receive int. on first char or spec.condit.
rxioa   equ  %00010000  ; receive int. on all char or spec.condit.
rxios   equ  %00011000  ; receive int. on spec.conditions only.
pisc    equ  %00000100  ; parity is special condition.
txie    equ  %00000010  ; transmitter interrupt enable.
esmien  equ  %00000001  ; external status master irq enable.
wr1std  equ  00         ; no irqs or dma.
*
* wr2 : irq vector register.(n.u on tsvme110).
*
```

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```
*
* wr3 : receiver parameters and control)
*
rxbpc8  equ %11000000   ; 8 bits per char.
rxbpc7  equ %01000000   ; 7 bits per char.
rxbpc6  equ %10000000   ; 6 bits per char.
rxbpc5  equ %00000000   ; 5 bits per char.
auto    equ %00100000   ; auto enable.
hunt    equ %00010000   ; enter hunt mode(sync).
rxcrc   equ %00001000   ; enable receiver crc.
adsch   equ %00000100   ; address search mode (sdlc).
sycli   equ %00000010   ; sych chsr load inhibit.
rxen    equ %00000001   ; receiver enable.
wr3std  equ rxbpc8+rxen ; 8 bits and receiver enable.
*
* wr4 : transmitter and misc receiver parameters.
*
cm64    equ %11000000   ; x64 clock mode.
cm32    equ %10000000   ; x32 clock mode.
cm16    equ %01000000   ; x16 clock mode.
cm01    equ %00000000   ; x01 clock mode.
sb1     equ %00000100   ; 1 stop bit.
sb15    equ %00001000   ; 1.5 stop bit.
sb2     equ %00001100   ; 2 stop bits.
penable equ %00000001   ; parity enable.
pev     equ %00000010   ; parity even.
podd    equ penable
peven   equ penable+pev
wr4std  equ cm16+sb1    ; 1 stop bit and x16 clock mode.
*
* wr5 : transmitter parameters and control.
*
dtron   equ %10000000   ; dtr is set (ie asserted low,cf wr14)
txbpc8  equ %01100000   ; 8 bits per char.
txbpc7  equ %00100000   ; 7 bits per char.
txbpc6  equ %01000000   ; 6 bits per char.
txbpc5  equ %00000000   ; 5 bits per char.
sdbrk   equ %00010000   ; send break (txd -) continuous 0)
txen    equ %00001000   ; transmitter enable.
rtson   equ %00000010   ; rts is set (ie 0 on output)
sd_crc  equ %00000100   ; sdlc*/crc16 crc polynomial used.(wr10)
tcrcen  equ %00000001   ; transmit crc enable.
wr5std  equ txbpc8+txen+rtson
*
* wr6 : sync characters or sdlc address field.(doc.7.1.7,fig 7-8)
*       not used in asynchronous mode.
*       - tx sync in momosync mode.
*       - 1rst byte of 16b-sync in external sync mode.
*       - secondary addr.field in sdlc modes.
*
```

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```
*
* wr7 : sync characters or sdlc flag.(doc.7.1.8,fig 7-9)
*       not used in asynchronous mode.
*       - rx sync in momosync mode.
*       - 2nd byte of 16b-sync in external sync mode.
*       - flag char. in sdlc modes.
*
* wr8 : transmit buffer.
*
* wr9 : master interrupt control.
*
sccrst  equ %11000000   ; force hardware reset.
sccrsta equ %10000000   ; force hardware reset on channel a.
sccrstb equ %01000000   ; force hardware reset on channel b.
sthl    equ %00010000   ; status high(v6-4):low(v1-3)rr2b.
mirq    equ %00001000   ; master irq enable.
novect  equ %00000010   ; no vector driven on ad(0-7) in iack*
vectist equ %00000001   ; vector includes status, depends sthl-)rr2b.
*
* wr10 : misc. tx/rx control bits.
*       not used in asynchronous mode.
*
crcpr   equ %10000000   ; set to 1 bits of crc generator/checker.
trnrz   equ %00000000   ; nrz  data encoding on tx and rx.
trnrzi  equ %00100000   ; nrzi  data encoding on tx and rx.
trfm1   equ %01000000   ; fm1  data encoding on tx and rx.
trfm0   equ %01100000   ; fm0  data encoding on tx and rx.
gaop    equ %00010000   ; go active on poll.(loop mode)
mkfgi   equ %00001000   ; mark/flag* idle.
abfgou  equ %00000100   ; abort/flag* on underrun.
loopm   equ %00000010   ; loop mode, sdlc mode.
sync6   equ %00000001   ; 6bits sync / else 8bits sync.
*
* wr11 : clock mode control.
*
* bit 7 = 0 -) no xtal - rtxc = ttl level clock.
*
rxcdpl  equ %01100000   ; rxc = dpll out.
rxcbrd  equ %01000000   ; rxc = baud rate
```

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```
*
* wr12 : time constant, lower byte.
*
brg384  equ 0    ; 38400 bauds for x16 on 2.4576mhz. (wr13std)
brg192  equ 2    ; 19200 bauds   "    "    "      "          "     .
brg96   equ 6    ; 9600 bauds    "    "    "      "          "     .
brg48   equ $e   ; 4800 bauds    "    "    "      "          "     .
brg24   equ $1e  ; 2400 bauds    "    "    "      "          "     .
brg12   equ $3e  ; 1200 bauds    "    "    "      "          "     .
brg6    equ $7e  ; 600 bauds     "    "    "      "          "     .
brg3    equ $fe  ; 300 bauds     "    "    "      "          "     .
brg151  equ $fe  ; 1500 bauds    "    "    "      "       (wr13=1).
*
wr12std equ brg96 ; 9600 bauds x16 on 2.4576mhz.
*
* wr13 : time constant, upper byte.
*
brg15h  equ 1    ; 1500 bauds for x16 on 2.4576mhz,wr12=brg151.
wr13std equ 0    ; 9600 bauds x16 on 2.4576mhz.
*
* wr14 : miscellaneous control bits.
*
snrzi   equ %11100000   ; set nrzi mode on dpll.
sfm     equ %11000000   ; set fm mode on dpll.
ssrtx   equ %10100000   ; set source = rtxc on dpll.
ssbrg   equ %10000000   ; set source = brg on dpll.
didpll  equ %01100000   ; disable dpll.
lcloop  equ %00010000   ; local loopback.
auten   equ %00001000   ; auto enable mode (test).
dtrrq   equ %00000100   ; dtr/request function. (see dtr in wr5).
sbrgpc  equ %00000010   ; brg source = pclk input/else rtxc.
brgen   equ %00000001   ; brg enable.
*
wr14std equ brgen               ; brgin=rtxc,brg enable.
*
* wr15 : external/status interrupt control.
*        if ext/status conditions are enabled in wr1.
*
brkabie equ %10000000   ; break/abort it.en.
txunie  equ %01000000   ; change on txunderrun/eom latch it.en.
ctsie   equ %00100000   ; cts it.en.
syncie  equ %00010000   ; sync.pin or state in hunt change it.en.
dcdie   equ %00001000   ; dcd it.en.
zcntie  equ %00000010   ; zero count it.en.
*
```

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```
*  read registers.
*
* rr0 : transmit/receive buffer status and external status.
*
brkab   equ %10000000   ; break/abort.
txun    equ %01000000   ; change on txunderrun/eom latch.
cts     equ %00100000   ; cts.
sync    equ %00010000   ; sync.pin or state in hunt change.
dcd     equ %00001000   ; dcd.
txemp   equ %00000100   ; tx buffer empty.
zcnt    equ %00000010   ; zero count.
rxaval  equ %00000001   ; rx char. available.
*
rx_bit  equ 0
tx_bit  equ 2
dcd_bit equ 3
cts_bit equ 5
*
* rr1 : add.transmit/receive buffer status and external status.
*
eof     equ %10000000   ; end of frame.(sdlc)
crcfer  equ %01000000   ; crc / framing error.
rxover  equ %00100000   ; receiver overrun error.
parer   equ %00010000   ; parity error.
mifld   equ %00001110   ; residue codes(2-0) 1-field sel.
allst   equ %00000001   ; all sent (async.mode)
*
* rr2 : interrupt vector written in wr2.
*       rr2b(channel b) include status information
*           on bits 1-2-3 or 6-5-4 (see sth1 in wr9).
* rr3 : interrupt pending register.
*       channel a only.
*       rr3b = 00.
* rr8 : receive data register.
*
* rr10 : miscellaneous status bits, not used in async.mode.
*
ckmis1  equ 7   ; one clock missing bit.
ckmis2  equ 6   ; two clock missing bit.
loopsd  equ 4   ; in sdlc mode,=1 when tx controls the loop.
onloop  equ 1   ; in sdlc mode,=1 when tx is active.
*
* rr12 : brg time constant, lower byte. (wr12)
* rr13 : brg time constant, upper byte. (wr13)
* rr15 : ext/status irq enable register. (wr13)
*                   see wr13 for bit values.
*
```

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```
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**********************************
* duscc z8530                    *
*            2 channels test     *
*            in local loopback   *
* 03/05/89   jgb                 *
**********************************
*       status in memory :
dusccsta equ    $27f0   := 16b word : hbyte - ch.a / lbyte - ch.b
*
duscctst equ    *
        lea     dusccsta,a1     ; status word in memory
        move.l  #4,d1           ; channel a test.
        clr.l   d2              ; status register
        bsr     duscct
        move.b  d2,(a1)         ; ch.a status -) dusccsta h.
        clr.l   d1              ; channel b test.
        clr.l   d2              ; status register
        bsr     duscct
        move.b  d2,1(a1)        ; ch.b status -) dusccsta l.
        jsr     $ec006c         ; vbug ch.1 init.function
        jsr     $ec0070         ; vbug ch.2 init.function
        trap    #15
        dc.w    0               ; return to vbug.
*
*
```

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```
*
* duscct -
*       test of a channel for non-interrupt i/o and local loopback.
*       input  : d1.b = channel number.
*       output : d2.b = channel test status :
*                       = 1 , time out on tx_bit
*                       = 2 ,  "    "  "  rx_bit
*                       = 4 , verify error : tx = rx.
*
duscct  lea     duart,a3                ; a3 = duscc addr.
*
        move.b  #R0,(a3,d1.w)
        move.b  #R9,(a3,d1.w)           ; master it control.
        move.b  (a3,d1.w),d2
        move.b  #R9,(a3,d1.w)           ; master it control.
        move.b  #sccrsta,d5
        tst.b   d1
        bne     dusct00                 ; branch if channel a.
        move.b  #sccrstb,d5
dusct00 move.b  d5,(a3,d1.w)            ; reset channel
        move.b  #R4,(a3,d1.w)           ; tx and rx parameters
        move.b  #wr4std,(a3,d1.w)       ; x16 clk,1 stop bit,no par.
        move.b  #R5,(a3,d1.w)           ; tx parameters and control.
        move.b  #wr5std-txen,(a3,d1.w)  ; 8 bit/txchar,txen,rtson,dcdon.
        move.b  #R3,(a3,d1.w)           ; rx parameters and control.
        move.b  #wr3std-rxen,(a3,d1.w)  ; 8 bit/rxchar,rxen.
        move.b  #R1,(a3,d1.w)           ; rx parameters and control.
        move.b  #wr1std,(a3,d1.w)       ; no irq or dma.
        move.b  #R9,(a3,d1.w)           ; master it control.
        move.b  #0,(a3,d1.w)            ; int.disabled
        move.b  #R10,(a3,d1.w)          ; misc. tx and rx controls.
        move.b  #trnrz,(a3,d1.w)        ; nrz
        move.b  #R11,(a3,d1.w)          ; clock mode control.
        move.b  #wr11std,(a3,d1.w)      ; rxc=txc=trxc*=brgout,rtxc=ttl in
        move.b  #R12,(a3,d1.w)          ; baud rate gen.time constant low
        move.b  #wr12std,(a3,d1.w)      ; 9600 bauds x16 on 2.4576Mhz.
        move.b  #R13,(a3,d1.w)          ; baud rate gen.time constant high
        move.b  #wr13std,(a3,d1.w)      ; 9600 bauds x16 on 2.4576Mhz.
        move.b  #R14,(a3,d1.w)          ; misc. control bits.
        move.b  #lcloop,(a3,d1.w)       ; dpll source=brg, brgin=rtxc,brg en.
*
        move.b  #R14,(a3,d1.w)          ; misc. control bits.
        move.b  #brgen+lcloop,(a3,d1.w) ; dpll source=brg, brgin=rtxc,brg en.
        move.b  #R5,(a3,d1.w)           ; tx parameters and control.
        move.b  #wr5std,(a3,d1.w)       ; 8 bit/txchar,txen,rtson,dcdon.
        move.b  #R3,(a3,d1.w)           ; rx parameters and control.
        move.b  #wr3std,(a3,d1.w)       ; 8 bit/rxchar,rxen.
*
        move    #8,d4
        move    #$20,d5
        move    d4,d0
*
duscct0 moveq.l #-1,d3
        cmp.b   #8,d0
        beq     duscc00                 ; tx char d5.
```

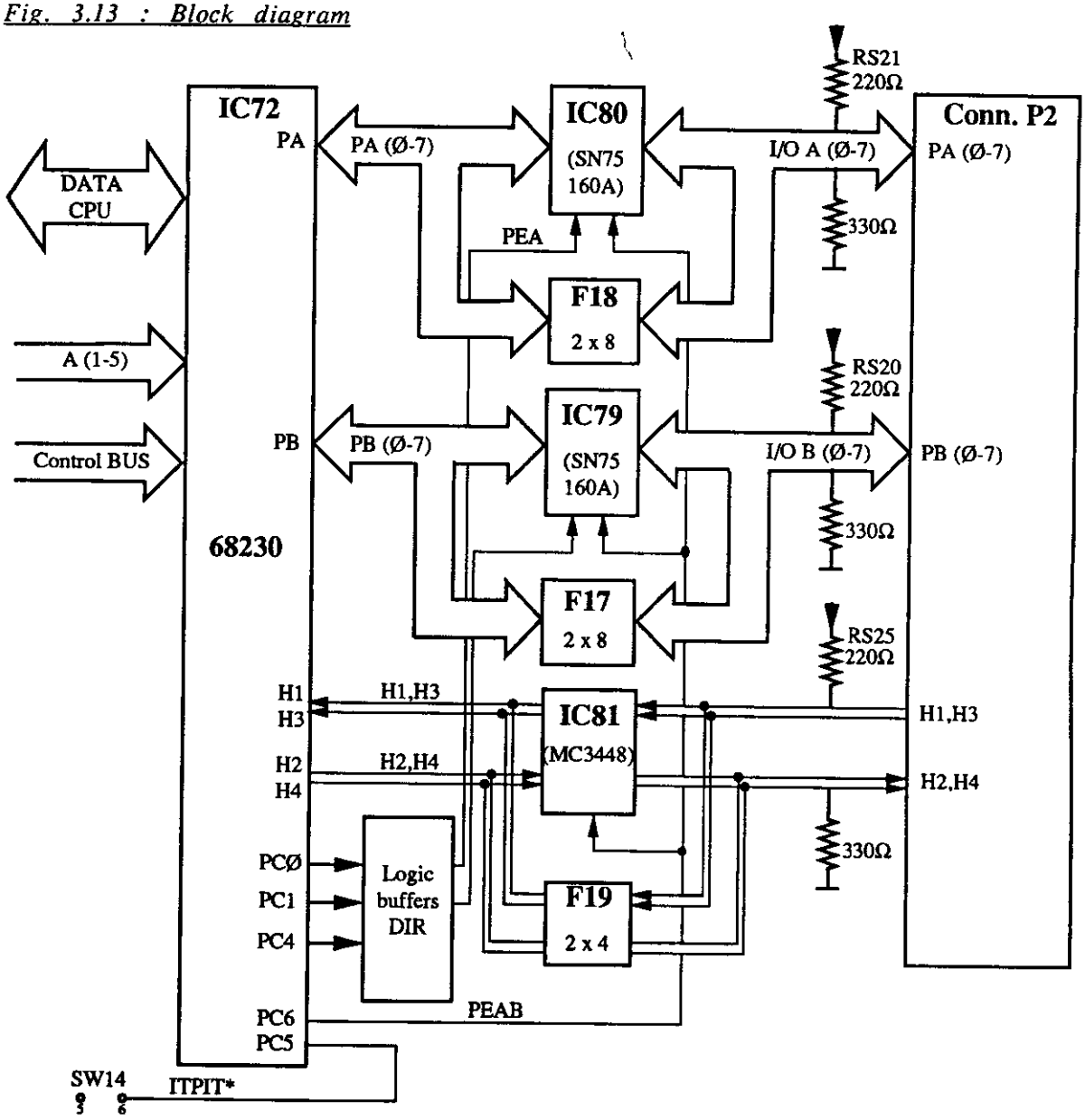
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```
          move.b   d4,d0                  ; send back space.
          bra      duscct1
duscc00   move.b   d5,d0
duscct1   move.b   #R0,(a3,d1.w)
          move.b   (a3,d1.w),d6
          btst     #tx_bit,d6
          bne      duscct2                ; branch if tx_buffer empty
          dbra     d3,duscct1             ; poll -> tempo end
          bra      duscer1                ; time out on tx_bit
duscct2   move.b   d0,sccd(a3,d1.w)       ; write char.
*
          moveq.l  #-1,d3
duscct3   move.b   #R0,(a3,d1.w)
          move.b   (a3,d1.w),d6
          btst     #rx_bit,d6
          bne      duscct4                ; branch if so.
          dbra     d3,duscct3             ; poll -> tempo end
          bra      duscer2                ; time out on rx_bit
duscct4   move.b   sccd(a3,d1.w),d3       ; get data
*
          cmp.b    d0,d3
          bne      duscer3                ; verify error.
*
          move     #10000,d3
duscct5   nop
          dbra     d3,duscct5
*
          cmp.b    #8,d0
          bne      duscct0                ; clear sent char.
          addq.b   #1,d5
          cmp.b    #$7f,d5
          bne      duscct0                ; next char. if < $80
*
          rts
*
duscer1   move.b #1,d2
          rts
*
duscer2   move.b #2,d2
          rts
*
duscer3   move.b #4,d2
          rts
*
          end
```

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3.8.3 - Parallel ports

Fig. 3.13 : Block diagram



As standard, the TSVME110 board has two 8-bit parallel ports managed by a 68230 PIT. In non-buffered configuration, ports A and B, together with latch signals H1, H2, H3, H4, are taken onto the P2 connector via solder beads F18, F17 and F19. In buffered configuration, SN75160A and MC3448 interface chips are fitted in sockets IC80/79/81, and the F17/18/19 links are open-circuit.

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3.8.3.1 - 68230 PIT

BASE ADDRESS : $F90001

$F9 0001	PGCR	Port General Control Register
$F9 0003	PSRR	" Service Request "
$F9 0005	PADR	" A Data Direction "
$F9 0007	PBDR	" B " " "
$F9 0009	PCDR	" C " " "
$F9 000B	PIVR	" Interrupt Vector "
$F9 000D	PACR	" A Control "
$F9 000F	PBCR	" B " "
$F9 0011	PADR	" A Data "
$F9 0013	PBDR	" B " "
$F9 0015	PAAR	" A Alternate "
$F9 0017	PBAR	" B " "
$F9 0019	PCDR	" C Data "
$F9 001B	PSR	" status "
$F9 001D	-	
$F9 001F	-	
$F9 0021	TCR	Timer control "
$F9 0023	TIVR	Timer interrupt vector Register
$F9 0025	-	
$F9 0027	CPRH	Counter Preload Register High
$F9 0029	CPRM	" " " Middle
$F9 002B	CPRL	" " " Low
$F9 002D	-	
$F9 002F	CRH	Count Register High
$F9 0031	CRM	" " Middle
$F9 0033	CRL	" " Low
$F9 0035	TSR	Timer Status Register
$F9 0037		
$F9 003F		

The PIT clock is at 8 MHz.

With interface buffer chips fitted at IC80, 79 and 81, ports A and B (and latch signals H1-H4) support PIT operating modes with the following restrictions:

- available modes:
  modes 0 and 1 : 8-/16-bit one-way
  mode 3 : 16-bit two-way
  Port A cannot be used in mode 2.

- H1 and H3 fixed as inputs
  H2 and H4 fixed as outputs

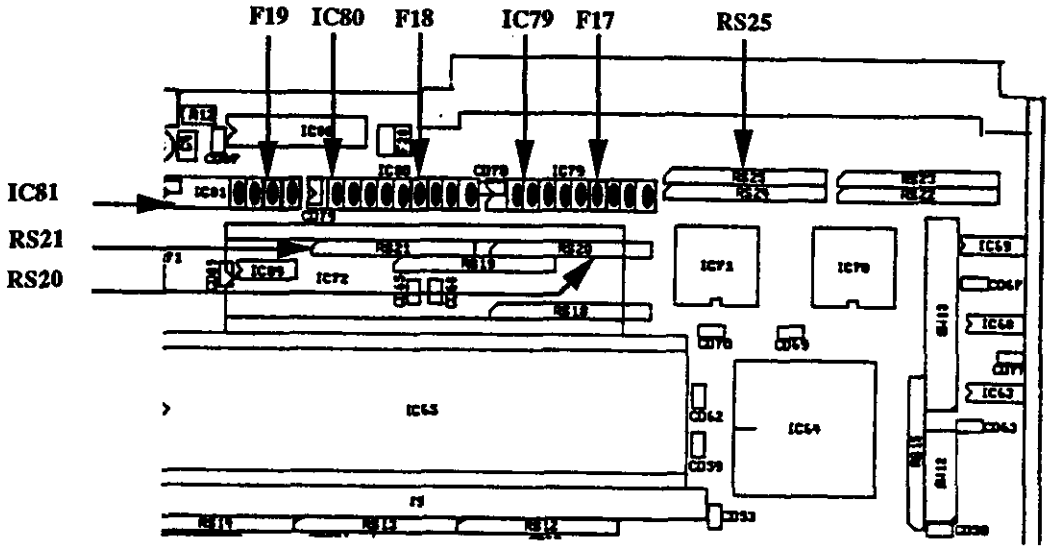
- Part of port C (PC0, PC1, PC4 and PC6) is used for controlling the port A and B buffers and the latch signals H1-H4.

PC5 is used as the PIT interrupt line.
PC2, PC3 and PC7 are not used.

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3.8.3.2 - Parallel ports: configurations available

(1) Non-buffered configuration: PIT I/Os on P2



Locations IC80, IC79 and IC81 hold empty sockets only; no buffer chips SN75160A and MC3448 are fitted on the TSVME110 board.

F18, F17 and F19 links are closed-circuit.

220-/330-ohm terminating resistance networks are not fitted at RS21, 20 and 25.

In non-buffered configuration, PC0, PC1, PC4 and PC6 are inoperative and all PIT operating modes are available.

(2) Buffered configuration

In buffered configuration, an MC3448 chip is fitted at IC81 and SN75160A chips are fitted at IC80 and IC79. Any solder beads links which might previously have been made at F18, F17 and F19 must be removed before these chips are fitted.

In buffered configuration, lines PC0, PC1, PC4 and PC6 are used for controlling the port A and B buffer directions in one-way (independent) mode or two-way 16-bit mode, and for controlling the type of output (three-state/open collector) for the buffers and the H2 and H4 latch signals on the MC3448.

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Note:

If mode 2 (port B two-way 8-bit) is used in buffered configuration, the 75160A chip at IC80 (Port A) must imperatively be removed. If this is done, the user may remake the F18 links to take the port A inputs/outputs directly out onto P2.

Port C is set as an input after a PIT reset (hardware or software). The port C lines which are used for parallel port control (PC0, PC1, PC4 and PC6) are kept high by pull-up resistors to Vcc.

- PC 0 : port A direction : modes 0 and 1

- PC 1 : port B direction : modes 0 and 1

- PC 4 : one-way / two-way (mode 3)
  = 1 : ports A and B one-way - controlled by PC0/1
  = 0 : ports A and B two-way - controlled by H1 (mode 3 only)

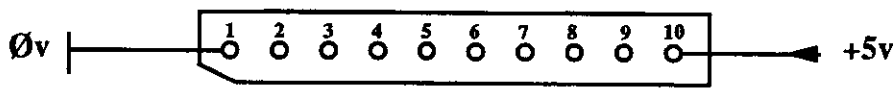
- PC6 : PEABC
  = 1: three-state signals on ports A and B and latch signals H2 and H4
  = 0: open-collector signals on ports A and B and latch signals H2 and H4

PC 0/1 DIR A/B	PCH 2-WAY	H1	TEA/B	FUNCTION	PIT MODE
1	1	X	0	Port A/B incoming	0 or 1
0	1	X	1	Port A/B outgoing	0 or 1
X	0	1	0	Ports A and B incoming	\ 3
X	0	0	1	Ports A and B outgoing	/

3.8.3.3 - Terminating networks

Locations RS20, 21 and 25 take resistance bridge terminating networks, with pin 1 connected to 0V and pin 10 to the +5V supply.

If the user wishes to install 9-pin networks for eight +5V pull-up resistors, these should be connected with the component pin marked "1" wired to socket pin number 10:



Wiring for RS21, 20 and 25

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3.8.3.4 - Connections on P2

Port A	I/OA 0	P2.a4
	I/OA 1	P2.c4
	I/OA 2	P2.a5
	I/OA 3	P2.c5
	I/OA 4	P2.a6
	I/OA 5	P2.c6
	I/OA 6	P2.a7
	I/OA 7	P2.c7
Port B	I/OB 0	P2.a9
	I/OB 1	P2.c9
	I/OB 2	P2.a10
	I/OB 3	P2.c10
	I/OB 4	P2.a12
	I/OB 5	P2.c12
	I/OB 6	P2.a13
	I/OB 7	P2.c13
Control	I/OH 1	P2.a8
	I/OH 2	P2.c8
	I/OH 3	P2.a14
	I/OH 4	P2.c14

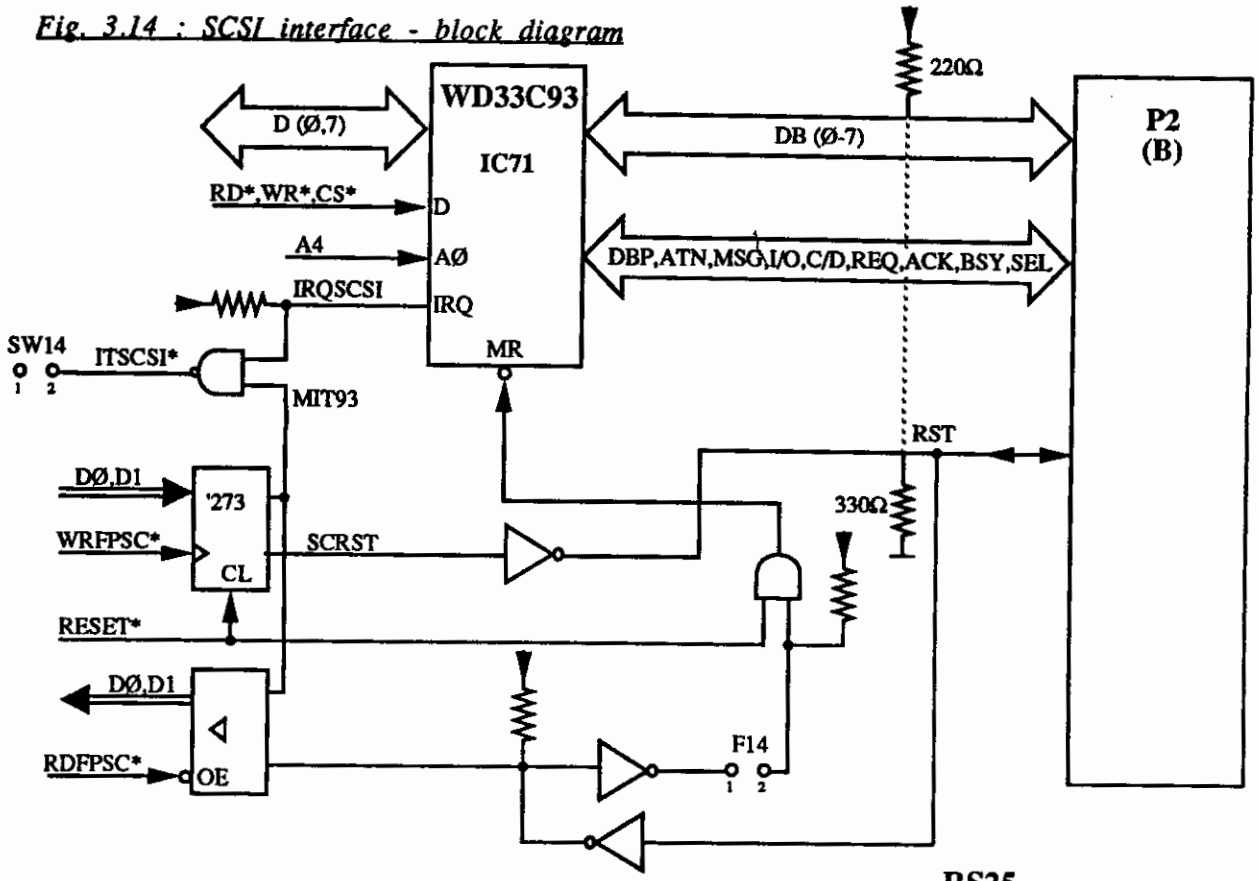
3.8.4 - SCSI bus controller option

With this option the TSVME110 board incorporates a WD33C93A SCSI controller and two bits are taken up in the optional SCSI/floppy interface control and status register (see § 3.5.5).

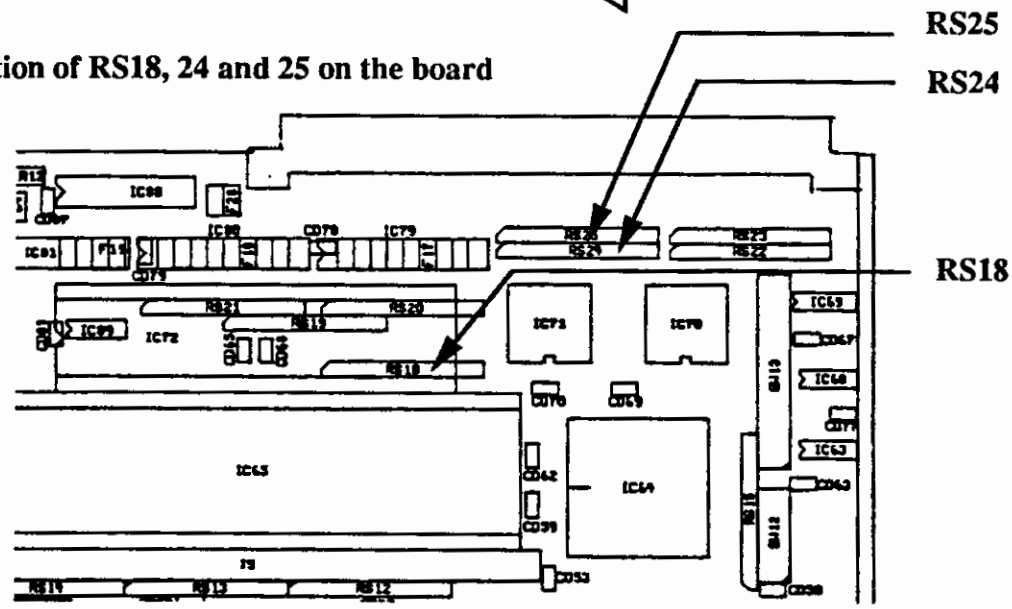
Connection onto the SCSI bus is via row B of the P2 connector. The F24 solder bead allows the SCSI : REQ connection onto P2. b22 or P2.b29

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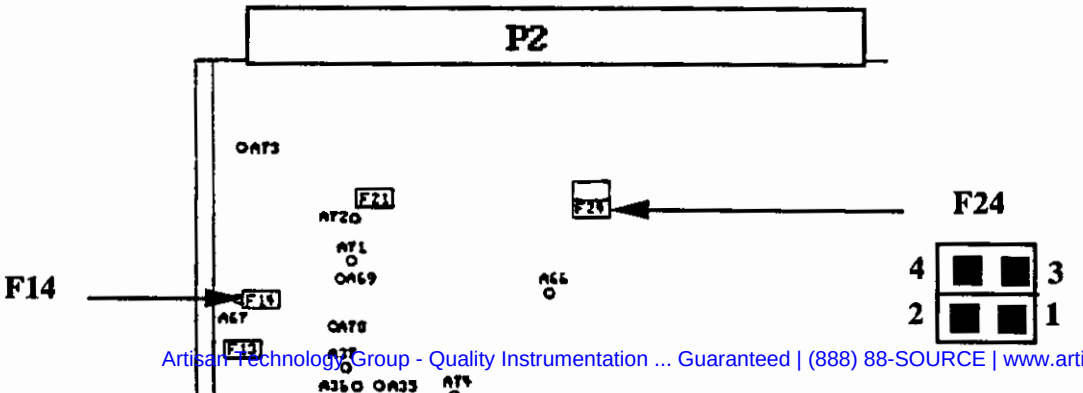
Fig. 3.14 : SCSI interface - block diagram



Location of RS18, 24 and 25 on the board



Location of F14 and F24 on the board



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3.8.4.1 - WD33C93 controller

On the TSVME110 board, the WD33C93 controller provides direct management of all SCSI signals except RST. It complies fully with ANSI SCSI X3T9.2 specifications and implements all SCSI bus features: arbitration; disconnect; reconnect; parity; synchronous data transfers up to 4 Mbytes/second with offset programmable from 1 to 5. However, on the TSVME110 board the controller is operated at a transfer rate lower than 0.5 Mbytes/second, as accesses are made in programmed mode.

The WD33C93 controller can be used as host (initiator) adaptor or peripheral (target) adaptor.

CPU interface:

The interface with the CPU consists of the following:

- Data bits D0 to D7
- Control signals CSSCSI*, RD*, WR* from decoding logic
- Address line A4, for distinguishing between accesses to the address register (W) and the auxiliary status register (RD) and distinguishing between accesses to the individual registers indexed by the address register
- Clock: 8 MHz
- Interrupt line: the WD33C93 controller IT line can be masked from bit 0 in the SCSI/floppy control and status register.
- Master Reset: The WD33C93 is reset by the TSVME110 board RESET* signal (hardware or software reset). It can also be reset by a reset on the SCSI bus, providing the F14 solder bead is set (operating in target environment).

Mapping: wired for indirect addressing mode

Address	R/W	Register accessed
$FDXX01	W	ADDRESS REGISTER
$FDXX01	R	AUXILIARY STATUS REGISTER
$FDXX11	R/W	INDIRECT ADDRESS REGISTERS 26 registers selected by the contents of the ADDRESS REGISTER

(see page 9 of WD33C93 data sheet)

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The WD33C93 interrupt request line is taken onto pin 2 of the local interrupt selector, SW14.

3.8.4.2 - SCSI/floppy control and status register - SCSI part

Address : $FBXXX5

bit D0 : SCRST SCSI bus reset
bit D1 : MIT93 WD33C93A interrupt mask

Write:

The control register is cleared by a board hardware or software reset and thereafter takes the values of bits d0 and d1 for each write to $FBXXX5.

bit d0 SCRST :

This signal is inverted to supply the SCSI bus RST signal:

= 0 SCSI bus RST deasserted
= 1 SCSI bus RST asserted

bit d1 MIT93 :

= 0 WD33C93 interrupt masked
= 1 WD33C93 interrupt enabled

Read: Status

bit d0 :

Status of SCSI bus RST signal (inverted)

= 0 SCSI bus RST deasserted
= 1 SCSI bus RST asserted

bit d1 : readback of MIT93 control register

Note : The SCSI bus supports multiple masters, and the TSVME110 board SCSI interface is able to act as target or initiator; it is therefore possible for the RST signal to be asserted by another master board.

3.8.4.3 - Terminating resistor networks

The TSVME110 board with SCSI option is supplied with 220-/330-ohm terminating networks fitted at R18, R24 and R25.

These networks must be removed if the board is not to occupy an end position on the SCSI bus.

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3.8.4.4 - P2 connections

Data bus	DB0*	P2.b4
	DB1*	P2.b5
	DB2*	P2.b6
	DB3*	P2.b7
	DB4*	P2.b8
	DB5*	P2.b9
	DB6*	P2.b10
	DB7*	P2.b11
Parity	DBP*	P2.b15
Control		
	ATN*	P2.b24
	MSG*	P2.b19
	I/O	P2.b23
	C/D	P2.b21
	REQ*	P2.b22 (F24 : 1-2) or P2.b29 (F24 : 3-4)
	ACK*	P2.b17
	BSY*	P2.b16
	SEL*	P2.b20
	RST*	P2.b18

3.8.5 - Floppy interface option

The TSVME110 board floppy interface is essentially controlled from the WD37C65 controller, with certain additional control functions performed by six bits in the SCSI/floppy control and status register. The SW13 selector configures the floppy interface seen from the P2 connector to match the type of floppy drive used. The F13 solder bead enables the "disk change" signal to be read on bit D7 of the operations register. The F21 solder bead sets the polarity of the floppy controller DRV input.

3.8.5.1 - WD37C65 floppy controller

The WD37C65 controller incorporates all the elements required for interfacing the CPU to a floppy drive: formatter/controller; data separation; write precompensation; selection of data transfer rate; clock generation; interface drivers and receivers; support for dual-speed motors.

The TSVME110 board implements all the main controller features, but with the following restrictions:

- DMA transfers are not used
- data transfer rates over the floppy interface are limited to 125, 250 or 500 Kbits/sec.

The SCSI/floppy control and status register sets the WD37C65 PCVAL input for a precompensation value of 125 ns or 187 ns and masks/enables the WD37C65 interrupt request line. This interrupt request line is taken onto pin 4 of the local interrupt selector, SW14.

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Mapping

Address	R/W	Access made
$FC0001	R	Read to main status register
$FC0001	W	Illegal
$FC0003	R	Read to data register
$FC0003	W	Write to data register
$FC0101	W	Write to control register
$FC0101	R	Read to control register
$FC0111	W	Write to operations register
$FC0111	R	Read to operations register DISK CHANGE on D7 with F13 set

3.8.5.2 - SCSI/floppy interface register - floppy interface part

Address $FBXXX5. The control register is cleared after a board hardware or software reset.

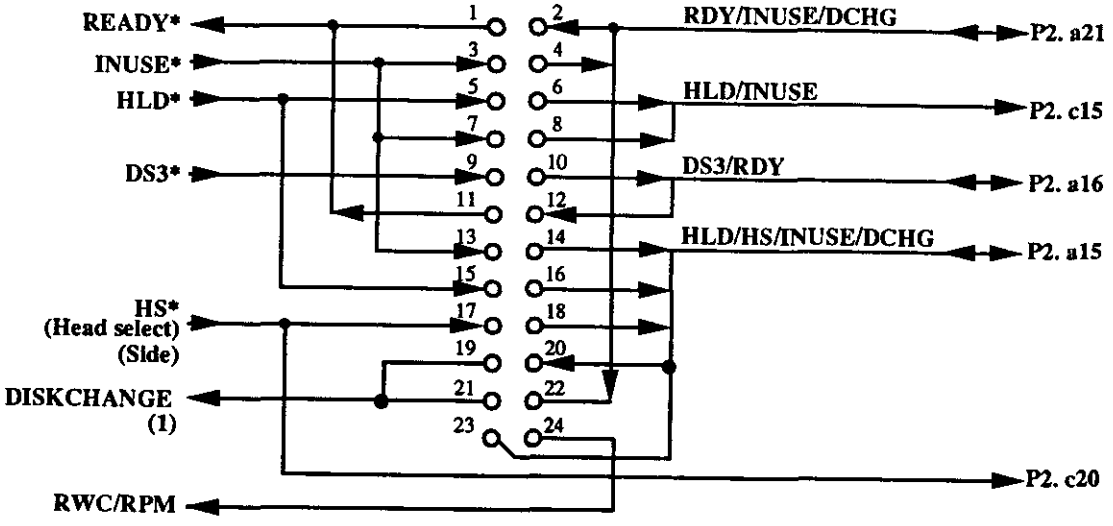
Bit	Write - Control	Read - Status
2	not used	IRQ65: WD37C65 IRQ line active at 1
3	FPCVAL: precompensation value = 0 187 ns = 1 125 ns	readback of FPCVAL
4	floppy interface INUSE* active at 0	readback of INUSE
5	floppy interface MOTOR ON* active at 0	readback of MOTORON
6	not used	floppy interface READY* active at 0
7	MIT65: WD37C65 IT mask = 0 IT masked = 1 IT enabled	readback of MIT65

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3.8.5.3 - Configuration of floppy interface - SW13, F13 and F21

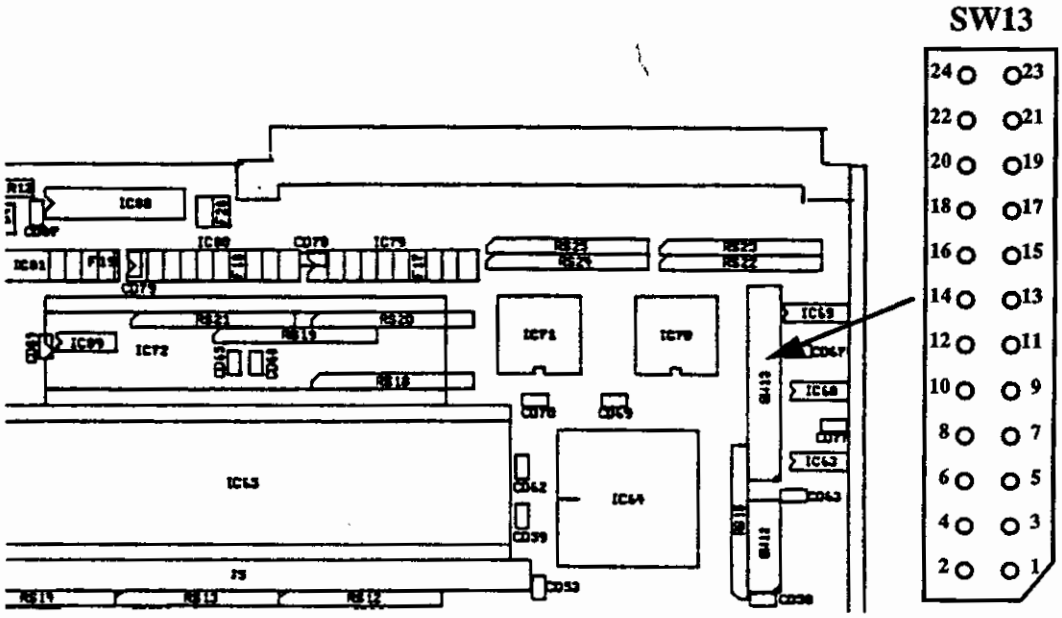
Selector SW13 configures the control signals on the pins of the P2 connector.

Fig. 3.15 : Wiring of SW13 selector

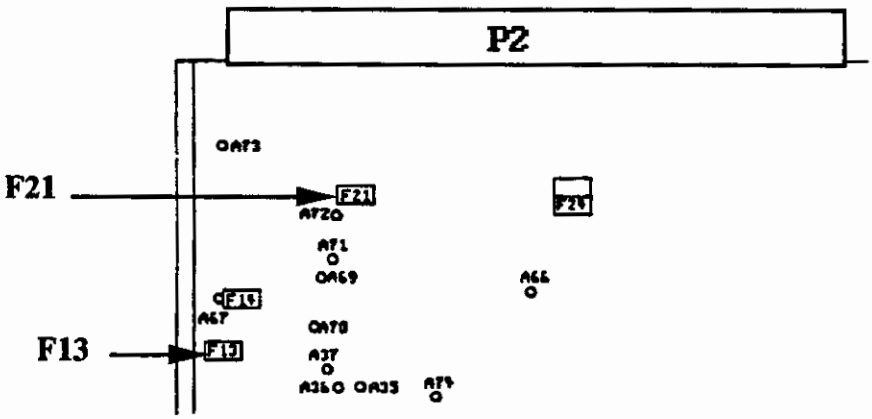


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LOCATION OF SW13 ON TSVME110 BOARD



LOCATION OF F21 AND F13 ON TSVME110 BOARD (soldered side)



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Examples of floppy interfaces for different drives, showing links between P2 connector and 34-pin floppy connector as configured from SW13:

pin on P2	pin on floppy connector	TEAC 5" SHUGART MITS	YEDATA 5"	YEDATA 3"	TEAC 3" FD235F	BASF	QUME	TEAC FD-235AF
a15	2	SPARE	SPARE	SPARE	READY*/ DISK CHANGE	HLD*		HIGH DENSITY/ DISK CHANGE*
c15	4	INUSE*	HLD*	INUSE*	OPEN		INUSE*	OPEN
a16	6	DS3*	DS3*	DS3*	DS3*	READY*	DS3*	RESERVED
b25	8	INDEX*	INDEX*	INDEX*	INDEX*	INDEX*	INDEX*	INDEX*
c16	10	DSO*	DSO*	DSO*	DSO*	DSO*	DSO*	DS0*
a17	12	DS1*	DS1*	DS1*	DS1*	DS1*	DS1*	DS1*
c17	14	DS2*	DS2*	DS2*	DS2*	DS2*	DS2*	RESERVED
a18	16	MOTON*	MOTON*	MOTON*	MOTON*	MOTON*	MOTON*	MOTON*
c18	18	DIR*	DIR*	DIR*	DIR*	DIR*	DIR*	DIR*
a19	20	STEP*	STEP*	STEP*	STEP*	STEP*	STEP*	STEP*
c19	22	WD*	WD*	WD*	WD*	WD*	WD*	WD*
a20	24	WG*	WG*	WG*	WG*	WG*	WG*	WG*
b26	26	TR00*	TR00*	TR00*	TR00*	TR00*	TR00*	TR00*
b27	28	WPRT*	WPRT*	WPRT*	WPRT*	WPRT*	WPRT*	WPRT*
b28	30	RD*	RD*	RD*	RD*	RD*	RD*	RD*
c20	32	SIDE*	SIDE*	SIDE*	SIDE*	SIDE*	SIDE*	SIDE*
a21	34	READY*	READY*	READY*	READY*/ DISK CHANGE	READY*/	READY*	HIGH DENSITY/ DISK CHANGE*

Fig. 3.16 : Pinouts for floppy drives from different manufacturers

Note:

The above table is given by way of example only. In certain cases, pinouts may vary with different serial numbers. The user should consult the documentation supplied with the particular floppy drive used.

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- Solder bead F13

  With link set, enables DCHG (Disk Change) input on WD37C65 floppy controller.

DISK CHANGE can be read back on D7 during reads to the WD37C65 operations register provided the F13 link is set; otherwise, this signal will be inoperative on the floppy interface.

- Solder bead F21

  Sets level of WD37C65 DRV (Drive Type) input

  link set : DRV = 0
  link not set : DRV = 1

In PC AT mode (control register at 1), DRV = 0 will set the WD37C65 RWC/RPM output to support the RPM function and assert this line by loading a 0 so as to reduce the drive speed to 260-300 rpm.

3.8.5.4 - P2 connections

WD	P2-c19
DIRC	-c18
STEP	-a19
WE*(WG)	-a20
RDD	-b28
INDEX	-b25
TR00	-b26
WP	-b27
DS0	-c16
DS1	-a17
DS2	-c17
RDY/INUSE/DCHG	-a21
HLD/INUSE	-c15
DS3/RDY	-a16
HLD/HS/DCHG/INUSE	-a15
HS (Side)	-c20
MOTON	-a18

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3.8.6 - CLOCK/CALENDAR option

The TSVME110 board is fitted as standard with a 24-pin JEDEC socket (IC11) for taking an STM MK48T02/12-25 "zero power timekeeper RAM" with maximum access time of 250ns.

This component incorporates the following:

- 2Kx8 of CMOS static RAM
- clock/calendar with crystal
- lithium cell

Mapping:

The timekeeper RAM is wired to D0-D7 and only accessible at odd bytes.

Address	Area accessed
$F00FFF	Year
$F00FFD	Month
$F00FFB	Date
$F00FF9	Day of the week
$F00FF7	Hours
$F00FF5	Minutes
$F00FF3	Seconds
$F00FF1	Control
$F00FFF : : odd bytes : $F0001	2 040 bytes of static RAM

Full details on programming the clock/calendar and monitoring the status of the lithium cell can be found in the appended data sheet, along with estimated cell lifespan figures for different operating temperatures and board power up / power down ratios.

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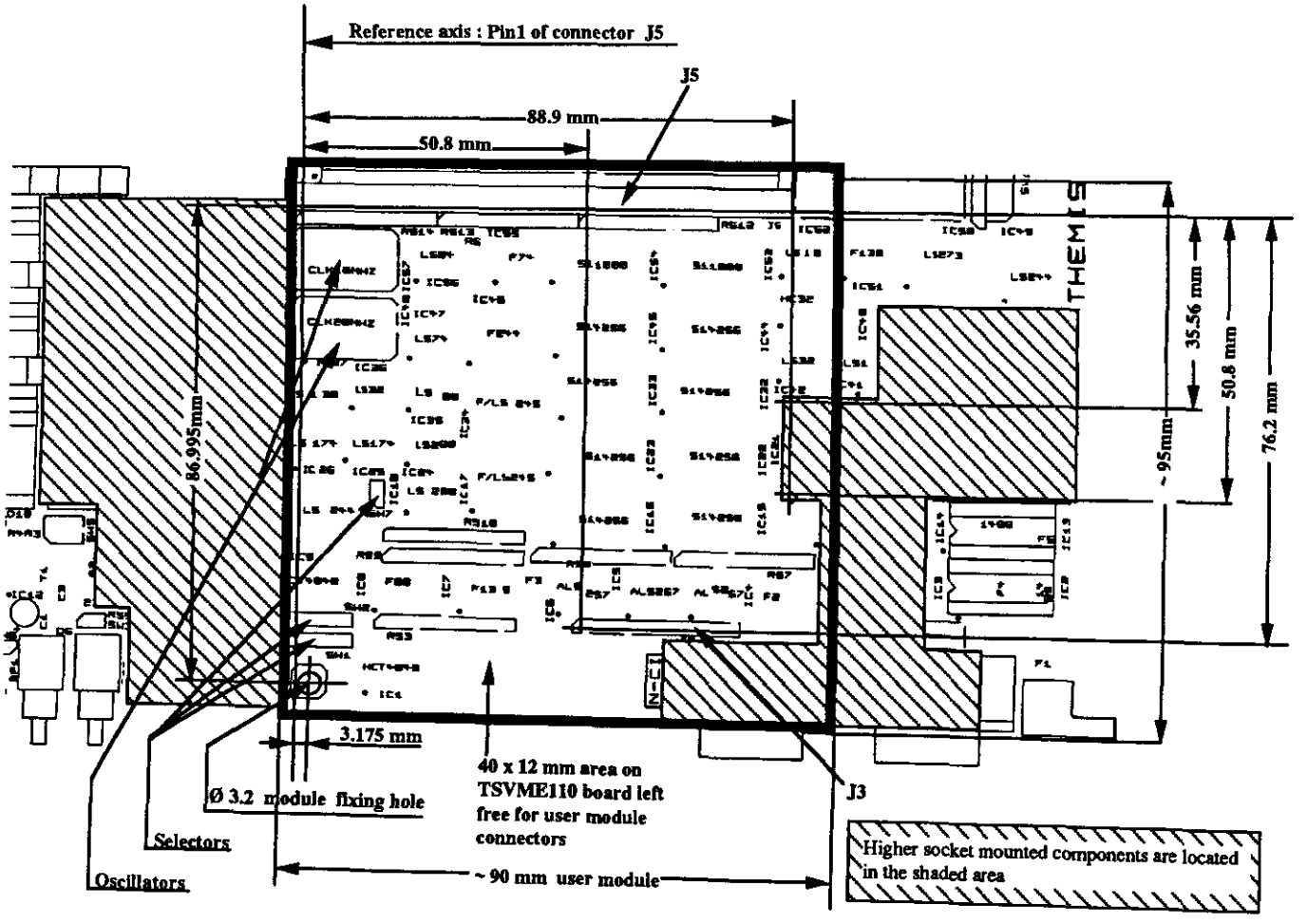
3.9 - USER INTERFACE MODULE

The TSVME110 board is designed to accommodate a custom-built user module connecting onto J3 and J5 and covering an area of 90x90mm. With the exception of selectors SW1, SW2, SW7 and oscillators IC48, 57, the TSVME110 board components located over this 90x90mm area are either of the CMS type (SOJ, SOIC) or low-profile resistor networks.

A 40 x 12 mm area is left completely free so that user module connectors can be taken out onto the front panel if required.

The J5 connector carries the CPU bus and the module control signals: CSMOD*, ITMOD*, +5V, ground.

The J3 connector carries connections from the module onto the P2 connector (8 wires), together with the + and - 12 V supplies



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3.9.1 - Control of user module from TSVME110 board

The J5 connector carries the TSVME110 local bus, i.e.:

- A(1-23)	68000 address bus
- D(0-15)	68000 data bus
- AS*	68000 address strobe
- LDS*, UDS*	68000 data strobe
- FC(0-2)	68000 function code
- RW	68000 signal
- VPA*, VMA*	68000 signal (VPA* is a TTL line asserted by the decoding logic)
- E	68000 signal
- DTACK*, BERR*	68000 signal
- BR*, BG*, BGACK*	68000 signal
- HALT*, RESET*	68000 signal
- TEST*	active at 0: disable decoding logic
- CLK8, CLK10/12.5	8, 10 or 12.5 MHz clocks (depending on option)
- VSYSCLK	16 MHz clock
- CSMOD*	Module selection from board address decoding (active at 0)
- ITMOD*	Module IT request This line is taken onto pin 8 of the local interrupt selector SW14 It must be of the open collector type and active at 0.

- **Local CPU accesses to the user module**:

$C00000 to $DFFFFF, i.e. 2 Mbytes

The user module must assert DTACK* or BERR* to acknowledge accesses from the CPU. Data exchanges must comply with 68000 (8 MHz) - 68010 (10 MHz or 12.5 MHz) specifications, depending on the board option.

With CSMOD* asserted (at 0), AS* and FC(0-2) addresses are valid. LDS* and UDS* must be polled to determine the active portion of the data bus.

On read accesses, data must go valid within 90 ns of DTACK being asserted for an 8 MHz 68000 , within 65 ns of DTACK being asserted for a 10 MHz 68010 and 50 ns for a 12.5 MHz 68010.

- **Interrupt servicing**:

Interrupts from the user module, like all local interrupts, are serviced by an AUTOVECTORED acknowledgement sequence, which means that the user is not required to supply an interrupt vector.

- **Local bus control**:

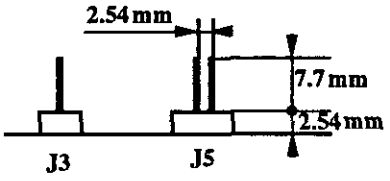
By managing the CPU signals BR*, BG* and BGACK*, user modules can be designed which are able to take control of the local TSVME110 bus for DMA transfers. Similarly, communication controllers with built-in DMA function can be used.

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3.9.2 - User module connectors

Both of the on-board user-module connectors have 7.7 mm pins with a spacing of 2.54 mm. J3 consists of a single row of 12 pins and J5 consists of two rows of 35 pins. The following female connectors are recommended for user modules:

BERG 76314135 for J5
76308112 for J3



J3 pinout: one row of 12 pins

Pin	Signal	P2 link
1	0V	
2	0V	
3	MOD0	a24
4	MOD1	a25
5	MOD2	a26
6	MOD3	a27
7	MOD4	a28
8	MOD5	a29
9	MOD6	a30
10	MOD7	a31
11	+12V	
12	-12V	

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J5 pinout: two rows of 35 pins

Signal	Pin	Pin	Signal
+5V	1	2	+5V
CLK8	3	4	GND
D5	5	6	D4
D6	7	8	D3
D7	9	10	D2
D8	11	12	D1
D9	13	14	D0
D10	15	16	AS*
D11	17	18	UDS*
D12	19	20	LDS*
D13	21	22	RW
D14	23	24	DTACK*
D15	25	26	BG*
GND	27	28	BGACK*
A23	29	30	BR*
A22	31	32	+5V
A21	33	34	VSYSCLK
+5V	35	36	GND
A20	37	38	HALT*
A19	39	40	RESET*
A18	41	42	VMA*
A17	43	44	E*
A16	45	46	VPA*
A15	47	48	BERR*
A14	49	50	CSMOD*
A13	51	52	ITMOD*
A12	53	54	TEST*
A11	55	56	FC2
A10	57	58	FC1
A9	59	60	FC0
A8	61	62	A1
A7	63	64	A2
A6	65	66	A3
A5	67	68	A4
CLK10/12.5	69	70	GND

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3.10 - P1 AND P2 CONNECTORS

The TSVME110 board uses the P1 and P2 connectors. The P1 connector carries the VME interface signals and the board power supplies.

IMPORTANT:
The P2 connector is wholly taken up with peripheral input/output signals, even on row B. This means that the board must not be used in a rack with a VME extension on P2 row B.

When the TSVME110 board is powered up, all the signals on row B of the P2 connector are at high impedance or incoming. This should reduce the risk of serious damage in the event of mishandling.

TABLE OF SIGNALS USED ON P1

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
A1	D0	B1	BBSY*	C1	D8
A2	D1	B2	BCLR*	C2	D9
A3	D2	B3	ACFAIL*	C3	D10
A4	D3	B4	BG0 IN*	C4	D11
A5	D4	B5	BG0 OUT*	C5	D12
A6	D5	B6	BG1 IN*	C6	D13
A7	D6	B7	BG1 OUT*	C7	D14
A8	D7	B8	BG2 IN*	C8	D15
A9	GND	B9	BG2 OUT*	C9	GND
A10	SYSCLK	B10	BG3 IN*	C10	SYSFAIL*
A11	GND	B11	BG3 OUT*	C11	BERR *
A12	DS1*	B12	BR0*	C12	SYSRESET*
A13	DS0*	B13	BR1*	C13	LWORD*
A14	WRITE*	B14	BR2*	C14	AM5
A15	GND	B15	BR3*	C15	A23
A16	DTACK*	B16	AM0	C16	A22
A17	GND	B17	AM1	C17	A21
A18	AS*	B18	AM2	C18	A20
A19	GND	B19	AM3	C19	A19
A20	IACK*	B20	GND	C20	A18
A21	IACKIN*	B21	NU	C21	A17
A22	IACKOUT*	B22	NU	C22	A16
A23	AM4	B23	GND	C23	A15
A24	A7	B24	IRQ7*	C24	A14
A25	A6	B25	IRQ6*	C25	A13
A26	A5	B26	IRQ5*	C26	A12
AJ4	A4	B27	IRQ4*	C27	A11
AJ4	A3	B28	IRQ3*	C28	A10
AJ4	A2	B29	IRQ2*	C29	A9
A30	A1	B30	IRQ1*	C30	A8
A31	-12V	B31	VMEVBB	C31	+12V
A32	+5V	B32	+5V	C32	+5V

NU : Not used

Fig. 3.17 : P1 connector

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Fig. 3.18 : Pinout for P2 connector

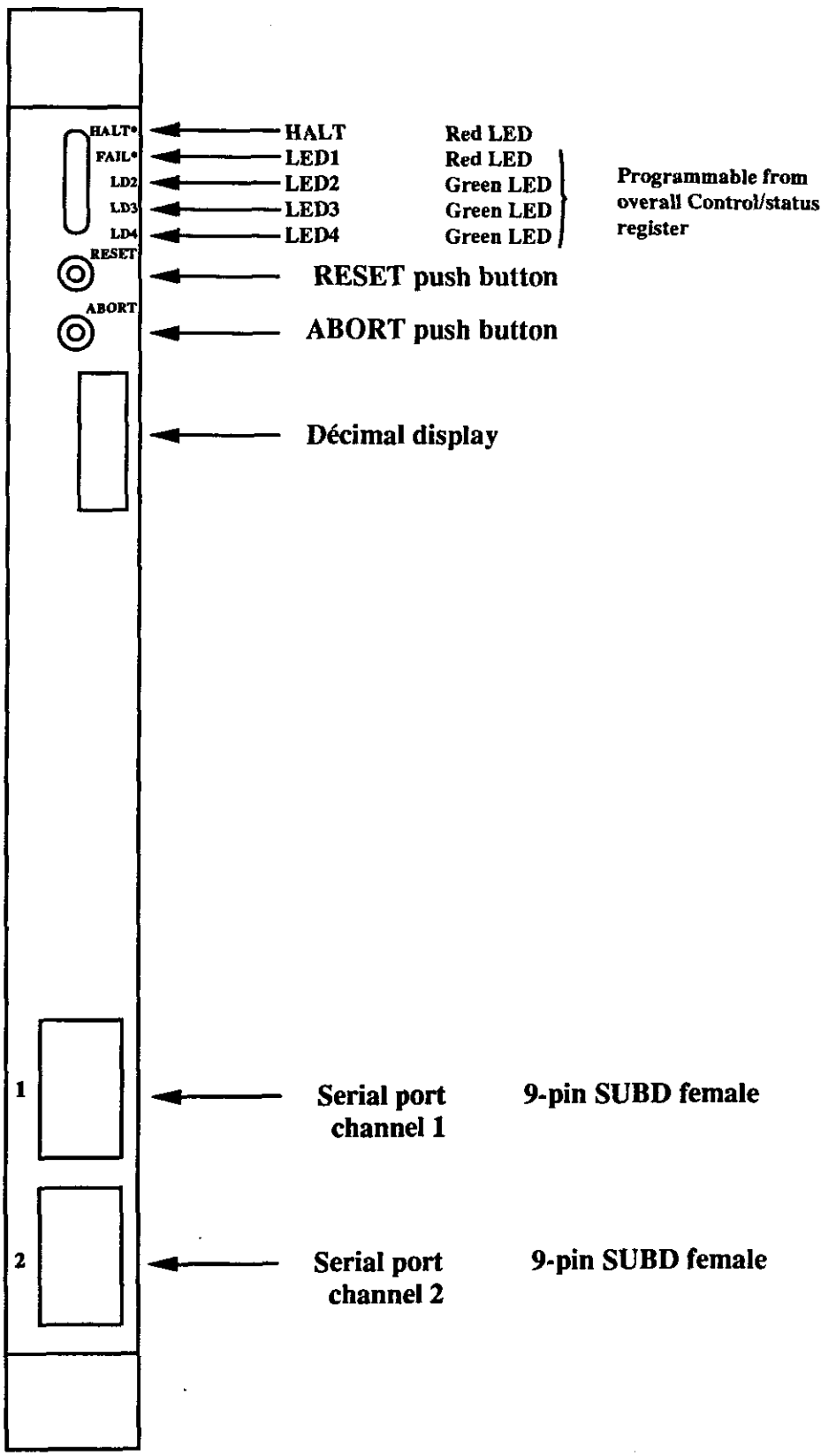
Row pin	A	Signal	Function	Row pin	B	Signal	Function	Row pin	C	Signal	Function
1		GND		1		Vcc		1		Gnd	
2		S1TXD	Serial	2		Gnd		2		S1RXD	Serial
			link								link
3		S1RTS	Channel 1	3		not used		3		S1CTS	Channel 1
4		I/OA0	Parallel	4		DB0*	SCSI	4		I/OA1	Parallel
			port								port
5		I/OA2	A(0-7)	5		DB1*		5		I/OA3	A(0-7)
6		I/OA4	even	6		DB2*		6		I/OA5	odd
7		I/OA6		7		DB3*		7		I/OA7	
8		I/OH1	H1	8		DB4*		8		I/OH2	H2
9		I/OB0	B(0-7)	9		DB5*		9		I/OB1	B(0-7)
10		I/OB2	even	10		DB6*		10		I/OB3	odd
11		Vcc		11		DB7*		11		Vcc	
12		I/OB4		12		Gnd		12		I/OB5	
13		I/OB6		13		Vcc		13		I/OB7	
14		I/OH3	H3	14		not used		14		I/OH4	H4
15		HLD/HS/DCHG*	Floppy	15		DBP*		15		HLD/INUSE*	Floppy
16		DS3/RDY*		16		BSY		16		DS0*	
17		DS1*		17		ACK*		17		DS2*	
18		MOTON*		18		RST*		18		DIRC*	
19		STEP*		19		MSG*		19		WD*	
20		WE*		20		SEL*		20		SIDE	
21		RDY/INUSE/ DCHG*		21		C/D		21		TIMGT*	Timer
22		TIMINT	Timer	22		REQ* (1)		22		TIMOUT	
23		WDGI*	Watch-dog	23		I/O		23		WDGO*	Watch-dog
24		MOD0		24		ATN*		24		S2TXD	
25		MOD1		25		INDEX*	Floppy	25		S2RXD	
26		MOD2	User	26		TR00*		26		S2RTS	Serial
27		MOD3	module	27		WP*		27		S2CTS	link
28		MOD4	(J3)	28		RDD		28		S2TXC	channel 2
29		MOD5		29		REQ* (2)		29		S2RXC	
30		MOD6		30		not used		30		S2DCD	
31		MOD7		31		GND		31		not used	
32		GND		32		Vcc		32		GND	

(1) SCSI REQ* on P2-b22 if F24 : 1-2

(2) on P2-b29 if F24 : 3-4

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3.11 - TSVME110 BOARD FRONT PANEL



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3.12 - P2 interconnection module for TSVME110 SO øø55

The SO øø55 module is designed to be plugged on the P2 connector of the TSVME110 board by a DIN 41612 female 96 points connector. On the other side, it owns :

- J1 - 2 x 25 points connector - SCSI bus compatible
- J4 - 2 x 17 points connector - floppy interface compatible
- J2,J3 - 2 x 5-pin connector connected via 9-wire ribbon cable to 9-pin female SUB-D connectors (crimped type), similar to J1 and J2 connectors on front panel.
- J5 - 2 x 5 points connector - user module I/O
- J6 - 2 x 25 points connector - parallel I/O, watchdog and timer signals wired on P2 of the TSVME110 board.

In the following tables, the signal names are same as used in the P2 connector pinout description for the TSVME110 board in fig. 3.18 of § 3.10.

The S1 selector allows on SO0055 the SCSI-REQ connection on P2-b22 or P2-b29 as the TSVME110 last versions (PCB : 50050-A0).

S1 Jumper	SCSI REQ	TSVME110 : F24 Link
1 - 2	P2-b22	1 - 2
2 - 2	P2-b29	3 - 4

The S1 jumper in 1-2 works with the previous TSVME110 versions - without F24 solder bead - and SCSI REQ* onto P2-b22 only.

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SO øø55 Connectors

J1 SCSI BUS

SIGNAL	PINS	SIGNAL
GND	1 2	DBø
GND	3 4	DB1
"	5 6	DB2
"	7 8	DB3
"	9 10	DB4
"	11 12	DB5
"	13 14	DB6
"	15 16	DB7
"	17 18	DBP
"	19 20	NU
"	21 22	NU
"	23 24	NU
"	25 26	NU
"	27 28	NU
"	29 30	NU
"	31 32	ATN *
"	33 34	NU
"	35 36	BSY *
"	37 38	ACK *
"	39 40	RST *
"	41 42	MSG *
"	43 44	SEL *
"	45 46	C/D
"	47 48	REQ *
"	49 50	I/O

J6 Parallel and watchdog and timer

SIGNAL	PINS	SIGNAL
GND	1 2	I/OAø
I/OA1	3 4	I/OA2
I/OA3	5 6	I/OA4
I/OA5	5 8	I/OA6
I/OA7	9 10	GND
I/OBø	11 12	I/OB1
I/OB2	13 14	I/OB3
I/OB4	15 16	I/OB5
I/OB6	17 18	I/OB7
GND	19 20	I/OH1
I/OH2	21 22	I/OH3
I/OH4	23 24	WDGO *
WDGI *	25 26	GND
TIMGT*	27 28	NU
NU	29 30	NU
NU	31 32	NU
NU	33 34	NU
NU	35 36	NU
NU	37 38	NU
NU	39 40	NU
NU	41 42	NU
NU	43 44	NU
NU	45 46	NU
NU	47 48	NU
TIMOUT	49 50	TIMINT

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J4 floppy bus

SIGNAL	PINS		SIGNAL
GND	1	2	HLD/HS/DCHG*
"	3	4	HLD/INUSE *
"	5	6	DS3/RDY*
"	7	8	INDEX*
"	9	10	DSø*
"	11	12	DS1*
"	13	14	DS2*
"	15	16	MOTON*
"	17	18	DIRC*
"	19	20	STEP*
"	21	22	WD*
"	23	24	WE*
"	25	26	TRøø*
"	27	28	WP*
"	29	30	RDD*
"	31	32	SIDE*
"	33	34	RDY/INUSE *

J2 serial post : channel 1

SIGNAL	PINS		SIGNAL
NU	1	2	NU
S1RXD	3	4	S1CTS
S1TXD	5	6	S1RTS
NU	7	8	NU
GND	9	10	NU

J3 serial port : channel 2

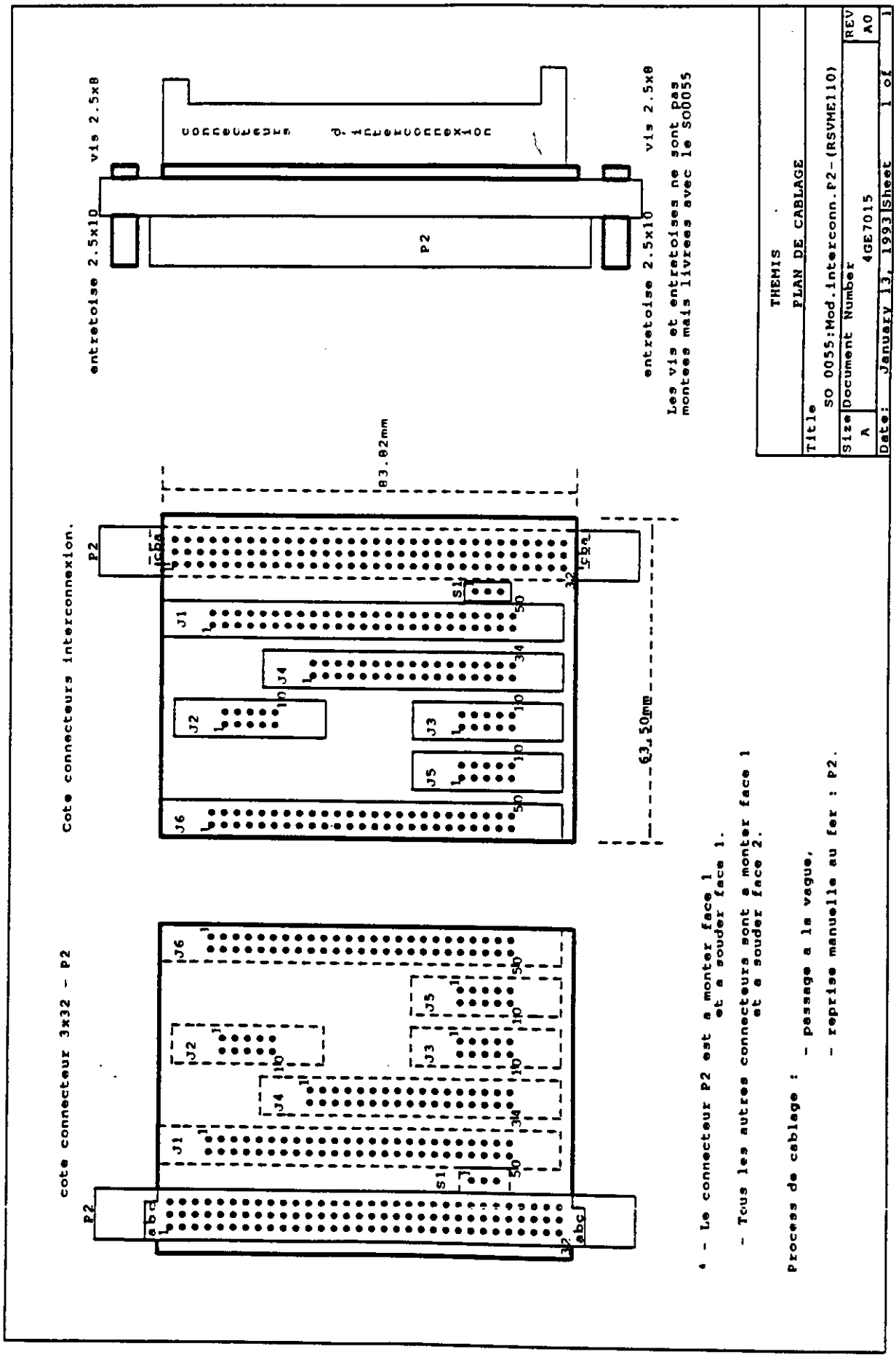
SIGNAL	PINS		SIGNAL
S2DCD	1	2	NU
S2RXD	3	4	S2CTS
S2TXD	5	6	S2RTS
S2RXC	7	8	S2TXC
GND	9	10	NU

J5 user module I/O

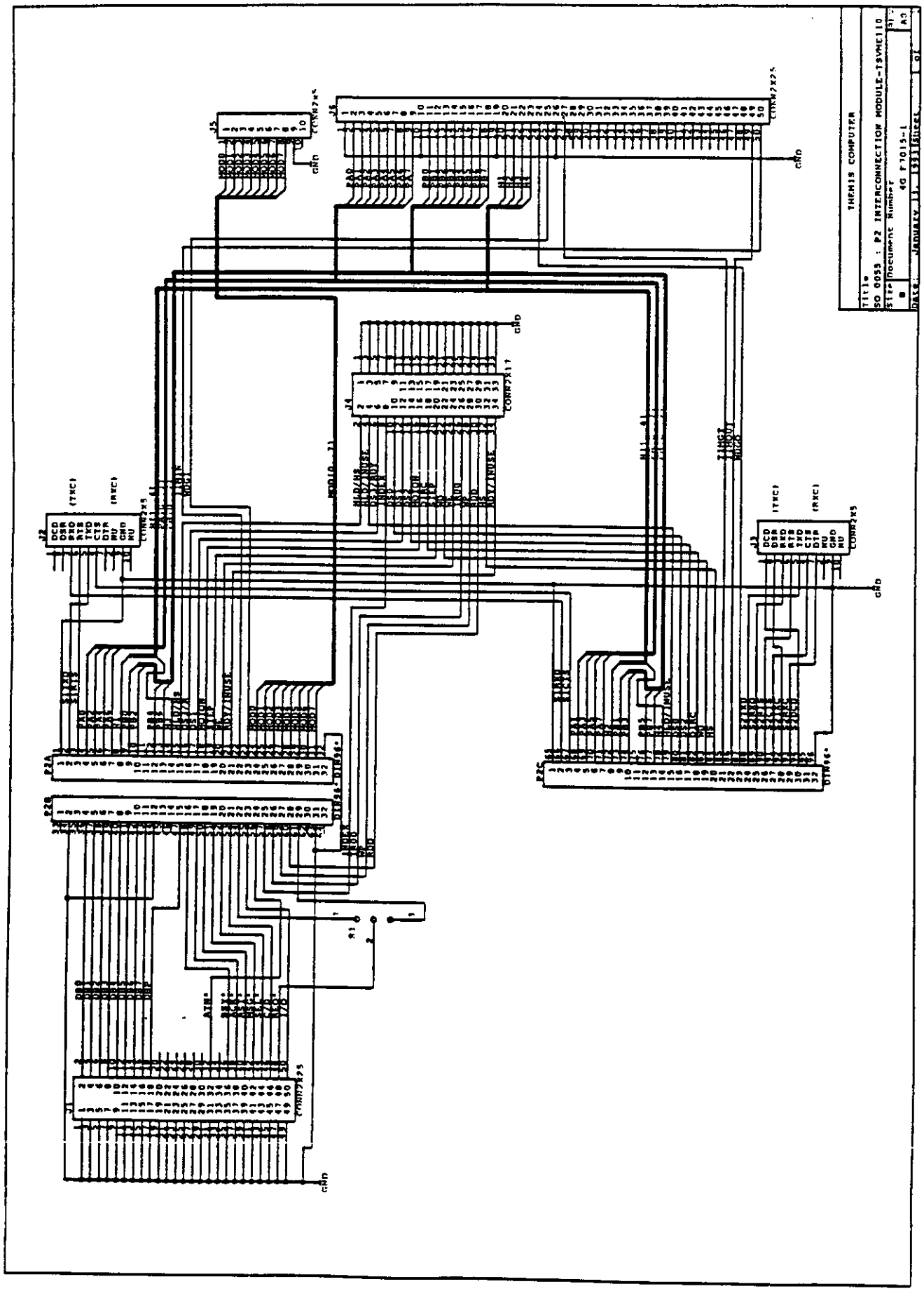
SIGNAL	PINS		SIGNAL
MODø	1	2	MOD1
MOD2	3	4	MOD3
MOD4	5	6	MOD5
MOD6	7	8	MOD7
GND	9	10	NU

The next pages give layout and schematic of the SO øø55.

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THEMIS COMPUTER
Title
SO 0053 : P2 INTERCONNECTION MODULE-TSVME110
Size
Document Number
4G F7015-1
Date: January 11, 1991
Sheet

IV - SOFTWARE

As standard, the TSVME110* board comes with a set of EPROMS containing the following:

- self-test run automatically on power up
- VBUG debugger with line-by-line assembler-deassembler
- software functions for use with the on-board clock/calendar chip

The debugger is discussed in 4.1, with additional information given in Appendices 1, 2 and 3.

Clock/calendar software functions are dealt with in 4.2.

4.1 - DEBUGGER AND SELF-TEST

4.1.1 - Introduction

4.1.1.1 - Software features

The TSVBUG110 product belongs to the "Vbug" range of debuggers developed for THEMIS boards built around 680xx microprocessors. The main features of the Vbug software are listed below:

- symbolic assembler-oriented debugging in the application environment without the need for dedicated hardware
- Vbug commands issued and programs downloaded/uploaded over host computer interface
- inputs/outputs reconfigurable for special characters, software flow control etc.
- interrupt handling from debugger or application
- memory windows
- reports parameterable for registers, memory windows, format
- M68000 or M68010 assembler/deassembler for rapid correction on application software

---

* The reference TSVME110 is taken here to cover all TSVME110.

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- TRAP 15 debugger calls, entry points
- position-independent code
- full board self-test on RESET
- repeated self-test feature (hard check - HCK command)

4.1.1.2 - Hardware environment

The TSVBUG110 software operates in a hardware environment consisting of a VME system with TSVME110 board. The debugger EPROMs occupy two of the memory sockets on the TSVME110 board. The debugger takes control on power up, providing a set of debugger commands and primitives for the application software.

4.1.1.3 - Type and location of debugger EPROMs

Two 27512 Eproms (64K x 8), referenced as follows:

	TSVME110-1	TSVME110-2	TSVME110-3	TSVME110-4	TSVME110-5
IC29	LP5282	LP5288	LP5340	LP5336	LP5338
IC30	LP5283	LP5289	LP5341	LP5337	LP5339

4.1.1.4 - Software/hardware identification, startup

The TSVBUG110 product identification is the first message to appear when the TSVME110 board is powered up.

TSVME110_X : SELF-TEST (X = n option)

The product version/release number also appears in the software prompt.

Details on the startup phase are given in the next section. The serial peripheral to be used as control terminal should be connected to connector "1" on the TSVME110 board front panel, with initial configuration as follows:

```
- baud rate         : 9600 bauds
- character size    : 8 bits
- character parity  : disabled
- stop bits         : one
- DTR, RTS etc.     : see documentation supplied with TSVME110 hardware
```

The initial values of virtual registers USP and SSP are as follows:

USP	SSP	
$FD00	$FF00	board versions with no dynamic RAM
$7FD00	$7FF00	board versions with 512Kbytes of dynamic RAM
$FFD00	$FFF00	board versions with 1Mbyte of dynamic RAM
$1FFD00	$1FFF00	board versions with 2Mbytes of dynamic RAM

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4.1.1.5 - Documentation: TSVBUG reference manual

The basic source documentation for the TSVBUG110 is the manual entitled:

TSVBUG : debugger + assembler/disassembler (ref.: A027)

4.1.1.6 - Other documentation

MC68000 16-Bit Microprocessor User's Manual (Motorola)
MC68010 16-Bit Microprocessor User's Manual (Motorola)

4.1.2 - TSVME110 board self-test

A hardware self-test is run on power-up. The stages involved in this self-test will vary with the board options fitted:

- Perform overall initializations.
- Test Z8530 chip. If this test fails, the front-panel FAIL indicator blinks; otherwise, the following message appears:

  TSVME 110-x : SELF-TEST
  Scc1 test : completed
  (where x is the board version)

- Test microprocessor (M68000 or M68010).
- Test PIT 68230, if fitted.
- Test 68B40 timer.
- Test dynamic RAM if fitted (clears RAM contents).
- Test static RAM if fitted (read only).
- Test MK48T02 timekeeper if fitted.
- Display date and time if MK48T02 fitted.
- if all tests run o.k., disable VME "SYSFAIL" signal and turn out FAIL led

Throughout the self-test, the FAIL led on the TSVME110 board front panel remains lit and the "SYSFAIL" signal remains asserted on the VMEbus. If successful, each phase of the test terminates with the message "COMPLETED"; otherwise, the message "** FAILED **" appears. The software will only turn out the "FAIL" led and display the prompt if all test phases have been successful.

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The list below is intended as an aid to troubleshooting. Possible causes of failure are examined and suggestions made regarding remedial measures and the possibility, or otherwise, of temporary operation in "limp-home" mode. Persistent problems should be referred to our dealer network, with detailed information on the type of fault encountered and the configuration used.

- red "FAIL" led flashes: Z8530 absent or defective; check module and restart.

- test phase terminates with "**FAILED**" message: self-test will continue, but "break" key must be pressed to return to prompt and access monitor commands. Subsequent operation of processor board liable to be jeopardized by defective function(s). In particular, a RAM error may prove disastrous if located in the exception vector area, the monitor working memory (stack !) etc.

- test crashes: possibly due to loss of interrupt.

- Self-test stops before last test is completed:

A bus error or spurious interrupt may cause the self-test to quit before completing all of its stages. Here, the vector displacement in the vector table will be displayed, the self-test will stop, and the VBUG prompt will appear as if the test had terminated normally. It will usually remain possible to access the board to determine the cause of the stoppage (second DUART chip not fitted, say).

If doubts persist as to the correct operation of the board, the self-test can be run in continuous mode by issuing the "HCK" (hard check) command.

e.g.:

HCK	loop self-test indefinitely
HCK &10	run 10 self-test loops

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Note 1:

Unlike the initial self-test, which lights the FAIL indicator and sends the SYSFAIL signal onto the bus, the self-test run by HCK will only light the FAIL indicator when an error is detected.

Note 2:

By setting user jumper SW7 (bit 4 in register $FBXXX1), the continuous self-test can be made to run automatically on RESET.

Self-test results

The results of the self-test are available in the form of a long word at address 0. If the test runs successfully, all the bits will be at zero; otherwise, failed test stages are indicated by bits at 1, as follows:

bit :	31	30	29	.....	3	2	1	0
test n° :	1	2	3	.....	29	30	31	32

Test numbers are as follows:

1 : SCC (serial I/O)
3 : MPU
4 : PIT
7 : TIMER
8 : RAM (dynamic RAM if fitted, static RAM otherwise)
12 : CALENDAR (if fitted)
23 : STATIC RAM (if fitted).

4.1.3 - Hardware resources managed by debugger

4.1.3.1 - EPROM and RAM

The USE command reports on the EPROM and RAM space used by VBUG.

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4.1.3.2 - Serial interfaces

The TSVBUG software manages the two TSVME110 serial interfaces provided by the Z8530 chip. These interfaces are accessible from RS232 connectors "1" and "2" on the board front panel.

The software can manage four distinct serial lines, each identified by a port number. The correspondence between debugger and hardware recognition of these lines is as follows:

Connector	Serial interface	Peripheral	Port number
1	Z8530 channel A	terminal	1
2	Z8530 channel B	host computer	2
2	Z8530 channel B	serial printer	3
2	Z8530 channel B	terminal/auxiliary	4

To switch from one type of peripheral to another, the wiring must be changed on the solder beads F1 or F2.

The PF (Port Format) command may be used to change the operating mode of a given port. This may be at hardware level (transfer rate, character format, handshake lines) or software level (null character filling, XON/XOFF protocol etc.). For further details refer to the TSVBUG manual.

Note:

The Z8530 channel A (managing the control terminal connected to "1") is initially programmed to ignore the absence of a CTS line on the terminal equipment. This option may also be reconfigured using the PF command.

4.1.3.3 - Interrupts

VBUG assumes that ABORT, PARITY ERROR and VFAIL generate level-7 interrupts. If this is the case, the display will show the type of IT received. If not, the display will show the vector number in question.

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4.1.4 - TSVME110-specific features

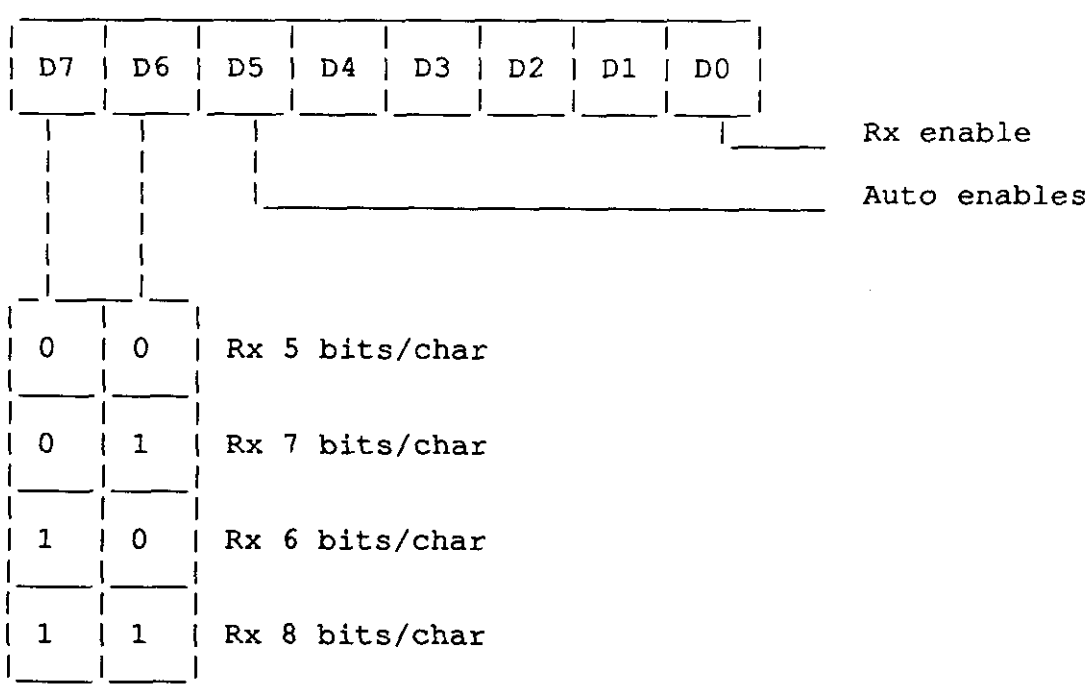
4.1.4.1 - PORT FORMAT : Configuration of I/O ports

A general description of this command can be found in the TSVBUG reference manual.

The values on initialization are given in Appendix 1.

The following tables are intended to aid in the fine programming of Z8530 registers WR3 and WR4, WR5 and WR12 for each channel. More detailed information on Z8530 programming can be found in the data sheet.

Table 4.2 : WR3 register bit format



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Table 4.3 : WR4 register bit format

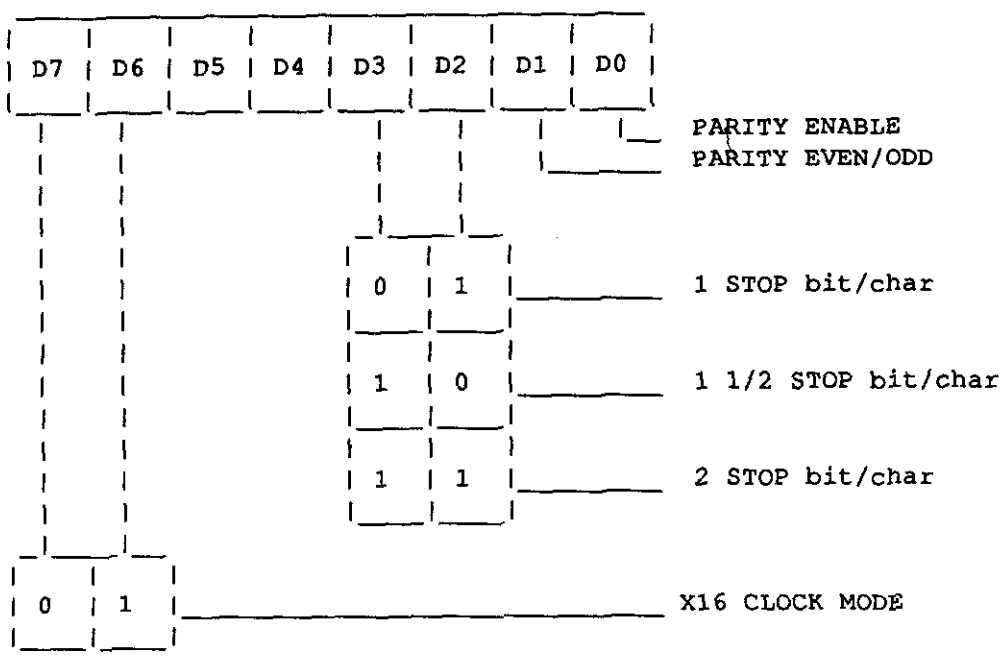
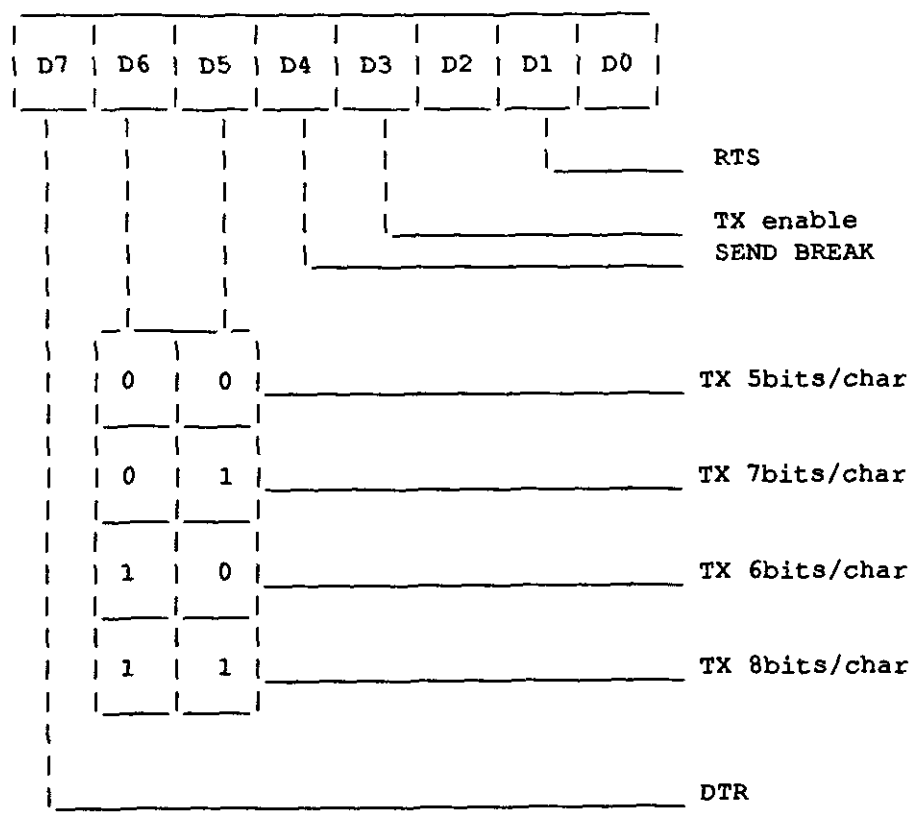


Table 4.4 : WR5 register bit format



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Table 4.5 : WR12 register bit format

BAUD RATE	HEX VALUE
38 400	0
19 200	2
9 600	6
4 800	E
2 400	1E
1 200	3E
600	7E
300	FE
150	1FE

Notes:

Vbug commands TM and PA will only operate correctly if the interfaces associated with the two active I/O ports are set to the same transfer rate.

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4.2 - TSVME110 SOFTWARE FUNCTIONS

TSVME110 board software functions take the form either of commands interpreted by VBUG, or of entry points to sub-routines, the parameters for which are passed via the stack.

Return values from these sub-routines are stored in the do.1 register, using the same C-language interface as that found on the THEMIS UNIX ™ computers.

TSVME110 software functions or commands are used for controlling the MK48T02 clock/calendar.

The TSVME110 board clock/calendar (MK48T02) is fully supported by the VBUG debugger. The following clock/calendar features are available: read, update, halt (battery economy), restart after halt. A calibration feature for fine frequency adjustment is also provided.

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VBUG commands are as follows:

CS [TOP]

Stop clock/calendar to economize battery. This command should only be used if the board is to be left unpowered for several months.

CR [ESTART]

Restart clock/calendar after CSTOP command. After this command is issued, a calibration byte is read in backed-up memory ($F0000A) for adjustment purposes.

This byte is structured: xxSy yyyy

xx :	bits ignored
S :	sign bit 1 : add to calibration value 0 : subtract from calibration value
y yyyy:	calibration value in units of 5.35 seconds/month

After an experimental phase, the user should be able to find the right calibration value to leave in backed-up memory.

TD

This command is used for reading and writing the date and time.
If required, the date can be left unchanged by simply entering a CR (carriage return) when asked to enter the date.

ENTER DATE (MM:DD:YY)= accepts entries in the form: MONTH (1-12) on one or two digits, followed by DAY (1-31) on one or two digits, followed by YEAR on two digits (e.g. 89). If the year is omitted, the previous year value is retained.

Examples:

```
12:25:89        (25 December 1989)
2:3:90          (3 February 1990)
1:1             (1 January)
```

ENTER TIME (HR:MIN:SEC)= accepts entries in the form: HOURS (0-23), MINUTES (0-59), and SECONDS (0-59). Entries may be made on one or two digits as desired. If the seconds are omitted, they are set at zero.

Examples:

```
12:54:22        (12H 54MIN 22 SEC)
12:54           (12H 54MIN  0 SEC)
2:3:4           ( 2H  3MIN  4 SEC)
```

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ENTRY POINT $2C0

The clock/calendar is read from an entry point to a VBUG sub-routine. This entry point is located at $2C0 from the start of PROM.

The interface in C language is as follows:

```
char buffer [30];
readcalt (buffer);          /* define at link_readcalt=0XEC02C0*/
```

The interface in assembler language is as follows:

```
BUFFER      DS.B        30
            MOVE.L      #BUFFER,-(A7)
            BSR         $EC02C0
            ADDQ.L      #4,(A7)
```

The following values are returned to the buffer area:

```
dow     ds.b    3       day of the week             e.g.: Sun
        ds.b    1       space
MMM     ds.b    3       month                       e.g. : Jan
        ds.b    1       space
DD      ds.b    2       day                         e.g.: 28
        ds.b    2       spaces
HH      ds.b    2       hour                        e.g.: 12
        ds.b    1       space
mm      ds.b    2       minute                      e.g.: 57
b       ds.b    1       space
ss      ds.b    2       second                      e.g.: 19
        ds.b    2       spaces
yyyy    ds.b    4       year                        e.g.: 1989
CR      ds.b    1       carriage return code ($0D)
LF      ds.b    1       line feed code ($0A)
```

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SOFTWARE APPENDICES

Appendix 1:

Tables showing configuration of serial input/output ports under Vbug

Appendix 2:

Table showing Vbug configuration after reset

Appendix 3:

Table showing TSVME110 board hardware configuration under Vbug

Appendix 4:

Description of backed-up memory used by Vbug

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SOFTWARE APPENDICES 1 - 2 - 3

Appendices 1 to 3 contain descriptions of those TSVME110 EPROM fields likely to be of interest to the user. Fields may be permanently modified, by duplicating and modifying the PROMS, in order to customize the debugger.

NOTE: Offsets are given in hexadecimal with respect to the EPROM start address ($EC0000 on TSVME110 board).

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APPENDIX 1

DEFAULT VALUES FOR SERIAL I/O PORT CONFIGURATION

Port 1

Offset *	Value	Description
$130	$F80005	Channel address
$134	'Z8530'	Device name
$139	$C0	WR3 : Rx : 8 bits
$13A	$44	WR4 : Clock x 16 1 stop bit no parity
$13B	$62	WR5 : Tx : 8 bits RTS
$13C	$06	WR12 : 9600 bauds
$13D	$FF	Reserved
$13E	$FF	Reserved
$13F	$FF	Reserved
$140	$00	Number of nulls after 1 character
$141	$00	Number of nulls after CR or LF
$142	$F9	Terminal input mode
$143	$06	Terminal output mode
$144	$13	XOFF = CTL-S
$145	$00	XON = any character
$146	$00	Value of break character (none)
$147	$00	Value of eof character (none)
$148	$OD	Value of end-of-line character (CR)
$149	$08	Value of delete char. character (BS)
$14A	$18	Value of delete line character (CTL-X)
$14B	$00	Delay after sending character, in ms (0)

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(.../...)

$14C	$00	Delay after sending end-of-line character, in ms (0)
$14D	80	Number of characters per line
$14E	24	Number of lines per page
$14F	'P'	Page mode
$150 - $153		Reserved

* Relative offset from start of PROM

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Port 2

Offset	Value	Description
$154	$F80001	Channel address
$158	'Z8530'	Device name
$15D	$C0	WR3 : Rx : 8 bits
$15E	$44	WR4 : Clock x 16 1 stop bit no parity
$15F	$62	WR5 : Tx : 8 bits RTS
$160	$06	WR12 : 9600 bauds
$161	$FF	Reserved
$162	$FF	Reserved
$163	$FF	Reserved
$164	$00	Number of nulls after 1 character
$165	$00	Number of nulls after CR or LF
$166	$47	Host input mode
$167	$38	Host output mode
$168	$13	XOFF = CTL-S
$169	$00	XON = any character
$16A	$00	Value of break character (none)
$16B	$00	Value of eof character (none)
$16C	$0D	Value of end-of-line character (CR)
$16D	$08	Value of delete char. character (BS)
$16E	$15	Value of delete line character (CTL-U)
$16F	$05	Delay after sending character, in ms (5)

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(.../...)

$170	$05	Delay after sending end-of-line character, in ms (5)
$171	80	Number of characters per line
$172	24	Number of lines per page
$173	'P'	Page mode
$174 - $177		Reserved

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Port 3

Offset	Value	Description
$178	$F80001	Channel address
$17C	'Z8530'	Device name
$181	$C0	WR3 : Rx : 8 bits
$182	$44	WR4 : Clock x 16 1 stop bit no parity
$183	$62	WR5 : Tx : 8 bits RTS
$184	$06	WR12 : 9600 bauds
$185	$FF	Reserved
$186	$FF	Reserved
$187	$FF	Reserved
$188	$00	Number of nulls after 1 character
$189	$00	Number of nulls after CR or LF
$18A	$47	Printer input mode
$18B	$23	Printer output mode
$18C	$13	XOFF = CTL-S
$18D	$00	XON = any character
$18E	$00	Value of break character (none)
$18F	$00	Value of eof character (none)
$190	$0D	Value of end-of-line character (CR)
$191	$08	Value of delete char. character (BS)
$192	$15	Value of delete line character (CTL-U)
$193	$00	Delay after sending character, in ms (0)

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(.../...)

$194	$00	Delay after sending end-of-line character, in ms (0)
$195	80	Number of characters per line
$196	24	Number of lines per page
$197	'P'	Page mode
$198 - $19B		Reserved

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Port 4

Offset	Value	Description
$19C	$F80001	Channel address
$1A0	'Z8530'	Device name
$1A5	$C0	WR3 : Rx : 8 bits
$1A6	$44	WR4 : Clock x 16 1 stop bit no parity
$1A7	$62	WR5 : Tx : 8 bits RTS
$1A8	$06	WR12 : 9600 bauds
$1A9	$FF	Reserved
$1AA	$FF	Reserved
$1AB	$FF	Reserved
$1AC	$00	Number of nulls after 1 character
$1AD	$00	Number of nulls after CR or LF
$1AE	$F9	Terminal input mode
$1AF	$06	Terminal output mode
$1B0	$13	XOFF = CTL-S
$1B1	$00	XON = any character
$1B2	$00	Value of break character (none)
$1B3	$00	Value of eof character (none)
$1B4	$0D	Value of end-of-line character (CR)
$1B5	$08	Value of delete char. character (BS)
$1B6	$18	Value of delete line character (CTL-X)
$1B7	$00	Delay after sending character, in ms (0)

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(.../...)

$1B8	$00	Delay after sending character, in ms (0)
$1B9	80	Number of characters per line
$1BA	24	Number of lines per page
$1BB	'P'	Page mode
$1BC to $1BF		Reserved

Notes :

If required, the standard EPROMs supplied may be permanently modified to obtain a different default configuration on power up.

Temporary modifications may be made whenever required using the PF command.

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APPENDIX 2

CONFIGURATION OF VBUG SESSION AFTER RESET

Offset	Value	Description
$1C0	$01	Port number for incoming VBUG commands
$1C1	$01	Port number for outgoing VBUG messages
$1C2	$01	Former port number for incoming VBUG commands before RC
$1C3	$01	Former port number for outgoing VBUG messages before RC
$1C4	$02	Host port number
$1C5	$03	Printer port number
$1C6	'M'	Outgoing message mode (see RC command)
$1C7	'M'	Former outgoing message mode before RC command
$1C8	$00	Number of port to be echoed (none) (see PA command)
$1C9	$00	Number of port for sending echo (none) (see PA command)
$1CA to $1CB		Reserved

Note: If so desired, the debugger can be customized by modifying the standard VBUG EPROMs supplied.

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APPENDIX 3

TSVME110 BOARD HARDWARE CONFIGURATION

Offset	Value	Description
$1CC	68000 or 68010	Type of mpu : 68000 (110-1) 68010 (110-2)
$1D0	'110 '	Type of cpu
$1D4	$EC0000	ROM start address
$1D8	$EFFFFF	ROM end address
$1DC	27512	Type of ROM : 27512
$1EO	$0	RAM start address
$1E4	$FFFF $FFFFF	RAM end address : depending on board version
$1E8	'Sram' 'Dram'	Type of RAM : depending on board version
$1EC	$1000	User-available RAM start address
$1F0	$FFFFF	User-available RAM end address
$1F4	$F80005	Address of I/O port 1
$1F8	$F80001	Address of I/O port 2
$1FC	$F80001	Address of I/O port 3
$200	$F80001	Address of I/O port 4
$204	0	Address of I/O port 5
$208	0	Address of I/O port 6
$20C	0	Address of I/O port 7
$210	0	Address of I/O port 8
$214	8530	Type of serial I/O chip : Z8530
$218	$FB0001	Control register start address

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Offset	Value	Description
$21C	$FB0007	Control register end address
$220	'mscr'	Type of control register
$224	$F00001	Backed-up RAM + Clock/Cal. Add. if present
$228	'SRAM'	Type of backed-up RAM : SRAM
$22C	$FA0001	TIMER address
$230	6840	Type of TIMER : 68B40
$234	$F90001	Address of parallel interface if present
$238	68230	Type of PIT : 68230
$23C	$FB0003	Display address
$240	DISP	Type of display : DISP
$244	$FD0000	Add. of SCSI controller if present
$248	SCSI	Type : SCSI if present
$24C	$FC0000	Add. of floppy controller if present
$250	FLOP	Type : FLOP if present
$254	$E00000	Address of static RAM if present
$258	SRAM	Type : SRAM if present
$25C	0	Reserved
$260	0	Reserved

Note:

The fields in the above table provide information on chip addresses, and can be displayed by the USE command. The user is recommended not to modify these fields.

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APPENDIX 4:

DESCRIPTION OF BACKED-UP RAM USED BY VBUG

$F00000 - $F00009	Reserved
$F0000A	MK48T02 calibration byte
$F0000B - $F000FF	Reserved

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