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USPIIe-cPCI Hardware Manual

Version 1.0—January 2003



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USPIIe-cPCI Hardware Manual

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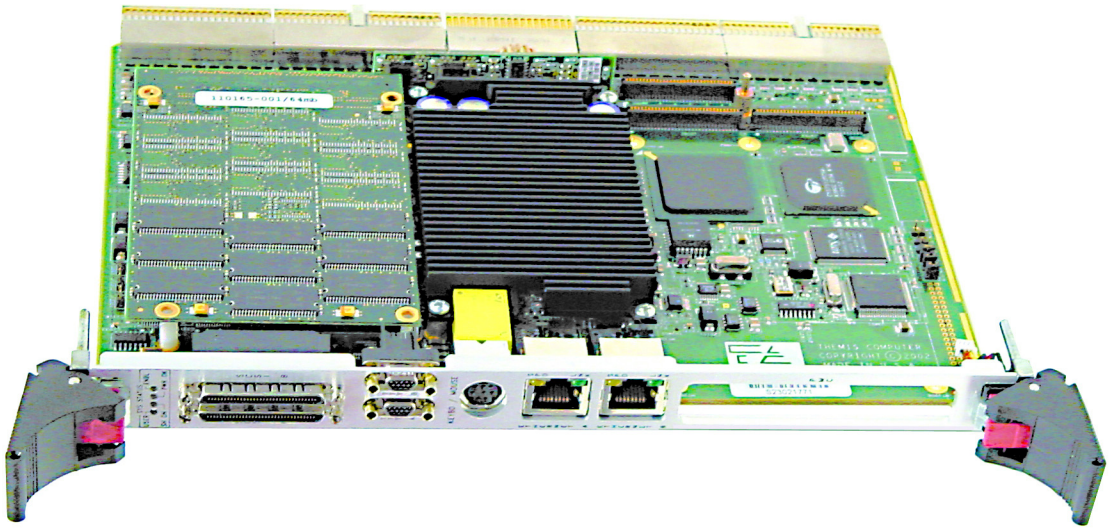
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How to Use This Manual

Introduction

This document describes the Themis USPII*e*-cPCI (see following photo), a SPARC version-9.0-compliant, single-board computer with a 6RU form factor and an UltraSPARC-II*e* Cu CPU operating at up to 650 MHz, with up to 2 GB of memory. I/O ports are located on the front faceplate, a user-installed PMC Module, and an optional board located behind the cPCI backplane (see following sections).



USPIIe-cPCI Baseboard (DIN-8 Port Version)

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The USPII*e*-cPCI offers the following I/O connections through its front faceplate:

- 2 LVD Ultra-2/SCSI-3 ports (68-pin 0.8-mm SCSI D) ..... *SCSI A / SCSI B*
- 2 asynchronous RS232 serial ports (9-pin mini-D) *TTY A /TTY B* (*Full Modem)*
- 1 PS/2 keyboard/mouse port (8-pin mini-DIN)
  or dual-USB port ..... *USB A / USB B*
- 2 Ethernet ports (8-pin RJ45)..... *Ethernet A / Ethernet B*
- Additional ports are available through a user-installed PMC Module

In addition, the following I/O connections are available through an *optional* 1-slot wide Rear Transition Board that can be attached to the cPCI backplane from behind:

- 2 LVD Ultra-2/SCSI-3 ports (68-pin 0.8-mm HDC SCSI-D) ... *SCSI A / SCSI B*
- 1 bi-directional parallel port (25-pin sub-D, female)
- 4 asynchronous RS232 serial ports (9-pin sub-D). *TTY A /TTY B* (*Full Modem)*
  ..... *TTY C / TTY D (Tx and Rx only)*
- Dual-USB port ..... *USB C / USB D*
- 2 audio lines (1 in, 1 out), 1 headphone out, 1 mic in (3-mm connectors)

Themis Computer values its customer comments and opinions; therefore, a “Reader Comment Card” is located at the end of this manual for your use. Please take the time to fill out this card with any comments concerning Themis products and services, and return it to Themis Computer. Your comments may also be forwarded to Themis by sending email to docfeedback@themis.com.

Before you begin your installation and operation of the USPII*e*-cPCI, carefully read each of the procedures in this manual and the associated software manual. Serious damage can be caused by improper handling of the equipment.

Intended Audience

This manual is written for system integrators and programmers. It contains all necessary information for installation and configuration of the USPII*e*-cPCI and assumes the OpenBoot PROM (OBP) program code is installed in the system Flash memory. If you intend to operate the USPII*e*-cPCI with an operating system other than Solaris, such as VxWorks or some other real-time kernel, please consult the appropriate documentation supplements accompanying your OS or kernel software.

Although all specific hardware and software features are described in the manuals, programmers wishing to write code for the USPII*e*-cPCI without the benefit of an

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operating system or real-time kernel will require additional data sheets. Please refer to the section “Related References” on page xvi for information concerning this documentation.

The reader should have a working knowledge of PCI local bus specifications, SPARC processor architecture, Ethernet protocol, and SCSI (ANSI 3.131-1994) specifications.

Unpacking



Caution: The USPII*e*-cPCI contains statically sensitive components. Industry-standard antistatic measures must be observed when removing the USPII*e*-cPCI from its shipping container and during any subsequent handling. A wrist strap provides grounding for static electricity between your body and the chassis of the system unit. Electric current and voltage do not pass through the wrist strap.

Remove the USPII*e*-cPCI and accessories from the shipping container and check the contents against the packing list. Be certain to observe industry-standard ESD protection procedures when handling static-sensitive components. The package should include all elements of your order.

Please report any shipping discrepancies to the Themis Computer Customer Support group immediately: support@themis.com or 1-510-252-0870.

How to Start Quickly

To start making the USPII*e*-cPCI operational quickly, Themis recommends that you read the following sections:

- Chapter 1, "USPIIe-cPCI Installation". This chapter contains information on configuring the USPII*e*-cPCI.
- Appendix B, "Jumper-Pin and Solder-Bead Configurations". This appendix contains a complete listing of all DIP switches, jumper pins, and solder beads, along with all default settings. Verify that the switches, jumpers, and beads on your system are set to meet your application requirements.

In addition to information contained in this manual—the *USPIIe-cPCI Hardware Manual* (Themis P/N-110553-022)—the *USPIIe-cPCI Software Manual* (Themis P/N-110553-023) contains information on software registers, address maps, and additional OpenBoot commands.

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Related References

The following is a list of related references

- *USPIIe-cPCI Software Manual* (Themis Computer P/N-110553-023)
- *CompactPCI Specification*, PICMG 2.0 D3.0, PCI Industrial Computers Manufacturers Group, June 21, 1999
- *PCI Local Bus Specification*, Revision 2.1, PCI Special Interest Group, Portland
- *PCI System Architecture,* by Shanley and Anderson, MindShare Press
- *IEEE Standard 1275-1994, Standard For Boot (Initialization, Configuration) Firmware*, Core Practices and Requirements
- *IEEE Standard 1275.1-1994, Standard For Boot (Initialization, Configuration) Firmware*, ISA Supplement for IEEE P1754 (SPARC)
- *IEEE Standard P1275.6/D4, Standard For Boot (Initialization, Configuration) Firmware*, 64 Bit Extensions
- *OpenBoot 3.x Command Reference*, Sun Microsystems (806-1377-10)
- *PCI Bus Binding to IEEE 1275-1994, Standard for Boot (Initialization, Configuration) Firmware*, Revision 1.0, 14 April 1994, Prepared by the Open Firmware Task Force of the PCI Alliance
- *OpenBoot 3.x Command Supplement for PCI*, Sun Microsystems (805-1627-10)
- *The SPARC Architecture Manual, Version 9*, David L. Weaver and Tom Germond, editors, PTR Prentice Hall
- *SunVTS™ 2.1 SunVTS User's Guide,* Part No. 802-7299 August 1997, Rev. A
- *SunVTS™ Quick Reference Card*, Part No. 816-0861-10
- *SunVTS™ 2.1.3 Test Reference Manual* Part No. 805-4163-10, May 1998, Rev. A

Integrated Circuit Specifications:

- *UltraSPARC-IIe User's Manual* (SUN P/N-806-tbd-00; Draft, June 8, 2001)
- *UltraSPARC-IIe Data Sheet* (SME1701CPGA-400/500, SUN P/N-806-0482-01, June 12, 2001)
- *SME2411BGA-66: Advanced PCI Bridge (APB) Data Sheet* (SUN P/N-805-0088-02)
- *SME2411BGA-66: Advanced PCI Bridge (APB) User's Manual*

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(SUN P/N-805-1251-01)

- *PCIO-2 Multifunction I/O Controller Data Sheet*, Sun Microsystems (SME2300BGA), 9/28/2001 (draft)
- *RIO I/O Controller Data Sheet*, Sun Microsystems, Version STPnnnnXXX, March 3, 2000
- *National Semiconductor DP83843 Phyter Data Sheet,* Version E, August, 1997, National Semiconductor Corporation
- *Symbios SYM53C896: PCI to Dual-Channel Ultra2 SCSI Multifunction Controller Technical Manual*, Version 3.0, January 2000

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Notes, Cautions, Warnings, and Sidebars

The following icons and formatted text are included in this document for the reasons described:



Note: A note provides additional information concerning the procedure or action being described that may be helpful in carrying out the procedure or action.



Caution: A caution describes a procedure or action that may result in injury to the operator or equipment damage. This may involve—but is not restricted to—heavy equipment or sharp objects. To reduce the risk, follow the instructions accompanying this symbol.



Warning: A warning describes a procedure or action that may cause injury to the operator or equipment as a result of hazardous voltages. To reduce the risk of electrical shock and danger, follow the instructions accompanying this symbol.



Sidebar: A "sidebar" adds detail to the section within which it is placed, but is not absolutely vital to the description or procedure of the section.

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Product Warranty and Registration

Please review the Themis Computer warranty and complete the product registration card delivered with your USPII*e*-cPCI board(s). Return of the registration card is not required to activate your product warranty but, by registering your USPII*e*-cPCI, Themis will be better able to provide you with timely information updates and product-enhancement notifications.

Our Customer Support department is committed to providing the best product support in the computer industry. Customer support is available 8am—5pm (PST), Monday through Friday, via telephone, fax, e-mail, and our website.

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E-mail: support@themis.com
Website: http://www.themis.com

In Case Of Difficulties

If the USPII*e*-cPCI does not behave as described or if you encounter difficulties installing or configuring the board, please call Themis technical support at +1 (510) 252-0870, fax your questions to +1 (510) 490-5529, or e-mail to *support@themis.com.* You can also contact us via our web site: http://www.themis.com.

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Installation Section

Chapter 1

USPIIe-cPCI Installation

1.1 Check Configurations

There are two types of USPII*e*-cPCI baseboards:

- DIN-8-Port Version
- USB-Port Version

When you first receive your USPII*e*-cPCI, check that it is the version you ordered. Also, confirm that the jumper-pin and solder-bead configurations are appropriate for your application. Appendix B, "Jumper-Pin and Solder-Bead Configurations" gives a complete listing of jumper-pin and solder-bead definitions, including default settings.

If you have to change a jumper-pin setting, check with Themis Customer Support first to make sure the new setting is supported.

Solder-bead settings are set by Themis at the factory before shipping and should be changed by Themis at the factory only.

Warning: Attempting to alter a solder-bead configuration could seriously damage the USPII*e*-cPCI. DO NOT ATTEMPT TO ALTER SOLDER-BEAD CONFIGURATIONS without a full understanding of their effect. In case of doubt, contact Themis to change any settings.

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1.1.1 DIN-8 Connector (*DIN-8-Port Version Only*)

The mini-DIN-8 connector (marked **KEYBD/MOUSE**) on the DIN-8-Port Version USPII*e*-cPCI front panel supports either a PS/2 keyboard/mouse port or dual USB (USB-A, USB-B) ports. Either option is selected by configuring five solder beads (SB3502 through SB3506; see *Table 1-1*), and both require special pigtail cables from Themis Computer.

[See section B.3.1, “Baseboard Solder Beads”, page B-6, for more details.]

Table 1-1. Front-Panel DIN-8 Settings

SB3502	SB3503 through SB3506	Front-Panel 8-Pin Mini-DIN Configuration	Comments
Open	**Short 1-2**	**PS/2 keyboard/mouse**	Accessible only through a special split pigtail cable (*Themis 110104-002*) • 8-pin mini-DIN to 6-pin keyboard DIN and 6-pin mouse DIN
Open	Short 2-3	*Not Applicable*	
Short	Short 1-2	*Not Applicable*	
Short	**Short 2-3**	**USB (USB-A, USB-B)**	Accessible only through a special split pigtail cable (*Themis 110473-001*) • 8-pin mini-DIN to dual 4-pin USB

1.1.2 USB Port A/B Connector (*USB-Port Version Only*)

If you have ordered the USB-Port Version USPII*e*-cPCI Baseboard, solder beads SB3502 through SB3506 have no affect on the operation of the board. For consistency, however, SB3502 should be shorted and SB3503 to SB3506 set to 2-3.

The dual-USB port A/B can be used to operate any USB device, including a USB keyboard/mouse. If you ordered the USB-Port Version, you cannot use a PS/2 keyboard/mouse; only a USB keyboard/mouse can be used.

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1.1.3 SCSI Terminations

All SCSI busses must be properly terminated. The USPII*e*-cPCI contains two SCSI ports (A and B) on the front panel of the USPII*e*-cPCI (see Appendix C, “Front and Rear Panel Diagrams”). In addition, both SCSI A and SCSI B are accessed through the Rear Transition Board behind the cPCI backplane (see *Figure 1-1*).

To avoid possible conflicts that can occur from improper on-board manual settings of terminators for SCSI bus A and SCSI bus B, the USPII*e*-cPCI has integrated an auto-termination circuit that will detect whether terminated devices are attached to either SCSI bus, either through the front panel or through the Rear Transition Board.

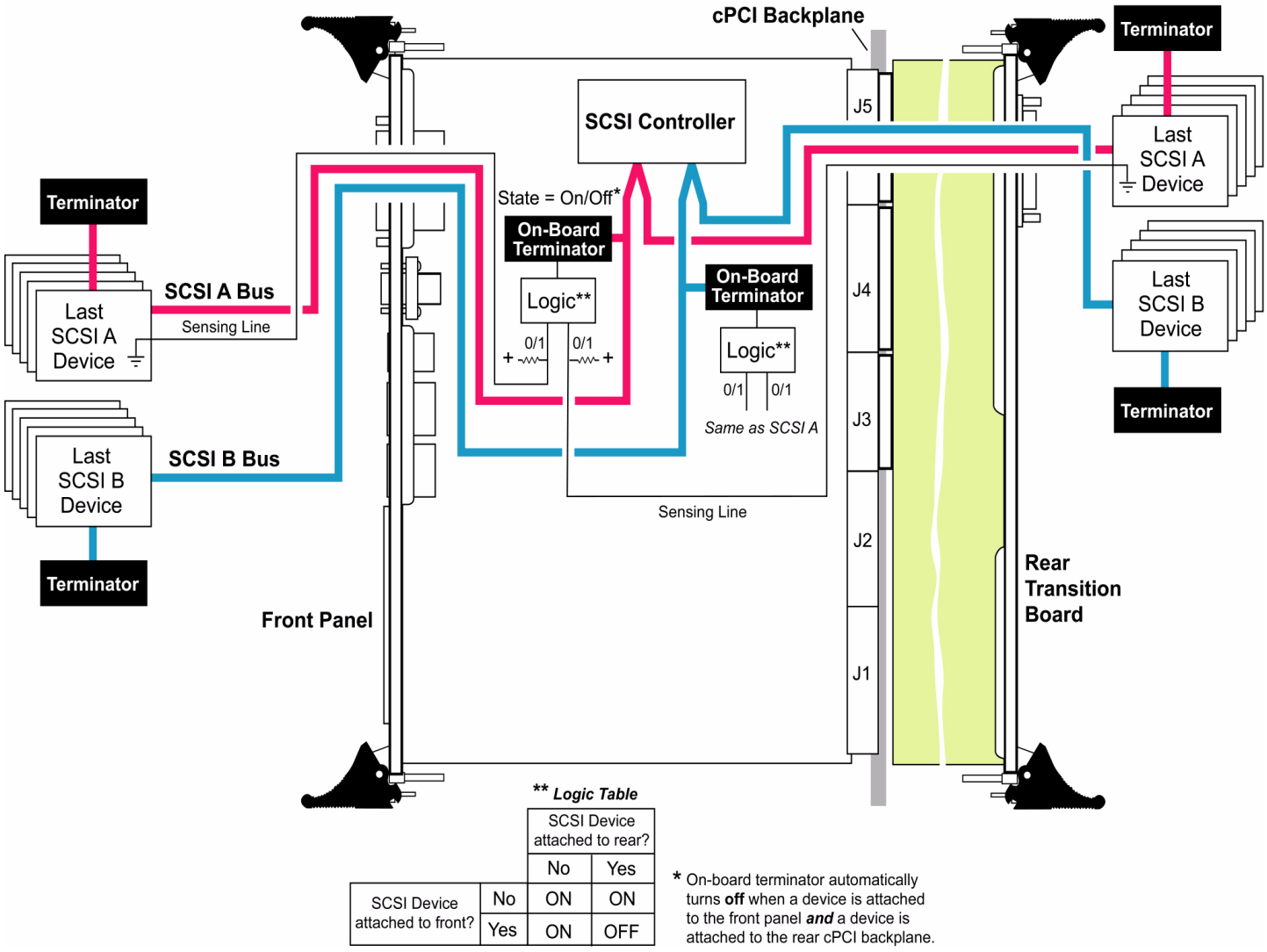


Figure 1-1. SCSI Termination on the USPIIe-cPCI Baseboard

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Caution: The auto-termination circuit of the USPII*e*-cPCI will detect the logic condition of SCSI bus A or B and automatically enable or disable on-board termination of either bus. However, the last (final) device at each end of the SCSI chain of either bus, whether at the front panel or the Rear Transition Board, must be properly terminated by the operator.

1.1.4 Ethernet A and B Connectors

Several solder beads affect the behavior of Ethernet A/B, as explained in *Table 1-2*. Make sure these solder beads are set correctly for your application purposes.

Table 1-2. Ethernet A and B Solder Bead Settings

Ethernet A/B Function	Baseboard SB2501 to SB2504, SB2506 to SB2509	Rear Transition Board SB1301 to SB1310
Accessible from front panel only	Short 1-2	Open
Accessible from rear using a 2.16-compliant cPCI backplane only	Short 2-3	Open

1.2 Install the PMC Module

If you intend to install a PMC Module onto the USPII*e*-cPCI Baseboard, you must do it before placing the Baseboard into its cPCI slot.

First, ensure that the PMC Module slot on the Baseboard has its signaling voltage polarizing key set to the proper location, and consistent with the signaling voltage used in the cPCI chassis. In other words, if your cPCI chassis has 3.3V signaling, you must verify that the polarizing key (see *Figure 1-2*, page 1-5) is set to 3.3 volts.

If the polarizing key is not in the proper key-hole, remove it and insert it into the key-hole corresponding to the V(I/O) voltage to which the backplane is configured.



Caution: Selecting a Universal PMC Module is the most elegant choice, since it can use either 3.3V or 5V to operate.

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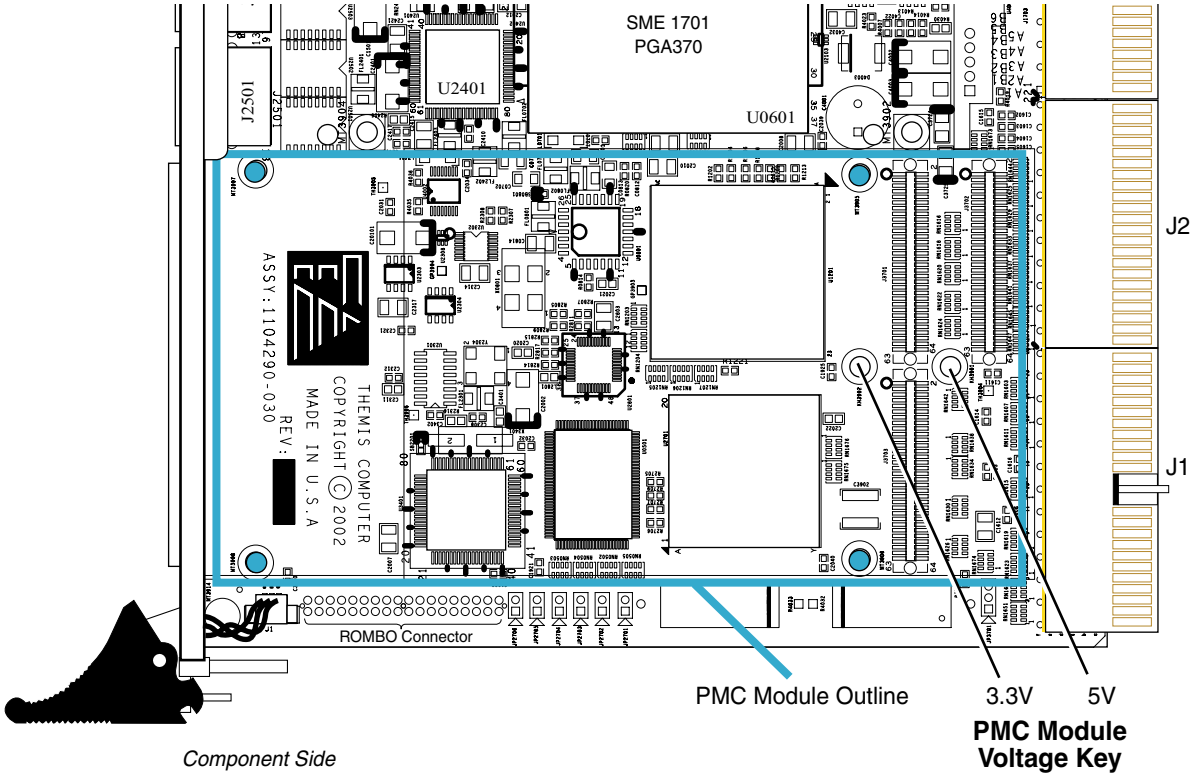


Figure 1-2. Location of the Signaling Voltage Polarizing Key

After removing the blank PMC Module plate from the faceplate (see *Figure C-1* on page C-2), attach the PMC Module to the lower portion of the Baseboard with the four screws provided by the vendor (see *Figure D-1* on page D-2).

1.3 Check the Memory Module

The memory capacity of the USPII*e*-cPCI should be specified with your order. Every USPII*e*-cPCI Baseboard shipped has a custom Memory Module (from 128 MB to 2 GB) installed, hence there is no need to add this Module to your system.

Before installing your USPII*e*-cPCI Baseboard into a cPCI backplane, check to see that the Memory Module has been installed (see *Figure D-1* on page D-2 for its location on the Baseboard).

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1.4 Install the USPIIe-cPCI Baseboard

The USPII*e*-cPCI offers the following I/O connections through its front faceplate:

- 2 LVD Ultra-2/SCSI-3 ports (68-pin 0.8-mm SCSI D) ..... *SCSI A / SCSI B*
- 2 asynchronous RS232 serial ports (9-pin mini-D) *TTY A /TTY B* (*Full Modem)*
- 1 PS/2 keyboard/mouse port (8-pin mini-DIN)
  or dual-USB port ..... *USB A / USB B*
- 2 Ethernet ports (8-pin RJ45)..... *Ethernet A / Ethernet B*
- Additional ports through a user-installed PMC Module..... *Optional*

Connect your cables to these ports after installing the Baseboard and before beginning operation (see "Attach All I/O Cables" on page 1-11).

The USPII*e*-cPCI comes with two Elma IEEE P1101.10 cPCI-type locking handles (one at the top and one at the bottom), which allow the Baseboard to be firmly locked into the 6RU cPCI backplane. In addition, the lower handle has a microswitch installed that signals whenever a board is being hot-swapped into and out of the cPCI backplane (see *Figure 1-3* on page 1-7).

Use the following steps to install the USPII*e*-cPCI Baseboard:

1. Make sure the slot at the extreme left of the cPCI backplane is vacant (see following *Note*). This is the master slot into which the USPII*e*-cPCI Baseboard will be installed (see *Figure A-2*, page A-2, for details).



Note: Not all cPCI backplanes position the master slot at the left; some position the master slot at the right or somewhere in the middle, instead. The USPII*e*-cPCI should be installed into a cPCI system slot that recognizes the delta (Δ) logo as the master slot (see *Figure A-2*, page A-2).

2. Before inserting the USPII*e*-cPCI Baseboard into the backplane, make sure both ejector handles are in the unlocked position (see *Table 1-3* on page 1-7). Guide the upper and lower rear corners of the Baseboard into an upper and lower channel of the card slot.

3. Push the faceplate evenly (at top and bottom) into the card slot until it engages the mating cPCI connectors (P1 through P5) on the cPCI backplane.

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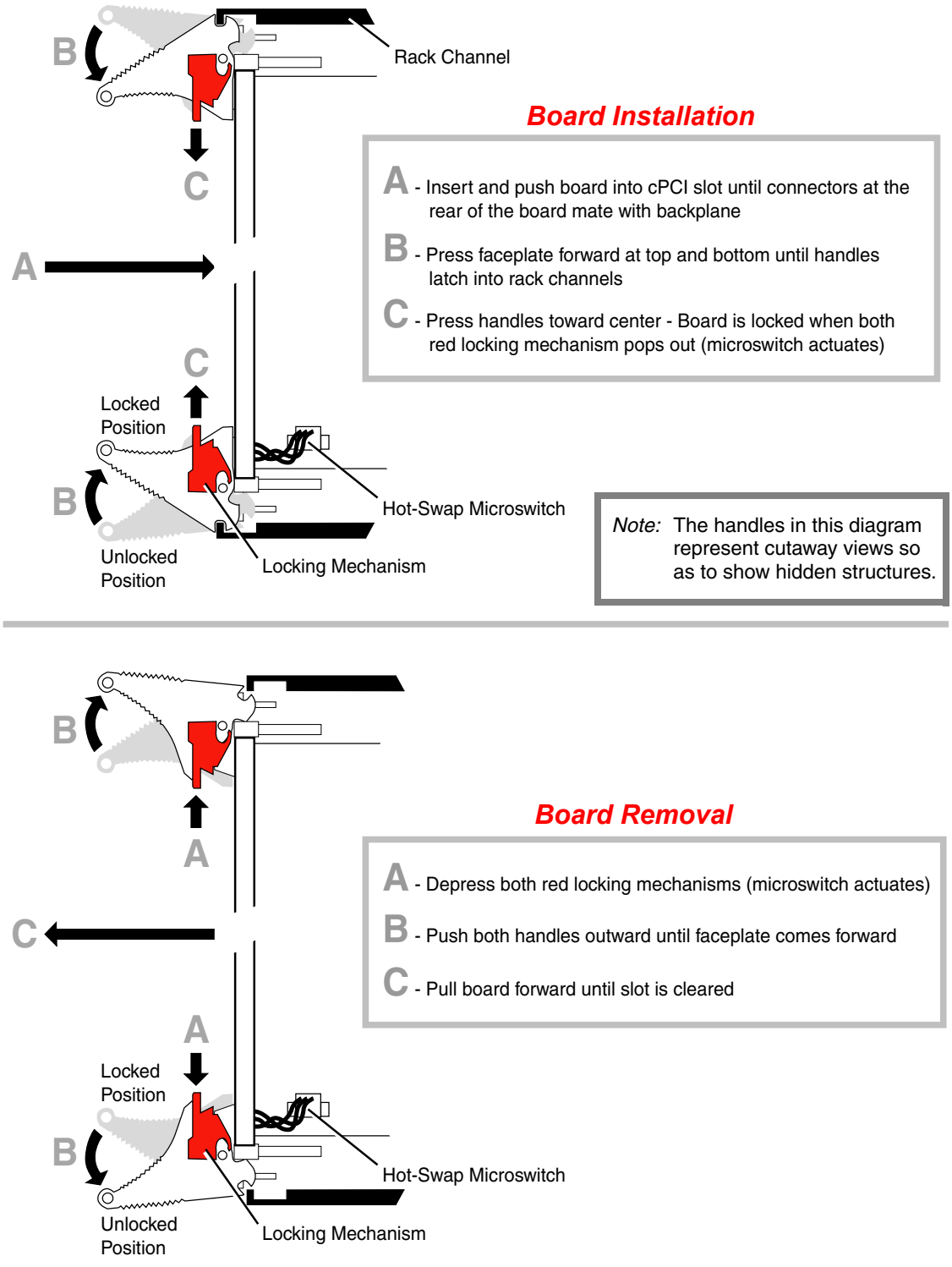


Figure 1-3. Installation (Injection) and Removal (Ejection) of the USPIIe-cPCI

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4. Continue pushing the faceplate until both handles latch into the rack channels. Press both handles toward the center of the faceplate until the red locking mechanism of both handles pops out.

5. When the Baseboard is fully installed and operable, the *yellow* (OK) and *green* (`Enable`) LEDs will light (see *Figure 1-4*, page 1-8).

1.4.1 LED Interpretation

System status LEDs on the Baseboard faceplate are illustrated in *Figure 1-4* and defined in *Table 1-3*. After all cables have been connected to the Baseboard, use *Table 1-3* to interpret all LEDs on the faceplate to determine whether the ports to which the cables are connected are operating properly.

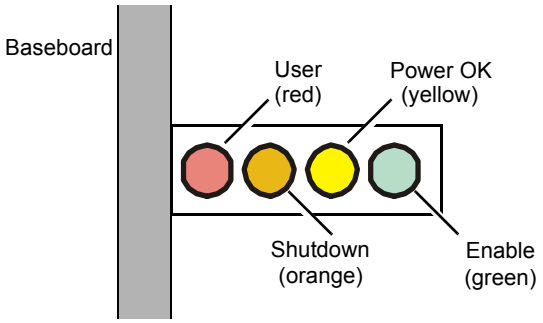


Figure 1-4. System Status LEDs on Baseboard Faceplate

Table 1-3. Definitions of Baseboard System Status LEDs

LED	Color	Definition
User	Red	*User-programmable*. Controlled through bit 0 of the Miscellaneous Register[a] of the on-board PLD logic-control chip (see *Figure 2-1* on page 2-2).
Shutdown	Orange	If LED is on, the on-board reset is active.
Power OK	Yellow	LED will turn on when Baseboard is fully powered up.
Enable	Green	If turned on, power is OK on cPCI backplane.

a—When bit 0 is set to 1, LED turns on (red).
When bit 0 is set to 0, LED turns off.
See Chapter 4 of the *USPIIe-cPCI Software Manual.*

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1.5 Install the Rear Transition Board

The Rear Transition Board attaches to the rear of the slot occupied by the USPII*e*-cPCI on the cPCI backplane (see *Figure 1-5*).

Note: The Rear Transition Board (P/N-110616) is included in the optional USPII*e*-cPCI Integration Kit, which can be ordered separately by the customer.

Use the same steps for installing the Rear Transition Board as with the Baseboard. Remember that the component side of the Transition Board is facing the same direction as the component side of the Baseboard, hence will have a reversed orientation when looking at the rear cPCI slots.

The Rear Transition Board provides connectors for:

- 2 LVD Ultra-2/SCSI-3 ports (68-pin 0.8-mm HDC SCSI-D) ...*SCSI A / SCSI B*
- 1 bi-directional parallel port (25-pin sub-D, female)
- 4 asynchronous RS232 serial ports (9-pin sub-D). *TTY A /TTY B (Full Modem)* ..... *TTY C / TTY D (Tx and Rx only)*
- Dual-USB port ..... *USB C / USB D*
- 2 audio lines (1 in, 1 out), 1 headphone out, 1 mic in (3-mm connectors)

Connect your cables to these ports after installation and before beginning operation (see “Attach All I/O Cables” on page 1-11).

[See section D.2, “Rear Transition Board”, page D-1 in Appendix D, “Board Diagrams” for a more complete description of the Rear Transition Board.]

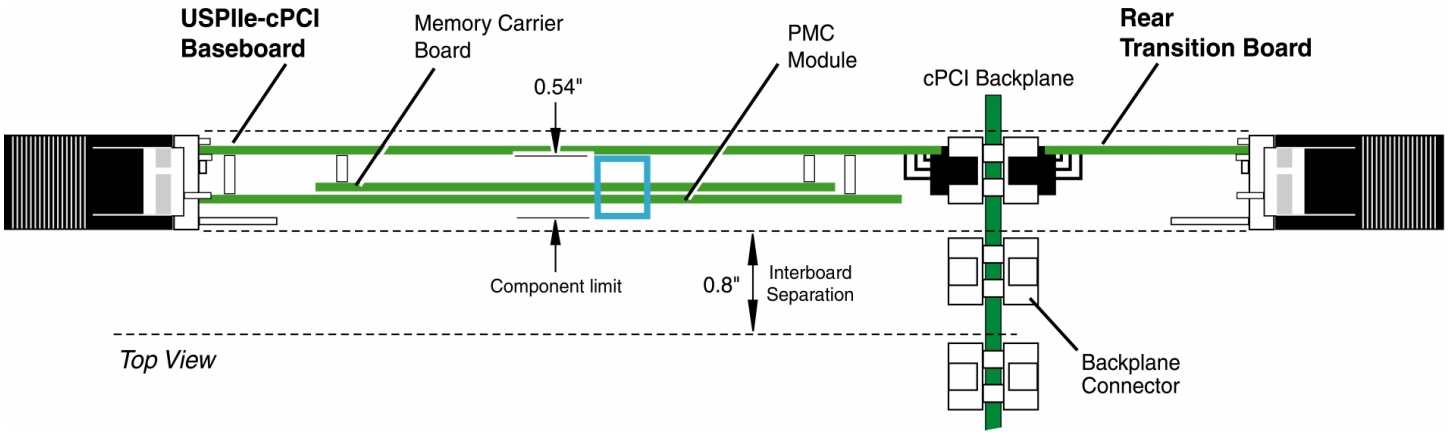


Figure 1-5. Installing the USPIIe-cPCI Rear Transition Board (Top View)

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1.5.1 LED Interpretation

Rear Transition Board cPCI status LEDs are illustrated in *Figure 1-6* and described in *Table 1-4*. After all cables have been connected to the Rear Transition Board, use *Table 1-4* to interpret all LEDs on the faceplate to determine whether the ports to which the cables are connected are operating properly.

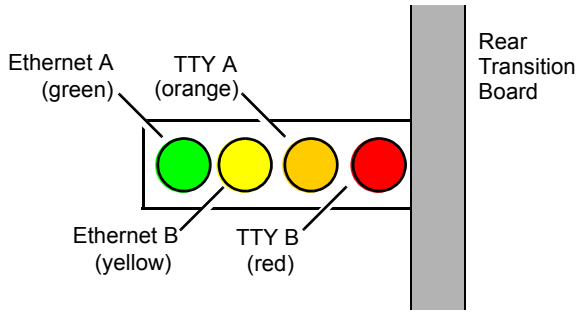


Figure 1-6. cPCI Status LEDs on Rear Transition Board

Table 1-4. Definitions of cPCI Status LEDs

LED	Color	Definition
Ethernet A	Green	*For Test Purposes Only.* Should be off under normal operation.
Ethernet B	Yellow	
TTY A	Orange	*Jumper-Pin Configurable.* If LED is active, connection is through Rear Transition Board faceplate only (see Appendix B, “Jumper-Pin and Solder-Bead Configurations”.
TTY B	Red	

1.5.2 Rear Plug-in Configuration

The Rear Transition Board is designed to be installed into a 5-row **in-line** rack configuration (see *Figure 1-5*), as opposed to an **offset** rack configuration. Characteristics of the in-line configuration are:

- Both front- and rear-mounted plug-in units (PCBs) are in alignment.
- The component sides of both front- and rear-mounted PCBs are facing in the same direction.

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1.6 Attach All I/O Cables

After the USPII*e*-cPCI Baseboard and Rear Transition Board (if needed) have been installed, attach all necessary cables to their respective ports on the front and rear panels. Connect the other ends of all cables to their respective system destinations. Consult Appendix A, “System Connectors”, for the type of connectors to use.

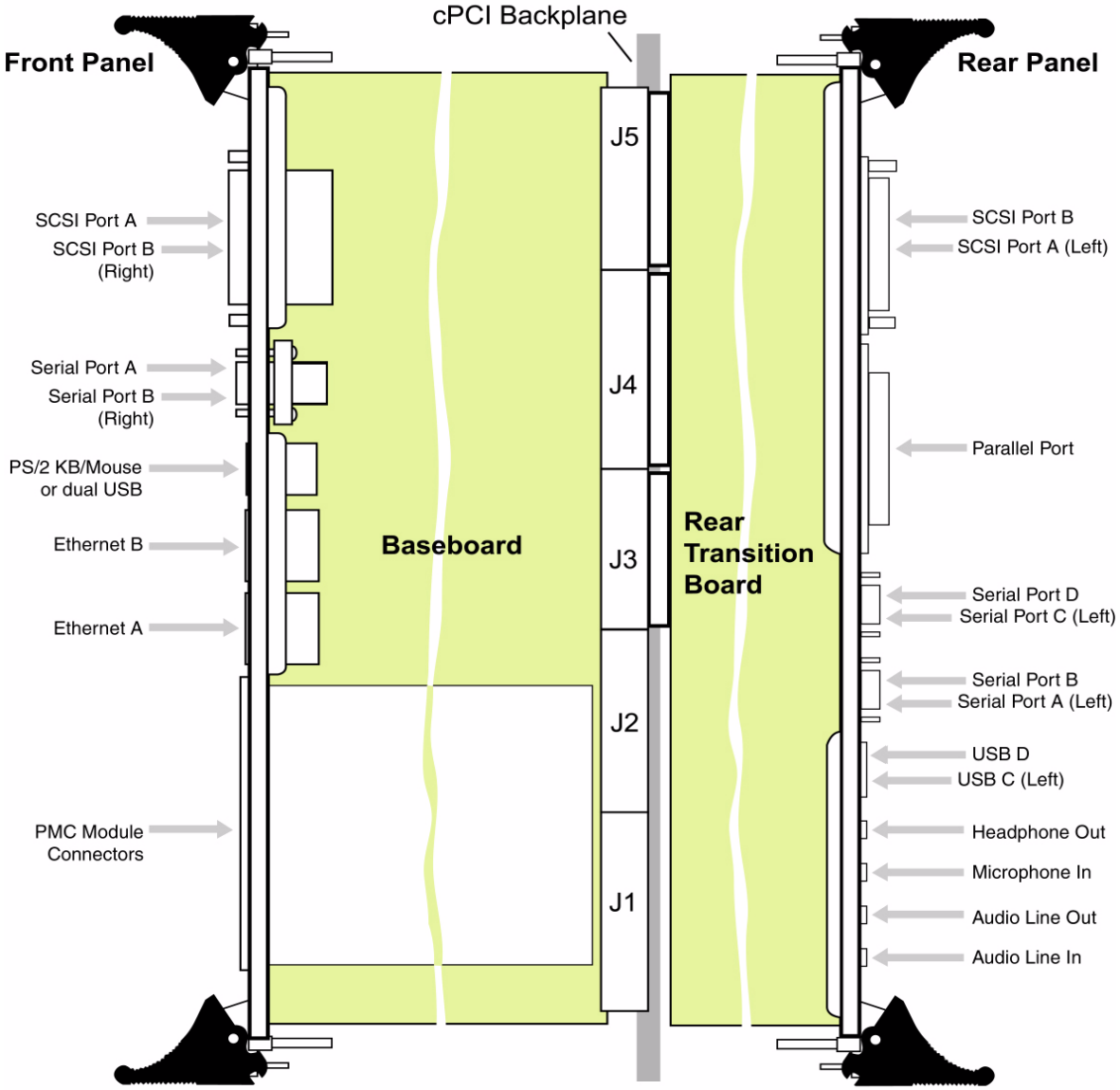


Figure 1-7. Attach all Cables to the USPIIe-cPCI System

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1.6.1 SCSI Ports A and B

It is possible to use both Baseboard Front Panel and Rear Transition Board SCSI A and/or SCSI B connections simultaneously (see *Figure 1-1* on page 1-3). As already explained in section 1.1.3, "SCSI Terminations", page 1-3, on-board termination of either SCSI bus is automatic.

All SCSI ports on the Baseboard and Rear Transition Board use the same 68-pin, 0.8-mm, miniature SCSI connectors (see Appendix A, "System Connectors" for connector pinouts), which can be converted to a standard 68-pin, 0.050-inch, SCSI-D connector (male) through an *optional* Themis adapter cable (P/N 108712).



Note: The SCSI adapter cable (P/N 108712) is included in the optional Themis USPII*e*-cPCI Integration Kit, which can be ordered separately by the customer.

You can verify proper physical connection by executing the OpenBoot command `probe-scsi-all`. This command transmits an inquiry command to SCSI devices connected to the system unit on-board SCSI interface. If the SCSI device is connected and active, the target address, unit number, device type, and manufacturer name is displayed.

The example below identifies the `probe-scsi-all` output message:

```
ok probe-scsi-all
/pci@1f,0/pci@1/scsi@8,1 ..........................SCSI B
Target 0
Unit 0 Disk QUANTUM ATLAS_V_9_WLS 0230

/pci@1f,0/pci@1/scsi@8 ............................SCSI A
Target 2
Unit 0 Disk QUANTUM ATLAS_V_9_WLS 0230

ok
```

1.6.2 Serial Ports A and B (TTYA/TTYB, *Full Modem*)

Serial Ports A and B provide signals for full modem support (see Appendix A, "System Connectors", for connector pinouts). When the Rear Transition Board is connected to the system, access to Serial Port A and/or Serial Port B can be either through the Baseboard Front Panel or the Rear Transition Board—but not both. This

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access depends on the settings of jumper pins JP1001 and JP1002 on the Rear Transition Board (see Appendix B, "DIP-Switch, Jumper-Pin, and Solder-Bead Configurations").



Note: A 9-pin D-shell serial cable (P/N-108113), suitable for connecting to Serial Ports A, B, C, and D, is included in the optional USPII*e*-cPCI Integration Kit, which can be ordered separately by the customer.

1.6.3 Serial Ports C and D (TTYC/TTYD, *Tx and Rx Only*)

Serial Ports C and D provide signals for Tx (transmit data) and Rx (receive data) only (see Appendix A, “System Connectors”, for connector pinouts). Access to Serial Port C and Serial Port D is only through the Rear Transition Board.



Note: A 9-pin D-shell serial cable (P/N-108113), suitable for connecting to Serial Ports A, B, C, and D, is included in the optional USPII*e*-cPCI Integration Kit, which can be ordered separately by the customer.

1.6.4 DIN-8 Port (*DIN-8-Port Version Only*)

The 8-pin mini-DIN port (female) on the Baseboard faceplate (see Appendix A, “System Connectors”, for connector pinouts) can be used to connect to:

- a PS/2 keyboard and mouse through a special split cable (P/N-110104-002), or
- two USB ports through a second split cable (P/N-110473-001), resulting in USB-A and USB-B.

1.6.5 USB Ports A and B (*USB-Port Version Only*)

The dual-USB port on the Baseboard faceplate (see Appendix A, “System Connectors”, for connector pinouts) can be used to connect to up to two USB devices, including a USB keyboard/mouse.

1.6.6 USB Ports C and D (*Rear Transition Board Only*)

The dual-USB port on the Rear Transition Board faceplate (see Appendix A, “System Connectors”, for connector pinouts) can be used to connect to up to two USB devices, including a USB keyboard/mouse.

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1.6.7 Ethernet Ports A and B

The USPII*e*-cPCI features two RJ45 Ports (A and B) on the Baseboard Front Panel for 10/100Base-T Ethernet interface connections.



Note: How the Ethernet ports are accessed are determined by solder beads settings on both the Baseboard and Rear Transition Board (see section 1.1.4, “Ethernet A and B Connectors”, page 1-4, and Appendix B, "DIP-Switch, Jumper-Pin, and Solder-Bead Configurations").

1.6.8 Parallel (Printer) Port (*Rear Transition Board Only*)

A printer can be attached to the parallel port (female) of the Rear Transition Board through a DB25 (male) cable connector (see Appendix A, “System Connectors”, for connector pinouts).

1.6.9 PMC (Expansion) Module Slot

The Baseboard contains a single PMC Module slot (see section 1.2, “Install the PMC Module”, page 1-4) that will contain I/O connector(s) associated with the Module installed. Consult the manufacturer’s operating manual for the type of cable(s) to use.

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Specification Section

Chapter 2

USPIIe-cPCI Specifications

2.1 Overview

The USPII*e*-cPCI was designed to provide an UltraSPARC-II*e* platform in an industry-standard single-slot cPCI, 6RU form factor. The USPII*e*-cPCI is based on an UltraSPARC-II*e* processor and a proprietary coplanar memory board.

The USPII*e*-cPCI is available at processor speeds of 500 MHz (256-KB L2-cache), 600, or 650 MHz (512-KB L2-cache)—see *Table 2-1* (boldface fonts indicate the default) and *Figure 2-1*, page 2-2.



Note: Solder-bead settings are the same for 500 MHz and 650 MHz, and depend on the type of CPU ordered (see *Table 2-1*).

Table 2-1. CPU Speed Settings

SB2703	SB2705	CPU[a] Speed (600/650 MHz)	CPU[b] Speed (500 MHz)
Short 1-2	**Short 1-2**	650 MHz	500 MHz
Short 1-2	Short 2-3	600 MHz	*Not applicable*
Short 2-3	Short 1-2	*Not applicable*	*Not applicable*
Short 2-3	Short 2-3	*Not applicable*	*Not applicable*

a—USPIIi-type.
b—USPIIe-type.

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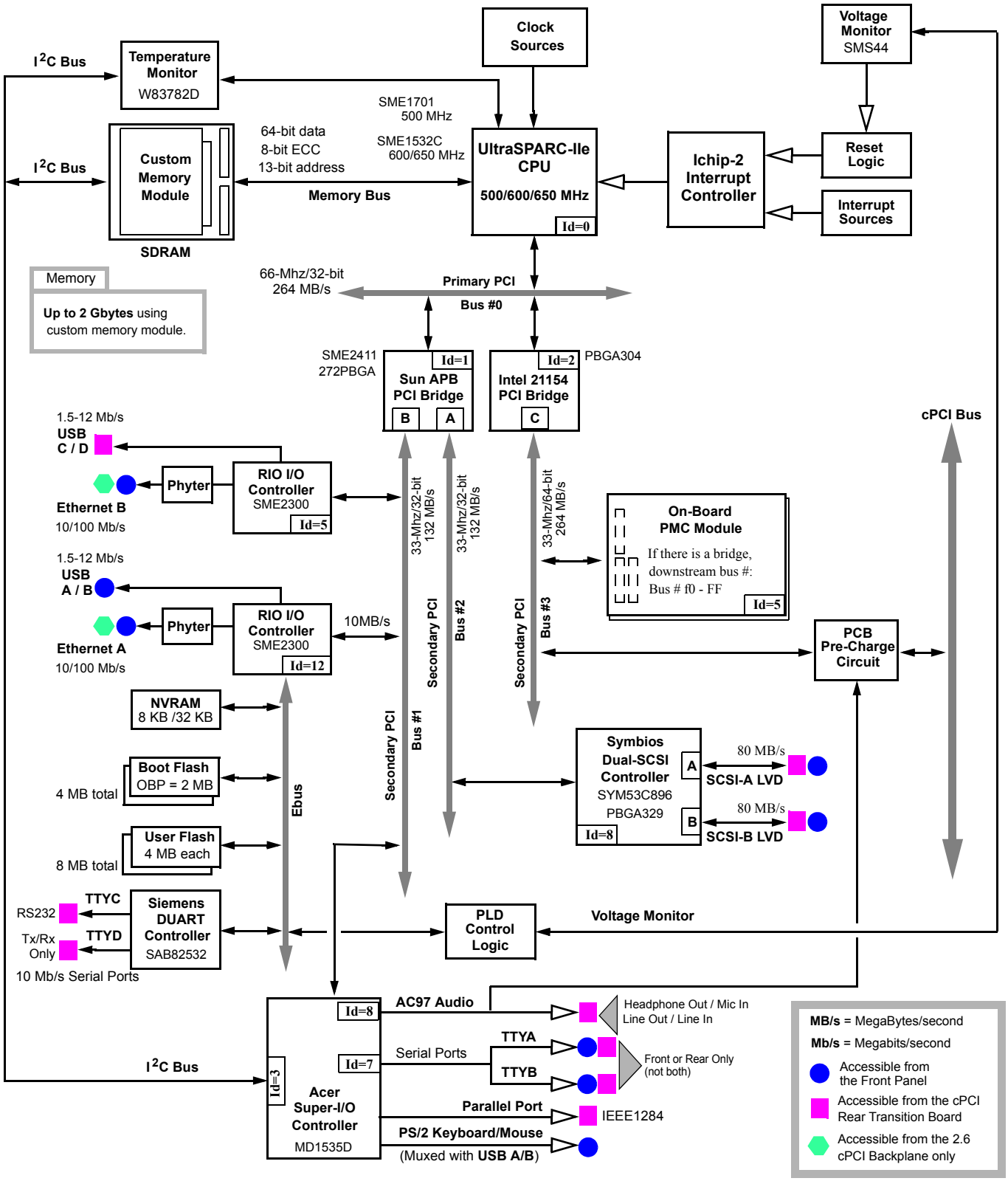


Figure 2-1. USPIIe-cPCI Block Diagram

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The Memory subsystem utilizes a custom high-capacity Themis Memory Module that supports several memory configurations up to 2 GigaBytes (see *Table 2-2*).

Table 2-2. Memory Configurations

Total Memory Capacity	Custom Themis Memory Module Supported
128 MB	YES
256 MB	YES
512 MB	YES
1 GB	YES
2 GB	YES

The local I/O subsystem is PCI-based, with separate PCI channels provided for I/O functions and external cPCI backplane access.

Specifically, the **Baseboard Front Panel** includes the following connectors (see Appendix C, "Front and Rear Panel Diagrams"):

- 2 LVD Ultra-2/SCSI-3 ports (68-pin 0.8-mm SCSI D) ..... *SCSI A / SCSI B*
- 2 asynchronous RS232 serial ports (9-pin mini-D) *TTY A /TTY B* (*Full Modem)*
- 1 PS/2 keyboard/mouse port (8-pin mini-DIN)
  or dual-USB port ..... *USB A / USB B*
- 2 Ethernet ports (8-pin RJ45)..... *Ethernet A / Ethernet B*
- Additional ports are available through a user-installed PMC Module

The cPCI backplane provides signals through **Rear Transition Board** connectors for:

- 2 LVD Ultra-2/SCSI-3 ports (68-pin 0.8-mm HDC SCSI-D) ... *SCSI A / SCSI B*
- 1 bi-directional parallel port (25-pin sub-D)
- 4 asynchronous RS232 serial ports (9-pin sub-D). *TTY A /TTY B* (*Full Modem)*
  ..... *TTY C / TTY D (Tx and Rx only)*
- Dual-USB port ..... *USB C / USB D*
- 2 audio lines (1 in, 1 out), 1 headphone out, 1 mic in (3-mm connectors)

[See Appendix A, "System Connectors", for details on the cPCI backplane interface.]

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2.2 System Specification

2.2.1 Processor & Memory Subsystems

Table 2-3 and *Table 2-4* contain processor and memory subsection specifications.

Table 2-3. Processor Specifications

Feature/Function	Specifications
Processor	UltraSPARC-IIe
Processor Speed	500, 600, and 650 MHz
Performance 650 MHz 600 MHz	 239 SPECint2000 @ 650 MHz (estimate) 260 SPECfp2000 @ 650 MHz (estimate) 220 SPECint2000 @ 600 MHz (estimate) 240 SPECfp2000 @ 600 MHz (estimate
Internal Cache	512 KB (600/650 MHz); 256 KB (500 MHz)
I/O Bus Interface	32 bit/66MHz PCI data path from CPU

Table 2-4. Memory Specifications

Feature/Function	Specifications
Main Memory	Custom Memory Modules for 128 MB to 2 GB (gigabytes)
Memory Bus Interface	72 bit Data Path from CPU, including 8 bit ECC 2 to 1 Interleave to SDRAM 13 bit Address Bus 3.3V Level Interface
Memory Modules	Custom Memory Module only (see *Table 2-2*, page 2-3)
Total Memory Configurations	From 128 MB to 2 GB (see *Table 2-2*, page 2-3)

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2.2.2 Auxiliary Functions

Table 2-5 summarizes the functional specifications of the auxiliary functions. These specifications apply to all product configurations.

Table 2-5. Auxiliary Functions Specifications

Feature/Function	Specifications
Flash Memory	Three (3) 4-MB Flash devices
NVRAM/TOD	8 KB, battery-backed UPI Static RAM plus timekeeper
System Status LEDs	Four LEDs are located on Front Panel of the USPIIe-cPCI and four LEDs on the Rear Transition Board [See *Figure C-1*, page C-2, Appendix C, ”Front and Rear Panel Diagrams”]
Watchdog Timers	*Two-Level Watchdog:* Level One: Interrupt Level Two: POR Reset
Voltage Sensors	*On-board monitoring:* Vdd-core, 3.3V, and 5V —USPIIe-cPCI is reset when any of these voltages are out of tolerance *cPCI backplane monitoring:* 3.3V and 5V —USPIIe-cPCI is reset when any of these voltages are out of tolerance *Environmental monitoring:* Vdd, 3.3 V, 5 V, +-12 V
Temperature Sensor	Monitors whether the CPU temperature stays within a specified range Range can be changed by software (OBP firmware)

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2.3 Environmental Specification

Table 2-6. USPIIe-cPCI Operating Environmental Specifications

Description	Minimum Value	Maximum Value
Temperature Range	-5°C	55 C
Humidity Range, relative non-condensing at 104°F (40°C)	0%	95%
Altitude Range	0 feet	9,843 feet (3,000 meters)
Air Flow (inlet)	300 lfm air flow at 50° C @ 600 MHz minimum	

Table 2-7. USPIIe-cPCI Non-operating Environmental Specifications

Description	Minimum Value	Maximum Value
Temperature Range	-40° C	85° C
Humidity Range, relative non-condensing at 104°F (40°C)	0%	95%
Altitude Range	0 feet (0 meters)	38,370 feet (12,000 meters)

2.4 Estimated Power Requirements

Table 2-8. Estimated Power Requirements

USPIIe-cPCI Configuration (USPIIe-cPCI/1 with 650 MHz processor)	Watts Dissipation (typical)
512 MBytes memory	21 Watts
1024 MBytes memory	23 Watts
2048 MBytes memory	23.5 Watts

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Overview Section

Chapter 3

Hardware Overview

The following sections provide a description of the major components of the USPII*e*-cPCI. Detailed explanations of certain subsystems are provided in later chapters.

3.1 UltraSPARC-II*e* Processor and Cache

The Central Processor Unit (CPU) that is used in the USPII*e*-cPCI is the Sun Microsystems UltraSPARC-II*e* (SME1532C, 600/650 MHz; SME1701, 500 MHz), which is described in the block diagram of *Figure 3-1* on page 3-2. The CPU is available in operating speeds of 500, 600, or 650 MHz.

USPII*e*-cPCI architecture complies with the SPARC V9 instruction set, which enables the system to use a wide range of peripherals and the high-performance Solaris operating system. For details on the UltraSPARC-II*e* CPU processor, refer to the Themis *USPIIe Software Manual* (110553-023), the Sun *UltraSPARC-IIe Processor Data Sheet* (SME1701CPGA-400/500), and the Sun *UltraSPARC-IIe User's Manual* (806-tbd-00]).

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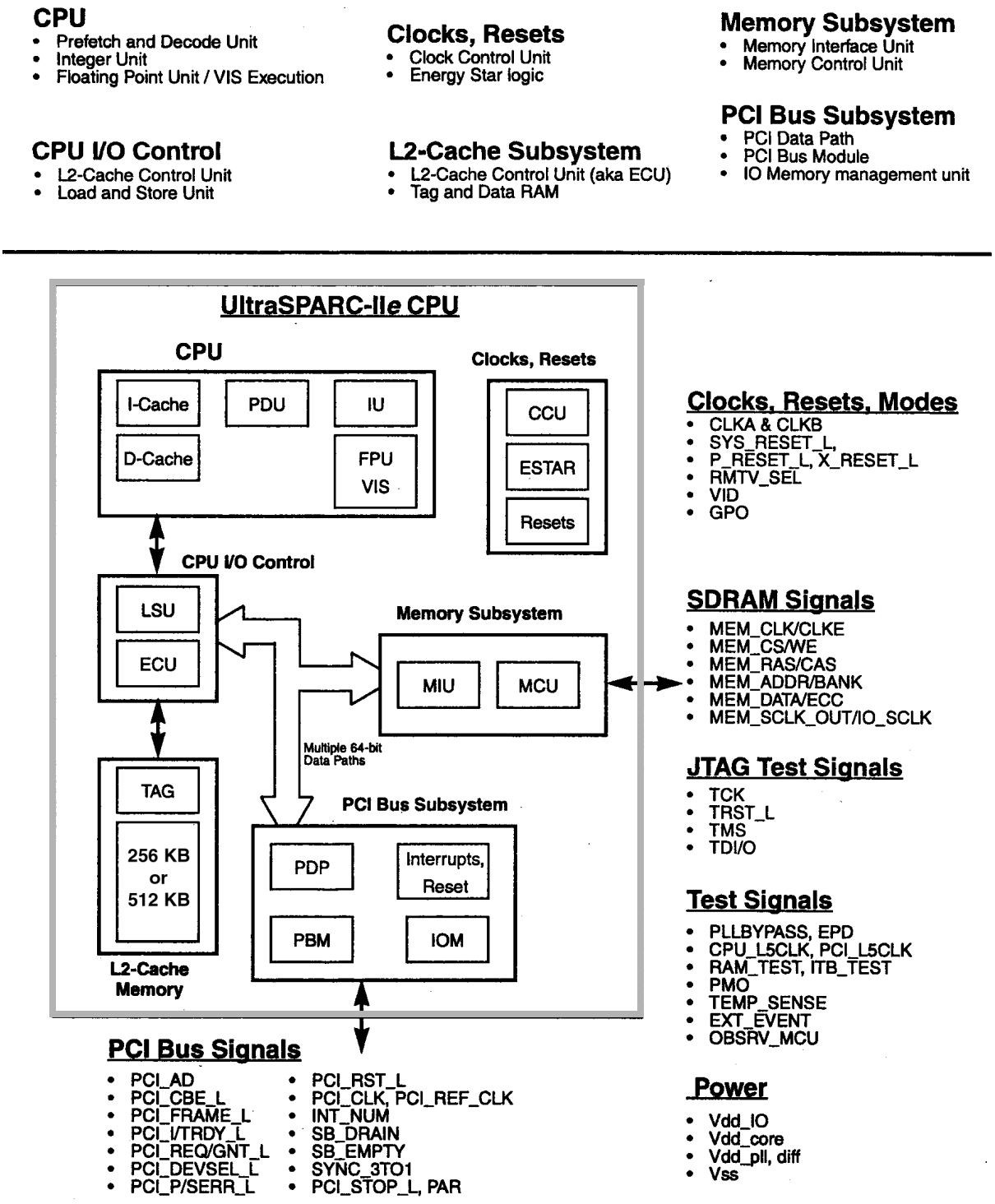


Figure 3-1. UltraSPARC-IIe CPU Block Diagram

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3.2 USPIIe-cPCI iChip-2 Interrupt Controller

The USPII*e*-cPCI iChip-2 Interrupt Controller manages system interrupts.

The interrupt controller on the iChip-2 accepts all interrupts from the USPII*e*-cPCI subsystems (up to 41 interrupts) and delivers encoded interrupts on the six interrupt lines routed to the UltraSPARC-II*e* microprocessor. The interrupts received by the iChip-2 are not passed to the UltraSPARC-II*e* in the order they are received. Instead, a priority level is assigned. Eight interrupt levels are implemented in hardware.

3.3 PCI-to-PCI Bridges

The USPII*e*-cPCI fans out the single 66-MHz/32-bit primary PCI bus (see *Figure 2-1*, page 2-2) into three secondary busses:

- Two 33-MHz/32-bit PCI busses using the Sun APB PCI-to-PCI interface chip
- One 33-MHz/64-bit PCI bus using the Intel 21154 PCI-to-PCI interface chip

The 66-MHz primary PCI-to-CPU bridge can achieve a peak bandwidth of 264 MB/sec. Within the USPII*e*-cPCI, the two 33-MHz/32-bit PCI busses are referred to as PCI-A and PCI-B and the single 33-MHz/64-bit PCI bus is referred to as PCI-C.

3.3.1 Sun Advanced PCI Bridge (APB)

One Sun secondary PCI bus is dedicated to on-board devices through two Sun Rio I/O controller chips (see following section "Sun Rio I/O Controller" on page 3-4) and an AcerLabs Super I/O Controller. The second Sun secondary PCI bus is used to access SCSI Port A and SCSI Port B through a SYM53C896 SCSI controller chip.

3.3.2 Intel 21154 PCI-to-PCI Bridge

The Intel 21154 PCI-to-PCI bridge complies with *PCI Local Bus Specification*, Revision 2.2, and has a 66-MHz/32-bit primary bus interface and a 33-MHz/64-bit secondary interface.

The 21154 provides full support for delayed transactions, which enables the buffering of memory read, I/O, and configuration transactions. The 21154 has separate posted write, read data, and delayed transaction queues with significant buffering capability. In addition, the 21154 supports buffering of simultaneous, multiple, posted write, and delayed transactions in both directions.

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Among the features of the 21154 are a programmable 2-level secondary bus arbiter, an IEEE standard 1149.1 JTAG interface, live insertion support, a 4-pin general-purpose I/O interface, individual secondary clock disables, and enhanced address decoding. The 21154 has enough clock and arbitration pins to support nine PCI bus master devices directly on its secondary interface. The 21154 allows two PCI buses to operate concurrently. This means that a master and a target on the same PCI bus can communicate while the other PCI bus is busy. This traffic isolation increases system performance.

3.4 Sun Rio I/O Controller

Sun's Rio I/O controller (SME2300) incorporates Ethernet, USB, and Ebus interfaces (see *Figure 2-1*, page 2-2). The Ethernet port autosenses the port speed as either 10 or 100 Mbits/sec, with no pin-jumpers required to set either rate.

The Ebus interface is used on only one of the Rio chips, and supports the NVRAM, boot flash and two user flashes, the system PLD control logic chip, and the DUART (dual UART). The DUART controls both TTYC (RS232) and TTYD (RS232) serial ports, which use transmit-data (Tx) and receive-data (Rx) signals only.

3.5 Symbios Dual-SCSI Controller

The Symbios Dual-SCSI Controller (SYM53C896) provides two LVD UltraWide SCSI-3 (Ultra3) interfaces (80 MB/sec). In order to balance throughput, it is attached directly to the 33-MHz/32-bit PCI-B bus segment connected to the APB PCI-to-PCI bridge. A maximum burst rate of up to 132 MB/sec is supported.

3.6 PLD

The PLD (Programmable Logic Device) on the USPII*e*-cPCI resides on the Ebus of one of the two Sun Rio I/O Controllers. The PLD has two main functions: one is to implement miscellaneous registers and manipulate the address map of Flash PROM devices; the other is to implement the reset logic.

[See Chapter 4, "Programmable Logic Device", for more information.]

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3.7 AcerLabs Super-I/O Controller

The Acer (M1535D) Super-I/O controller chip controls the AC97 (Audio Codec 97) audio, the IEEE 1284 parallel port, the PS/2 keyboard/mouse (multiplexed with USB A and B), and both TTYA and TTYB ports with full modem support. Each component is individually configured to maximize the performance of the USPII*e*-cPCI.

3.8 Siemens DUART Controller (SAB82532)

The Siemens DUART SAB82532 Enhanced Serial Communications Controller provides support for Serial Ports C and D. A maximum external data transfer rate of 460,800 bauds is attainable on each port.

3.9 Flash Memory

The USPII*e*-cPCI includes three (3) Flash EPROM devices (4-MB), located on the USPII*e*-cPCI solder side and accessible through the USPII*e*-cPCI Ebus. Any Flash can be jumper-configurable as the boot device.

The boot Flash normally contains Sun's OBP or another BIOS boot ROM. The mapping of each Flash is largely configurable by the PLD. It is also possible to divide each flash into two (2) sections, permitting a total of six (6) on-board boot devices.

To initially bring up the board, an additional external boot device (called ROMBO) is attached through a connector on the bottom edge of the USPII*e*-cPCI Baseboard (see *Figure D-1*, page D-2). *This external boot feature is for Themis use only.*

3.10 NVRAM and TOD

The Non-Volatile RAM (NVRAM) and a Time-of-Day (TOD) clock are both contained in the timekeeper chip (SGS-Thomson, M48T59Y-70MH1). The NVRAM has its own lithium battery to operate the clock and maintain the contents of the NVRAM during power-off situations.

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The battery device is an SGS Thomson Microelectronics BT1402. This single lithium battery provides backup for approximately 10 years and the real-time clock circuitry provides accuracy of +/- one (1) second per day.

NVRAM and TOD are programmed using the FORTH toolkit in the OpenBoot PROM (OBP).

3.11 Memory Subsystem

As seen in *Figure 3-2*, the USPII*e*-cPCI supports a single custom Themis Memory Module, plugged directly into the USPII*e*-cPCI (see *Figure 3-3*, page 3-7). The memory data path is 72 bits with 8 bits assigned to ECC. Memory complies to PC-133 timing.

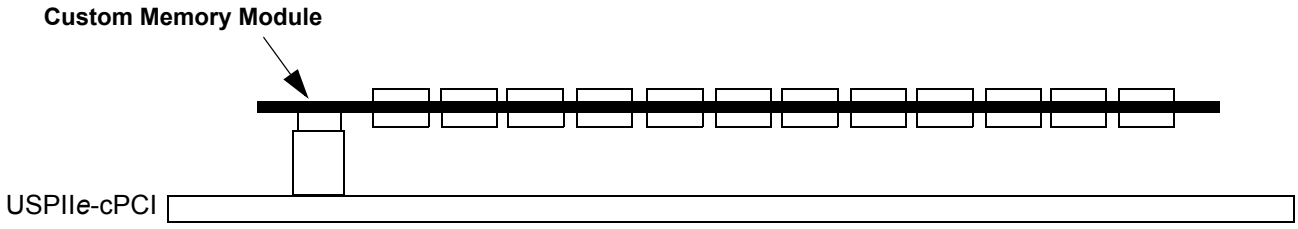


Figure 3-2. Custom Memory Module Topology (Side View)

Memory capacities are offered in **128 MB** (MegaBytes), **256 MB**, **512 MB**, **1 GB**, and **2 GB** capacities (see *Table 2-2*, page 2-3), and the memory subsystem includes Error Correction Code (ECC). A single bit error in a 64-bit word is corrected without loss of a cycle.

In designing the memory subsystem, considerable attention was paid to minimizing overall power consumption. The typical active power consumption of a USPII*e*-cPCI with a 1-GB memory module is 23 watts (see *Table 2-8* on page 2-6 for other power requirements).



Caution: Because of the *cPCI Specification* requiring a 0.8-inch interboard separation (see *Figure 1-5* on page 1-9) between cPCI slots, only one Memory Module can be installed onto a USPII*e*-cPCI Baseboard (*stacking is not supported*).

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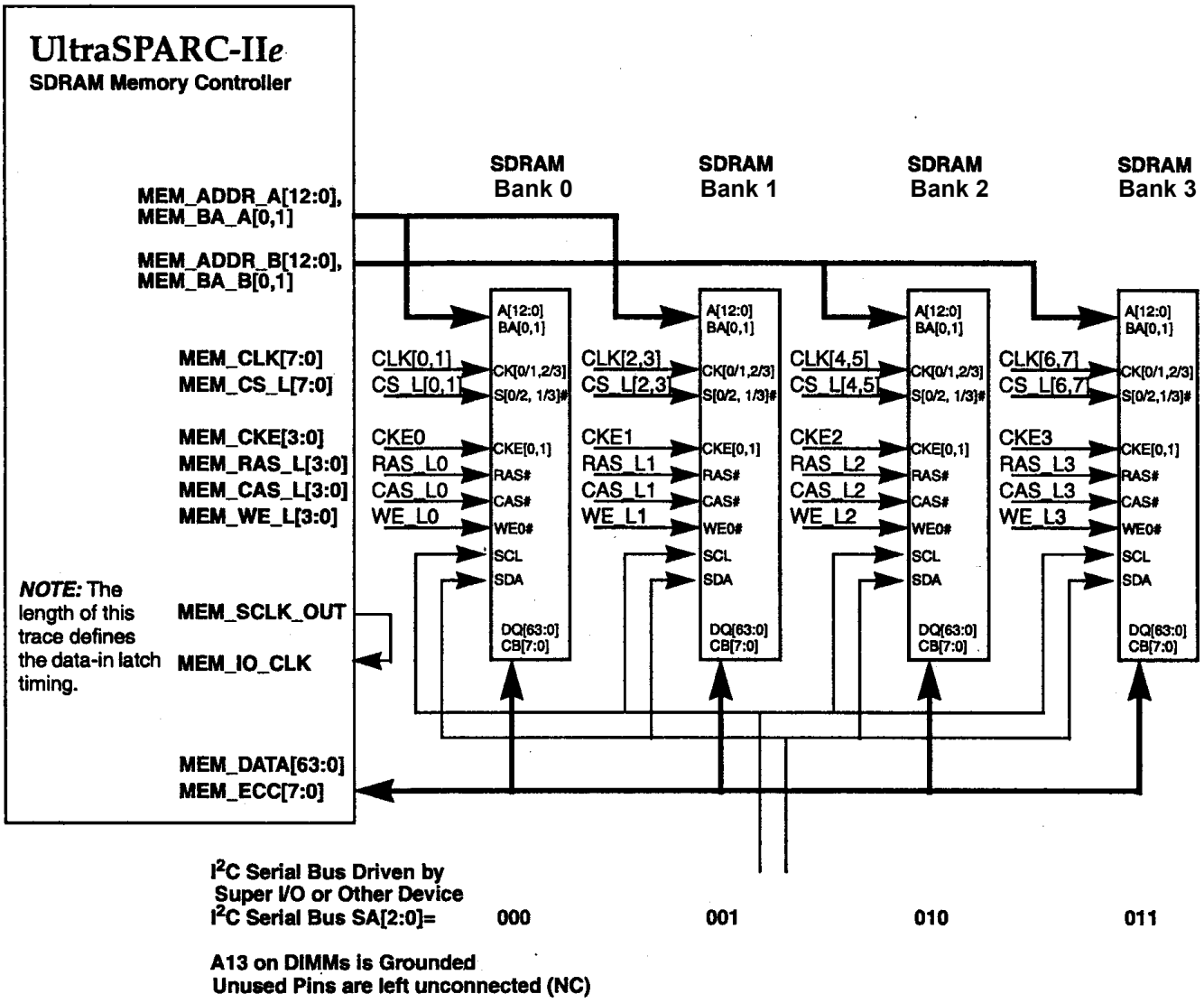


Figure 3-3. SDRAM Memory Subsystem

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3.12 Open Boot PROM

The Open Boot PROM (OBP) can be accessed through the Ebus. OBP code is contained in Flash Memory and provides the following functionality:

- Runs start-up diagnostic tests.
- Initializes the host machine.
- Reads non-volatile RAM (NVRAM) and executes the boot sequence. The Diagnostic Executive or standalone programs can also be executed.
- Includes the abbreviated system monitor. Entry into the system monitor is signified by the "`ok`" prompt. If a boot attempt fails, the OBP tries to start the abbreviated system monitor.
- Supplies program code for the FORTH Toolkit; the on-board diagnostics contain the FORTH Toolkit and the FORTH language interpreter. Entry into the FORTH Toolkit is signified by the "`ok`" prompt.

For more information on the OBP please refer to the *OpenBoot Command Reference* from Sun Microsystems and the Themis Computer *USPIIe-cPCI Software Manual.*

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Operation Section

Chapter 4

Programmable Logic Device

4.1 Introduction

The Programmable Logic Device or PLD (see *Figure 2-1*, page 2-2) resides on the Ebus of one of the two Sun Rio I/O Controllers on the USPII*e*-cPCI. It provides the following functions:

- Implements the reset logic of the USPII*e*-cPCI
- Implements an extensive boot address decoder and mapping control of the flashes
- Provides miscellaneous registers to control the behavior of the USPII*e*-cPCI
- Implements a 2-level Watchdog
- Implements power management and thermal management
- Implements miscellaneous features like cPCI slot-ID detection

4.2 Flash Mapping and Boot Control

Flash mapping is controlled by Jumper Pins JP2701, JP2702, and JP2703 (see *Table B-1*, page B-2). Write accesses to the Flash memory can be enabled or disabled using Jumper Pins JP2201, JP2202, and JP2203.

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Selection of the boot device (FLASH0, FLASH1, FLASH2, or ROMBO connector) is controlled by the combined settings of Jumper Pins JP2701 and JP2702 (see *Table B-2*, page B-5).

4.3 PLD Registers

The PLD implements the following registers:

Table 4-1. PLD Register Address Map

Register	Register Name	Offset Address	Description
0	pld_ID/rev	0x1FF.F120.0000	Revision and ID of the base_Usp2e_PLD
1	flash_status	0x1FF.F120.0002	Boot addess space mapping
2	cpci_slot_ID	0x1FF.F120.0003	USPIIe-cPCI id status register
3	*Reserved for future use*	0x1FF.F120.0004	
4	patch_status	0x1FF.F120.0005	Status of JP2704, JP2705, and JP2706
5	test_status	0x1FF.F120.0006	Presence bits of plug-in boards
6	voltage_status	0x1FF.F120.0007	Voltage status
7	TTY/KBM_config	0x1FF.F120.0008	TTY ports and Keyboard/Mouse setting (Front panel versus cPCI)
8	SCSI_A_status	0x1FF.F120.0009	SCSI-A termination and others
9	misc_status	0x1FF.F120.000a	
10	watchdog 1 counter	0x1FF.F120.0010	Watch dog 1 counter loaded value
11	watchdog 1 Limit	0x1FF.F120.0014	Watch dog 1 limiter loaded value
12	watchdog 1 status	0x1FF.F120.0018	Watchdog 1 status
13	watchdog 2 counter	0x1FF.F120.0020	Watch dog 2 counter loaded value
14	watchdog 2 Limit	0x1FF.F120.0024	Watch dog 2 limiter loaded value
15	watchdog 2 status	0x1FF.F120.0028	Watchdog 2 status
16	watchdog int mask	0x1FF.F120.0040	Watchdog interrupt mask
17	semaphore status	0x1FF.F120.00F0	Semaphore status and requester flag
18	semaphore request1	0x1FF.F120.00F1	requester’s image of semaphore

[See the *USPIIe-cPCI Software Manual*, Chapter 4, “PLD Register Set”, for more details.]

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4.4 2-Level Watchdog

A 2-level watchdog is implemented in the PLD. The states of the watchdog are “normal”, “warning”, and “failed”. Each watchdog may be programmed to expire within the range of 0.1 seconds to approximately 6500 seconds and contains a 16-bit counter register, a 16-bit limit register, and an 8-bit status register. The counter register and the status register are read-only while the limit register is read/write. Refer to the *USPIIe-cPCI Software Manual* for a description of the Watchdog Registers.



Note: The 2-level watchdog implemented in the PLD is entirely separate from the internal watchdog of the UltraSPARC-II*e*. For more information on the watchdog implemented in the UltraSPARC-II*e* refer to the *UltraSPARC-IIe User’s Manual*, published by SUN Microelectronics (SME).

When no watchdogs have expired, the USPII*e*-cPCI is in a “normal” state. When the level 1 watchdog expires, a maskable interrupt is sent to the iChip, and the USPII*e*-cPCI is considered to be in a ‘warning’ state. Upon expiration, the level 2 watchdog causes a “serious alarm condition”. The USPII*e*-cPCI is then considered to be in a “failed” state. This signal will generate a non-maskable `power-on-reset` to be issued to the UltraSPARC-II*e* and propagated throughout the system.

Upon expiration, any higher-order watchdog will reset a lower-order watchdog; i.e., the expiration of watchdog 2 resets watchdog 1 to its initial, programmed states.

4.5 Voltage Monitoring

The USPII*e*-cPCI uses several voltage sources in order to operate. 5V, 3.3V, and Vdd-core (CPU) are monitored by the SMS44 voltage monitor/controller, which generates a `power-ok` signal to the PLD only if the three voltage sources are within tolerance.

4.6 Temperature Management

The PLD is involved in the temperature management of the board, although an external temperature monitor IC chip is used.

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The temperature sensor/monitor is composed of the I^2C W83782D connected to a sensor (diode) located in the UltraSPARC-II*e* CPU. A temperature threshold can be defined by software. If the CPU junction temperature exceeds the programmed thresholds, W83782D generates an over-temperature indicator signal to the PLD.

If the CPU thermal shutdown option is enabled (through PLD control register #10), the PLD will generate an over-temperature interrupt to the iChip and force a `SYS-RESET` to the CPU.

[See the *USPIIe-cPCI Software Manual*, Chapter 3, “Temperature Monitoring”, for more details.]

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Operation Section

Chapter 5

Resets

5.1 Overview

This chapter presents a brief discussion of the reset structure of the USPII*e*-cPCI. The various types of resets, some possible reset sources, and reset effects are explained.

Resets are used to force all or part of the system into a known state. A Reset is defined as any action or signal that places the UltraSPARC-II*e* in Reset, Error, or Debug State (RED_State). This state will be entered under any of the following conditions:

- A trap is taken when:
  - — Trap_Level = Max_Trap_Level - 1
- One of the reset request signals (POR, XIR, WDR) becomes active
- A reset request, SIR, is issued when the Trap_Level < Max_Trap_Level (if Trap_Level = Max_Trap_Level, the UltraSPARC-II*e* enters an error_state)
- An *Internal_processor_error* exception or *catastrophic_error* exception occurs
- The setting of PSTATE.RED by system software

The RED_state is indicated by the PSTATE.RED bit being set. For more information on the RED_state, consult Section 17.3, “RED_state”, of the *UltraSPARC-IIe User’s Manual*, published by Sun Microsystems.

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The USPII*e*-cPCI reset tree uses the UltraSPARC-II*e* CPU in conjunction with the power monitor (SMS44) and PLD. The PLD receives the `power-ok` signal (see *Figure 5-1* on page 5-3) from the SMS44 and receives a reset input to set the `B_POR` bit in the `reset_control_register` (see *Table 5-1*, "UltraSPARC-IIe Reset_Control Register', on page 5-6). When any of the system voltages are out of their preset ranges, `power_ok` will be deasserted, which in turn will place the UltraSPARC-II*e* and the system in a reset state until all voltages are within their specified ranges.

The PLD also receives input from the local `Reset`. When the PLD receives this signal it issues a POR (Power-On Reset) to the UltraSPARC-II*e*. The UltraSPARC-II*e* will then place the system in a reset state.

The system, or part of the system, may also be reset by a `Watchdog_Reset` (WDR) or a `Software-Initiated_Reset` (SIR). These resets originate within the UltraSPARC-II*e* core and are only observed by the processor core. Depending on the conditions and type of reset, the processor may propagate the reset throughout the system, as in the case of a POR, or reset part of the system; i.e., the processor core itself.



Note: Unlike other UltraSPARC-based systems, the UltraSPARC-II*e* does not support a wake-up reset for power management.

5.2 UltraSPARC-IIe Reset Request Signals

The reset request signals accepted by the UltraSPARC-II*e* on the USPII*e*-cPCI board are explained in this section. The signals are: `System_Reset` and `P_Reset`, initiated when power is applied to the system or when a system-wide reset is needed; `Externally_Initiated_Reset` (X_Reset), initiated in response to a signal external to the UltraSPARC-II*e* processor generally indicating a critical system event; `Watchdog_Reset` (WDR), initiated in response to the error_state; and `Software_Initiated_Reset` (SIR), initiated by software with the SIR command.

`System_Reset`, `P_Reset`, and X_Reset are received by the UltraSPARC-II*e* from the PLD, while WDR and SIR are internally generated by the UltraSPARC-II*e* and affect only the processor core. Reset priorities, from highest to lowest, are: `System_Reset` and P_Reset, X_Reset, WDR, and SIR.

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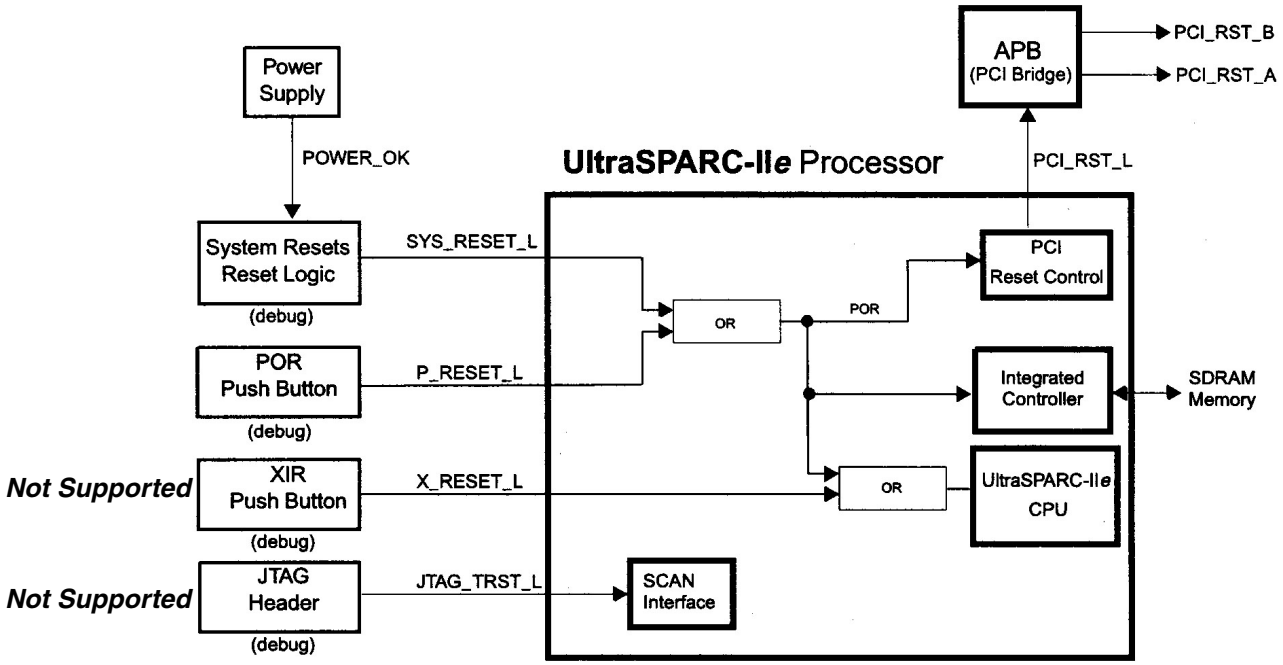


Figure 5-1. Simplified System Reset Architecture

5.2.1 System_Reset and P_Reset

A `Power-On Reset` (POR) event is caused by two different sources: the `System_Reset` (`SYS_RESET_L`) and the `P_Reset` (`P_RESET_L`). A `System_Reset` input or `P_Reset` input to the UltraSPARC-II*e* CPU is a POR for processor and board reset. When POR is active, all other resets and traps are ignored. A POR initiates the power-on sequence of all CPU functional units (PCI I/F, memory controller, and the CPU core itself).

The UltraSPARC-II*e* CPU will propagate this reset to all of the subsystems of the USPII*e*-cPCI, through the Intel 21154 PCI Bridge and through the Advanced PCI Bridge (APB) to all other devices connected to the secondary side of the PCI bridges.

5.2.2 Externally Initiated Reset (X_Reset or XIR)—*Not Supported*

An XIR event is caused by the activation of the `X_RESET_L` input of the CPU, and has a higher priority than all other resets except `System_Reset` and `P_Reset`. It

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is initiated by a source external to the UltraSPARC-II*e*, such as an external component. It does *not* propagate a reset outside the CPU.

XIR does not cause a system-wide reset (memory controller and PCI I/O are unaffected). It preserves the existing state of all registers on the board with the exception of UltraSPARC-II*e* registers. If the UltraSPARC-II*e* is in an error_state, XIR brings it to a RED_state.

5.2.3 Watchdog_Reset (WDR)—*Not Supported*

There are two Watchdog Reset (WDR) mechanisms on the USPII*e*-cPCI. One WDR is built into the CPU itself (see the *UltraSPARC-IIe User's Manual* referred to in "Related References" on page xx for a full description of this internal Watchdog Reset). The second WDR is implemented in the PLD external to the CPU.

Upon expiration of the first WDR timeout, an interrupt is sent to the CPU. Upon expiration of the second WDR timeout, a board reset is initiated.

5.2.4 Software_Initiated_Reset (SIR)

A `Software_Initiated_Reset` is initiated by an SIR instruction from supervisory software. It is initiated within the UltraSPARC-II*e* core itself and affects only the UltraSPARC-II*e*. An SIR is not propagated to the I/O or external system.

5.3 Reset Sources

The UltraSPARC-II*e* accepts three reset signals from the PLD, `System_Reset`, `P_Reset`, and `X_Reset`. `System_Reset` and `P_Reset` propagate from the processor to the entire board. `X_Reset` does not propagate outside the processor.

POR can be generated from on-board power management and from the 2-Level Watchdog reset. POR can also be initiated by software.

5.3.1 CPU System Reset

The `System_Reset` will be asserted under the following conditions:

1. On power-up of the cPCI chassis (backplane) when the USPII*e*-cPCI is already plugged in.

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2. Upon hot-insertion of the USPII*e*-cPCI into the cPCI chassis.
3. When an abnormal thermal situation occurs (overtemperature conditions reported by the Winbond thermal monitoring device).

5.3.2 P_Reset

The `P_Reset` input of the CPU is activated under the following conditions:

1. On power-up of the cPCI chassis (backplane) when the USPII*e*-cPCI is already plugged in.
2. Upon hot-insertion of the USPII*e*-cPCI into the cPCI chassis.
3. When the 2-Level Watchdog timeout expires.
4. When the cPCI reset signal is asserted on the cPCI backplane.
5. Also, if any of the cPCI voltages (3.3V and 5V) are out of their accepted ranges, the P_Reset is will be asserted, keeping the USPII*e*-cPCI in reset mode until the faulty condition is corrected.

5.3.3 Software POR

Software may initiate a reset equivalent to a `Power-On-Reset` (POR) by setting the SOFT_POR bit in the UltraSPARC-II*e* `Reset_Control Register` (see *Table 5-1*). This bit will remain set until software clears it, to allow software to detect the source of the reset.

5.3.4 Software XIR

Software may initiate a reset equivalent to an `Externally-Initiated-Reset` (XIR) by setting the SOFT_XIR bit in the UltraSPARC-II*e* Reset_Control Register (*Table 5-1*). This bit will remain set until software clears it, to allow software to detect the source of the reset.

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5.4 UltraSPARC-IIe Reset_Control Register

The UltraSPARC-II*e* `reset_control register` indicates the source of a reset and provides control of software reset generation. It is located at 0x1FE.0000.F020.



Note: Internal to the UltraSPARC-II*e* are the Watch Dog Reset (WDR) and Software Initiated Reset (SIR). These two resets are initiated within the processor core and affect only the processor.

Table 5-1. UltraSPARC-IIe Reset_Control Register

Field	Bits	Value	Description	Type
Reserved	63:32	0	Reserved	R0
POR	31	*[a]	Set if the last reset was due to the assertion of SYS_RESET_L	R/W1C
SOFT_POR	30	*	Setting to 1 causes a POR reset; stays set until software clears it	R/W
SOFT_XIR	29	*	Setting to 1 causes an XIR trap; stays set until software clears it	R/W
B_POR	28	*	Set if the last reset was due to the assertion of P_RESET_L	R/W1C
B_XIR	27	*	Set if the last reset was due to the assertion of an X_Reset_L	R/W1C
Reserved	26:0	*	Reserved	R0

a—The highest priority reset source has its bit set. Only the bits marked with "*" are set.

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Appendix A

System Connectors

This appendix provides a description of the connectors, including pinouts where applicable, for the USPII*e*-cPCI, Rear Transition Board, and Memory Module. For connector locations, refer to Appendix C, “Front and Rear Panel Diagrams”.

A.1 USPIIe-cPCI Baseboard

The USPII*e*-cPCI Baseboard contains five connectors (J1, J2, J3, J4, and J5) on its rear edge that plug into the cPCI backplane connectors P1 through P5 (see *Figure A-2* on page A-2), and seven assorted connectors on its front-panel faceplate. In addition, any PMC Module installed on the board will have its own connectors.

A.1.1 J1 Connector

- *Connector Type:* CompactPCI bus, 5-row x 25-position (3 x 5 key area) female pin array (see *Figure A-1*, *Table A-1*, page A-3). One ground row (F).

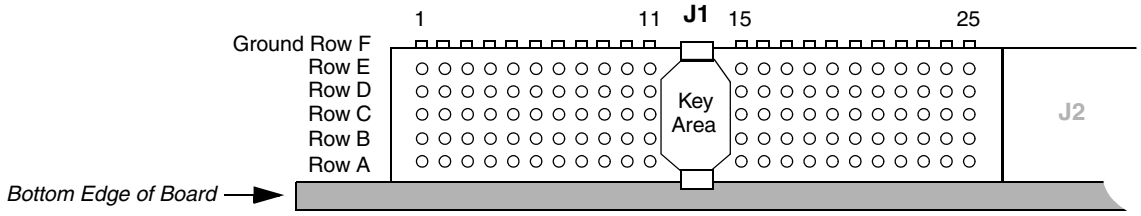


Figure A-1. USPIIe-cPCI J1 Connector (Rear View)

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Note: The CompactPCI Specification includes two additional rows—Z and F, which are used primarily to carry ground signals. While both rows Z and F are included in cPCI backplanes, the USPII*e*-cPCI Baseboard includes only row F.

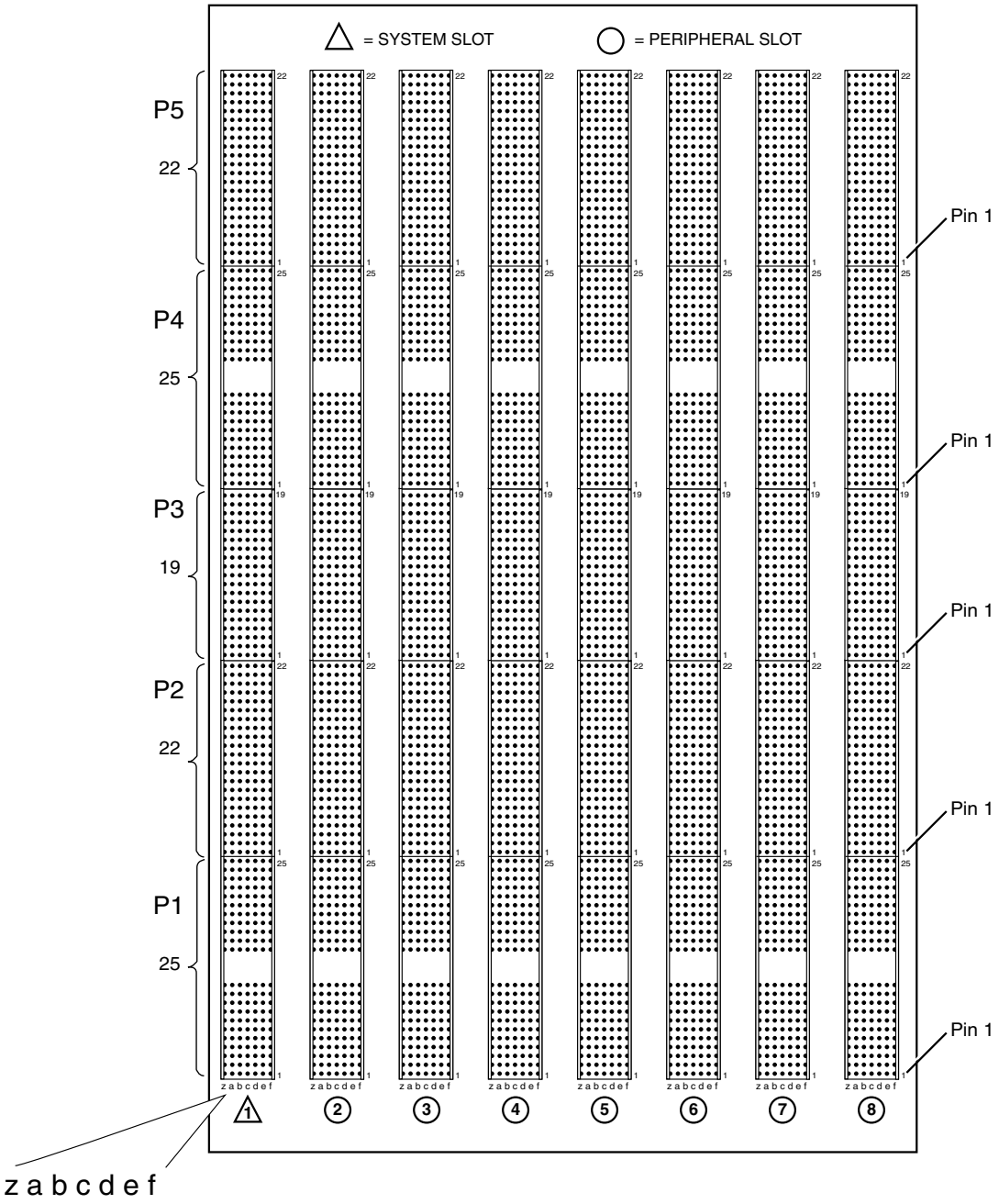


Figure A-2. Typical cPCI Backplane (Front View)

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Table A-1. J1 cPCI Backplane Pinout Signals

Pin	Row Z	Row A	Row B	Row C	Row D	Row E	Row F[a]
25	GND	5V[b]	REQ64#	ENUM#	3.3V	5V	GND
24	GND	AD[1]	5V	**V(I/O)[c]**	AD[0]	ACK64#	
23	GND	3.3V	AD[4]	AD[3]	**5V**	AD[2]	GND
22	GND	AD[7]	GND	**3.3V**	AD[6]	AD[5]	
21	GND	3.3V	AD[9]	AD[8]		C/BE[0]#	GND
20	GND	AD[12]	GND	V(I/O)	AD[11]	AD[10]	
19	GND	3.3V	AD[15]	AD[14]	**GND**	AD[13]	GND
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	
17	GND	3.3V			**GND**	PERR#	GND
16	GND	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	
15	GND	3.3V	FRAME#	IRDY#	BD_SEL#[d]	TRDY#	GND
14	Key Area						
13							
12							
11	GND	AD[18]	AD[17]	AD[16]	**GND**	C/BE[2]#	GND
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	
9	GND	C/BE[3]#		AD[23]	**GND**	AD[22]	GND
8	GND	AD[26]	GND	V(I/O)	AD[25]	AD[24]	
7	GND	AD[30]	AD[29]	AD[28]	**GND**	AD[27]	GND
6	GND	REQ#	GND	**3.3V**	CLK	AD[31]	
5	GND			PCI-RST#	**GND**	GNT#	GND
4	GND		HEALTHY#	**V(I/O)**	INTP	INTS	
3	GND	INTA#	INTB#	INTC#	**5V**	INTD#	GND
2	GND		5V				
1	GND	5V	-12V		+12V	5V	GND

a—Row F and Z GND pins are long length as per the *CompactPCI Standard*.

b—All entries utilize medium-length pins unless otherwise indicated.

c—Entries with white characters and dark-tinted backgrounds = long pin.

d—Entries within thick borders = short pin.

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A.1.2 J2 Connector

Connector Type: CompactPCI bus, 5-row x 22-position female pin array plus one ground row (see *Figure A-3* and *Table A-2*).

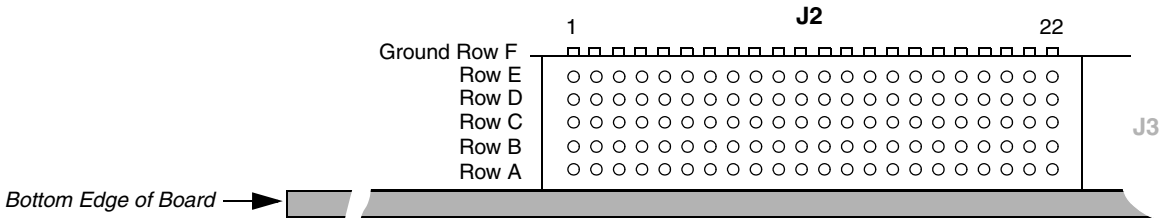


Figure A-3. USPIIe-cPCI J2 Connector (Rear View)

Table A-2. J2 cPCI Backplane Pinout Signals[a]

Pin	Row Z	Row A	Row B	Row C	Row D	Row E	Row F
22	GND	GA4	GA3	GA2	GA1	GA0	GND
21	GND	CLK6	GND				
20	GND	CLK5	GND		GND	SV	GND
19	GND	GND	GND				
18	GND				GND		GND
17	GND		GND	PRST#	REQ6#	GNT6#	
16	GND			DEG#	GND		GND
15	GND		GND	FAL#	REQ5#	GNT5#	
14	GND	AD[35]	AD[34]	AD[33]	GND	AD[32]	GND
13	GND	AD[38]	GND	V(I/O)[b]	AD[37]	AD[36]	
12	GND	AD[42]	AD[41]	AD[40]	GND	AD[39]	GND
11	GND	AD[45]	GND	V(I/O)	AD[44]	AD[43]	
10	GND	AD[49]	AD[48]	AD[47]	GND	AD[46]	GND
9	GND	AD[52]	GND	V(I/O)	AD[51]	AD[50]	
8	GND	AD[56]	AD[55]	AD[54]	GND	AD[53]	GND
7	GND	AD[59]	GND	V(I/O)	AD[58]	AD[57]	

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Table A-2. J2 cPCI Backplane Pinout Signals[a] (Continued)

Pin	Row Z	Row A	Row B	Row C	Row D	Row E	Row F
6	GND	AD[63]	AD[62]	AD[61]	GND	AD[60]	GND
5	GND	C/BE[5]#		V(I/O)	C/BE[4]#	PAR64	
4	GND	V(I/O)		C/BE[7]#	GND	C/BE[6]#	GND
3	GND	CLK4	GND	GNT3#	REQ4#	GNT4#	
2	GND	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
1	GND	CLK1	GND	REQ1#	GNT1#	REQ2#	

a—All P2 pins are medium length.

b—V(I/O) signals are either 5 V OR 3.3 V, depending on system implementation.

A.1.3 J3 Connector

Connector Type: CompactPCI bus, 5-row x 19-position female pin array plus one ground row (see *Figure A-4* and *Table A-3*).

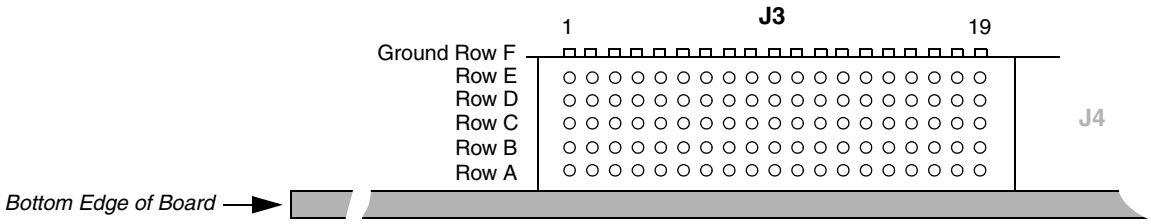


Figure A-4. USPIIe-cPCI J3 Connector (Rear View)

Table A-3. J3 cPCI Backplane Pinout Signals[a]

Pin	Row Z	Row A	Row B	RowC	Row D	Row E	Row F
19	GND	GND	GND	GND	GND	GND	GND
18	GND	PSB_LPA_DA+	PSB_LPA_DA-	GND			
17	GND	PSB_LPA_DB+	PSB_LPA_DB-	GND			GND
16	GND	PSB_LPB_DA+	PSB_LPB_DA-	GND			
15	GND	PSB_LPB_DB+	PSB_LPB_DB-	GND			GND

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Table A-3. J3 cPCI Backplane Pinout Signals[a] (Continued)

Pin	Row Z	Row A	Row B	Row C	Row D	Row E	Row F
14	GND	GND	GND	GND	GND	GND	
13	GND	*NC*	*NC*	*NC*	*NC*	*NC*	GND
12	GND	*NC*	*NC*	*NC*	*NC*	*NC*	
11	GND	*NC*	*NC*	*NC*	*NC*	*NC*	GND
10	GND	*NC*	*NC*	*NC*	*NC*	*NC*	
9	GND	*NC*	*NC*	*NC*	*NC*	*NC*	GND
8	GND	*NC*	*NC*	*NC*	*NC*	*NC*	
7	GND	*NC*	*NC*	*NC*	*NC*	*NC*	GND
6	GND	*NC*	*NC*	*NC*	*NC*	*NC*	
5	GND	*NC*	*NC*	*NC*	*NC*	*NC*	GND
4	GND	*NC*	*NC*	*NC*	*NC*	*NC*	
3	GND	*NC*	*NC*	*NC*	*NC*	*NC*	GND
2	GND	PC13_PCI _RST_L	*NC*	*NC*	*NC*	*NC*	
1	GND	V(IO)	VCC	VCC	VDD_3V	VDD_3V	GND

a—All P3 pins are medium length.

A.1.4 J4 Connector

Connector Type: CompactPCI bus, 5-row x 25-position female pin array plus one ground row (see *Figure A-5* and *Table A-4* on page A-7).

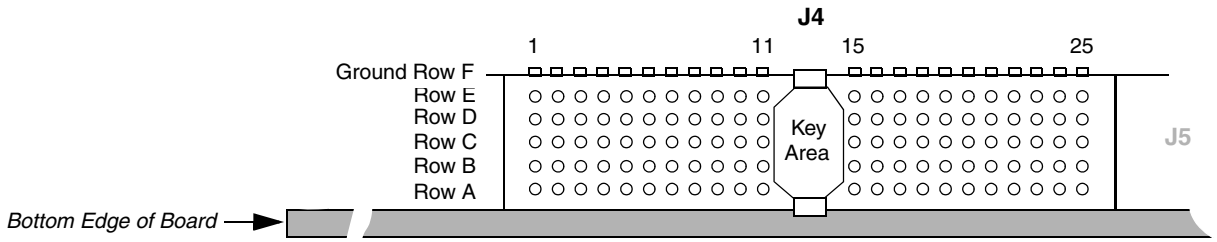


Figure A-5. USPIIe-cPCI J4 Connector (Rear View)

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Table A-4. J4 cPCI Backplane Pinout Signals

Pin	Row Z	Row A	Row B	Row C	Row D	Row E	Row F[a]
25	GND	CRTC _PRES_L	SCSI_A _RPRES_L	SCSI_A _DIFFSENS	SCSI_B _RPRES_L	SCSI_B _DIFFSENS	GND
24	GND	PP_RDAT0	PP_RAUTO_ FD_L	PP_RSTB_L	SER_B_RXD	SER_A_RXD	
23	GND	PP_RDAT1	PP_RACK_L	ENB_SER_A _FRONT_L	SER_B_DCD	SER_A_DCD	GND
22	GND	PP_RDAT2	PP_RBUSY	ENB_SER_B _FRONT_L	SER_B_DSR	SER_A_DSR	
21	GND	PP_RDAT3	PP_RPE	SER_C_TXD	SER_B_CTS	SER_A_CTS	GND
20	GND	PP_RDAT4	PP_RSLCT	SER_C_RXD	SER_B_RI	SER_A_RI	
19	GND	PP_RDAT5	PP_RSLIN_L	SER_D_TXD	SER_B_TXD	SER_A_TXD	GND
18	GND	PP_RDAT6	PP_RINIT_L	SER_D_RXD	SER_B_RTS	SER_A_RTS	
17	GND	PP_RDAT7	PP_RERR_L	*NC*[b]	SER_B_DTR	SER_A_DTR	GND
16	GND	*NC*	*NC*	*NC*	CRTC_GP _IN_L	CRTC_GP _OUT1	
15	GND	*NC*	*NC*	*NC*	CRTC_GP _OUT2	CRTC_GP _OUT0	GND
14	Key Area						
13							
12							
11	GND	*NC*	*NC*	*NC*	*NC*	AC97_RST_L	GND
10	GND	*NC*	*NC*	*NC*	*NC*	AC97_SYNC	
9	GND	*NC*	*NC*	*NC*	*NC*	AC97_DOUT	GND
8	GND	*NC*	*NC*	*NC*	*NC*	AC97_BCLK	
7	GND	*NC*	*NC*	*NC*	*NC*	AC97_DIN	GND
6	GND	*NC*	*NC*	*NC*	*NC*		
5	GND	*NC*	*NC*	*NC*	*NC*	USB3_REAR _D_P	GND
4	GND	*NC*	*NC*	*NC*	*NC*	USB3_REAR _D_N	
3	GND	*NC*	*NC*	*NC*	*NC*		GND
2	GND	*NC*	*NC*	*NC*	*NC*	USB2_REAR _D_P	
1	GND	*NC*	*NC*	*NC*	*NC*	USB2_REAR _D_N	GND

a—Row F and Z GND pins are long length as per the *CompactPCI Standard*.

b—NC = No Connection.

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A.1.5 J5 Connector

Connector Type: CompactPCI bus, 5-row x 22-position female pin array plus one ground row (see *Figure A-6* and *Table A-5*).

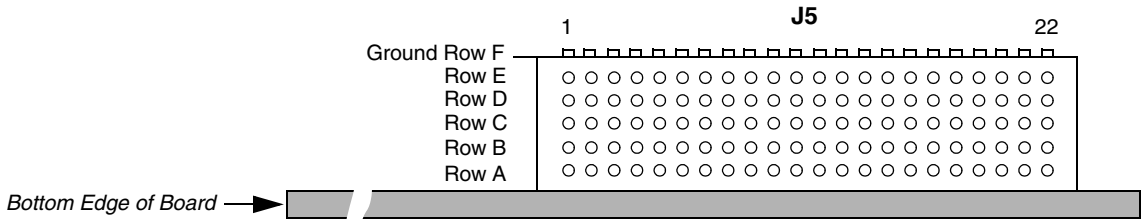


Figure A-6. USPIIe-cPCI J5 Connector (Rear View)

Table A-5. J5 cPCI Backplane Pinout Signals[a]

Pin	Row Z	Row A	Row B	Row C	Row D	Row E	Row F
22	GND	SCSI_A_DAT _H12	SCSI_A_DAT _H13	SCSI_A_DAT _H14	SCSI_B_DAT _H12	SCSI_B_DAT _H13	GND
21	GND	SCSI_A_DAT _L12	SCSI_A_DAT _L13	SCSI_A_DAT _L14	SCSI_B_DAT _L12	SCSI_B_DAT _L13	
20	GND	SCSI_A_DAT _H15	SCSI_A_PAR _H1	SCSI_A_DAT _H0	SCSI_B_DAT _H14	SCSI_B_DAT _H15	GND
19	GND	SCSI_A_DAT _L15	SCSI_A_PAR _L1	SCSI_A_DAT _L0	SCSI_B_DAT _L14	SCSI_B_DAT _L15	
18	GND	SCSI_A_DAT _H1	SCSI_A_DAT _H2	SCSI_A_DAT _H3	SCSI_B_PAR _H1	SCSI_B_DAT _H0	GND
17	GND	SCSI_A_DAT _L1	SCSI_A_DAT _L2	SCSI_A_DAT _L3	SCSI_B_PAR _L1	SCSI_B_DAT _L0	
16	GND	SCSI_A_DAT _H4	SCSI_A_DAT _H5	SCSI_A_DAT _H6	SCSI_B_DAT _H1	SCSI_B_DAT _H2	GND
15	GND	SCSI_A_DAT _L4	SCSI_A_DAT _L5	SCSI_A_DAT _L6	SCSI_B_DAT _L1	SCSI_B_DAT _L2	
14	GND	SCSI_A_DAT _H7	SCSI_A_PAR _H0	SCSI_A_ATN _H	SCSI_B_DAT _H3	SCSI_B_DAT _H4	GND

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Table A-5. J5 cPCI Backplane Pinout Signals[a] (Continued)

Pin	Row Z	Row A	Row B	Row C	Row D	Row E	Row F
13	GND	SCSI_A_DAT _L7	SCSI_A_PAR _L0	SCSI_A_ATN _L	SCSI_B_DAT _L3	SCSI_B_DAT _L4	
12	GND	SCSI_A_BSY _H	SCSI_A_ACK _H	SCSI_TERMP WR_A	SCSI_B_DAT _H5	SCSI_B_DAT _H6	GND
11	GND	SCSI_A_BSY _L	SCSI_A_ACK _L	SCSI_TERMP WR_B	SCSI_B_DAT _L5	SCSI_B_DAT _L6	
10	GND	SCSI_A_RST _H	SCSI_A_MSG _H	SCSI_B_DAT _H7	SCSI_B_PAR _H0	SCSI_B_ATN _H	GND
9	GND	SCSI_A_RST _L	SCSI_A_MSG _L	SCSI_B_DAT _L7	SCSI_B_PAR _L0	SCSI_B_ATN _L	
8	GND	SCSI_A_SEL _H	SCSI_A_CD_ H	SCSI_B_BSY _H	SCSI_B_ACK _H	SCSI_B_RST _H	GND
7	GND	SCSI_A_SEL _L	SCSI_A_CD_ L	SCSI_B_BSY _L	SCSI_B_ACK _L	SCSI_B_RST _L	
6	GND	SCSI_A_REQ _H	SCSI_A_IO_H	SCSI_B_MSG _H	SCSI_B_SEL _H	SCSI_B_CD_ H	GND
5	GND	SCSI_A_REQ _L	SCSI_A_IO_L	SCSI_B_MSG _L	SCSI_B_SEL _L	SCSI_B_CD_ L	
4	GND	SCSI_A_DAT _H8	SCSI_A_DAT _H9	SCSI_B_REQ _H	SCSI_B_IO_ H	SCSI_B_DAT _H8	GND
3	GND	SCSI_A_DAT _L8	SCSI_A_DAT _L9	SCSI_B_REQ _L	SCSI_B_IO_L	SCSI_B_DAT _L8	
2	GND	SCSI_A_DAT _H10	SCSI_A_DAT _H11	SCSI_B_DAT _H9	SCSI_B_DAT _H10	SCSI_B_DAT _H11	GND
1	GND	SCSI_A_DAT _L10	SCSI_A_DAT _L11	SCSI_B_DAT _L9	SCSI_B_DAT _L10	SCSI_B_DAT _L11	

a—All P5 pins are medium length.

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A.1.6 SCSI A / SCSI B Connectors

- *Connector Type:* Dual SCSI-2 (80 MB/sec; female), 68 Pin, 0.8 mm Pitch
- *Manufacturer; Part Number:* Honda; HDRA-E68W1LFDT-1EC-SL

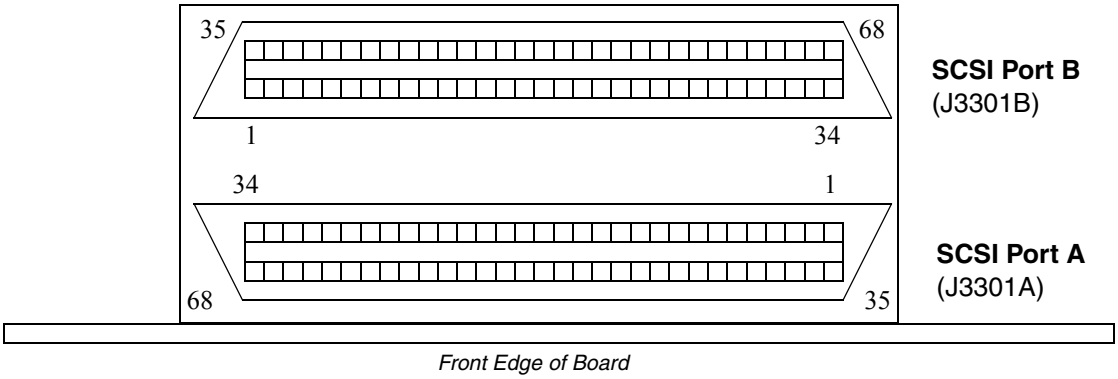


Figure A-7. Baseboard SCSI A and B Connector Orientation (Front View)

Table A-6. Baseboard SCSI A and B Pinout

Pin	Signal Name	Pin	Signal Name
1	positive DAT<12>	35	negative DAT<12>
2	positive DAT<13>	36	negative DAT<13>
3	positive DAT<14>	37	negative DAT<14>
4	positive DAT<15>	38	negative DAT<15>
5	positive PAR<1>	39	negative PAR<1>
6	positive DAT<0>	40	negative DAT<0>
7	positive DAT<1>	41	negative DAT<1>
8	positive DAT<2>	42	negative DAT<2>
9	positive DAT<3>	43	negative DAT<3>
10	positive DAT<4>	44	negative DAT<4>
11	positive DAT<5>	45	negative DAT<5>
12	positive DAT<6>	46	negative DAT<6>

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Table A-6. Baseboard SCSI A and B Pinout (Continued)

Pin	Signal Name	Pin	Signal Name
13	positive DAT<7>	47	negative DAT<7>
14	positive PAR<0>	48	negative PAR<0>
15	GND	49	GND
16	DIFFSENS	50	GND
17	TERMPWR	51	TERMPWR
18	TERMPWR	52	TERMPWR
19	*No Connection*	53	*No Connection*
20	SCSI FP[a]	54	GND
21	positive ATN	55	negative ATN
22	GND	56	GND
23	positive BSY	57	negative BSY
24	positive ACK	58	negative ACK
25	positive RST	59	negative RST
26	positive MSG	60	negative MSG
27	positive SEL	61	negative SEL
28	positive CD	62	negative CD
29	positive REQ	63	negative REQ
30	positive IO	64	negative IO
31	positive DAT<8>	65	negative DAT<8>
32	positive DAT<9>	66	negative DAT<9>
33	positive DAT<10>	67	negative DAT<10>
34	positive DAT<11>	68	negative DAT<11>

a—This is part of the Automatic SCSI termination logic: The SCSI FP signal will be forced to ground by the mating SCSI connector when attached. This will disable the active on-board SCSI terminator on the front side.

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A.1.7 Serial Port A and Port B Connectors

- *Connector Type:* 2 stacked Sub-miniature-DB9 (male)
- *Manufacturer; Part Number:* ITT Cannon; MDSM-18PE-Z10

Both serial (TTY) port A and port B are RS232 interfaces with full modem support (see *Figure A-8* and *Table A-7*).

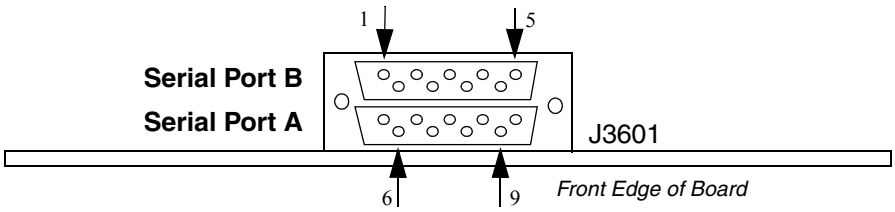


Figure A-8. Front-Panel Serial Ports A and B (Front View)

Table A-7. Serial Ports A and B Connector Pinout

Pin	Signal Name	Description
1	DCD	Data Carrier Detect
2	RXD	Receive Data
3	TXD	Transmit Data
4	DTR	Data Terminal Ready
5	GND	Signal Ground
6	DSR	Data Set Ready
7	RTS	Request To Send
8	CTS	Clear To Send
9	RI	Ring Indicator

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A.1.8 DIN-8 Connector (*PS/2-Port Version Only*)

- *Connector Type:* 8-Pin Mini-DIN (female)
- *Manufacturer; Part Number:* Amp; AMP-749179-1

The mini-DIN-8 connector (marked **KEYBD/MOUSE**) on the PS/2-Port Version Baseboard front panel supports a PS/2 keyboard/mouse port or dual-USB (USB-A, USB-B) ports. Either option is selected by configuring five solder beads (SB3502 through SB3506; see *Table 1-1* in Chapter 1, "USPIIe-cPCI Installation", and *Table B-5*, Appendix B, "Jumper-Pin and Solder-Bead Configurations").

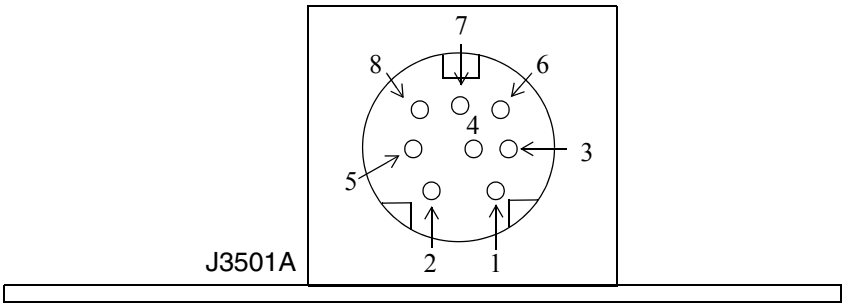


Figure A-9. Front-Panel Mini-DIN-8 Connector (Front View)

Table A-8. 8-Pin Mini-DIN PS/2–USB Pinouts

Pin	PS/2 KB/M Signal[a]	USB Signal[a]
1	GND 0	GND 0
2	GND 1	GND 1
3	VCC 0	VCC 0
4	PS2_MS_DAT	USB1_D_P (USB-B)[b]
5	PS2_KBD_CLK	USB1_D_N (USB-B)[b]
6	PS2_KBD_DAT	USB0_D_P (USB-A)[b]
7	PS2_MS_CLK	USB0_D_N (USB-A)[b]
8	VCC 1	VCC 1

a—Signals are dependant on SB3503–SB3506 settings (see *Table B-5*, page B-8).

b—P = positive; N = negative.

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A.1.9 USB Port A and Port B (*USB-Port Version Only*)

- *Connector Type:* Dual-USB, Type A
- *Manufacturer; Part Number:* SMP Technology; U001-0800-104

The dual-USB connector (marked **USB A B**) on the USB-Port Version Baseboard front panel supports dual-USB (USB-A, USB-B) ports. Configuring the five solder beads (SB3502 through SB3506; see *Table 1-1* in Chapter 1, “USPIIe-cPCI Installation”, and *Table B-5*, Appendix B, "Jumper-Pin and Solder-Bead Configurations") has no effect on this connector.

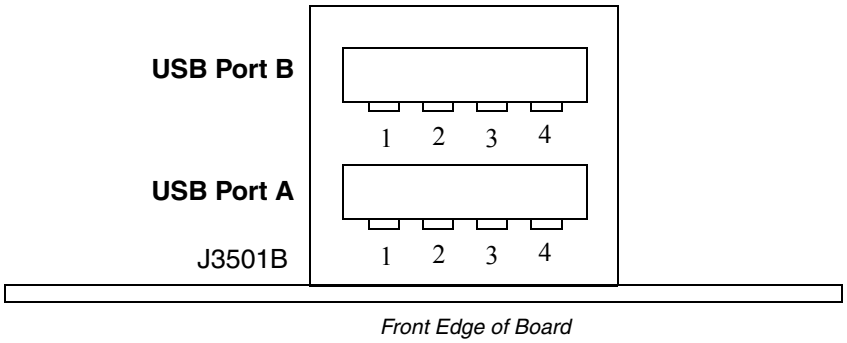


Figure A-10. Front-Panel Mini-DIN-8 Connector (Front View)

Table A-9. USB A/B Pinouts

Pin	USB Signal	Description
1	PWR	Power source
2	D_N	Data, Negative
3	D_P	Data, Positive
4	GND	Ground

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A.1.10 Ethernet A / Ethernet B Connectors

- *Connector Type:* RJ45 TP Ethernet with LEDs (2)
- *Connector Part Number:* Amp; 406549-1

Ethernet A and Ethernet B on the front panel

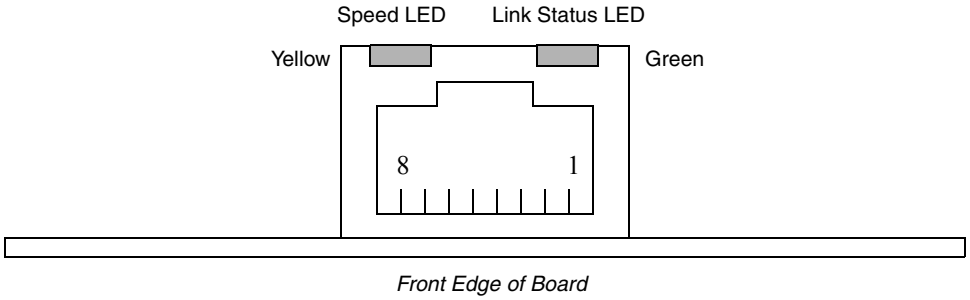


Figure A-11. Ethernet A or B Connector Orientation (Front View)

Table A-10. RJ45 Ethernet A Pinout

Pin	Signal Name
1	TXD+
2	TXD–
3	RXD+
4	TXGND
5	TXGND
6	RXD–
7	RXGND
8	RXGND

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A.2 Rear Transition Board

A.2.1 SCSI A / SCSI B Connectors

- *Connector Type:* Dual SCSI-2 (80 MB/sec; female), 68 Pin, 0.8 mm Pitch
- *Manufacturer; Part Number:* Honda; HDRA-E68W1LFDT-1EC-SL

Both SCSI bus A and SCSI bus B operate in low-voltage differential (LVD) mode. When SCSI devices are attached to both the front-panel (through either SCSI A and/or B) and through the same SCSI bus on the Rear Transition Board, it is important that the on-board termination for that SCSI bus be disabled (see "SCSI Terminations" on page 1-3. in Chapter 1, "USPIIe-cPCI Installation").

SB3201 and SB3203 enable or disable the USPII*e*-cPCI terminator for SCSI bus A, and SB3202 and SB3204 enable or disable the on-board terminator for SCSI bus B (see Section B.3.1, "Baseboard Solder Beads," on page B-6).

See *Figure A-12* and *Table A-11* for a description of SCSI A/B pinouts.

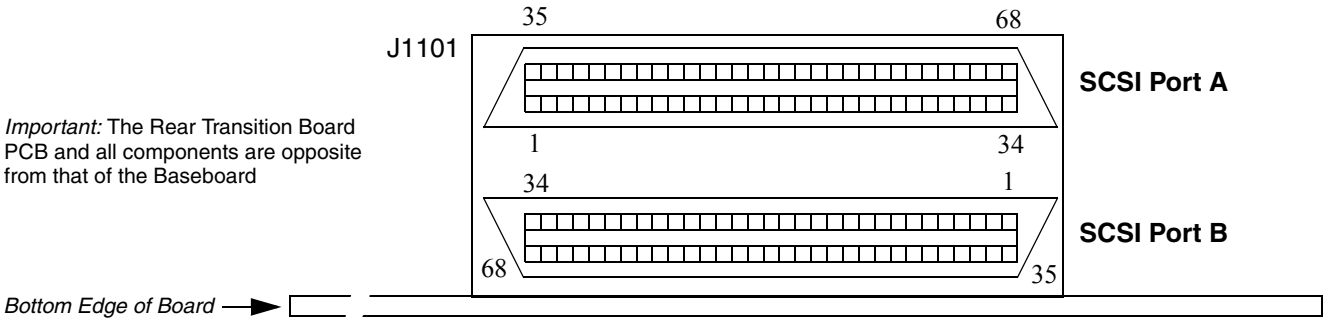


Figure A-12. Rear Transition Board SCSI A and B Connector (Rear View)

Table A-11. Rear Transition Board SCSI A and B Pinout

Pin	Signal Name	Pin	Signal Name
1	positive DAT<12>	35	negative DAT<12>
2	positive DAT<13>	36	negative DAT<13>
3	positive DAT<14>	37	negative DAT<14>
4	positive DAT<15>	38	negative DAT<15>
5	positive PAR<1>	39	negative PAR<1>

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Table A-11. Rear Transition Board SCSI A and B Pinout (Continued)

Pin	Signal Name	Pin	Signal Name
6	positive DAT<0>	40	negative DAT<0>
7	positive DAT<1>	41	negative DAT<1>
8	positive DAT<2>	42	negative DAT<2>
9	positive DAT<3>	43	negative DAT<3>
10	positive DAT<4>	44	negative DAT<4>
11	positive DAT<5>	45	negative DAT<5>
12	positive DAT<6>	46	negative DAT<6>
13	positive DAT<7>	47	negative DAT<7>
14	positive PAR<0>	48	negative PAR<0>
15	GND	49	GND
16	DIFFSENS	50	GND
17	TERMPWR	51	TERMPWR
18	TERMPWR	52	TERMPWR
19	*No Connection*	53	*No Connection*
20	SCSI FP[a]	54	GND
21	positive ATN	55	negative ATN
22	GND	56	GND
23	positive BSY	57	negative BSY
24	positive ACK	58	negative ACK
25	positive RST	59	negative RST
26	positive MSG	60	negative MSG
27	positive SEL	61	negative SEL
28	positive CD	62	negative CD
29	positive REQ	63	negative REQ
30	positive IO	64	negative IO
31	positive DAT<8>	65	negative DAT<8>
32	positive DAT<9>	66	negative DAT<9>
33	positive DAT<10>	67	negative DAT<10>
34	positive DAT<11>	68	negative DAT<11>

a—This is part of the Automatic SCSI termination logic. The SCSI FP signal will be forced to ground by the mating SCSI connector when attached. This will disable the active on-board SCSI terminator on the front side.

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A.2.2 Parallel Port Connector

- *Connector Type:* 2 stacked Sub-miniature-DB9 (female)
- *Manufacturer; Part Number:* Amp; 787202-1

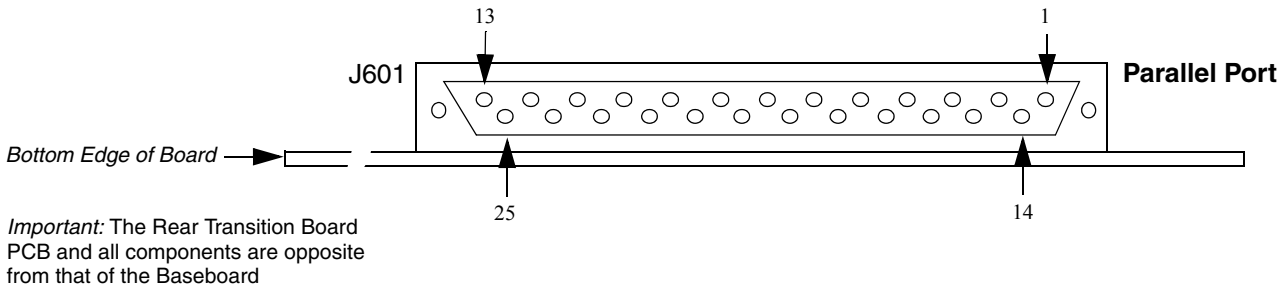


Figure A-13. Front-Panel Serial Ports A and B (Rear View)

Table A-12. Serial Ports A and B Connector Pinout

Pin	Signal Name	Description
1	STB_L	– Strobe
2	DAT0	Data 0
3	DAT1	Data 1
4	DAT2	Data 2
5	DAT3	Data 3
6	DAT4	Data 4
7	DAT5	Data 5
8	DAT6	Data 6
9	DAT7	Data 7
10	ACK_L	– Acknowledge
11	BUSY	+ Busy
12	PE	+ Paper End
13	SLCT	+ Select In

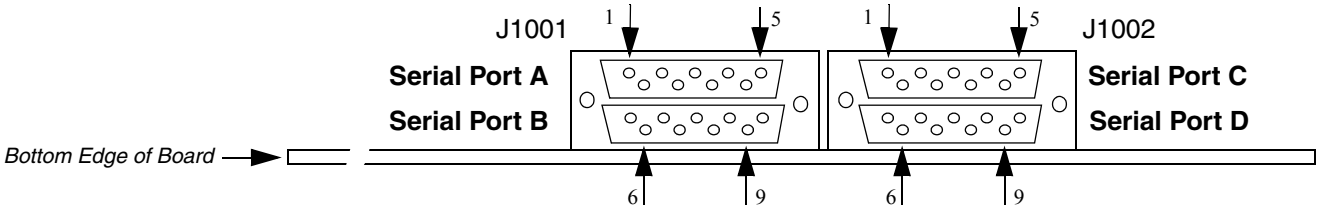
Pin	Signal Name	Description
14	AUTO_FD_L	– Auto Feed
15	ERR_L	– Error
16	INIT_L	– Initialize
17	SLIN_L	– Select Printer
18	GND	Signal Ground
19	GND	Signal Ground
20	GND	Signal Ground
21	GND	Signal Ground
22	GND	Signal Ground
23	GND	Signal Ground
24	GND	Signal Ground
25	GND	Signal Ground

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A.2.3 Serial Port A, Port B, Port C, and Port D Connectors

- *Connector Type:* 2 stacked sub-miniature-DB9 (male)
- *Manufacturer; Part Number:* ITT Cannon; MDSM-18PE-Z10

Serial Port A and Port B are RS232 interfaces with full modem support (see *Figure A-14* and *Table A-13*). Serial Port C and Port D are limited RS232 interfaces with transmit and receive data signals only (see *Table A-13*).



Important: The Rear Transition Board PCB and all components are opposite from that of the Baseboard

Figure A-14. Front-Panel Serial Ports A and B (Rear View)

Table A-13. Serial Ports A, B, C, and D Connector Pinout

Serial Port A and Port B		
Pin	**Signal Name**	**Description**
1	DCD	Data Carrier Detect
2	RXD	Receive Data
3	TXD	Transmit Data
4	DTR	Data Terminal Ready
5	GND	Signal Ground
6	DSR	Data Set Ready
7	RTS	Request To Send
8	CTS	Clear To Send
9	RI	Ring Indicator

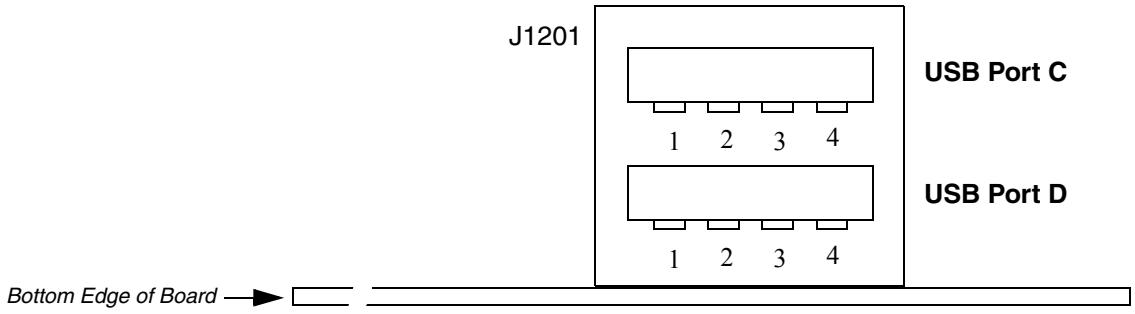
Serial Port C and Port D		
Pin	**Signal Name**	**Description**
1		
2	RXD	Receive Data
3	TXD	Transmit Data
4		
5	GND	Signal Ground
6		
7		
8		
9		

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A.2.4 USB Port C and Port D

- *Connector Type:* Dual-USB, Type A
- *Manufacturer; Part Number:* SMP Technology; U001-0800-104

The dual-USB connector (marked **USB C D**) on the faceplate of the Rear Transition Board supports the USB-C and USB-D ports (see *Figure A-15* and *Table A-14*). These ports are functionally independent of the version of the USPII*e*-cPCI Baseboard (PS/2 or USB).



Important: The Rear Transition Board PCB and all components are opposite from that of the Baseboard

Figure A-15. Front-Panel Mini-DIN-8 Connector (Rear View)

Table A-14. USB C/D Pinouts

Pin	USB Signal	Description
1	PWR	Power
2	D_N	Data, Negative
3	D_P	Data, Positive
4	GND	Ground

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A.2.5 Audio (Stereo) Connectors

- *Connector Type:* Mini-phone stereo jack
- *Manufacturer; Part Number:* Connect-Tech; CTP-354W-S1

Pinouts for the four audio stereo connectors on the faceplate of the Rear Transition Board are described in *Table A-15*. As *Table A-15* indicates, these connectors support audio line in, audio line out, microphone in, and headphone out.

Table A-15. Rear Transition Board Audio Connector Pinouts

Connector	Pin	Signal	Description
Audio Line In	1	IN_SHLD	Shield
	2	IN_L	Left input
	3	*No Connection*	
	4	IN_R	Right input
	5	*No Connection*	
Audio Line Out	1	OUT_SHLD	Shield
	2	OUT_L	Left input
	3	*No Connection*	
	4	OUT_R	Right input
	5	*No Connection*	
Microphone In	1	IN_SHLD	Shield
	2	IN_L	Left input
	3	*No Connection*	
	4	*No Connection*	
	5	*No Connection*	
Headphone Out	1	OUT_SHLD	Shield
	2	OUT_L	Left input
	3	*No Connection*	
	4	OUT_R	Right input
	5	*No Connection*	

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A.2.6 User-Defined I/O Connectors

- *Connector Type:* 3-pin shrouded Molex (2)
- *Manufacturer; Part Number:* Molex; 70553-0002

Two 3-pin shrouded Molex connectors have been placed on the top (component) side of the Rear Transition Board. One (J1602) is for user input, the second is for user output triggered by an on-board relay (SW1601).

[Consult *Figure D-2* on page D-3 in Appendix A, "System Connectors", to see a diagram showing placement of these connectors on the Rear Transition Board.]

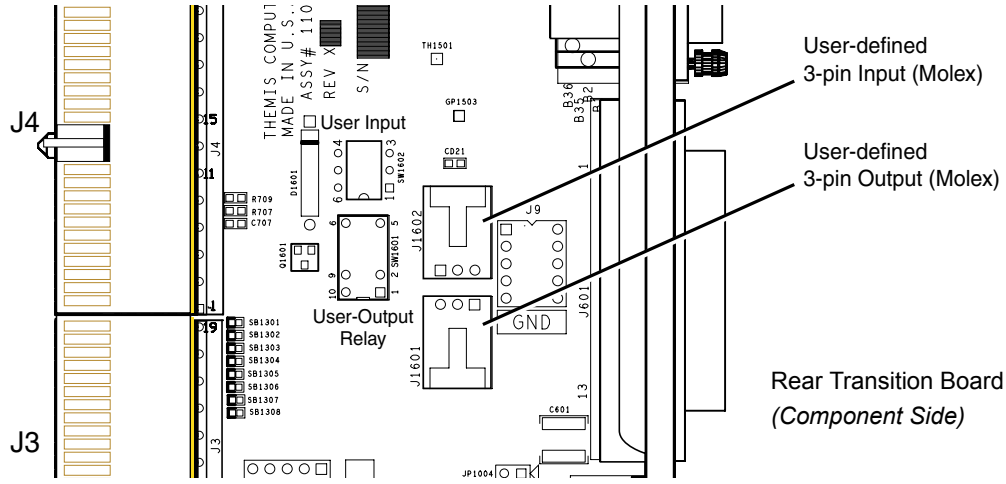


Figure A-16. User-Defined I/O Connector (Front View)

Table A-16. User-Defined Connector Pinout

Output (J1601)	
Pin	**Signal Name**
1	Normally Closed
2	Common
3	Normally Open

Input (J1602)	
Pin	**Signal Name**
1	Input
2	Ground
3	N/C

A.2.6.1 User Input

User input on Molex connector J1602 is current-controlled. A positive current must flow from pin 1 to pin 2, and a current of 0.15 mA or less will guarantee a logic state of 0. A current greater than 2 mA (but not exceeding 20 mA) will guarantee a logic state of 1; 5 mA is the recommended value.

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A.2.6.2 User Output

The mechanical relay is from OMRON (P/N-G5V-1). Maximum switching capability is 0.5 A at 30 Vdc.

A.2.7 Ethernet A / Ethernet B Test Connectors (*Themis-Authorized Personnel Only*)

- *Connector Type:* RJ45 TP Ethernet with LEDs (2)
- *Manufacturer; Part Number:* Amp; 406549-1

Two test RJ45 connectors for Ethernet A and Ethernet B have been placed on the top (component) side of the Rear Transition Board. These connectors are designed to be used for testing purposes by *Themis-authorized personnel only.*

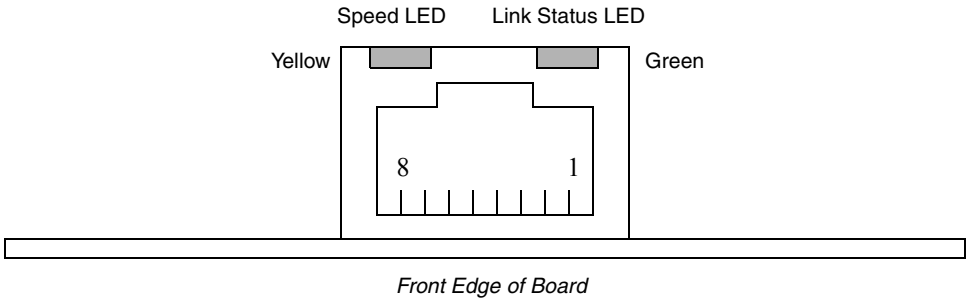


Figure A-17. Ethernet A or B Connector Orientation (Front View)

Table A-17. RJ45 Ethernet A Pinout

Pin	Signal Name
1	TXD+
2	TXD–
3	RXD+
4	TXGND
5	TXGND
6	RXD–
7	RXGND
8	RXGND

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A.3 Memory Module Connector

- *Connector Type:* 2-Part (Receptacle/Plug), 2-row, 200-pin, Board-to-Board (Receptacle is mounted on Baseboard)
- *Manufacturer; Part Number:* Molex; 52760-2009 (R), 53481-2009 (P)

The custom Memory Module is installed onto the USPII*e*-cPCI Baseboard with one connector to attach it to the Baseboard (see *Figure A-18*).

Caution: Because of the *cPCI Specification* requiring a 0.8-inch interboard separation (see *Figure 1-5* on page 1-9) between cPCI slots, only one Memory Module can be installed onto a USPII*e*-cPCI Baseboard (*stacking not supported*).

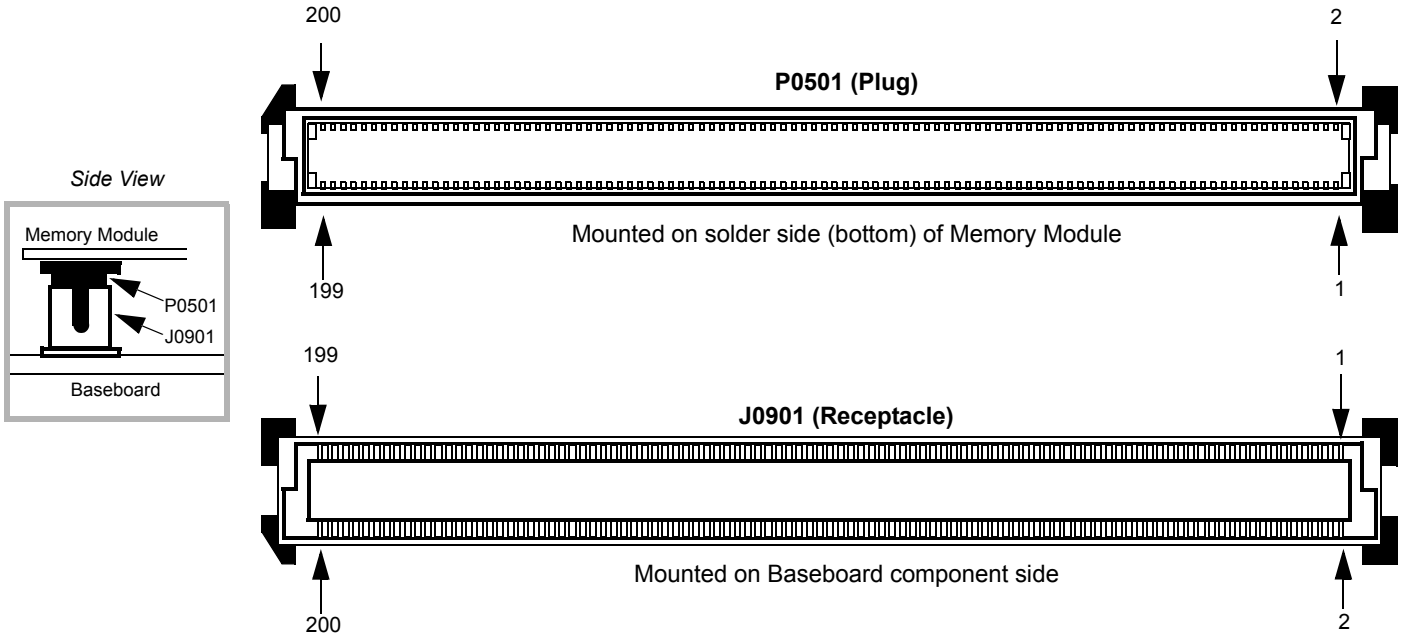


Figure A-18. Memory Module Baseboard Connectors (Receptacle & Plug)

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Appendix B

Jumper-Pin and Solder-Bead Configurations

B.1 Overview

This appendix provides a summary of the jumper-pin and solder-bead configurations for the USPII*e*-cPCI Baseboard and Rear Transition Board (the Memory Module does not contain jumper pins or solder beads). **Jumper pins** are considered "field-configurable" and may be altered on site. **Solder beads** are considered "factory-configurable" and *must not be altered* by the user. If a solder bead requires re-configuration, contact Themis Customer Service.



Warning: Attempting to alter a solder-bead configuration could seriously damage the USPII*e*-cPCI.
DO NOT ATTEMPT TO ALTER SOLDER-BEAD CONFIGURATIONS.

B.2 Field-Configurable

B.2.1 Baseboard Jumper Pins

Jumper pins are found only on the *top* (component) side of the USPII*e*-cPCI Baseboard and are described in *Table B-1* on page B-2.

In *Table B-1*, an **ON** jumper position means the jumper is installed, shorting the pins and completing the circuit. **OFF** means there is no jumper installed, hence the path between the pins is open, breaking the circuit.

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Figure B-1, page B-3, provides the location of all jumpers on the USPII*e*-cPCI Baseboard. In *Figure B-1*, jumper pin 1 is identified with a **square** and a **triangle**.

Table B-1. Baseboard Jumper-Pin Settings

Jumper Pins	Jumper Position[a]	Description
JP2201	**ON**	Flash 0 is writable.
	OFF	Flash 0 is NOT writable.
JP2202	**ON**	Flash 1 is writable.
	OFF	Flash 1 is NOT writable.
JP2203	**ON**	Flash 2 is writable.
	OFF	Flash 2 is NOT writable.
JP2701, JP2702	**ON**	JP2701 and JP2702 determine the boot device (*see Table B-2)*. *(JP2701 and JP2702 are configured together.)*
	OFF	
JP2703	**ON**	Use the first (lower) bank in the Flash PROM.
	OFF	Use the second (upper) bank in the Flash PROM.
JP2704 to JP2706	**ON**	Select OBP patch execution during reset.
	OFF	*Reserved for Themis engineering use.*
JP3701	Short 1–2	On-board PMC 0 Module does not support 64-bit PCI bus.
	Short 2–3	On-board PMC 0 Module supports 64-bit PCI bus.

a—Boldface = the default jumper position.

Table B-2. Boot-Device Settings[a]

JP2702	JP2701	Boot Device
Jumper ON	**Jumper ON**	Flash 0 PROM
Jumper ON	Jumper OFF	Flash 1 PROM
Jumper OFF	Jumper ON	Flash 2 PROM
Jumper OFF	Jumper OFF	ROMBO

a—See also Tables 4-3 and 4-4 in Chapter 4 of the *USPIIe-cPCI Software Manual*.

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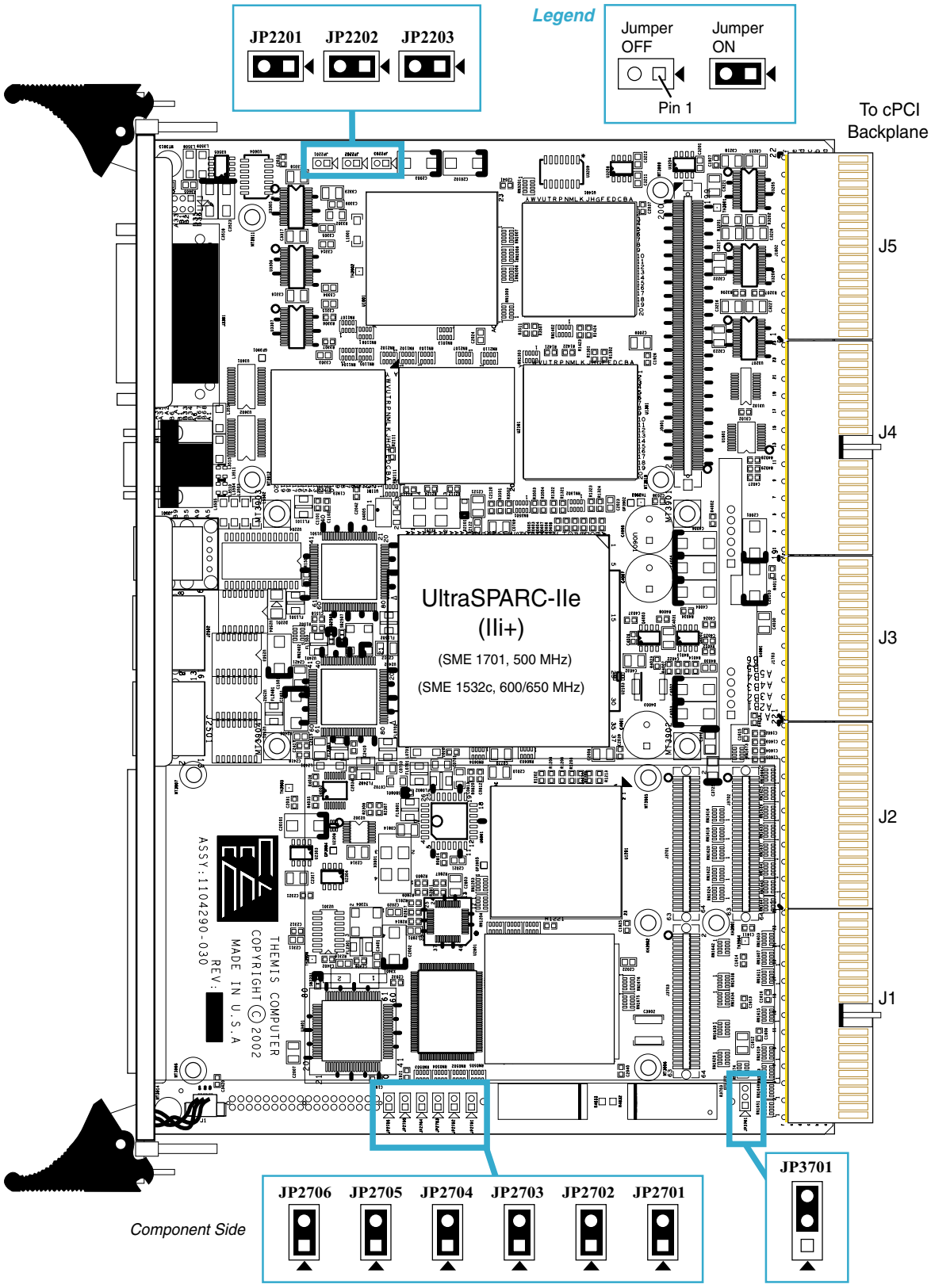


Figure B-1. Baseboard Jumper-Pin Locations (Component Side)

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B.2.2 Rear Transition Board Jumper Pins

There are four sets of jumper pins on the *top* (component) side of the USPII*e*-cPCI Rear Transition Board. These are described in *Table B-1* and *Figure B-2*, page B-5.

Table B-3. Rear Transition Board Jumper-Pin Settings

Jumper Pins	Jumper Position[a]	Description
JP1001	Short 1–2	Enable serial port A on the Rear Transition Board. [Serial port A is disabled on the Front Panel.]
	Short 2–3	Disable serial port A on the Rear Transition Board. [Serial port A is enabled on the Front Panel.]
JP1002	Short 1–2	Enable serial port B on the Rear Transition Board. [Serial port B is disabled on the Front Panel.]
	Short 2–3	Disable serial port B on the Rear Transition Board. [Serial port B is enabled on the Front Panel.]
JP1003	Short	*Themis testing use only.* [When shorted, TTY C will loop back transmit to receive signals.]
	Open	
JP1004	Short	*Themis testing use only.* [When shorted, TTY D will loop back transmit to receive signals.]
	Open	

a—Boldface = the default jumper position.

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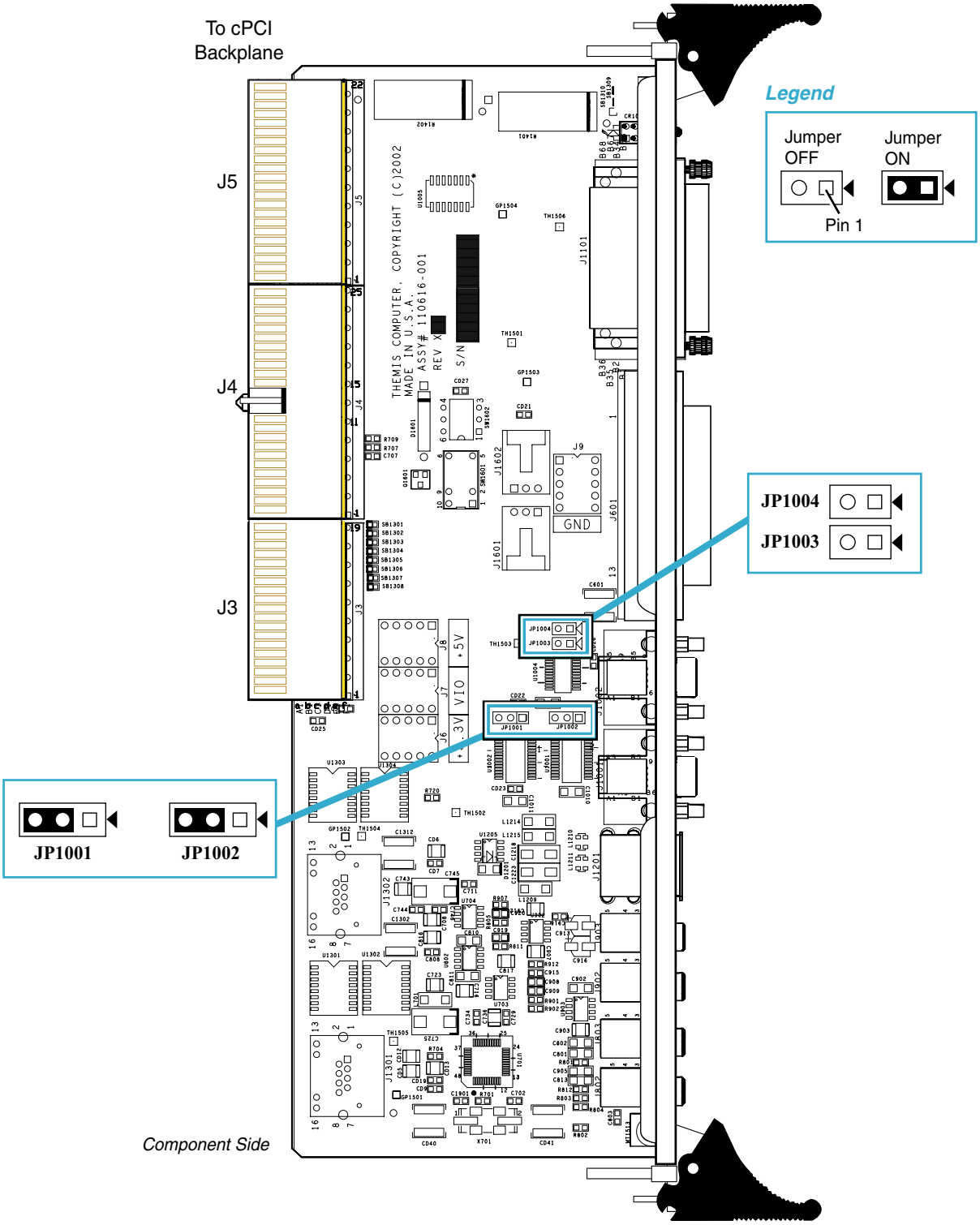


Figure B-2. Rear Transition Board Jumper-Pin Locations (Component Side)

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B.3 Factory-Configurable

B.3.1 Baseboard Solder Beads

Solder beads are found on both the *top* (component) side and *bottom* (solder) side of the USPII*e*-cPCI Baseboard and are described in *Table B-4*.

In *Table B-4*, if no pin number is given, only **2** solder pins exist. If there are **3** solder pins, the two pins listed are shorted together. **Short** means a solder bead is installed, creating an electrical path between two contacts. **Open** means no solder bead is installed, hence the path between the contacts is open.

Figure B-3 on page B-9 and *Figure B-4* on page B-10 provides the locations of all Baseboard solder beads. Pin 1 is indicated on the board by a **thick bar line**.



Caution: When dealing with a **3-pin** solder-bead switch, a solder bead will short only one set of pins, either 1–2 or 2–3.
If a solder bead shorts more than 2 pins, call Themis Customer Support.

Table B-4. Baseboard Solder-Bead Settings (Both Sides)

Solder Bead	Top Side Setting[a]	Bottom Side Setting[a]	Description
SB0801	Short		CPU CLK PLL (clock phase-locked loop) can be programmed (*normal mode*).
	Open		CPU clock generator serial load is disabled.
SB2201	**Short 1–2**		Only 5V is connected to programming power of flash memory.
	Short 2–3		Only 12V is connected to programming power of flash memory.
SB2204		**Short 1–2**	TOD/NVRAM is M48T59.
		Short 2–3	TOD/NVRAM is M48T35.
SB2205		Short	TOD/NVRAM is M48T35.
		Open	TOD/NVRAM is M48T59.
SB2501 to SB2504; SB2506, SB2508		**Short 1–2**	Ethernet A and B ports are accessible from front panel only.
		Short 2–3	Ethernet A and B ports are accessible from rear using 2.16-compliant cPCI backplane only (not through Rear Transition Board).
SB2507, SB2509	**Short 1–2**		Ethernet A and B ports are accessible from front panel only.
	Short 2–3		Ethernet A and B ports are accessible from rear using 2.16-compliant cPCI backplane only (not through Rear Transition Board).

Note: Footnotes are described at the end of *Table B-4* on page B-7.

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Table B-4. Baseboard Solder-Bead Settings (Both Sides) (Continued)

Solder Bead	Top Side Setting[a]	Bottom Side Setting[a]	Description
SB2701		Short	The 3.3V standby signal is disabled (*battle mode*).
		Open	The 3.3V standby signal is enabled.
SB2702		Short	The Vdd-core standby signal is disabled (*battle mode*).
		Open	The Vdd-core standby signal is enabled.
SB2703		**Short 1–2**	CPU speed setting. *See Table B-6, page B-8 (SB2703 and SB2705 are set together)*
		Short 2–3	
SB2704		Short	*Manufacturing use only.*
		Open	Disable PLD clock test.
SB2705		Short 1–2	CPU speed setting. *See Table B-6, page B-8 (SB2703 and SB2705 are set together)*
		Short 2–3	
SB2706		Short 1–2	*Manufacturing use only:* The secondary ROMBO chip-select (implemented for debugging purposes only) is asserted when the CPU accesses the upper half of the 1-MB address window assigned to the PLD.
		Short 2–3	*Manufacturing use only:* The secondary ROMBO chip-select (implemented for debugging purposes only) is a copy of one of 8 Rio chip-selects as indicated by the *test_status register* of the PLD (see *cPCI Software Manual*).
SB3201, SB3203		Short 1–2	*Factory set to define type of on-board terminator:* Beads 2-3 will be shorted if Dallas DS2119M is installed. Beads 1-2 will be shorted if Unitrode UCC5673 installed.
		Short 2–3	
SB3202, SB3204		Short 1–2	
		Short 2–3	
SB3502[b]		Short	USB is indicated for the front-panel DIN (8-pin) connector.
		Open	PS/2 is indicated for the front-panel DIN (8-pin) connector.
SB3503[b] to SB3506		**Short 1–2**	PS/2 is enabled on the front-panel DIN (8-pin) connector.
		Short 2–3	USB-A and USB-B are enabled on the front-panel DIN (8-pin) connector.

a—Boldface = the default solder-bead position.

b—SB3502 through SB3506 must be set together; see *Table B-5* on page B-8.
SB3502 through SB3506 affect PS/2-Port Versions only; these solder beads do not affect the USB-Port Version USPII*e*-cPCI.

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Table B-5. Front-Panel DIN/USB Solder-Bead Settings

		Type of Front-Panel Connector		
		DIN-8[a]		Dual USB
Electrical Interface	PS/2	SB3502	Open	*Not Available*
		SB3503 to SB3506	Short 1-2	*Not Available*
	USB	SB3502	Short	*Don't Care*
		SB3503 to SB3506	Short 2-3	*Don't Care*

a—PS/2 is accessible only through a special split pigtail cable (Themis 110104-002)

- 8-pin mini-DIN to 6-pin keyboard DIN and 6-pin mouse DIN

USB is accessible only through a special split pigtail cable (Themis 110473-001)

- 8-pin mini-DIN to dual 4-pin USB

Table B-6. CPU Speed Settings

SB2703	SB2705	CPU[a] Speed (600/650 MHz)	CPU[b] Speed (500 MHz)
Short 1-2	Short 1-2	650 MHz	500 MHz
Short 1-2	Short 2-3	600 MHz	*Not applicable*
Short 2-3	Short 1-2	*Not applicable*	*Not applicable*
Short 2-3	Short 2-3	*Not applicable*	*Not applicable*

a—USPIIi-type.
b—USPIIe-type.

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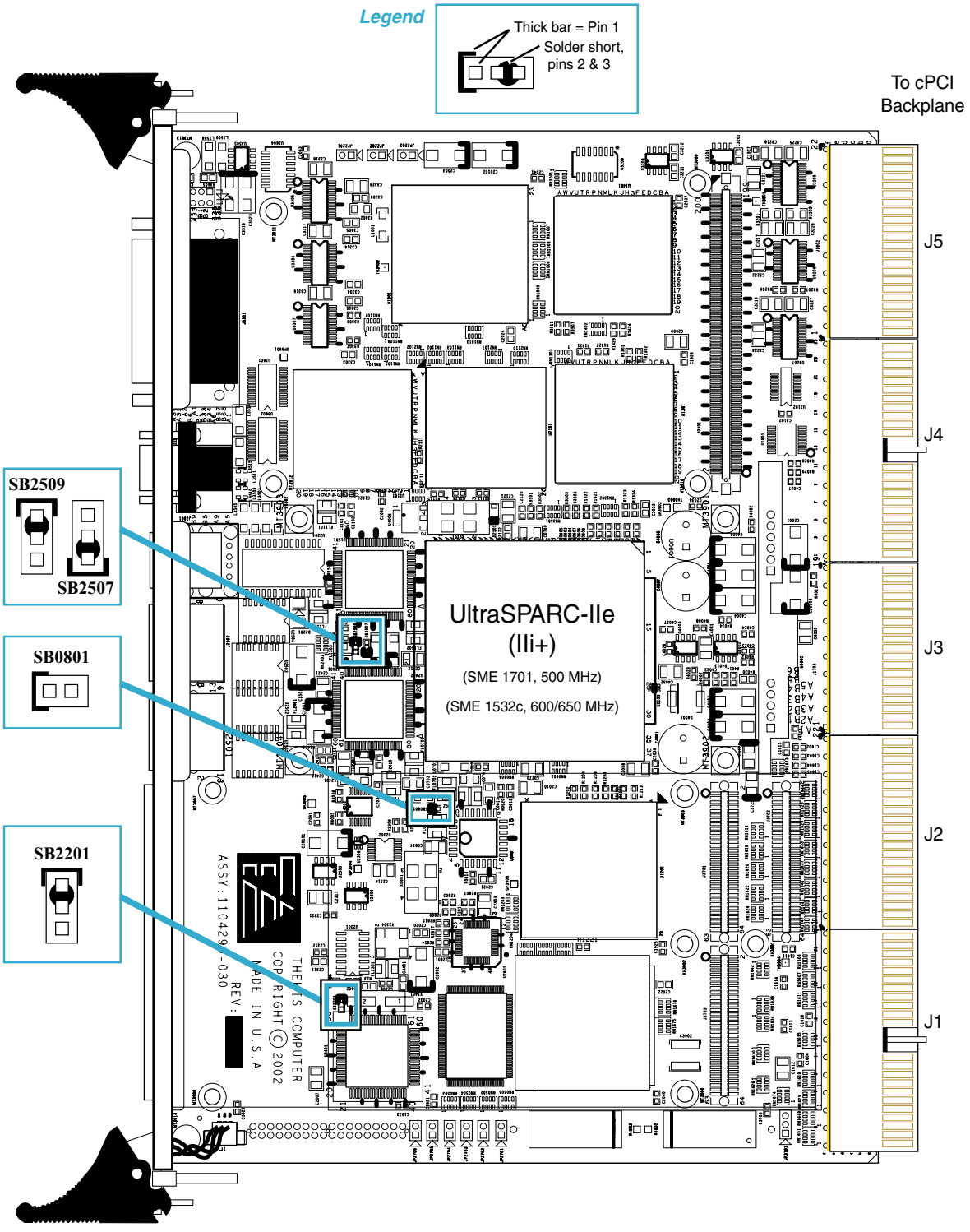


Figure B-3. Baseboard Solder-Bead Locations (Component Side)

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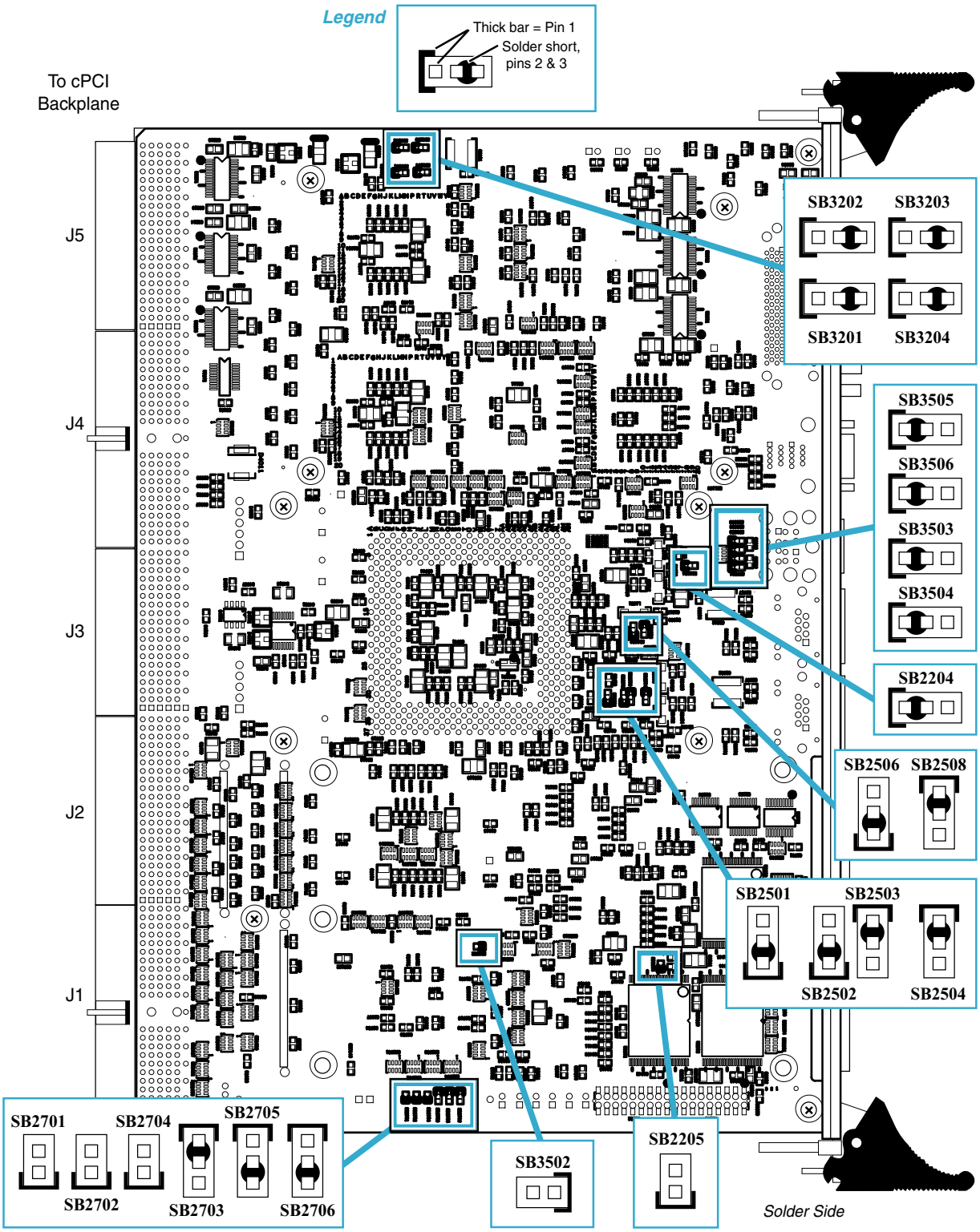


Figure B-4. Baseboard Solder-Bead Locations (Solder Side)

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B.3.2 Rear Transition Board Solder Beads

There are 10 sets of solder beads on the USPII*e*-cPCI Rear Transition Board, located on the *top* (component) side of the board (see *Table B-7*, *Figure B-5*, page B-12).

Table B-7. Rear Transition Board Solder-Bead Settings

Solder Bead	Top Side Setting[a]	Description
SB1301[b]	Short	*Themis use only.*[c]
	Open	Ethernet A and B ports are accessible from rear using 2.16-compliant cPCI backplane only (not through Rear Transition Board).
SB1302	Short	*Themis use only.*[c]
	Open	Ethernet A and B ports are accessible from rear using 2.16-compliant cPCI backplane only (not through Rear Transition Board).
SB1303	Short	*Themis use only.*[c]
	Open	2.16-compliant Ethernet A/B are accessible from cPCI backplane.
SB1304	Short	*Themis use only.*[c]
	Open	2.16-compliant Ethernet A/B are accessible from cPCI backplane.
SB1305	Short	*Themis use only.*[c]
	Open	2.16-compliant Ethernet A/B are accessible from cPCI backplane.
SB1306	Short	*Themis use only.*[c]
	Open	2.16-compliant Ethernet A/B are accessible from cPCI backplane.
SB1307	Short	*Themis use only.*[c]
	Open	2.16-compliant Ethernet A/B are accessible from cPCI backplane.
SB1308	Short	*Themis use only.*[c]
	Open	2.16-compliant Ethernet A/B are accessible from cPCI backplane.
SB1309	Short	*Themis use only.*[c]
	Open	2.16-compliant Ethernet A/B are accessible from cPCI backplane.
SB1310	Short	*Themis use only.*[c]
	Open	2.16-compliant Ethernet A/B are accessible from cPCI backplane.

a—Boldface = the default solder-bead position.

b—SB1301 through SB1310 must be all open or all closed.

c—Access to Ethernet ports A and B is through connectors on surface of Rear Transition Board.

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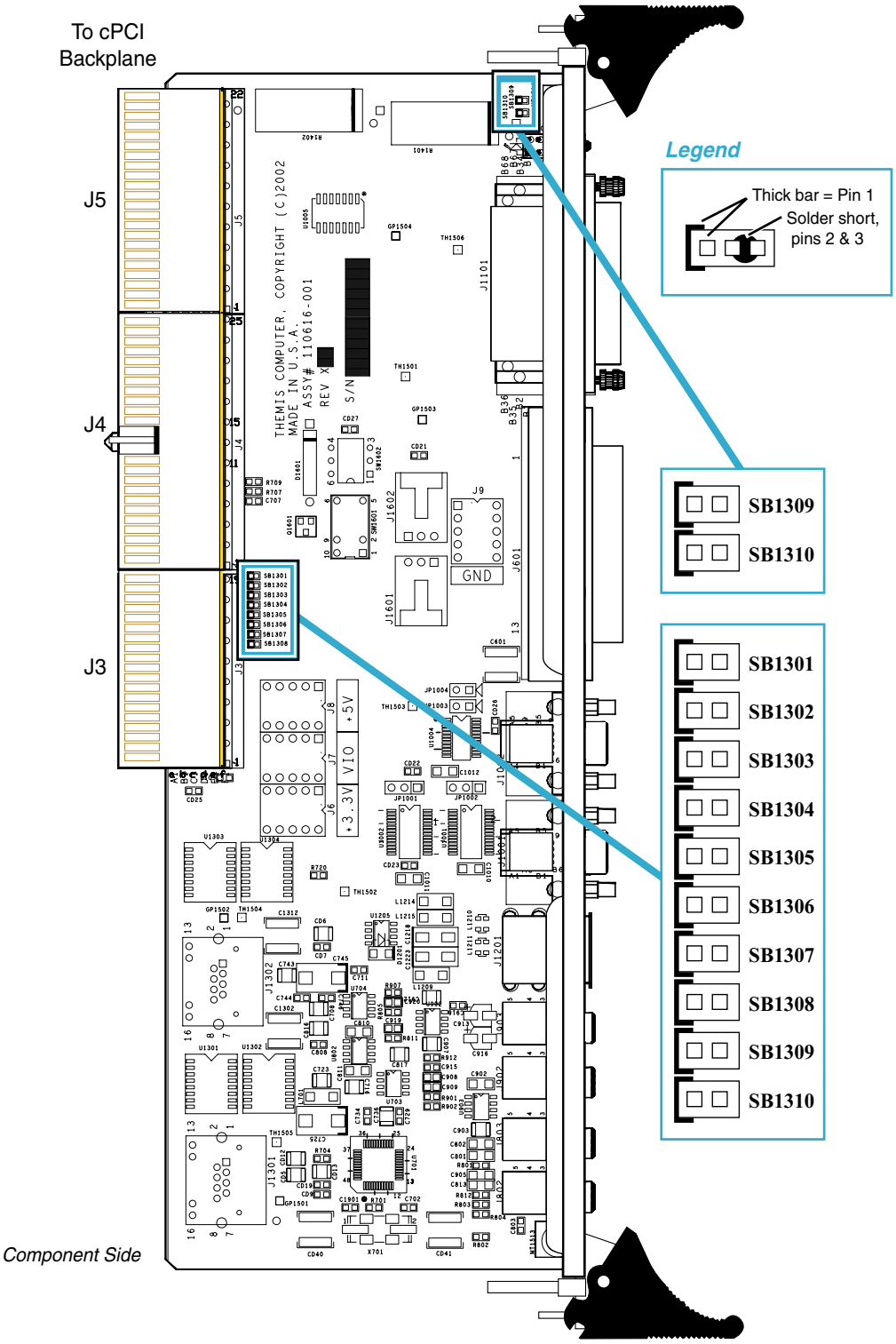


Figure B-5. Rear Transition Board Solder-Bead Locations (Component Side)

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Appendix C

Front and Rear Panel Diagrams

C.1 Introduction

This appendix contains diagrams of the front and rear panels (faceplates) for the USPII*e*-cPCI Baseboard and the Rear Transition Board.

C.2 USPII*e*-cPCI Baseboard Faceplate

Figure C-1 on page C-2 illustrates the faceplate for the USPII*e*-cPCI Baseboard.

C.2.1 Faceplate Dimensions

All front panels measure 264-mm (10.4”) high by 20-mm (0.8”)wide.

C.2.2 PS/2 and USB Protocols

Themis must be advised of whether you desire the PS/2 or USB option at the time the USPII*e*-cPCI is ordered, since it requires the installation, respectively, of either a mini-DIN-8-type or a dual-USB-type front-panel connector. This choice must then be supported by the setting of multiple solder beads at the factory before shipping (see Appendix B, “Jumper-Pin and Solder-Bead Configurations”).

Table C-1 on page C-3 describes devices that are supported by these protocols.

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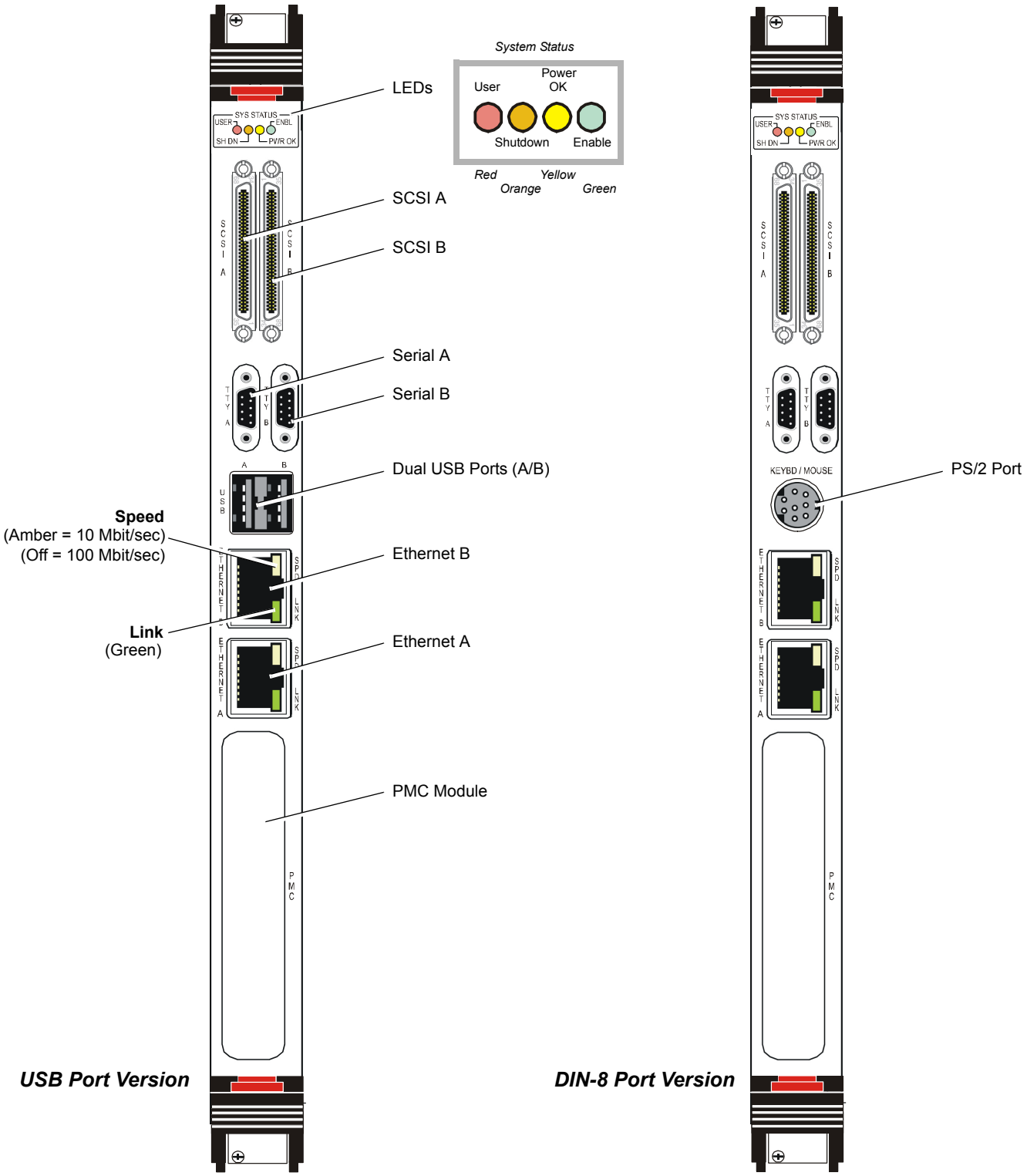


Figure C-1. USPIIe-cPCI Baseboard Faceplate

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Table C-1. PS/2 and USB Protocols and Connectors

Device Protocol	Type of Connector	
	Mini-DIN-8	**Dual-USB**
PS/2 (Keyboard/Mouse only)	*Adapter required:* DIN-8 → DIN-6, DIN-6 *Part: 110104-002*	
USB (Sun Keyboard/Mouse or any USB device)	*Adapter required:* DIN-8 → USB-A, USB-B *Part: 110473-001*	• Standard USB cable for each port (keyboard, mouse, or USB device)

Important: If you require a dual-USB port instead of a mini-DIN-8 port on your Baseboard front panel, make sure to specify this at the time of your order.

C.2.3 Ejector Handles

The USPII*e*-cPCI comes with two Elma IEEE P1101.10 cPCI-type locking handles (one at the top and one at the bottom), which allow the Baseboard to be firmly locked into the 6RU cPCI backplane. In addition, the lower handle has a microswitch installed that signals whenever a board is being hot-swapped into and out of the cPCI backplane (see *Figure C-2* on page C-4).

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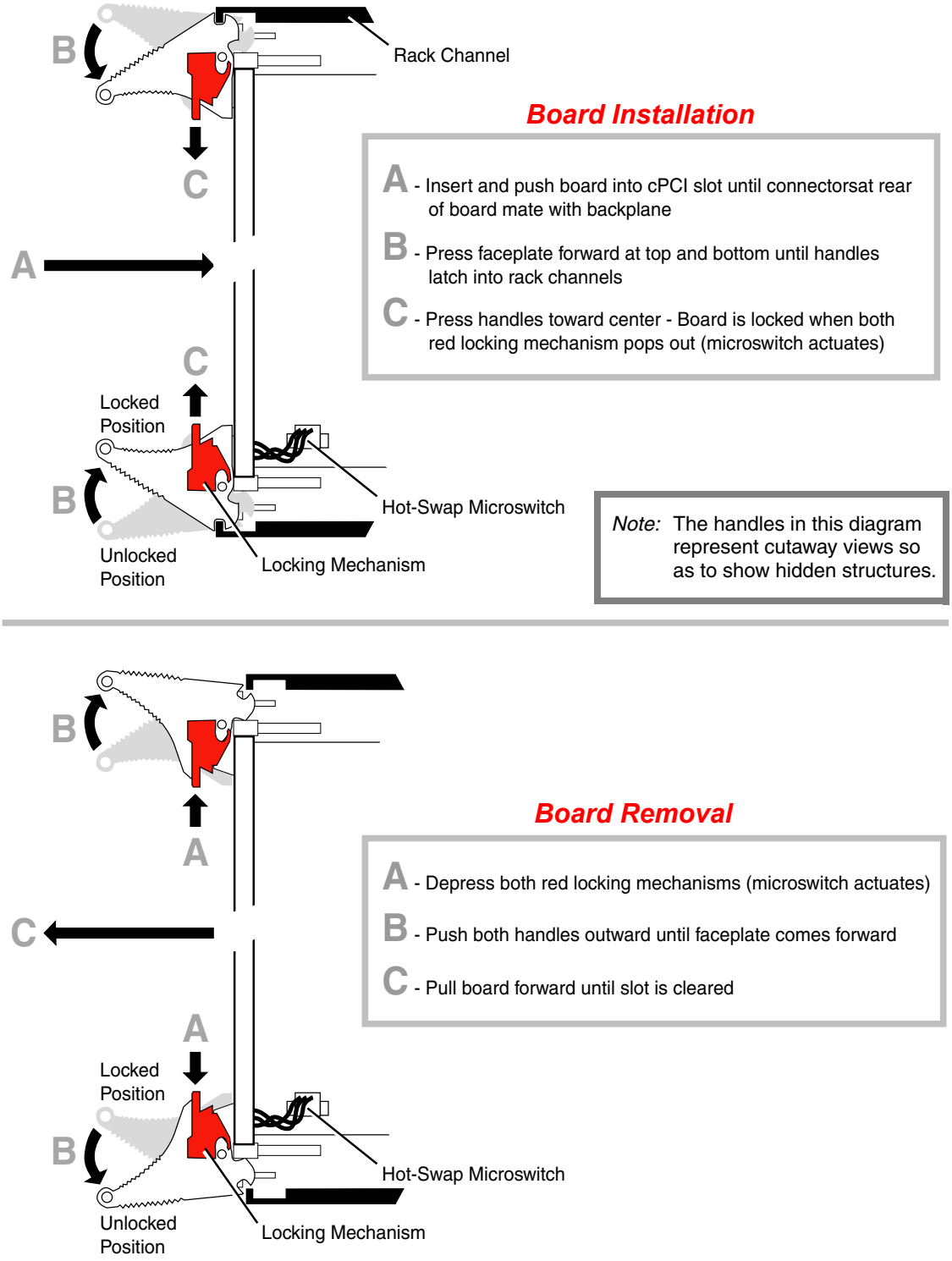


Figure C-2. Installation (Injection) and Removal (Ejection) of the USPIIe-cPCI

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C.3 Rear Transition Board Faceplate

Figure C-3 on page C-6 illustrates the faceplate for the USPII*e*-cPCI Rear Transition Board.

C.3.1 Ejector Handles

The Rear Transition Board comes with two Elma IEEE P1101.11 cPCI-type locking handles (one at the top and one at the bottom), which allow the Rear Transition Board to be firmly locked into the rear of the 6RU cPCI backplane. There is no microswitch installed in either handle.

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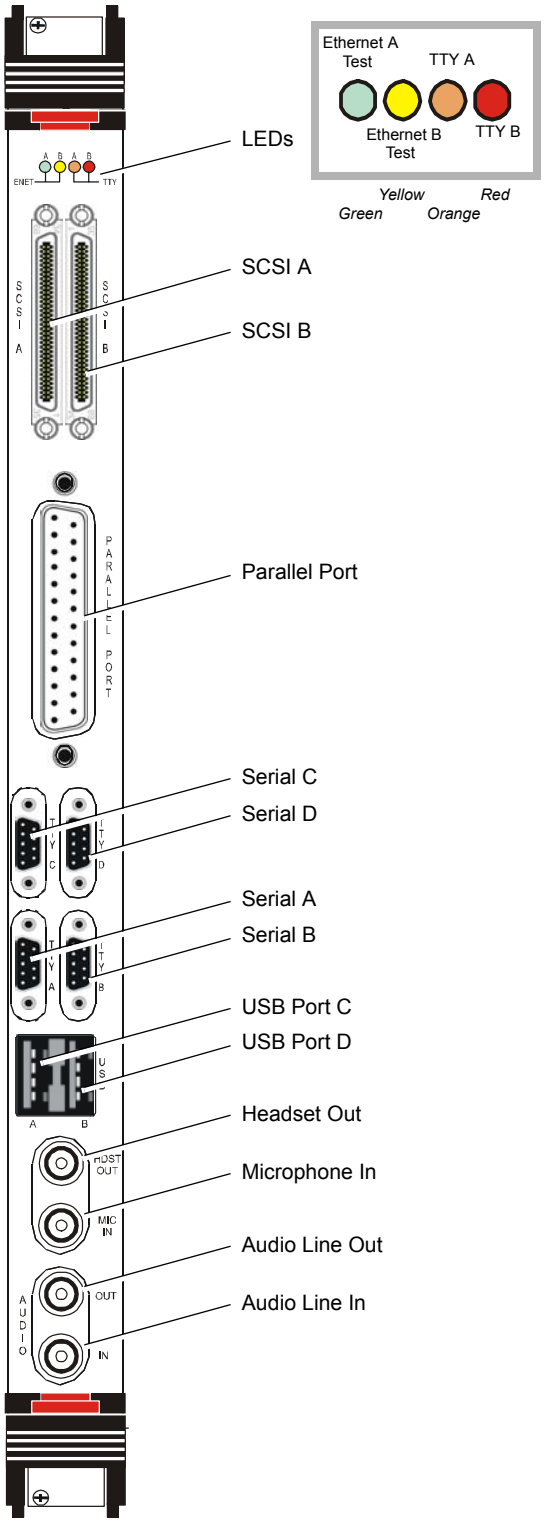


Figure C-3. USPIIe-cPCI Rear Transition Board Faceplate

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Appendix D

Board Diagrams

This appendix contains PC board diagrams of the USPII*e*-cPCI Baseboard and the Rear Transition Board. It is intended as a quick reference to component and connector identification.

See Appendix B, ”Jumper-Pin and Solder-Bead Configurations”, for a description of jumper-pin and solder-bead configurations. See Appendix C, ”Front and Rear Panel Diagrams”, for a front view of the Baseboard and Rear Transition Board faceplates.

D.1 Baseboard

Figure D-1 on page D-2 identifies major connectors and surface components as seen from the component side of the Baseboard. For a view of Baseboard connectors from the front panel, see *Figure C-1* on page C-2.

D.2 Rear Transition Board

Figure D-2 on page D-3 identifies the major components on the Rear Transition Board, as viewed from the component side. For a view of Transition Board connectors from the front panel, see *Figure C-3* on page C-6.

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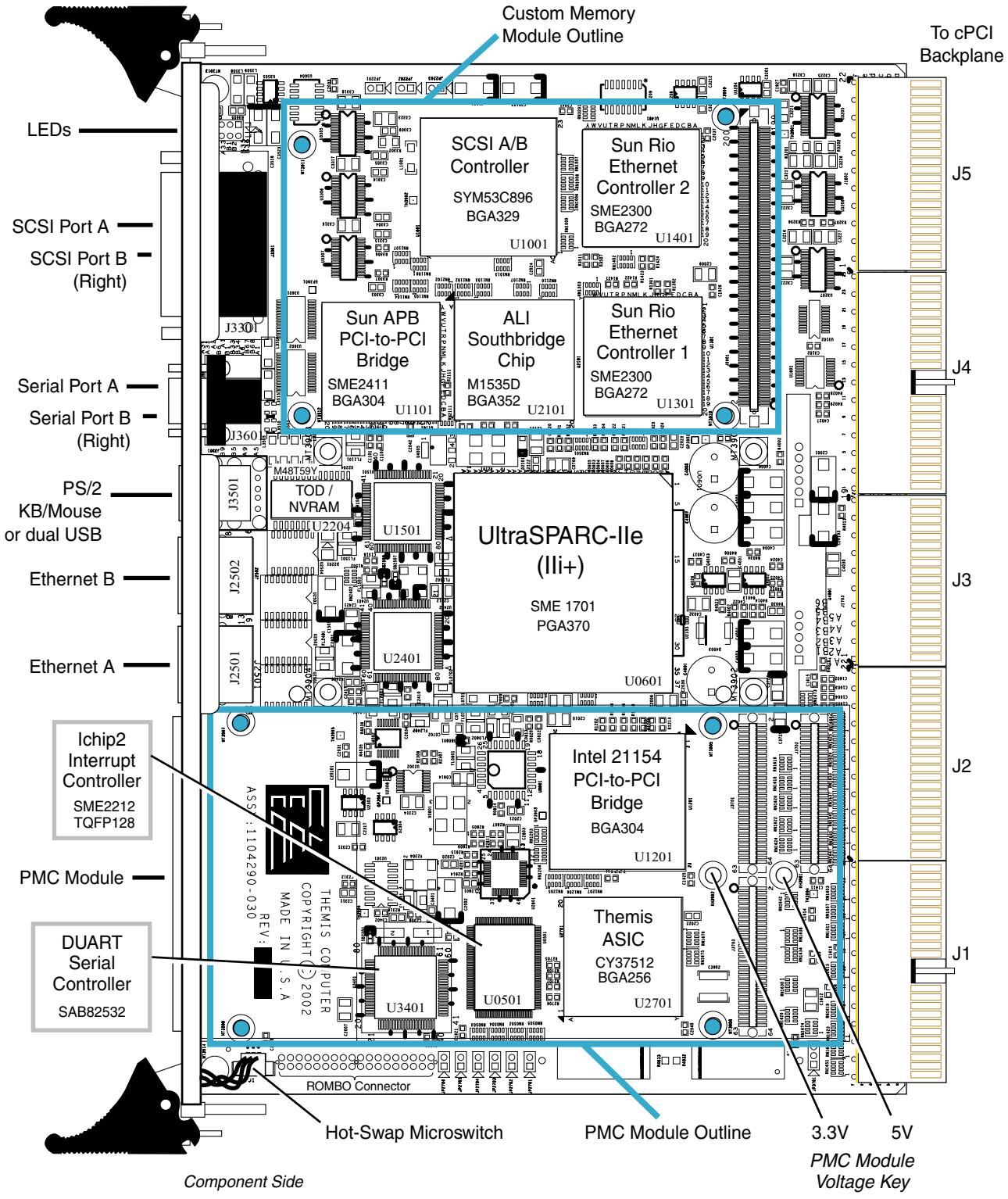


Figure D-1. USPIIe-cPCI Front-Panel, Component, and Connector Diagram

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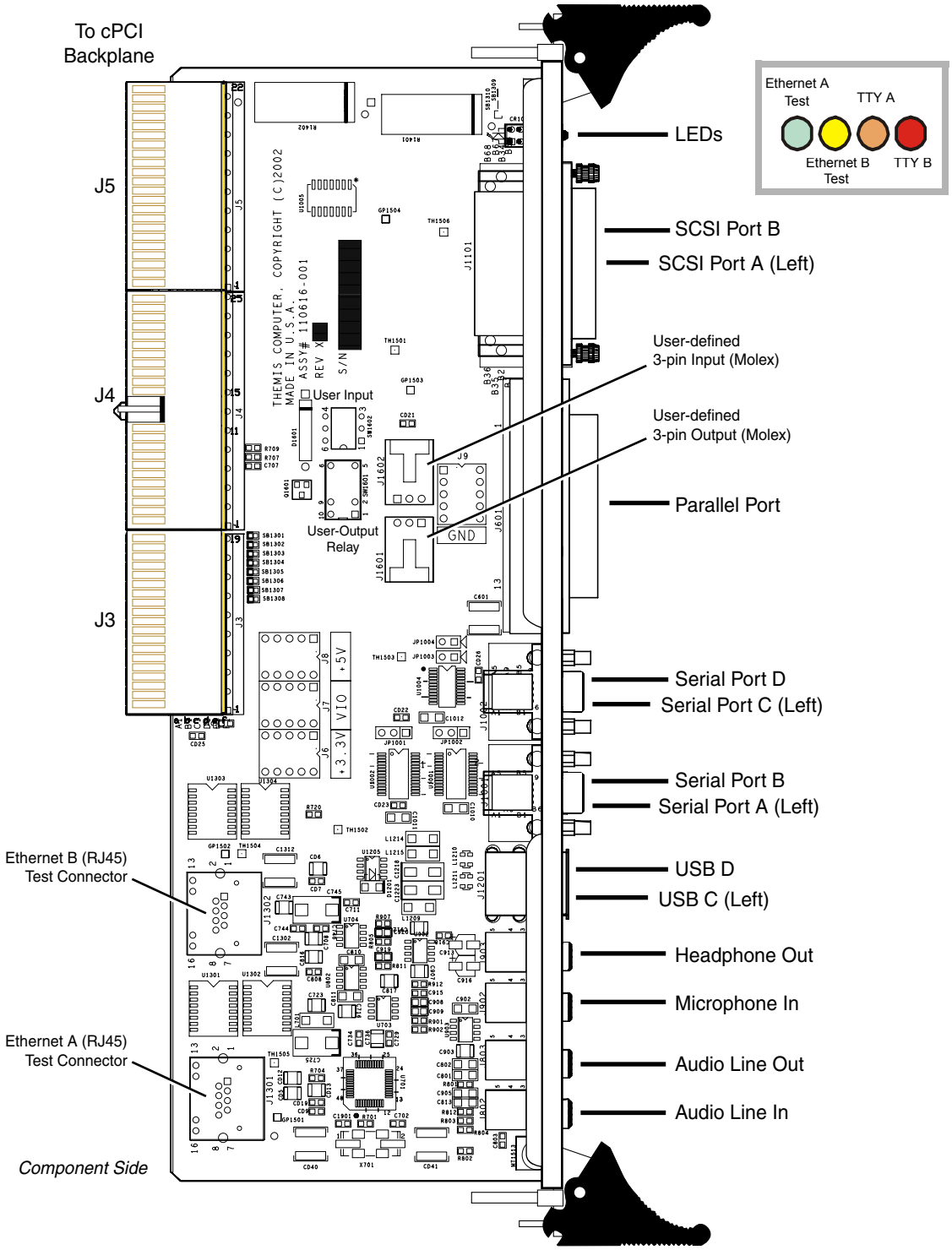


Figure D-2. Rear Transition Board (Component Side)

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Caution: Connect the Rear Transition Board to the **P3**/**P4**/**P5** connectors of the cPCI backplane only (see *Figure A-2* on page A-2 for details). Connection to any other connectors will cause malfunctions.

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Appendix E

Glossary

The terminology used in this manual follows industry conventions. The following list defines the specific meanings of words or terms that *may* be used in this manual.

APB: Advanced PCI Bridge

Arbitration: The process of assigning a resource to one of several requestors.

ASI: An abbreviation for "Address Space Identifier."

Boot: The process of initializing the hardware to execute and run an operating system such as Solaris.

cPCI: Compact PCI. An adaptation of the PCI Specification for industrial and/or embedded applications requiring a more robust mechanical form factor than desktop PCI applications.

CPI: Cycles per Instruction. The number of clock cycles required to execute one instruction.

CTS: Clear to send (DCE to DTE).

DCD (or CD): Data carrier detected (tone from a modem; DCE to DTE).

DCE: Data circuit-terminating/communications equipment (a modem, for example).

Device tree: The OBP probing process constructs a hierarchal representation of the hardware devices that are found on the bus, the host-bus being the root. The device tree includes several device nodes (PCI bus is a device-node).

DMA: Direct Memory Access. A facility of some architectures that allows a peripheral to read and write memory without intervention by the CPU. DMA is a lim-

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ited form or bus mastering.

DSR: Data set ready (DCE to DTE).

DTE: Data terminal equipment (a computer, terminal, or printer, for example).

DTR: Data terminal ready (DTE to DCE).

DUART: Dual Universal Asynchronous Receiver/Transmitter. *See* UART

Firmware: This is software that stays with the hardware, usually in a PROM or similar device. Referred to as OBP in IEEE 1275 standards. In the USPII*e* implementation, release version 3.10.x and later are supported. This version comes with the motherboard. The user may upgrade the OBP to a newer version if needed.

FPGA: Field-Programmable Gate Array. A gate array where the logic network can be programmed into the device after its manufacture. An FPGA consists of an array of logic elements, either gates or lookup table RAMs, flip-flops, and programmable interconnect wiring.

GBIC: GigaBit Interface Converter. A hardware module used to attach network devices to fiber-based transmission systems such as Fibre Channel and Gigabit Ethernet. The GBIC converts serial electrical signals to serial optical signals and vice versa.

GHz: Gigahertz (billions of cycles per second, 10^6 cps); unit of frequency.

GUI: The use of pictures rather than words to represent both the input and the output of a program. A program with a GUI runs under some windowing system.

HVD: High-Voltage Differential; usually shortened to Differential (see LVD).

Hardware: On the USPII*e*, the CPU module, cables, and peripheral devices are typical examples of hardware.

may: A keyword indicating flexibility of choice with no implied preference.

LED: Light-Emitting Diode.

LVD: Low-Voltage Differential (Device).

IOM: I/O Module.

ISR: In-Service Reprogramming.

MHz: Megahertz (millions of cycles per second, 10^9 cps); unit of frequency.

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MII: Medium Independent Interface.

MMU: Memory Management Unit.

NA or **N/A**: Not Applicable.

NC or **N/C**: No Connection.

NVRAMRC: Acronym for *N*on-*V*olatile *R*andom-*A*ccess *M*emory *R*un *C*ommand. This refers to the executable OBP script that is written in the NVRAM. Other text information or binary data may exist in the NVRAM, but is not referred as NVRAMRC.

OBP: Acronym for *O*pen*B*oot *P*ROM. This refers to a program that consists of code executable by the UltraSPARC-II*e* CPU. The Code is responsible for initialization of the hardware and booting the system to bring up the Solaris operating system or another operating system such as VxWorks.

PCI: Peripheral Component Interconnect (bus). A high-performance 32- or 64-bit bus with multiplexed address and data lines, as specified in the PCI Local Bus Specification, Revision 2.1, June 1, 1995. The internal bus on the Sun Microsystems UltraSPARC-II*e* is a PCI bus.

PHY: Physical transceiver or sublayer.

Physical Address: An address that maps to real physical memory or I/O device space.

PIO: Programmed I/O. A method of accessing devices under UNIX as special files (as opposed to mapping the physical address range to a process's virtual address space).

PLD: Programmable Logic Device.

PLL: Phase-Locked Loop. A feedback control system that automatically adjusts the phase of a locally generated signal to match the phase of an input signal.

PMC: PCI Mezzanine Card.

POR: Power-On Reset.

Probing: A process implemented in the firmware and software to identify on-board hardware devices and add-on cards on the PCI bus. The probing process creates the device-tree.

R0: An abbreviation used to indicate "Read Zero." When software attempts to read an R0 area, zero will be returned. Writes to R0 are not permitted.

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RC (RCK): Receiver clock input (external).

Read Cycle: A bus cycle used to transfer 1, 2, 3, 4, or 8 bytes from a Slave to a master.

Read-Modify-Write Cycle: A bus cycle used to read from, and then write to, a Slave location without permitting any other Master to access that location during that cycle.

RED_state: The Reset, Error, and *D*ebug state of the UltraSPARC-II*e* processor. The UltraSPARC-II*e* enters the RED_state when PSTATE.RED=1.

RI: Ring indicator (ring tone detected; DCE to DTE)).

RIC: Reset, Interrupt, Clock.

RMW: Read, Modify, Write.

RTS: Ready/request to send (DTE to DCE).

RXD (or RD): Receive data (DCE to DTE).

SCSI: Small Computer System Interface.

SCTS: Secondary clear to send (DCE to DTE).

SDCD: Secondary data carrier detected (tone from a modem; DCE to DTE).

SDRAM: Synchronous-Dynamic Random-Access Memory.

SE: Single-Ended (as in Single-Ended Differential SCSI).

SG: Signal ground.

SME: Sun Micro-Electronics.

SO-DIMM: Small-Outline Dual-Inline Memory Module.

Software: A collection of machine-readable information, instructions, data, and procedures that enable the computer to perform specific functions. Typically stored on electronic media.

Solaris: Sun Microsystems, Inc.'s version of the UNIX operating system. In addition to the core operating system, Solaris includes networking software, the Java Virtual Machine, the CDE/Desktop that includes an X11-based windowing environment, and a graphical user interface (GUI).

SRTS: Secondary ready to send (DTE to DCE).

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SRXD: Secondary receive data (DCE to DTE).

STXD: Secondary transmit data (DTE to DCE).

TLB: Translation Lookaside Buffer. A hardware cache that contains copies of recently used translations. Separate TLBs reside both in the MMU and the IOM.

TSB: Translation Storage Buffer. A one-level, software data structure that maintains address translation information. Separate TSBs reside both in the MMU and the IOM.

TSOP: Thin Small-Outline Package. A very thin surface-mount chip package with gull-wing pins on the short sides. TSOPs are approximately a third of the thickness of SOJ chips.

TXD (or TD): Transmit data (DTE to DCE).

UART: Universal Asynchronous Receiver/Transmitter. An integrated circuit used for serial communications that contains a transmitter (parallel-to-serial converter) and a receiver (serial-to-parallel converter), each clocked separately.

Virtual Address: An address produced by a processor that maps all system-wide, program-visible memory. Virtual addresses usually are translated by a combination of hardware and software to physical addresses, which can be used to access physical memory.

Write Cycle: A bus cycle used to transfer 1, 2, 3, 4 or 8 bytes from a Master to a Slave.

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