ARTISAN®
TECHNOLOGY GROUP

Your **definitive** source for quality pre-owned equipment.

Artisan Technology Group
(217) 352-9330 | sales@artisantg.com | artisantg.com

Full-service, independent repair center
with experienced engineers and technicians on staff.

We buy your excess, underutilized, and idle equipment
along with credit for buybacks and trade-ins.

Custom engineering
so your equipment works exactly as you specify.

- Critical and expedited services
- In stock / Ready-to-ship
- Leasing / Rentals / Demos
- ITAR-certified secure asset solutions

Expert team | Trust guarantee | 100% satisfaction

All trademarks, brand names, and brands appearing herein are the property of their respective owners.

Find the *Mercury Computer Systems / Themis USPIIe-USB/2048-650-PS2* at our website: *Click HERE*

USPIIe-USB Hardware Manual

Version 1.3—June 2009



Themis Computer—Americas and Pacific Rim
47200 Bayside Parkway
Fremont, CA 94538
Phone (510) 252-0870
Fax (510) 490-5529
World Wide Web http://www.themis.com

Themis Computer—Rest of World
5 Rue Irene Joliot-Curie
38320 Eybens, France
Phone +33 476 14 77 80
Fax +33 476 14 77 89

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Copyright © 2009 Themis Computer, Inc.

ALL RIGHTS RESERVED. No part of this publication may be reproduced in any form, by photocopy, microfilm, retrieval system, or by any other means now known or hereafter invented without the prior written permission of Themis Computer.

The information in this publication has been carefully checked and is believed to be accurate. However, Themis Computer assumes no responsibility for inaccuracies. Themis Computer retains the right to make changes to this publication at any time without prior notice. Themis Computer does not assume any liability arising from the application or use of this publication or the product(s) described herein.

RESTRICTED RIGHTS LEGEND: Use, duplication, or disclosure by the United States Government is subject to the restrictions set forth in DFARS 252.227-7013 (c)(1)(ii) and FAR 52.227-19.

TRADEMARKS

THEMIS® is a registered trademark of Themis Computer, Inc.

SOLARIS™ is a trademark of Sun Microsystems

SPARC® and UltraSPARC® are registered trademarks of SPARC International

All other trademarks or registered trademarks used in this publication are the property of their respective owners.

Themis Customer Support

North America, South America, and Pacific Rim

Telephone: 510-252-0870
Fax: 510-490-5529
E-mail: support@themis.com
Web Site: http://www.themis.com

USPIIe-USB Hardware Manual, Version 1.3

June 2009

Part Number: 110534-022

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Version Revision History

Version 1.3.....June 2009

- Modified solder-bead SB0902 in *Table B-8*, page B-12, to reflect change in default status and setting descriptions.
- Other assorted minor revisions and corrections throughout the manual.

Version 1.2.....August 2005

Version 1.1.....October 2003

Version 1.0.....October 2002

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Table of Contents

How to Use This Manual xvii

1. USPII*e*-USB Installation 1-1

1.1 Determine Board Type 1-1

1.2 Check Configurations 1-2

1.2.1 Combination PS/2–USB Connector 1-3

1.2.2 SCSI Termination 1-4

1.3 Installing USPII*e*-USB Paddle Boards 1-7

1.3.1 Standard Paddle Board 1-7

1.3.2 Multiple-I/O Paddle Board 1-7

1.4 Attaching Cables and Accessing USPII*e*-USB Peripheral Devices 1-9

1.4.1 Serial Ports A/B (TTYA and TTYB) 1-9

1.4.1.1 Front Panel Connection 1-9

1.4.1.2 VME P2 Connection 1-9

1.4.2 Serial Ports C/D (TTYC and TTYD) 1-9

1.4.3 Serial Ports E/F (TTYE/F) 1-10

1.4.3.1 Front Panel Connection 1-10

1.4.3.2 VME P2 Connection 1-10

1.4.4 Parallel (Printer) Port 1-10

1.4.5 PMC (Expansion) Module Slots 1-10

1.4.6 Ethernet Network 1-10

1.4.7 SCSI A and B 1-11

1.4.8 USB-0 and USB-1 1-11

1.4.9 USB-2 1-12

1.4.10 Miscellaneous I/O 1-12

1.4.10.1 From the Baseboard VME P2 1-12

1.4.10.2 From the PMC Carrier Board VME P2 1-12

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

1.5 Configuring the VME Interface 1-13
1.5.1 Using OBP to Program the VME Interface 1-13
1.5.1.1 OBP Commands 1-13
1.5.1.2 OBP Environment Variables 1-13
1.6 TOD/NVRAM Battery Replacement 1-14

2. USPII*e*-USB Specifications 2-1
2.1 Baseboard 2-1
2.2 PMC Carrier Board 2-4
2.3 Graphics Board 2-6
2.4 Paddle Boards 2-7
2.4.1 Standard Paddle Board 2-7
2.4.2 Multiple I/O Paddle Board 2-7
2.5 Backplane Jumper Settings 2-8
2.6 System Specifications 2-8
2.6.1 Processor and Memory Subsystems 2-8
2.6.2 I/O Subsystem 2-9
2.6.3 Auxiliary Functions 2-12
2.7 Environmental Specifications 2-13
2.8 Estimated Power Requirements 2-13

3. Hardware Overview 3-1
3.1 Baseboard 3-1
3.1.1 UltraSPARC-II*e* Processor and Cache 3-1
3.1.2 USPII*e*-USB ICHIP-2 Interrupt Controller 3-3
3.1.3 PCI-to-PCI Bridges 3-4
3.1.3.1 Advanced PCI Bridge (APB) 3-4
3.1.3.2 Intel 21154 PCI-to-PCI Bridge 3-4
3.1.4 Sun Rio I/O Controller 3-5
3.1.5 Symbios SCSI Controller 3-5
3.1.6 Tundra Universe II 3-5
3.1.7 PLD 3-6
3.1.8 Acer Super I/O Controller 3-6
3.1.9 Seimens SAB 82532 Controller 3-6
3.1.10 Flash Memory 3-6

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

3.1.11 TOD and NVRAM 3-6
3.1.12 Memory Subsystem 3-7
3.2 PMC Carrier Board 3-9
3.3 OpenBoot PROM 3-9

4. Universe II Description 4-1
4.1 Features 4-1
4.2 VMEbus Interface 4-2
4.2.1 VMEbus Configuration 4-2
4.2.2 Universe II as the VMEbus Slave 4-2
4.2.3 Universe II as the VMEbus Master 4-3
4.2.4 VMEbus First Slot Detector 4-5
4.2.4.1 Automatic Slot Identification 4-6
4.2.4.2 Register Access at Power Up 4-7
4.2.5 Universe II's Hardware Power-Up Options 4-7
4.3 Slave Image Programming 4-9
4.3.1 VME Slave Images 4-9
4.3.1.1 VMEbus Fields 4-10
4.3.1.2 PCI Bus Fields 4-11
4.3.1.3 Control Fields 4-11
4.3.2 PCI Bus Target Images 4-12
4.3.2.1 PCI Bus Fields 4-12
4.3.2.2 VMEbus Fields 4-13
4.3.2.3 Control Fields 4-14
4.3.2.4 Special PCI Target Image 4-15
4.4 Universe II's Interrupt and Interrupt Handler 4-17
4.4.1 VME and PCI Interrupters 4-17
4.4.2 VMEbus Interrupt Handling 4-18
4.4.3 Universe II's Mailbox Registers 4-18
4.4.4 Universe II's Semaphores 4-18
4.4.5 Programmable Slave Images on the VMEbus and PCI bus 4-18
4.4.6 DMA Controller 4-19

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

5. Programmable Logic Device 5-1
5.1 Introduction 5-1
5.2 Flash Mapping and Boot Control 5-2
5.3 PLD registers 5-2
5.4 2-Level Watchdog 5-3
5.5 Power management 5-4
5.6 Temperature management 5-5

6. Resets 6-1
6.1 Overview 6-1
6.2 UltraSPARC-II*e* Reset Request Signals 6-2
6.2.1 System_Reset and P-Reset 6-3
6.2.2 Externally Initiated Reset (XIR) 6-3
6.2.3 Watchdog Reset (WDR) 6-3
6.2.4 Software Initiated Reset (SIR) 6-3
6.3 Reset Sources 6-4
6.3.1 Push-Button Reset 6-4
6.3.2 Power Management Resets 6-4
6.3.3 VMEbus Resets 6-4
6.3.4 2-Level Watchdog Resets 6-5
6.3.5 Software POR 6-5
6.3.6 Software XIR 6-6
6.4 UltraSPARC-II*e* Reset_Control_Register 6-6

Appendix A. Connector Pinouts, LEDs, Switches A-1
A.1 Baseboard VME P1 ..... A-1
A.2 Baseboard VME P2 ..... A-3
A.3 Baseboard A-5
A.3.1 SCSI A and B A-5
A.3.2 Ethernet Port A A-7
A.3.3 Combination PS/2–USB Connector A-8
A.3.4 Serial Port A (RS232) and B (RS232/422) A-9

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

A.3.5 PMC Module Slot 0 ..... A-10
A.3.6 LEDs A-10
A.3.7 Push-Button RESET A-11
A.4 PMC Carrier Board A-11
A.4.1 PMC Carrier Board VME P1 Connector A-12
A.4.2 PMC Carrier Board VME P2 Connector A-14
A.4.3 PMC Module Slot User I/O A-16
A.4.3.1 PMC Module Slot 1: 64-Bit User I/O Configuration A-17
A.4.3.2 PMC Module Slot 1: 32-Bit User I/O Configuration A-18
A.4.3.3 PMC Module Slot 2: 32-Bit User I/O Configuration A-19
A.4.3.4 PMC Module Slot 3: 0-Bit User I/O Configuration A-20
A.4.4 Serial Ports E and F (RS232) A-21
A.4.5 Ethernet Port B A-22
A.4.6 Stereo Audio Connectors A-22
A.5 Paddle Boards A-23
A.5.1 Standard Paddle Board A-23
A.5.1.1 SCSI Port A Connector A-23
A.5.1.2 Serial (TTY) Port B Connector A-24
A.5.2 Multiple I/O Paddle Board A-26
A.5.2.1 Ultra160 SCSI Port A (68-pin female) A-27
A.5.2.2 Parallel Port A-27
A.5.2.3 Serial Port A, C, and D (RS-232) A-27
A.5.2.4 Serial Port B (RS-232 with modem support) A-27
A.5.2.5 Dual USB Port A-27
A.5.2.6 PS/2 Keyboard/Mouse Port (mini-DIN-8) A-27
A.5.2.7 Stereo Audio Line Out and Line In A-27
A.6 Memory Module Connector A-28

Appendix B. DIP-Switch, Jumper-Pin, and Solder-Bead Configurations B-1

B.1 Overview B-1
B.2 Field-Configurable B-1
B.2.1 DIP Switch B-1
B.2.2 Baseboard Jumper Pins B-3
B.2.3 Paddle Board Jumper Pins B-5
B.2.4 PMC Carrier Board Jumper Pins B-5

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

B.3 Factory-Configurable B-7
B.3.1 Baseboard Solder Beads B-7
B.3.2 Memory Module Solder Beads B-9
B.3.3 Paddle Board Solder Beads B-9
B.3.4 PMC Carrier Board Solder Beads B-11

Appendix C. Front Panel Diagrams C-1

C.1 Introduction C-1
C.1.1 Front-Panel Dimensions C-2
C.1.2 Ejector Handles C-2
C.1.2.1 VME64-type Handles Only C-2
C.1.3 PS/2 and USB Protocols C-3

C.2 USPII*e*-USB Front Panels C-3
C.2.1 USPII*e*-USB/1 (Single VME Slot) C-4
C.2.2 USPII*e*-USB/2G—Baseboard & 1 Graphics Board C-5
C.2.3 USPII*e*-USB/3G2—Baseboard & 2 Graphics Boards C-6
C.2.4 USPII*e*-USB/3GP2—Baseboard, 1 Graphics Board, and 2-PMC Carrier Boards C-7
C.2.5 USPII*e*-USB/3GP3—Baseboard, 1 Graphics Board, and 3-PMC Carrier Boards C-8
C.2.6 USPII*e*-USB/2P2 (2 VME Slots) C-9
C.2.7 USPII*e*-USB/2P3 (2 VME Slots) C-10

Appendix D. Board Diagrams D-1

D.1 Baseboard D-1
D.2 PMC Carrier Board D-1
D.3 Paddle Boards D-1

Appendix E. Glossary E-1

Appendix F. VME Slot Configurations F-1

Index..... Index-1

Reader Comment Card

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

List of Figures

Figure 1-1 USPII*e*-USB and Paddle Board Installed in a VME Backplane 1-5
Figure 1-2 SCSI Termination Configurations 1-6
Figure 1-3 USPII*e*-USB Multiple-I/O Paddle Board 1-8
Figure 1-4 Location of the TOD/NVRAM Battery 1-14
Figure 1-5 TOD/NVRAM Battery Replacement 1-15
Figure 2-1 USPII*e*-USB Baseboard Block Diagram 2-2
Figure 2-2 USPII*e*-USB PMC Carrier Board Block Diagram 2-5
Figure 3-1 UltraSPARC-II*e* CPU Block Diagram 3-2
Figure 3-2 USPII*e*-USB Reset Architecture 3-3
Figure 3-3 Custom Memory Module Topology (Side View) 3-7
Figure 3-4 SDRAM Memory Subsystem 3-8
Figure 4-1 Universe II Architectural Diagram 4-4
Figure 4-2 Address Translation for VMEbus to PCI Bus Transfers 4-11
Figure 4-3 Address Translation for PCI Bus to VMEbus Transfers 4-13
Figure 4-4 Memory Mapping in the Special PCI Target Image 4-17
Figure A-1 Baseboard VME P1 Connector Orientation A-1
Figure A-2 Baseboard VME P2 Connector Orientation A-3
Figure A-3 Baseboard SCSI A and B Connector Orientation A-5
Figure A-4 Ethernet A Connector Orientation A-7
Figure A-5 Front-Panel Mini-DIN Connector A-8
Figure A-6 Front-Panel Serial Ports A and B A-9
Figure A-7 PMC Module Slot 0 Connector A-10
Figure A-8 PMC Carrier Board VME P1 Connector Orientation A-12
Figure A-9 PMC Board VME P2 Connector A-14
Figure A-10 PMC Carrier Board User I/O Connector A-16
Figure A-11 Front-Panel Serial Ports E and F A-21
Figure A-12 Ethernet B Connector A-22

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Figure A-13 Dual Stereo Audio Connector A-22
Figure A-14 Standard Paddle Board SCSI Connector A-23
Figure A-15 Paddle Board Serial Port B Connector A-24
Figure A-16 USPII*e*-USB Multiple-I/O Paddle Board A-26
Figure A-17 Line Out/In Stereo Audio Connectors A-28
Figure A-18 Memory Module Baseboard Connectors (Receptacle & Plug) A-29
Figure B-1 Location and Configuration of SW1101 (Top Side) B-2
Figure B-2 Baseboard Jumper Locations (Top Side) B-6
Figure B-3 Baseboard Solder-Bead Locations (Bottom Side) B-10
Figure B-4 PMC Carrier Board Solder-Bead Locations (Bottom Side) B-16
Figure C-1 Placement of Mating Pins on Elma Handles C-2
Figure C-2 Single-Slot Front Panel (Baseboard) C-4
Figure C-3 2-Slot Front Panels (Baseboard and Graphics Board) C-5
Figure C-4 3-Slot Front Panels (Baseboard and 2 Graphics Boards) C-6
Figure C-5 3-Slot Front Panels (Baseboard, Graphics Board, and 2 PMC Carrier Boards) C-7
Figure C-6 3-Slot Front Panels (Baseboard, Graphics Board, and 3 PMC Carrier Boards) C-8
Figure C-7 Double-Slot Front Panels (Baseboard and 2 PMC Carrier Boards) C-9
Figure C-8 Double-Slot Front Panels (Baseboard and 3 PMC Carrier Boards) C-10
Figure D-1 Baseboard Front-Panel, Component, and Connector Diagram D-2
Figure D-2 USPII*e*-USB/2P2 PMC Carrier Board Component and Connector Diagram. D-3
Figure D-3 USPII*e*-USB/2P3 PMC Carrier Board Component and Connector Diagram. D-4
Figure D-4 Standard Paddle Board (P2 Connector and I/O Connector Sides) D-5
Figure D-5 Multiple I/O Paddle Board (Component and Connector Side) D-6
Figure F-1 USPII*e*-USB VME Slot Configurations F-3

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

List of Tables

Table 1-1 USPII*e*-USB Model Configurations 1-1
Table 1-2 Front-Panel DIN Settings 1-3
Table 2-1 CPU Speed Settings 2-1
Table 2-2 Memory Configurations 2-3
Table 2-3 Processor Specifications 2-8
Table 2-4 Memory Specifications 2-9
Table 2-5 USPII*e*-USB I/O Subsystem Specifications 2-10
Table 2-6 Auxiliary Functions Specifications 2-12
Table 2-7 USPII*e*-USB Operating Environmental Specifications 2-13
Table 2-8 USPII*e*-USB Non-operating Environmental Specifications 2-13
Table 2-9 Estimated Power Requirements 2-13
Table 4-1 Universe II Miscellaneous Control Register (MISC_CTL) 4-5
Table 4-2 Universe II Power-Up Options 4-7
Table 4-3 PCI Configuration Base Address 0 Register (PCI_BS0) 4-9
Table 4-4 PCI Configuration Base Address 1 Register (PCI_BS1) 4-9
Table 4-5 VMEbus Fields for VMEbus Slave Image 4-10
Table 4-6 PCI Bus Fields for VMEbus Slave Image 4-11
Table 4-7 Control Fields for VMEbus Slave Image 4-12
Table 4-8 PCI Bus Fields for PCI Bus Target Image 4-13
Table 4-9 PCI Bus Fields for PCI Bus Target Images 4-14
Table 4-10 Control Fields for PCI Bus Target Image 4-14
Table 4-11 PCI Bus Fields for Special PCI Bus Target Image 4-15
Table 4-12 Control Fields for Special PCI Bus Target Image 4-15
Table 4-13 Special PCI Target Image Register (Offset 188) 4-16
Table 5-1 PLD Register Address Map 5-2
Table 6-1 UltraSPARC-II*e* Reset_Control_Register 6-6

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Table A-1 Baseboard VME P1 Pinouts A-2
Table A-2 Baseboard VME P2 Connector Pinouts A-4
Table A-3 SCSI Ports A and B Connector Pin Signals A-6
Table A-4 RJ45 Ethernet A Pinout A-7
Table A-5 8-Pin Mini-DIN/PS/2–USB Pinouts A-8
Table A-6 Serial Port A and B Connector Pinouts A-9
Table A-7 Color Interpretation of Front-Panel LEDs A-10
Table A-8 PMC Carrier Board VME P1 Pinouts A-13
Table A-9 PMC Carrier Board VME P2 Pinout A-15
Table A-10 PMC Carrier Slot 1 with 64 Bits of User I/O A-17
Table A-11 PMC Carrier Slot 1 with 32 Bits of User I/O A-18
Table A-12 PMC Carrier Slot 2 with 32 Bits of User I/O A-19
Table A-13 PMC Carrier Slot 3 with 0 Bits of User I/O A-20
Table A-14 Serial Port E and F Connector Pinout A-21
Table A-15 RJ45 Ethernet B Pinout A-22
Table A-16 Paddle Board SCSI Port A Connector Pinouts A-24
Table A-17 Paddle Board Serial Port B Connector Pinouts A-25
Table A-18 Audio Signal Assignments A-28
Table B-1 Baseboard Jumper-Pin Settings (Top Side) B-3
Table B-2 Combined JP1401/JP1402 Configurations B-4
Table B-3 SCSI A Access Definition B-5
Table B-4 Boot-Device Settings B-5
Table B-5 Baseboard Solder-Bead Settings (Bottom Side) B-7
Table B-6 Front-Panel DIN Settings B-9
Table B-7 CPU Speed Settings B-9
Table B-8 PMC Carrier Board Solder-Bead Settings (Both Sides) B-12
Table B-9 Audio Input/Output Settings (2P2 Only) B-13
Table B-10 VME P2 Connector Configuration (2P2 and 2P3) B-14

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Table B-11 PMC Carrier Board Selection Settings (2P2 and 2P3) B-14
Table B-12 PCB Revision Settings..... B-14
Table B-13 VME P2 Pin Signal Interpretation B-15
Table B-14 PMC Carrier Board VME P2 Connector SB2801–SB2832 Configuration .. B-17
Table C-1 USPII*e*-USB Model Configurations C-1
Table C-2 PS/2 and USB Protocols and Connectors C-3
Table D-1 Standard Paddle Board Connector J0206 Pinout..... D-5
Table F-1 USPII*e*-USB Model Configurations F-1

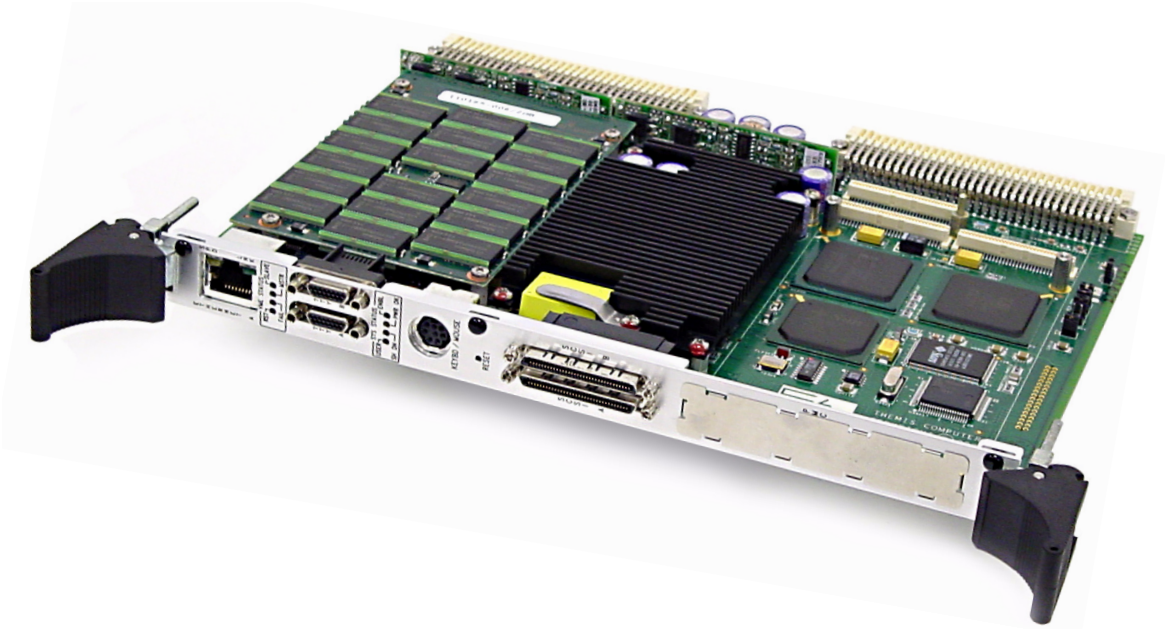
Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

How to Use This Manual

Introduction

Thank you for purchasing the Themis USPII*e*-USB single-board computer (see photo below; Baseboard only). This *USPIIe*-USB *Hardware Manual* describes all models of the USPII*e*-USB, a SPARC version 9.0 compliant computer with a VME-bus interface and an UltraSPARC-II*e* processor.



Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Themis Computer values its customer comments and opinions; therefore, a “Reader Comment Card” is located at the end of this manual for your use. Please take the time to fill out this card with any comments concerning Themis products and services, and return it to Themis Computer. Your comments may also be forwarded to Themis by sending email to docfeedback@themis.com.

Before you begin, carefully read each of the procedures in this manual and the associated Software manual. Serious damage can be caused by improper handling of the equipment.

USPII*e*-USB Models

The USPII*e*-USB has a total of seven models (see *Table 1*).

Table 1. USPII*e*-USB Model Configurations

Model	Baseboard	TGA3D/3D+ Graphics Board		PMC Carrier Board	
	VME Slot 1	VME Slot 2	VME Slot 3	2-PMC Slots VME Slot 2 or 3	3-PMC Slots VME Slot 2 or 3
USPII*e*-USB / 1	Yes				
USPII*e*-USB / 2G	Yes	Yes			
USPII*e*-USB / 3G2	Yes	Yes	Yes		
USPII*e*-USB / 3GP2	Yes	Yes		Yes (*VME Slot 3*)	
USPII*e*-USB / 3GP3	Yes	Yes			Yes (*VME Slot 3*)
USPII*e*-USB / 2P2	Yes			Yes (*VME Slot 2*)	
USPII*e*-USB / 2P3	Yes				Yes (*VME Slot 2*)

All models are based on a combination of four different VME boards: the USPII*e*-USB Baseboard, the TGA Graphics Board, and two PMC Carrier Boards (one with 2 PMC slots and one with 3 PMC slots).

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

In addition, two paddle boards are available for the USPII*e*-USB that provide I/O connections through the P2 backplane: the Standard Paddle Board—2-slot wide, single-slot connector, VME P2 Paddle Board and the Multiple I/O Paddle Board—a 1-slot wide, 3- or 5-row connector, VME P2 paddle board.

Intended Audience

This manual is written for system integrators and programmers. It contains all necessary information for installation and configuration of the USPII*e*-USB and assumes the OpenBoot PROM (OBP) program code is installed in the system Flash memory. If you intend to operate the USPII*e*-USB with an operating system other than Solaris, such as VxWorks or some other real-time kernel, please consult the appropriate documentation supplements accompanying your OS or kernel software.

Although all specific hardware and software features are described in the Hardware and Software manuals, programmers wishing to write code for the USPII*e*-USB without the benefit of an operating system or real-time kernel will require additional data sheets. Please refer to the section “Related References” on page xxi for information concerning this documentation.

The reader should have a working knowledge of VMEbus and PCI local bus specifications, SPARC processor architecture, Ethernet, and SCSI (ANSI 3.131-1994) specifications.

Unpacking



Caution: The USPII*e*-USB contains statically sensitive components. Industry-standard antistatic measures must be observed when removing the USPII*e*-USB from its shipping container and during any subsequent handling. A wrist strap provides grounding for static electricity between your body and the chassis of the system unit. Electric current and voltage do not pass through the wrist strap.

Remove the USPII*e*-USB and accessories from the shipping container and check the contents against the packing list. Be certain to observe industry-standard ESD protection procedures when handling static-sensitive components. The package should include all elements of your order.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Please report any shipping discrepancies to the Themis Computer Customer Support group immediately: support@themis.com or 1-510-252-0870.

Remove all USPII*e*-USB boards from their antistatic wrapping and verify that they have the ordered configuration (refer to Chapter 2, "USPIIe-USB Specifications").

How to Start Quickly

To start operating the USPII*e*-USB quickly, Themis Computer recommends that you read the following sections:

- Chapter 1, "USPIIe-USB Installation". This chapter contains vital information on configuring the USPII*e*-USB, and designing and setting up VMEbus-based systems.
- Appendix B, "DIP-Switch, Jumper-Pin, and Solder-Bead Configurations". This appendix contains a complete listing of all DIP switches, jumper pins, and solder beads, along with all default settings. Verify that the switches, jumpers, and beads on your system are set to meet your application requirements.

In addition to information contained in the *USPIIe*-USB *Hardware Manual* (Themis P/N-110534-022), the *USPIIe*-USB *Software Manual* (Themis P/N-110290-023) contains information on software registers, address maps, additional OpenBoot commands, as well as a description of the Themis Computer VME software package for Solaris.

Chapter Overview

The chapters and appendices of this manual are briefly outlined as follows:

- Chapter 1, "USPIIe-USB Installation" provides instructions on the installation and configuration of the USPII*e*-USB for your particular environment and application. The information contained in this chapter is **mandatory** for the correct operation of the USPII*e*-USB. This chapter should be read in its entirety**.**
- Chapter 2, "USPIIe-USB Specifications" provides a brief overview of the USPII*e*-USB, along with its System, Environmental, and Power specifications.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

- Chapter 3, "Hardware Overview" describes the major components on the USPII*e*-USB, the memory subsystem, and the Open Boot Program code (OBP).
- Chapter 4, "Universe II Description" provides detailed information concerning the PCI-to-VMEbus interface for the USPII*e*-USB, the Tundra Universe II. For a more detailed description of the Universe II, refer to the *Universe II User's Manual*, available on the Tundra website at http://www.tundra.com.
- Chapter 5, "Programmable Logic Device" provides a description of the Programmable Logic Device (PLD) on the USPII*e*-USB. Included in this chapter are descriptions of the temperature warning system, boot address decoder, and the power management system.
- Chapter 6, "Resets" describes the Reset Tree of the USPII*e*-USB.
- Appendix A, "Connector Pinouts, LEDs, Switches" provides connector part numbers and pinouts for the User I/O on the USPII*e*-USB.
- Appendix B, "DIP-Switch, Jumper-Pin, and Solder-Bead Configurations" provides a detailed description of each of the user-configurable jumper-pins and DIP switches on the USPII*e*-USB, as well as diagrams illustrating the location of all jumper-pins, DIP switches, and solder beads.
- Appendix C, "Front Panel Diagrams" illustrates front panels for single- and double-slot configurations of the USPII*e*-USB.
- Appendix D, "Board Diagrams" provides board diagrams of the USPII*e*-USB.
- Appendix E, "Glossary" provides the general definition of terms and abbreviations used in this manual.
- Appendix F, "VME Slot Configurations" provides slot configurations for all models of the USPII*e*-USB, including those with the TGA3D/3D+ Graphics Board and two versions of the PMC Carrier Board.

Related References

The following is a list of related references

- USPII*e*-USB Software Manual (P/N-110290-023)
- PCI Local Bus Specification, Revision 2.1, PCI Special Interest Group, Portland
- *American National Standard for VME64*, ANSI/VITA, 1994; also *VME64x*

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

- *PCI System Architecture*, by Shanley and Anderson, MindShare Press
- *IEEE Standard 1275-1994, Standard For Boot (Initialization, Configuration) Firmware*, Core Practices and Requirements
- *IEEE Standard 1275.1-1994, Standard For Boot (Initialization, Configuration) Firmware*, ISA Supplement for IEEE P1754 (SPARC)
- *IEEE Standard P1275.6/D4, Standard For Boot (Initialization, Configuration) Firmware*, 64 Bit Extensions
- *OpenBoot 3.x Command Reference*, Sun Microsystems (806-1377-10)
- *PCI Bus Binding to IEEE 1275-1994, Standard for Boot (Initialization, Configuration) Firmware*, Revision 1.0, 14 April 1994, Prepared by the Open Firmware Task Force of the PCI Alliance
- *OpenBoot 3.x Command Supplement for PCI*, Sun Microsystems (805-1627-10)
- *The SPARC Architecture Manual, Version 9*, David L. Weaver and Tom Germond, editors, PTR Prentice Hall
- *SunVTS™ 2.1 SunVTS User's Guide*, Part No. 802-7299 August 1997, Rev. A
- *SunVTS™ Quick Reference Card*, Part No. 816-0861-10
- *SunVTS™ 2.1.3 Test Reference Manual* Part No. 805-4163-10, May 1998, Rev. A

Integrated Circuit Specifications:

- *UltraSPARC-IIe User's Manual* (SUN P/N-806-tbd-00; Draft, April 2001)
- *UltraSPARC-IIe Data Sheet* (SUN, Preliminary, April 2001)
- *SME2411BGA-66: Advanced PCI Bridge (APB) Data Sheet* (SUN P/N-805-0088-02)
- *SME2411BGA-66: Advanced PCI Bridge (APB) User's Manual* (SUN P/N-805-1251-01)
- *SME STP2003QFP: PCI Input to Output Controller Data Sheet* (SUN P/N-802-7836-02)
- *SME STP2003QFP: PCI Input to Output Controller User's Manual* (SUN P/N-802-7837-01)

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

- *National Semiconductor DP83843 Phyter Data Sheet*, Version E, August, 1997, National Semiconductor Corporation
- *Symbios SYM53C896: PCI to Dual-Channel Ultra2 SCSI Multifunction Controller Technical Manual*, Version 3.0, January 2000
- *Universe II User Manual*, Tundra, Spring, 1998

Sun documents are available for download on websites http://www.sun.com or http://docs.sun.com. Non-Sun documents are available from their respective vendors.

Notes, Cautions, Warnings, and Sidebars

The following icons with accompanying formatted text are included in this document for the reasons described:



Note: A note provides additional information that may be helpful in carrying out the procedure or action being described.



Caution: A caution describes a procedure or action that may result in injury to the operator or equipment. This may involve—but is not restricted to—heavy equipment or sharp objects. To reduce the risk, follow the instructions accompanying this symbol.



Warning: A warning describes a procedure or action that may cause injury to the operator or equipment as a result of hazardous voltages. To reduce the risk of electrical shock and danger, follow the instructions accompanying this symbol.



Sidebar: A “sidebar” adds detail to the section within which it is placed, but is not absolutely vital to the description or procedure.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Website Information

Themis Computer corporate and product information may be accessed on the World Wide Web by browsing the website http://www.themis.com.

The Sales and Marketing Department may be reached at info@themis.com.

Product Warranty and Registration

Please review the Themis Computer warranty and complete the product registration card delivered with your USPII*e*-USB board(s). You are not required to return the registration card to activate your product warranty, however, by registering your USPII*e*-USB, Themis Computer will be better able to provide you with timely information updates and product-enhancement notifications.

Our Customer Support department is committed to providing the best product support in the computer industry. Customer support is available 8am–5pm (PST), Monday through Friday, via telephone, fax, e-mail, and our website.

Themis Customer Support:

Telephone: +1 510-252-0870
Fax: +1 510-490-5529
E-mail: support@themis.com
Website: http://www.themis.com

In Case of Difficulties

If the USPII*e*-USB does not behave as described or if you encounter difficulties installing or configuring the board, please call Themis Computer technical support at +1 (510) 252-0870, fax your questions to +1 (510) 490-5529, or send an e-mail to *support@themis.com*. You can also contact us via our web site: http://www.themis.com.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Your Comments are Welcome

We are interested in improving our documentation and welcome your comments and suggestions. You can email your comments to us at **docfeedback@themis.com** or fill out and return the Reader Comment card at the end of this manual. Please include the document part number (110534-022) in the subject line of your email.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Installation Section

Chapter 1

USPIIe-USB Installation

1.1 Determine Board Type

The Themis USPII*e*-USB single-board computer is available in seven models, as defined in *Table 1-1*.

Table 1-1. USPII*e*-USB Model Configurations

Model	Baseboard	TGA3D/3D+ Graphics Board		PMC Carrier Board	
	VME Slot 1	VME Slot 2	VME Slot 3	2-PMC Slots VME Slot 2 or 3	3-PMC Slots VME Slot 2 or 3
USPII*e*-USB / 1	Yes				
USPII*e*-USB / 2G	Yes	Yes			
USPII*e*-USB / 3G2	Yes	Yes	Yes		
USPII*e*-USB / 3GP2	Yes	Yes		Yes (*VME Slot 3*)	
USPII*e*-USB / 3GP3	Yes	Yes			Yes (*VME Slot 3*)
USPII*e*-USB / 2P2	Yes			Yes (*VME Slot 2*)	
USPII*e*-USB / 2P3	Yes				Yes (*VME Slot 2*)

To determine your Baseboard type, check the white sticker located near your Baseboard's VME P2 connector. It contains information on board type, serial number, and release number.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

For example:

[**USPII*e***-USB/**1-512-512-600 A1**] [**S1300786**]

— Board Type: USPII*e*-USB/1—Revision: A1

— L2 Cache: 512 KBytes—Serial Number: S1300786

— SDRAM: 512 MBytes—CPU Frequency: 600 MHz

To install the USPII*e*-USB, a standard VME chassis with a P1/P2 backplane (3-row or 5- row connector) is required. If the USPII*e*-USB is to be used in a workstation configuration instead of an embedded controller, a hard disk and graphics frame buffer or serial terminal will also be required.

1.2 Check Configurations

When you first receive the USPII*e*-USB, confirm that the jumper-pin and solder-bead configurations are appropriate for your application. Appendix B, ”DIP-Switch, Jumper-Pin, and Solder-Bead Configurations” gives a complete listing of jumper-pin and solder-bead definitions, including default settings.

If you have to change a jumper-pin setting, check with Themis Customer Support first to make sure the new setting is supported.

Solder-bead settings are set by Themis at the factory before shipping and should be changed by Themis at the factory only.



Warning: Attempting to alter a solder-bead configuration could seriously damage the USPII*e*-USB. DO NOT ATTEMPT TO ALTER SOLDER-BEAD CONFIGURATIONS. Instead, contact Themis to change any settings.

The following section describes the proper configuration for the mini-DIN-8 connector on the Baseboard front panel.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

1.2.1 Combination PS/2–USB Connector

The mini-DIN-8 connector (marked **KEYBD/MOUSE**) on the Baseboard front panel supports either a PS/2 keyboard/mouse port or dual-USB (USB-0, USB-1) port. Either option is selected by configuring five solder beads (SB3502 through SB3506; see *Table 1-2*), and both require special pigtail cables from Themis.

Table 1-2. Front-Panel DIN Settings

SB3502	SB3503 through SB3506	Front-Panel 8-Pin Mini-DIN Configuration	Comments
Open	**Short 1-2**	**PS/2 keyboard/mouse**	Accessible only through special split pigtail cable (*Themis 110104-002*) • 8-pin mini-DIN to 6-pin keyboard DIN and 6-pin mouse DIN
Open	Short 2-3	*Not Applicable*	
Short	Short 1-2	*Not Applicable*	
Short	**Short 2-3**	**USB (USB-0, USB-1)**	Accessible only through special split pigtail cable (*Themis 110473-001*) • 8-pin mini-DIN to dual 4-pin USB

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

1.2.2 SCSI Termination

All SCSI busses must be properly terminated. The USPII*e*-USB contains two SCSI ports (A and B) on the Front Panel of the Baseboard (see Appendix C, “Front Panel Diagrams”). The SCSI A bus is accessed through the Front Panel and the VME P2 connector (through a Paddle Board) behind the VME backplane (see *Figure 1-1* on page 1-5).

The SCSI B bus is accessed through the Front Panel only. As a result, the USPII*e*-USB SCSI Controller is always at one end of the SCSI B bus, hence the on-board SCSI B terminator is always enabled. The SCSI A bus, on the other hand, can have several configurations, which determine whether or not the bus is terminated at the USPII*e*-USB. Possible SCSI A bus configurations are shown in *Figure 1-2* on page 1-6, along with the SCSI B bus flow path.



Caution: SCSI busses must be properly terminated in order for SCSI devices to operate correctly.

Only one device (including the SCSI Controller) at each end of a SCSI bus chain should be terminated. If both the Front Panel and the Paddle Board have SCSI-A devices attached, then the on-board SCSI-A terminator should be **disabled** (Off); otherwise, the on-board SCSI-A termination should be **enabled** (On).

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

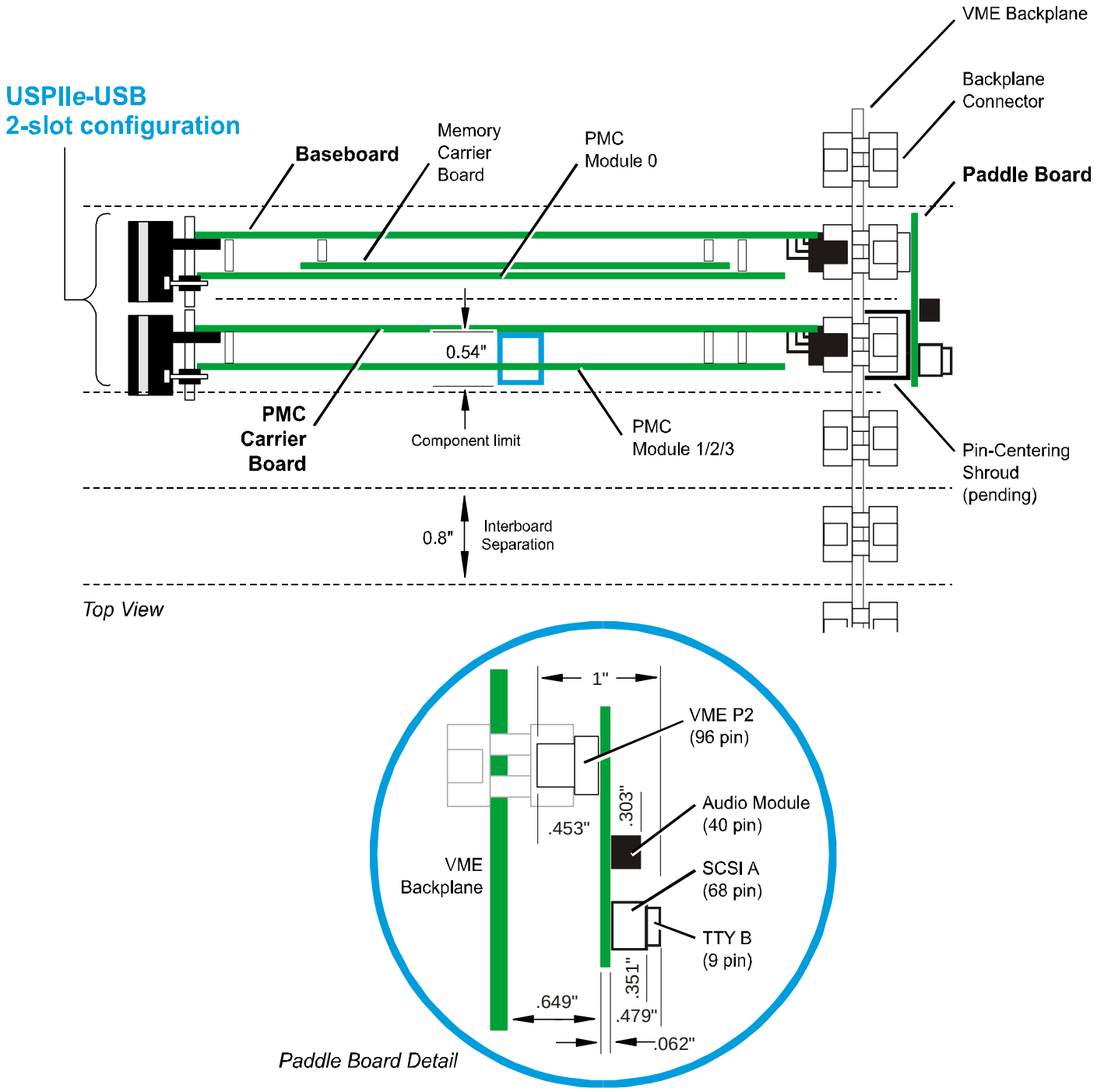


Figure 1-1. USPIIe-USB and Paddle Board Installed in a VME Backplane

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

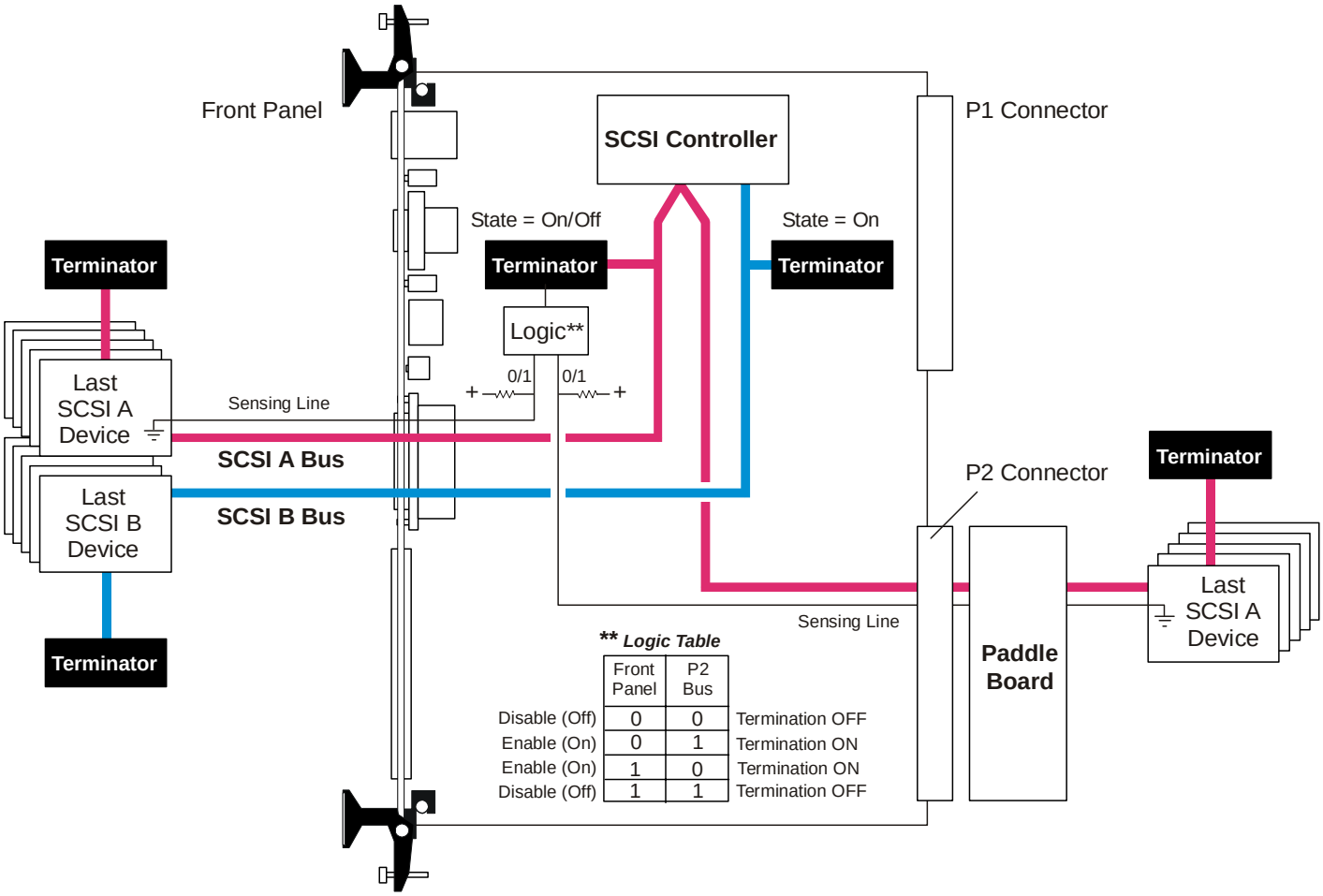


Figure 1-2. SCSI Termination Configurations

Note: The SCSI-A channel actually has two terminating circuits. One is associated with the front-panel SCSI-A connection, which automatically turns itself off whenever a SCSI device is attached to the front panel. The other is associated with the VME P2 SCSI-A connection, which also automatically turns itself off whenever a SCSI device is attached to the P2 connector.

This design allows for proper SCSI-A bus termination for any combination of devices that may be attached (e.g., no devices at either end of the SCSI-A bus, a device on one end but not the other, or a device on each end).

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

1.3 Installing USPIIe-USB Paddle Boards

There are two major types of paddle boards available for the USPII*e*-USB: the *Standard* Paddle Board and the *Multiple-I/O* Paddle Board.

1.3.1 Standard Paddle Board

The Standard Paddle Board (P/N 110094-30) attaches to the rear of the slot occupied by the USPII*e*-USB Baseboard on the VME P2 backplane (see *Figure 1-1* on page 1-5). The Standard Paddle Board provides connectors for:

- SCSI Port A (SE mode)
- Serial Port B (RS232)
- Power fail, software alarm, and high-temperature trip signals
- Polyswitch Vcc power fuse

[See section “Paddle Boards” on page D-1 for a more complete description.]

1.3.2 Multiple-I/O Paddle Board

As shown in *Figure 1-3*, the Multiple-I/O Paddle Board (P/N 110778-001) provides I/O connectors for:

- Ultra160 SCSI Port A (wide-LVD mode)
- Parallel Port (DB25)
- 4 Serial Ports: Port A (TTY-A), Port B (RS232), Port C (TTY-C), and Port D (TTY-D)
- Dual (2) USB Ports
- PS/2 Keyboard/Mouse Port (mini-DIN-8)
- Audio Line Out (stereo jack)
- Audio Line In (stereo jack)

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

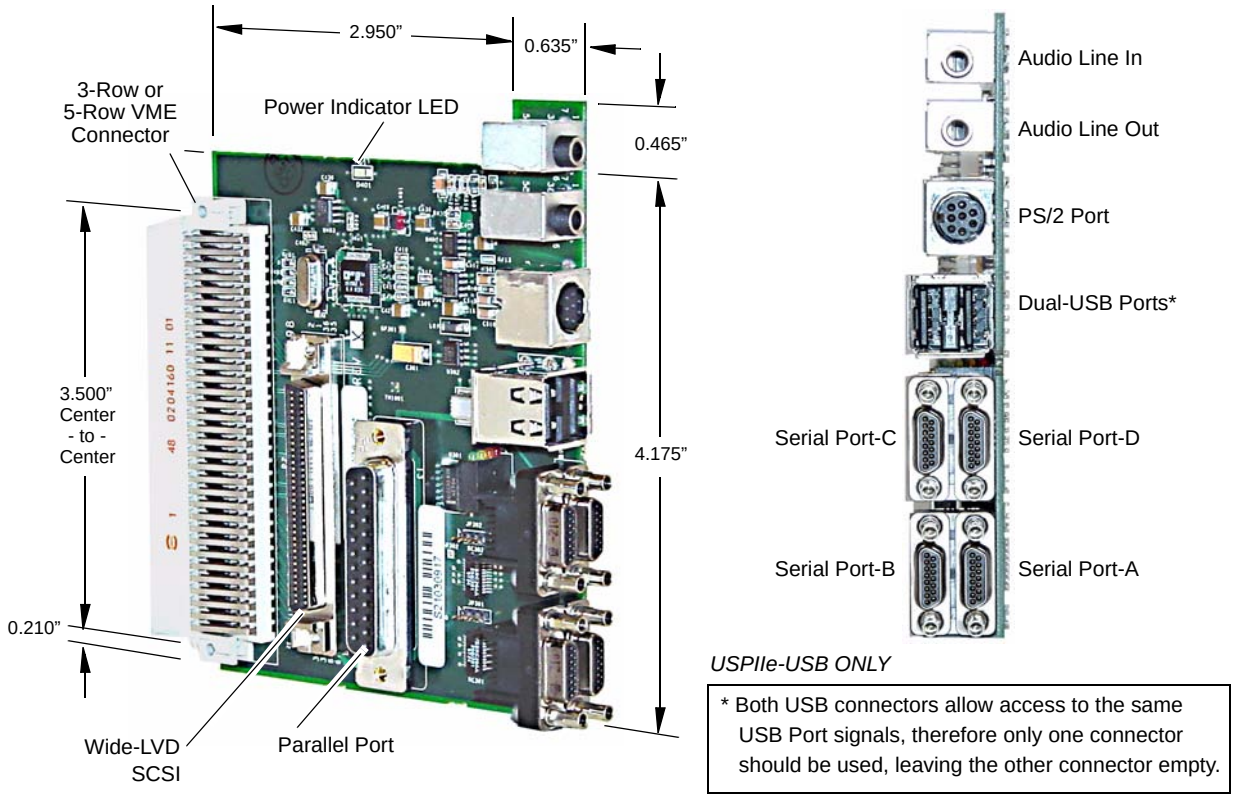


Figure 1-3. USPIIe-USB Multiple-I/O Paddle Board

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

1.4 Attaching Cables and Accessing USPII*e*-USB Peripheral Devices

Attach adapter cables to the appropriate Front Panel and VME P2 Paddle Board connectors. The following sections provide information on what adapter cables are required and how to attach them. Also refer to Appendix A, “Connector Pinouts, LEDs, Switches” and Appendix C, “Front Panel Diagrams”.

1.4.1 Serial Ports A/B (TTYA and TTYB)

Depending on the setting of solder bead SB3501 (see Appendix B, ”DIP-Switch, Jumper-Pin, and Solder-Bead Configurations”), TTYA (RS232 only) and TTYB (RS232 or RS422) are available from the Front Panel or from the Baseboard VME P2 connector, and are supported by the serial controller.

1.4.1.1 Front Panel Connection

RS232 mode: TTYA is only available in RS232 mode. Use cable P/N-108373 of the integration kit (15-pin male-to-male Micro-DB15 to SubD25).

RS422 mode: TTYB can be configured in either RS232 or RS422 mode (see JP3401) from the Front Panel, and RS232 only from the VME P2 bus.

1.4.1.2 VME P2 Connection

TTYA (RS232 only) and TTYB (RS232 only) are also available through the VME P2 bus, depending on the setting of solder bead SB3501. The Standard USPII*e*-USB VME P2 Paddle Board is designed to access TTYB signals only. If you want to connect to TTYA signals, you will need a Multiple I/O Paddle Board; or you may provide your own connectivity, or call Themis Computer for a cost estimate on building a *custom* Paddle Board.

1.4.2 Serial Ports C/D (TTYC and TTYD)

TTYC and TTYD are supported by the Siemens SAB82532 DUART chip. TTYC/D are used as general-purpose serial ports. These ports are only available out of the Baseboard VME P2 connector (refer to *Table A-2*, page A-4). The Standard Paddle Board cannot be used to access TTYC/D out of the back. You will need a Multiple I/O Paddle Board; or you may provide your own connectivity, or call Themis Computer for a cost estimate on building a *custom* paddle board.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

1.4.3 Serial Ports E/F (TTYE/F)

TTYE and TTYF are supported by the Siemens SAB82532 DUART serial controller, located on the PMC Carrier Board. They are available from the PMC Carrier Board Front Panel or from the PMC Carrier Board VME P2 bus.

1.4.3.1 Front Panel Connection

Use cable P/N-108113 of the integration kit (male Micro DB9 to male SubDB25). Please contact Themis Computer Technical Support for more details.

1.4.3.2 VME P2 Connection

The available paddle boards cannot be used for VME P2 connection (see *Table B-14*, page B-17). You will need to provide your own connectivity, or call Themis Computer for a cost estimate on building a *custom* Paddle Board.

1.4.4 Parallel (Printer) Port

A printer can be attached to the Baseboard VME P2 (refer to *Table A-2*, page A-4). Please note that the Standard Paddle Board cannot be used to access the parallel port. You will need a Multiple I/O Paddle Board; or you may also provide your own connectivity or call Themis Computer for a cost estimate on building a *custom* Paddle Board.

1.4.5 PMC (Expansion) Module Slots

The Baseboard contains a single PMC Module slot (see Appendix C, “Front Panel Diagrams”). The PMC Carrier Board contains two (USPII*e*-USB/2P2) or three (USPII*e*-USB/2P3) PMC Module slots. User I/O pins are available on the PMC Carrier Board VME P2 connector. For information on how to access the user I/O pins, please refer to Appendix A, “Connector Pinouts, LEDs, Switches”.

1.4.6 Ethernet Network

The USPII*e*-USB features an RJ45 port on the Front Panel for 10/100Base-T Ethernet interface connections.

In the case of the **USPII*e*-USB/1**, where only the Baseboard is present, a single network connection (Ethernet A) is available through the RJ45 connector. In the case of the **USPII*e*-USB/2P2**, a second network (Ethernet B) can be available through the Audio/Ethernet/Serial-I/O section of the P2 Carrier Board Front Panel. Both Ethernet A and B may be active simultaneously.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

After attaching the USPII*e*-USB to a network, you can verify proper physical connection by executing the OBP network selftest (`test net`). This test will indicate external loopback failure on each of the network interfaces when there is not a proper physical connection.

1.4.7 SCSI A and B

Themis provides adapter cables for SCSI A or B with conversion to standard 68-pin, 0.050 inch, male SCSI connectors. Attach cable P/N-108712 to the desired SCSI connection (SCSI A or SCSI B) on the Front Panel mini-din 68 labelled either **SCSI A** or **SCSI B**. Additionally, you can attach cable P/N-108432 to the SCSI connector of the standard Paddle Board (SCSI A only). It is possible to use both Front Panel and Paddle Board SCSI A connections simultaneously (see *Figure 1-2* on page 1-6).

You can verify proper physical connection by executing the OpenBoot command `probe-scsi` (for SCSI A) or `probe-scsi-all` (for SCSI A and B). This command transmits an inquiry command to SCSI devices connected to the system unit onboard SCSI interface. If the SCSI device is connected and active, the target address, unit number, device type, and manufacturer name is displayed.

The example below identifies the `probe-scsi` output message:

```
ok probe-scsi
Primary UltraSCSI bus:
Target 0
Unit 0 Disk SEAGATE ST32272W 0876
Target 6
Unit 0 Removable Read Only device TOSHIBA CD-ROM X6201TA1037
Secondary UltraSCSI bus:
ok
```

1.4.8 USB-0 and USB-1

USB ports 0 and 1 are located together on the Front Panel of the USPII*e*-USB (see Appendix C, “Front Panel Diagrams”). Pin signal descriptions are given in *Table A-5* on page A-8 (Appendix A, ”Connector Pinouts, LEDs, Switches”).

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

1.4.9 USB-2

Signals for USB port 2 are accessible through the P2 connector of the USPII*e*-USB VME backplane (see *Table A-2*, page A-4, in Appendix A, ”Connector Pinouts, LEDs, Switches”). Please note that the standard Paddle Board cannot be used to access the USB-2 port. You will need a Multiple I/O Paddle Board; or you may also provide your own connectivity or call Themis Computer for a cost estimate on building a *custom* Paddle Board.

1.4.10 Miscellaneous I/O

The following I/O signals are also available:

1.4.10.1 From the Baseboard VME P2

- SW alarm Pin
- HI-TEMP TRIP signal
- POWER fail

1.4.10.2 From the PMC Carrier Board VME P2

Please refer to Section A.4.2, "PMC Carrier Board VME P2 Connector," on page A-14, for information on how to access these I/O signals.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

1.5 Configuring the VME Interface

Themis has implemented a variable and flexible VMEbus interface using both onboard jumpers, OpenBoot PROM (OBP) commands (see Section 1.5.1), and OBP environment variables specific to the USPII*e*-USB board.

The USPII*e*-USB is typically re-configured when VMEbus boards are added, removed, or changed in the chassis. Board configuration normally involves allocation of the VMEbus master access address, interrupts, and slave base addresses.

Only the VME SYSRST function is configured by a hardware jumper (JP1501). Consult Appendix B, ”DIP-Switch, Jumper-Pin, and Solder-Bead Configurations”, section “Baseboard Jumper Pins” on page B-3 for details. All other VMEbus interface-related options are configured using extensions to the Sun OBP monitor program.

Details on configuring the VME interface are described in the *USPIIe*-USB *Software Manual*, Themis P/N-110102-023.

1.5.1 Using OBP to Program the VME Interface

1.5.1.1 OBP Commands



Caution: Before the following commands can be recognized, you must first issue a `vme select-dev` OBP command.

You can access Universe II registers using the following 3 OBP commands:

- `ok show-universe-regs`
  This will display the UNIVERSE II registers
- `ok <offset> universe-reg@ .`
  This will display the register at offset <offset>
- `ok <data> <offset> universe-reg!`
  This will write the value <`data`> into register at offset <`offset`>

1.5.1.2 OBP Environment Variables

OBP has been modified to include environment variables to help program and control the VME interface. Use the `setenv` OBP command to program these variables (see Chapter 5 of the *USPIIe*-USB *Software Manual* for details).

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

1.6 TOD/NVRAM Battery Replacement

The Non-Volatile RAM (NVRAM) and a Time-of-Day (TOD) clock are both contained in the timekeeper chip (see Chapter 3, "Hardware Overview"). The chip has its own lithium battery to operate the TOD clock and maintain the contents of the NVRAM during a power shutdown. Located directly on top of the timekeeper chip, the battery provides power backup for approximately 10 years.

In the event the battery must be replaced, follow these steps:

1. Locate the lithium battery on the top (component) side of the USPII*e*-USB board (see *Figure 1-4*).

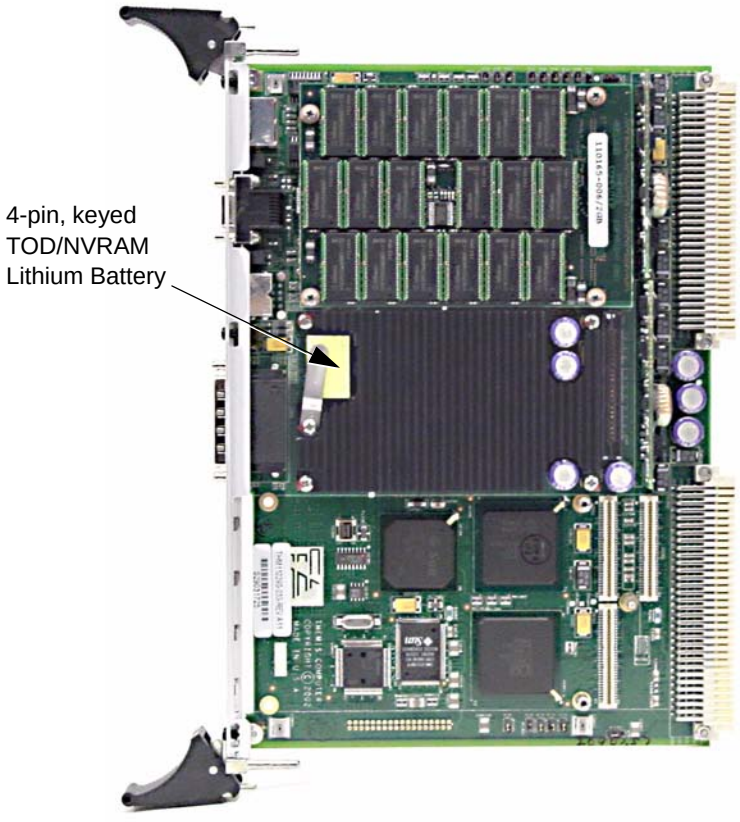


Figure 1-4. Location of the TOD/NVRAM Battery

2. Remove the phillips-head screw securing the battery holder to the board (see **A** and **B** in *Figure 1-5* on page 1-15).

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

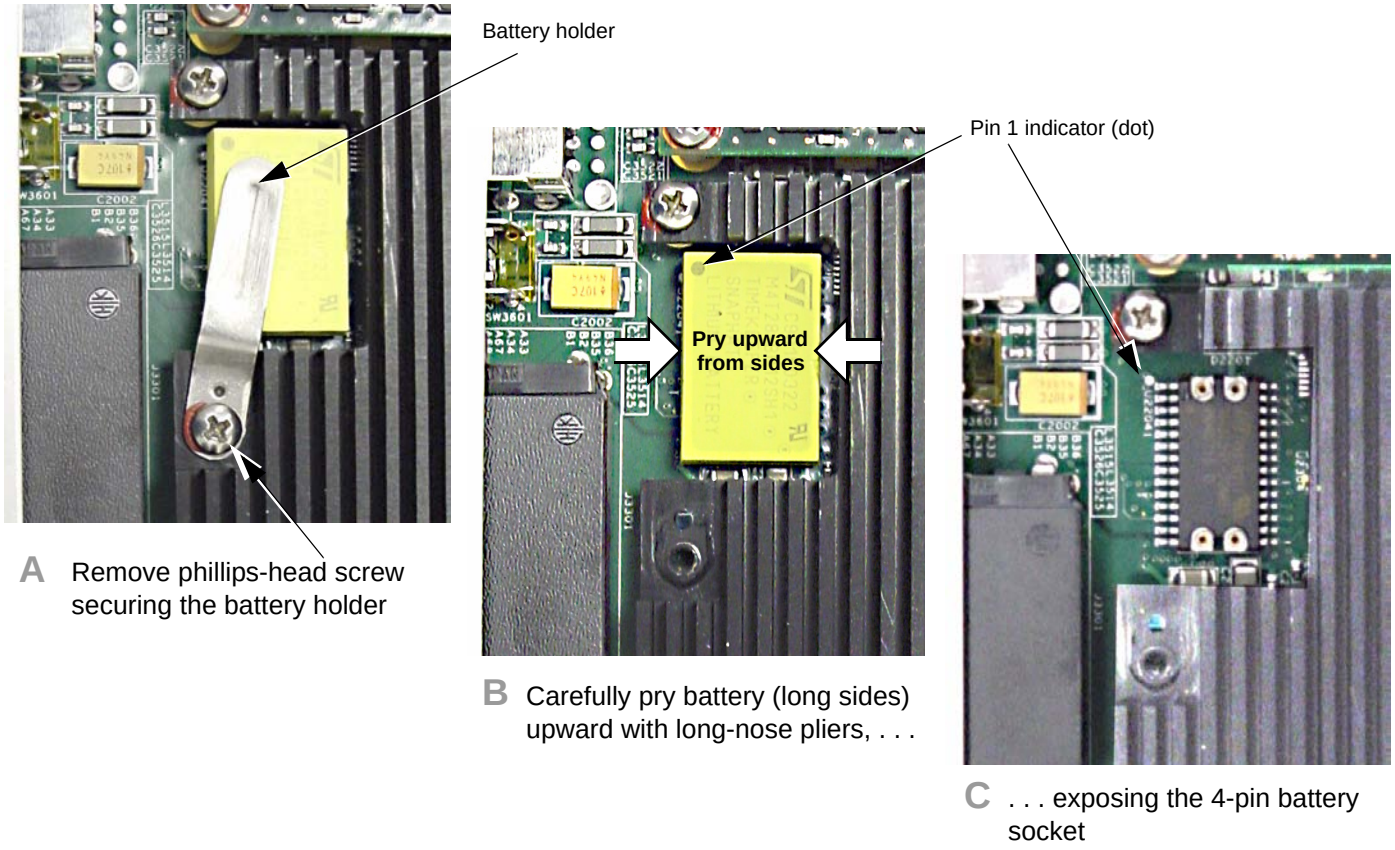


Figure 1-5. TOD/NVRAM Battery Replacement

3. With a long-nose pliers (or other suitable tool), carefully pry the long sides of the battery back and forth and upward until the four battery pins are free of the battery socket. Discard the old battery in a suitable manner.

Caution: When prying off the battery, be careful not to break traces on the PCB surface or apply pressure directly to the timekeeper chip that houses the socket.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

4. Position the new (replacement) battery over the timekeeper chip socket so that the pin-1 indicator on the battery is aligned with the pin-1 indicator on the PCB (see *Figure 1-5*). Carefully push the battery into the socket when the four battery pins have engaged the socket holes. The battery will be fully seated when you hear a “snap” as you push down.

5. Replace the battery holder and the phillips-head screw previously removed and secure it to the USPII*e*-USB board.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Specification Section

Chapter 2

USPIIe-USB Specifications

2.1 Baseboard

The USPII*e*-USB Baseboard was designed to provide an UltraSPARC-II*e* platform in an industry-standard single-slot, 6RU, VME form factor. The Baseboard is implemented as a single-slot VMEbus board with an on-board UltraSPARC-II*e* processor and proprietary coplanar memory boards.

The Baseboard is available at processor speeds of 650, 600, or 550 MHz (512-KB L2-cache)—see *Table 2-1* below and *Figure 2-1* on page 2-2.

Table 2-1. CPU Speed Settings

SB2703	SB2705	CPU Speed
Short 1-2	Short 1-2	650 MHz
Short 1-2	Short 2-3	600 MHz
Short 2-3	Short 1-2	550 MHz
Short 2-3	Short 2-3	*Not applicable*

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

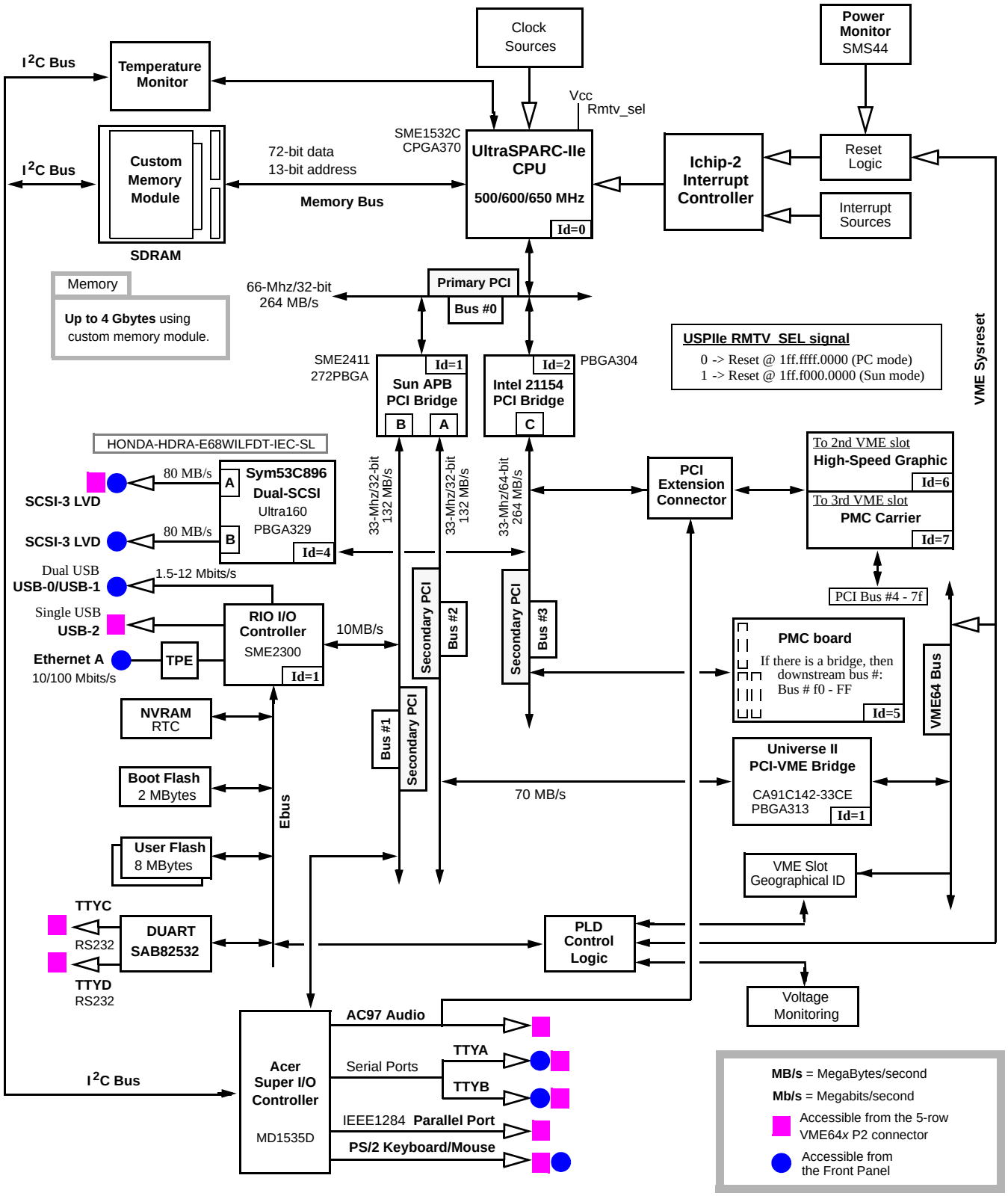


Figure 2-1. USPIIe-USB Baseboard Block Diagram

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

The Memory subsystem utilizes a custom high-capacity Themis Memory Module that supports several memory configurations up to 4 GigaBytes (see *Table 2-2*).

Table 2-2. Memory Configurations

Total Memory Capacity	Custom Themis Memory Module Supported
128 MB	YES
256 MB	YES
512 MB	YES
1 GB	YES
2 GB	YES
4 GB	YES

The local I/O subsystem is PCI-based, with separate PCI channels provided for I/O functions and external VMEbus P2 backplane access. Specifically, the **Baseboard Front Panel** includes the following (see Appendix C, “Front Panel Diagrams”):

- Ethernet port A..... *10100Base-T*
- Serial port A (TTYA)..... *RS232*
- Serial port B (TTYB)..... *RS232/RS422*
- Keyboard/Mouse (PS/2) or Dual-USB (USB-0, USB-1) port... *DIN-8 with Adapter*
- SCSI port A ..... *Ultra2 LVD*
- SCSI port B ..... *Ultra2 LVD*
- PMC Module slot 0

The back-panel VMEbus **P2 interface** provides signals for:

- Serial port A (TTYA)..... *RS232 (RXD and TXD)*
- Serial port B (TTYB)..... *RS232 (RXD, TXD, and modem signals)*
- Serial port C (TTYC)..... *RS232 (RXD and TXD)*
- Serial port D (TTYD) ..... *RS232 (RXD and TXD)*
- USB-2 port
- PS/2 Keyboard/Mouse
- Parallel port
- SCSI port A..... *Single-ended (3-row access; A/B/C) or LVD (5-row access)*
- Audio Input/Output
- Additional signals provide Power Fail, High-Temp Trip, and Software alarms.

[See *Table A-2*, page A-4, Chapter A, "Connector Pinouts, LEDs, Switches" for details on the VME P2 interface.]

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

2.2 PMC Carrier Board

The USPII*e*-USB/**2P2** PMC Carrier Board (see *Figure 2-2*, page 2-5) supports two (2) PMC Module slots (to support vendor-specific, 32/64-bit, 33-MHz, PMC expansion Modules) and on-board Audio/Ethernet/Serial-I/O features.

The USPII*e*-USB/**2P3** PMC Carrier Board supports three (3) PMC Module slots (to support vendor-specific, 32/64-bit, 33-MHz, PMC expansion Modules).

User I/O on the PMC Carrier Board can be accessed from both front-panel and paddle-board connectors. In some instances, accessing a signal from one of these access sources prevents the signal from being accessed from the second source.

Note: User I/O signals can be brought from PMC Modules in **slot 1** and **slot 2** to the VME P2 connector of the PMC Carrier Board.
A PMC Module in **slot 3** has ***no*** I/O-signal access through the VME P2 connector of the PMC Carrier Board.

User I/O on the PMC Carrier Board may be reconfigured. For example, 64 bits of user I/O may be made available on PMC Module slot 1, presuming the user I/O on PMC Module slot 2 is not used. On the other hand, 32 bits of user I/O may be made available on both PMC Module slot 1 and PMC Module slot 2.

For example, if TTYA is routed to the VME P2 backplane, then TTYA cannot be accessed from the Front Panel (in this case, the parallel port also cannot be accessed from the VME P2 backplane).

Caution: It is important to make sure that a jumper-pin or solder-bead configuration does not result in an **unwanted change** of system operational parameters. READ ALL CONFIGURATION DESCRIPTIONS CAREFULLY.

The PMC Carrier Board has the following I/O support on its Front Panel:

USPIIe-USB/2P2

- Serial (TTY) port E *RS232*
- Serial (TTY) port F *RS232*

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

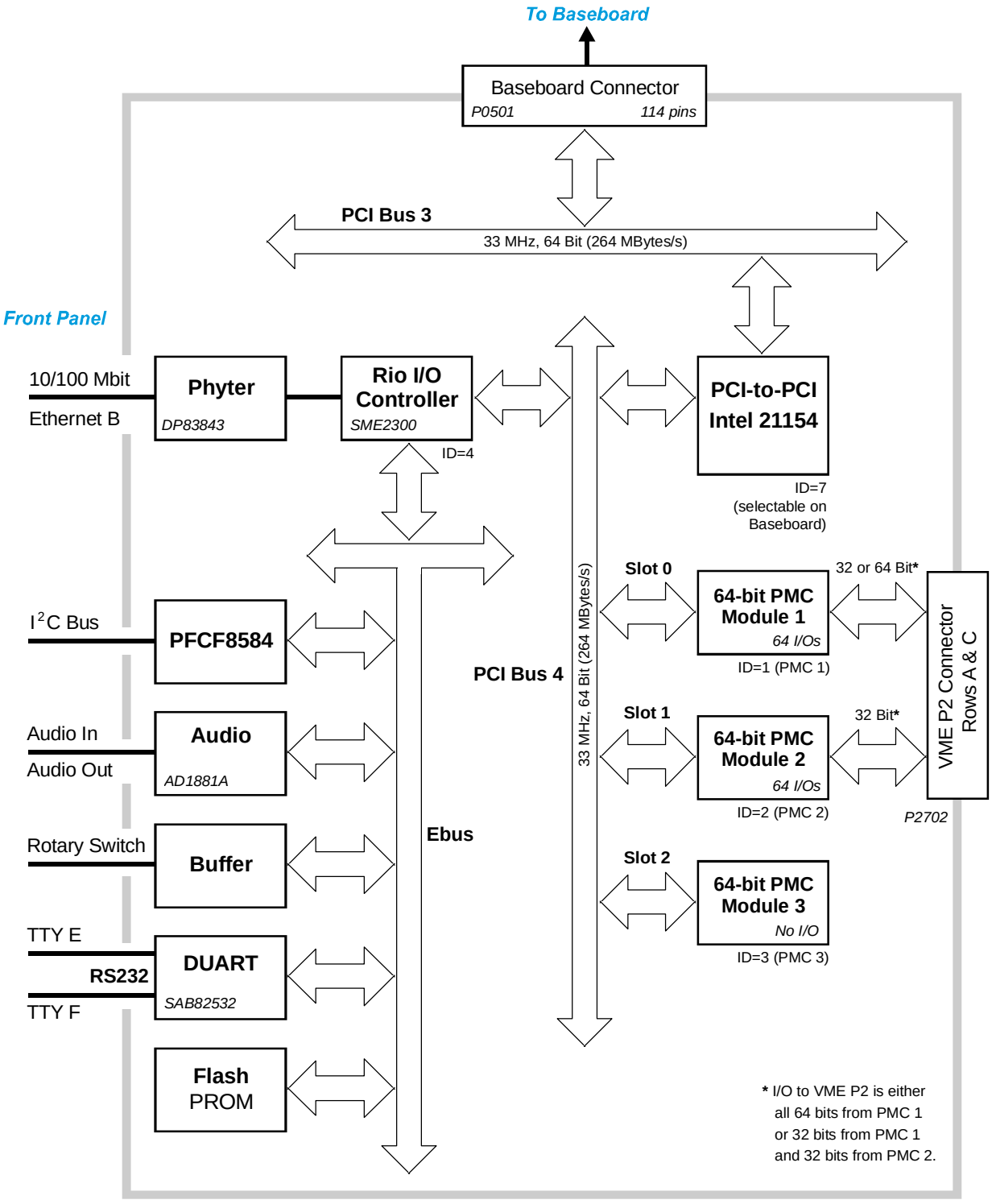


Figure 2-2. USPIIe-USB PMC Carrier Board Block Diagram

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

- Ethernet port B
- PMC Module slot 1
- PMC Module slot 2
- Audio Line-in or Mic-in
- Audio Line-out or Headphones
- User-defined 16-position Rotary Switch (see following *Note*)



Note: OBP *version 2.4* records the value of the User-defined Rotary Switch as an OBP environment variable called **themis-switch-value**. The default value for this variable is 255 (0xff), which is assigned if the PMC Carrier Board is not connected. If the Board is connected, a value from 0 through 15 is assigned.

To find the value of the Switch setting from OBP, type:

```
ok printenv themis-switch-value
```

To find the value of the Switch setting from Solaris, type:

```
# prtconf -vp | grep themis
```

USPIIe-USB/2P3

- PMC Module slot 1
- PMC Module slot 2
- PMC Module slot 3

2.3 Graphics Board

The USPII*e*-USB is supported by the Themis TGA3D/3D+ Graphics Board, a high-performance graphics accelerator designed to be installed in a VMEbus.

For more information on the TGA3D/3D+ Graphics Board, consult the *TGA3D/3D+ Graphics Board Installation Guide*, Themis part number 110102-021.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

2.4 Paddle Boards

There are two major types of paddle boards available for the USPII*e*-USB: the *Standard* Paddle Board and the *Multiple-I/O* Paddle Board.

2.4.1 Standard Paddle Board

The Standard Paddle Board is a 2-slot wide, single-slot connector, VME P2 paddle board (P/N 110094-030), providing connection for:

- SCSI Port A (SE mode)
- Serial (TTY) Port B
- power fail, software alarm, and high-temperature trip signals
- Polyswitch Vcc power fuse

2.4.2 Multiple I/O Paddle Board

The Multiple-I/O Paddle Board is a 1-slot wide, 3- or 5-row connector, VME P2 paddle board (P/N 110778-001), providing I/O connection for:

- Ultra160 SCSI Port A (wide-LVD mode)
- Parallel Port (DB25)
- 4 Serial Ports: Port A (TTY-A), Port B (RS232), Port C (TTY-C), and Port D (TTY-D)
- Dual (2) USB Ports
- PS/2 Keyboard/Mouse Port (mini-DIN-8)
- Audio Line Out (stereo jack)
- Audio Line In (stereo jack)



Note: Access to other VME P2 I/O signals requires a custom paddle board design; call Themis Computer for cost estimates.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

2.5 Backplane Jumper Settings

In compliance with the VME Specification, the PMC Carrier Board assures the continuity between bus grants BG[0..3]IN to BG[0..3]OUT, and the interrupt acknowledge daisy-chain IACKIN to IACKOUT.

2.6 System Specifications

2.6.1 Processor and Memory Subsystems

Table 2-3 and *Table 2-4* contain processor and memory subsection specifications.

Table 2-3. Processor Specifications

Feature/Function	Specifications
Processor	UltraSPARC-II*e*
Processor Speed	550, 600, and 650 MHz
Performance 650 MHz 600 MHz	 239 SPECint2000 @ 650 MHz (estimate) 260 SPECfp2000 @ 650 MHz (estimate) 220 SPECint2000 @ 600 MHz (estimate) 240 SPECfp2000 @ 600 MHz (estimate
Internal Cache	512 KB (600/650 MHz); 256 KB (500 MHz)
I/O Bus Interface	32 bit/66MHz PCI data path from CPU

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Table 2-4. Memory Specifications

Feature/Function	Specifications
Main Memory	Custom Memory Modules for 128 MB to 4 GB (gigabytes)
Memory Bus Interface	72 bit Data Path from CPU, including 8 bit ECC 2 to 1 Interleave to DRAM 13 bit Address Bus 3.3V Level Interface
Memory Modules	Custom Memory Module only (see *Table 2-2*, page 2-3)
Total Memory Configurations	From 128 MB to 4 GB (see *Table 2-2*, page 2-3)

2.6.2 I/O Subsystem

Table 2-5 summarizes the I/O subsystem functionality of the various USPII*e*-USB product configurations. I/O access on the USPII*e*-USB/**2P3** is through installed PMC Modules.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Table 2-5. USPIIe-USB I/O Subsystem Specifications

Function	Single Slot (Baseboard) Front-Panel Access	Dual Slot 2P2 (Baseboard and PMC Carrier Board) Front-Panel Access	VME P2 Access (Baseboard or PMC Carrier Board
PS/2 KB/Mouse or Dual USB (USB-0, USB-1) (Mini-DIN-8 Port)	Slot 1 Faceplate	Slot 1 Faceplate	**Yes** (see *Table B-5*, page B-7, and *Table B-6* on page B-9 for solder-bead settings)
USB-2	—	—	**Yes**
Serial Port A (Async RS-232[a])	Slot 1 Faceplate[b] (only if no P2 connection)	Slot 1 Faceplate[b] (only if no P2 connection)	**Yes** [b] (RS232 only; Tx, Rx)
Serial Port B (Async RS232, front FP & rear P2; 422, front only)	Slot 1 Faceplate[b] (only if no P2 connection)	Slot 1 Faceplate[b] (only if no P2 connection)	**Yes** [b] (RS232 only; full modem)
Serial Port C Asynchronous/Synchronous RS232[a]	—	—	**Yes** (RS232 only; Tx, Rx)
Serial Port D Asynchronous/Synchronous RS232[a]	—	—	**Yes** (RS232 only; Tx, Rx)
Serial Port E Asynchronous/Synchronous RS232[a]	—	Slot 2 Faceplate	
Serial Port F Asynchronous/Synchronous RS232[a]	—	Slot 2 Faceplate	
Parallel Port Bi-Directional IEEE1284	—	—	**Yes**
Ethernet Port A (RJ45) Auto-negotiating 10/100BaseT	Slot 1 Faceplate	Slot 1 Faceplate	

Note: Footnotes are described at the end of *Table 2-5* on page 2-11.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Table 2-5. USPIIe-USB I/O Subsystem Specifications (Continued)

Function	Single Slot (Baseboard) Front-Panel Access	Dual Slot 2P2 (Baseboard and PMC Carrier Board) Front-Panel Access	VME P2 Access (Baseboard or PMC Carrier Board
Ethernet Port B (RJ45) Auto-negotiating 10/100BaseT	—	Slot 2 Faceplate	
SCSI Port A Ultra2 LVD SCSI 80 MB/s	Slot 1 Faceplate	Slot 1 Faceplate	**Yes**[c]
SCSI Port B Ultra2 LVD SCSI 80 MB/s	Slot 1 Faceplate	Slot 1 Faceplate	
PMC Expansion[d], 32/64-bit/33 MHz PMC #0 PMC #1 PMC #2	 Slot 1 Faceplate — —	 Slot 1 Faceplate Slot 2 Faceplate Slot 2 Faceplate	 No **Yes** **Yes**
Graphics	PMC add-in	PMC add-in	
Audio: Line-in or Mic-in Impedance = 10 Kohm Vrms(max) = 2 V	—	Slot 2 Faceplate	
Audio: Line-out or Headphones Impedance = 200 ohm Vrms(max) = 2 V	—	Slot 2 Faceplate	

Key:
- VME P2 Access - Interface is via a VME P2 connector.
- Slot 1 and 2 refer to the two VME slots occupied by the USPIIe. The Baseboard is always in slot 1, the PMC Carrier Board is in slot 2.

a—RS232 port supports only RXD and TXD signals.

b—Serial ports A & B must be configured by solder-bead SB3501 to be accessed through either the front panel or the VME P2.

c—A 3-row VME backplane supports only SE (single-ended) SCSI devices.
A 5-row VME backplane supports both LVD and SE SCSI devices.

d—The User I/O on the PMC Carrier Board may be configured. Either 64 bits of User I/O may be made available on PMC #1, while the User I/O on PMC #2 is not used. Or 32 bits of User I/O may be made available on both PMC #1 and PMC #2.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

2.6.3 Auxiliary Functions

Table 2-6 summarizes the functional specifications of the auxiliary functions. These specifications apply to all product configurations.

Table 2-6. Auxiliary Functions Specifications

Feature/Function	Specifications
Flash Memory	Three (3) 4-MB Flash devices
NVRAM/TOD	8 KB, battery-backed UPI Static RAM plus timekeeper
System Status LEDs	Four LEDs located on Front Panel of the Baseboard [See “USPIIe-USB/1 (Single VME Slot)”, page C-4, Appendix C, ”Front Panel Diagrams”]
VME Status LEDs	Four LEDs located on Front Panel of the Baseboard [See “USPIIe-USB/1 (Single VME Slot)”, page C-4, Appendix C, ”Front Panel Diagrams”]
Reset Switch	Momentary Push-button - Generates POR Located on Front Panel
Watchdog Timers	Two Level Watchdog: Level One: Interrupt Level Two: POR
Voltage Sensors	Monitors Vdd, 3.3V, and 5V POR reset signal is generated when voltage is out of tolerance POR voltage Environmental monitoring: Vdd, 3.3 V, 5 V, +-12 V
Temperature Sensor	Monitors whether the CPU temperature stays within a specified range Range can be changed by software (OBP firmware)

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

2.7 Environmental Specifications

Table 2-7. USPIIe-USB Operating Environmental Specifications

Description	Minimum Value	Maximum Value
Temperature Range	-5°C	55 C
Humidity Range [a] relative non-condensing at 104°F (40°C)	0%	95%
Altitude Range	0 feet	9,843 feet (3,000 meters)
Air Flow (inlet)	300 lfm air flow at 50° C @ 600 MHz minimum	

a—A non-condensing environment must be maintained at all times. Themis recommends that the board be operational (powered on) and temperature stabilized before and during humidity testing.

Table 2-8. USPIIe-USB Non-operating Environmental Specifications

Description	Minimum Value	Maximum Value
Temperature Range	-40° C	85° C
Humidity Range [a] relative non-condensing at 104°F (40°C)	0%	95%
Altitude Range	0 feet (0 meters)	38,370 feet (12,000 meters)

a—Board must be non-operational until such time as the environment can be assured to be non-condensing, and any or all condensation has been evaporated.

2.8 Estimated Power Requirements

Table 2-9. Estimated Power Requirements

Baseboard Configuration (USPIIe-USB/1)	Watts Dissipation, typical (600-MHz processor)	Watts Dissipation, typical (650-MHz processor)
512 MBytes memory	21 Watts	23 Watts
1024 MBytes memory	23 Watts	25 Watts
2048 MBytes memory	23.5 Watts	25.5 Watts

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Overview Section

Chapter 3

Hardware Overview

The following sections provide a description of the major components of the USPII*e*-USB. Detailed explanations of certain subsystems are provided in later chapters.

3.1 Baseboard

3.1.1 UltraSPARC-IIe Processor and Cache

The Central Processor Unit (CPU) that is used in the USPII*e*-USB is the Sun Microsystems UltraSPARC-II*e* (SME1532C), described in the block diagram of *Figure 3-1* on page 3-2. The CPU is available in operating speeds of 550, 600, or 650 MHz.

The architecture complies with the SPARC V9 instruction set, which enables the system to use a wide range of peripherals and the high-performance Solaris operating system. For details on the UltraSPARC-II*e* CPU processor, refer to the Themis *USPIIe Software Manual* (110102-023), the Sun UltraSPARC-II*e Processor Data Sheet* (SME1701CPGA-400/500), and the Sun *UltraSPARC-IIe User's Manual* (806-tbd-00]).

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

CPU
- Prefetch and Decode Unit
- Integer Unit
- Floating Point Unit / VIS Execution

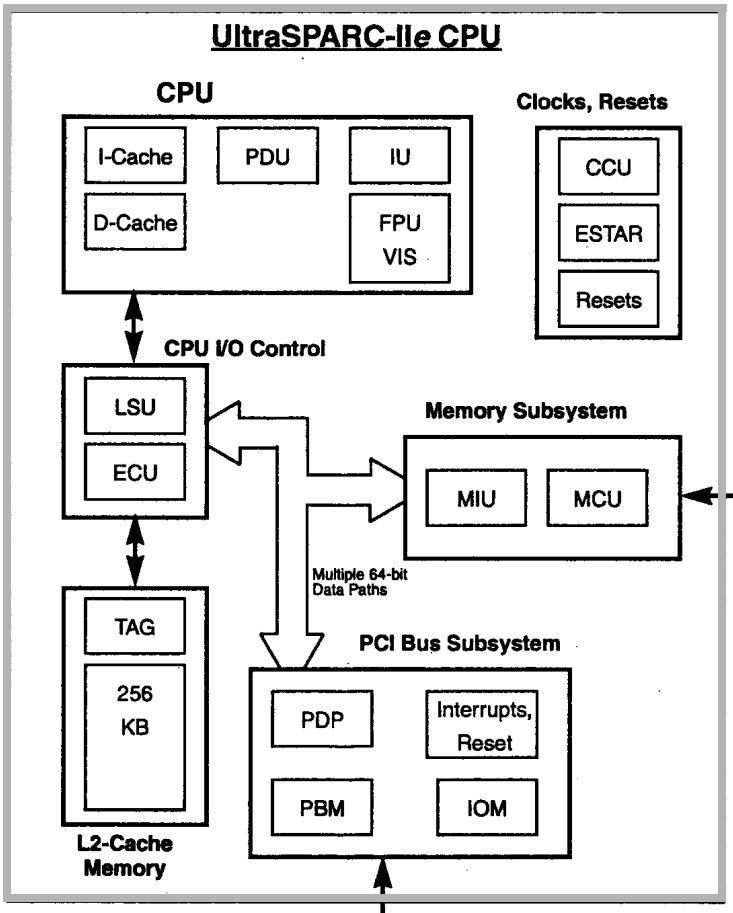
Clocks, Resets
- Clock Control Unit
- Energy Star logic

Memory Subsystem
- Memory Interface Unit
- Memory Control Unit

PCI Bus Subsystem
- PCI Data Path
- PCI Bus Module
- IO Memory management unit

CPU I/O Control
- L2-Cache Control Unit
- Load and Store Unit

L2-Cache Subsystem
- L2-Cache Control Unit (aka ECU)
- Tag and Data RAM



Clocks, Resets, Modes
- CLKA & CLKB
- SYS_RESET_L,
- P_RESET_L, X_RESET_L
- RMTV_SEL
- VID
- GPO

SDRAM Signals
- MEM_CLK/CLKE
- MEM_CS/WE
- MEM_RAS/CAS
- MEM_ADDR/BANK
- MEM_DATA/ECC
- MEM_SCLK_OUT/IO_SCLK

JTAG Test Signals
- TCK
- TRST_L
- TMS
- TDI/O

Test Signals
- PLLBYPASS, EPD
- CPU_L5CLK, PCI_L5CLK
- RAM_TEST, ITB_TEST
- PMO
- TEMP_SENSE
- EXT_EVENT
- OBSRV_MCU

PCI Bus Signals
- PCI_AD
- PCI_CBE_L
- PCI_FRAME_L
- PCI_I/TRDY_L
- PCI_REQ/GNT_L
- PCI_DEVSEL_L
- PCI_P/SERR_L
- PCI_RST_L
- PCI_CLK, PCI_REF_CLK
- INT_NUM
- SB_DRAIN
- SB_EMPTY
- SYNC_3TO1
- PCI_STOP_L, PAR

Power
- Vdd_IO
- Vdd_core
- Vdd_pll, diff
- Vss

Figure 3-1. UltraSPARC-IIe CPU Block Diagram

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

3.1.2 USPII*e*-USB ICHIP-2 Interrupt Controller

The USPII*e*-USB ICHIP-2 Interrupt Controller provides a variety of functions on the USPII*e*-USB (see *Figure 3-2*). The ICHIP-2 manages system resets, system interrupts, and some clock control functions. These functions are divided into independent functional blocks.

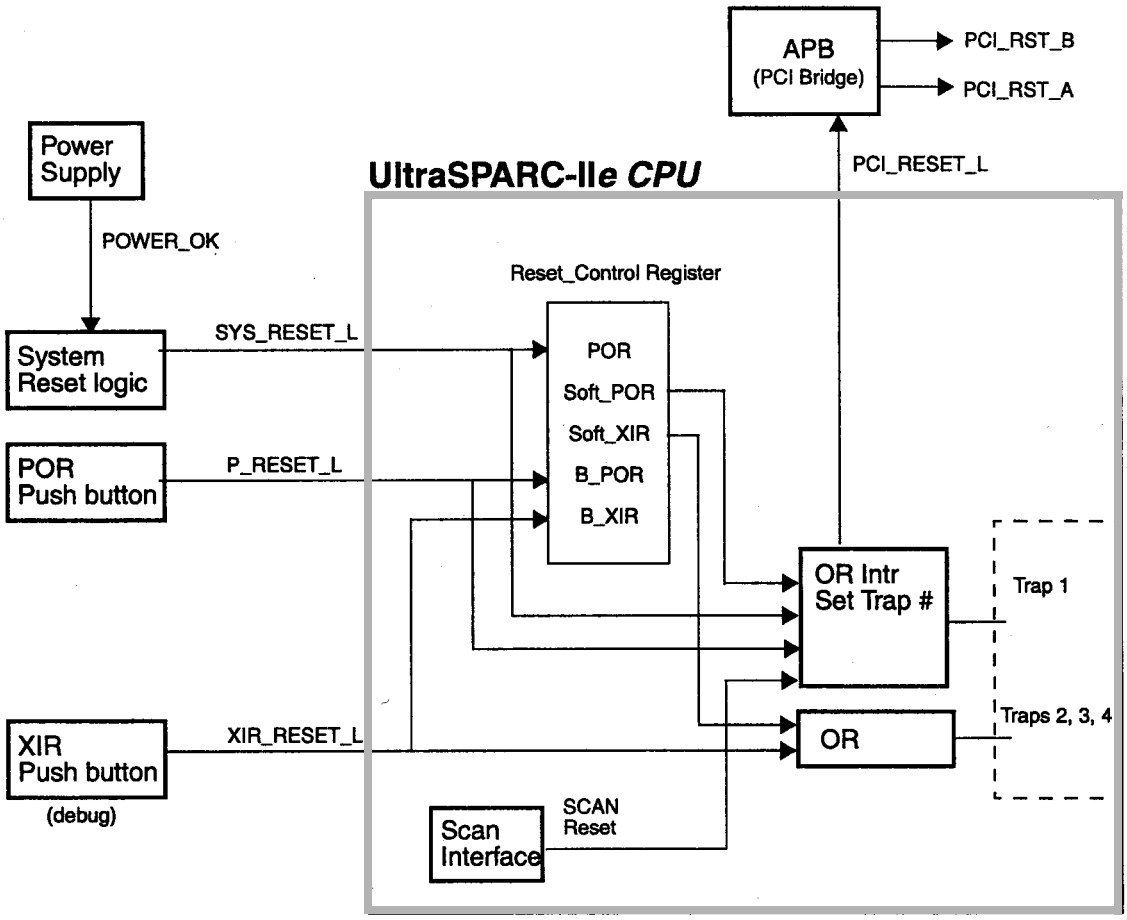


Figure 3-2. USPII*e*-USB Reset Architecture

The interrupt controller on the ICHIP-2 accepts all interrupts from the USPII*e*-USB subsystems (up to 41 interrupts) and delivers encoded interrupts on the six (6) interrupt lines routed to the UltraSPARC-II*e* microprocessor. The interrupts received by the ICHIP-2 are not passed to the UltraSPARC-II*e* in the order they are received. Instead, a priority level is assigned. Eight (8) interrupt levels are implemented in hardware. For more information concerning the USPII*e*-USB ICHIP-2, refer to Chapter 6, "Resets".

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

3.1.3 PCI-to-PCI Bridges

The USPII*e*-USB fans out the single 66-MHz/32-bit primary PCI bus (see *Figure 2-1* on page 2-2) into three secondary busses:

- Two 33-MHz/32-bit PCI busses using the Sun APB PCI-to-PCI interface chip
- One 33-MHz/64-bit PCI bus using the Intel 21154 PCI-to-PCI interface chip

One APB-based PCI bus is dedicated to data traffic to the VME bus through the Universe II PCI-to-VME bridge chip.

The second APB-based PCI bus is dedicated to remaining onboard devices through the Sun Rio controller chip (see the following section "Sun Rio I/O Controller" on page 3-5.

The “transparent” Intel-based PCI bus is dedicated to servicing disk traffic from the SCSI controller and all I/O to the on-board PMC Module slot, and all other PMC Modules on any PCM Carrier and TGA3D/3D+ Graphics boards that may be installed in the second and third VME slots (see Appendix C, “Front Panel Diagrams”).

3.1.3.1 Advanced PCI Bridge (APB)

The USPII*e*-USB Advanced PCI Bridge (SME2411) interfaces directly with the UltraSPARC-II*e* microprocessor and concentrates two (2), 32-bit, 33MHz PCI buses into one 32-bit, 66-MHz PCI bus that interfaces directly with the UltraSPARC-II*e*. The 66-MHz PCI-to-CPU bridge can achieve a peak bandwidth of 2 GBits/sec. Within the USPII*e*-USB, the two 33-MHz PCI busses are referred to as PCIA and PCIB.

3.1.3.2 Intel 21154 PCI-to-PCI Bridge

The Intel 21154 PCI-to-PCI bridge complies with *PCI Local Bus Specification*, Revision 2.2, and has a 66-MHz/32-bit primary bus interface and a 33-MHz/64-bit secondary interface.

The 21154 provides full support for delayed transactions, which enables the buffering of memory read, I/O, and configuration transactions. The 21154 has separate posted write, read data, and delayed transaction queues with significant buffering capability. In addition, the 21154 supports buffering of simultaneous, multiple, posted write, and delayed transactions in both directions.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Among the features of the 21154 are a programmable 2-level secondary bus arbiter, an IEEE standard 1149.1 JTAG interface, live insertion support, a 4-pin general-purpose I/O interface, individual secondary clock disables, and enhanced address decoding. The 21154 has enough clock and arbitration pins to support nine PCI bus master devices directly on its secondary interface.

The 21154 allows the two PCI buses to operate concurrently. This means that a master and a target on the same PCI bus can communicate while the other PCI bus is busy. This traffic isolation increases system performance.

3.1.4 Sun Rio I/O Controller

Sun's Rio I/O controller (SME2300) incorporates an Ethernet interface, USB, and an Ebus interface. The Ethernet port autosenses the port speed as either 10 or 100 Mbit/sec, with no pin-jumpers required to set either rate.

The Ebus supports the NVRAM, boot flash, user flash 0, 1, and 2, system PLD, and DUART (dual UART). The DUART controls both TTYC (RS232) and TTYD (RS232) serial ports.

3.1.5 Symbios SCSI Controller

The Symbios SCSI Controller (SYM53C896) provides two (2) LVD UltraWide SCSI-3 interfaces (80 MB/sec). In order to maximize speed, it is attached directly to the 33-MHz/64-bit PCI bus connected to the Intel 21154 PCI-to-PCI bridge. A maximum burst rate of up to 264 MB/sec is supported.

3.1.6 Tundra Universe II

The Tundra Universe II (Tundra CA91C142B) ASIC interfaces the local 32-bit PCI bus to the 64-bit VMEbus. The Universe II includes a 33-MHz, 32-bit PCI bus interface, a fully compliant, high-performance, 64-bit VMEbus interface, as well as a broad range of VMEbus address and data transfer modes of:

- A32/A24/A16 master and slave transfer, except for A64 and A40
- D64/D32/D16/D08 master and slave transfer, except for MD32
- MBLT, BLT, ADOH, RMW, LOCK, and location monitors

The Universe II also includes support for full VMEbus System Controller, eight user-programmable slave images, and seven interrupt lines. For more information on the Universe II, refer to Chapter 4, "Universe II Description" and the *Tundra Universe II User Manual* (Tundra 8091142.MD300.01).

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

3.1.7 PLD

The PLD (Programmable Logic Device) on the USPII*e*-USB resides on the Ebus of the Sun Rio I/O Controller. There are two main functions of this PLD: one is to implement miscellaneous registers and manipulate the address map of the Flash devices; the other is to implement the reset logic.

3.1.8 Acer Super I/O Controller

The Acer (M1535D) Super-I/O controller chip controls AC97 (Audio Codec 97) audio, the IEEE 1284 parallel port, the PS/2 keyboard/mouse, and both TTYA and TTYB serial ports. Each component is individually configured to maximize the performance of the USPII*e*-USB.

3.1.9 Seimens SAB 82532 Controller

The Seimens SAB 82532 Enhanced Serial Communication Controller provides support for Serial Ports C and D. A maximum external data transfer rate of 10 Mbits/second and a maximum internal data transfer rate of 2 Mbits/second is attainable on each port.

3.1.10 Flash Memory

The USPII*e*-USB includes three (3) Flash EPROM devices (4-MB). They are located on the Baseboard bottom side (solder side) and are accessible through the Baseboard Ebus2. Any Flash can be jumper configurable as the boot device. The boot Flash normally contains Sun's OBP or Wind River's VxWorks boot ROM. The mapping of each Flash is largely configurable by the PLD. It is also possible to divide each flash into two (2) sections, permitting a total of eight (8) boot devices.

3.1.11 TOD and NVRAM

The Non-Volatile RAM and a Time of Day (TOD) clock are both contained in the timekeeper chip (SGS-Thomson, M48T59Y-70MH1). The NVRAM has its own lithium battery to operate the clock and maintain the contents of the NVRAM during power-off situations. The battery device is an SGS Thomson M4T28-BR12SH1. This single lithium battery provides backup for approximately 10 years, and the real-time clock circuitry provides accuracy of +/- one (1) second per day.

NVRAM and TOD are programmed using the FORTH toolkit in the OpenBoot PROM (OBP). To learn how to replace the battery, consult Section 1.6, “TOD/NVRAM Battery Replacement,” on page 1-14.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

3.1.12 Memory Subsystem

As seen in *Figure 3-3*, the USPII*e*-USB supports a single custom Themis Memory Module, plugged directly into the Baseboard (see *Figure 3-4* on page 3-8). The memory data path is 72 bits with 8 bits assigned to ECC. Memory complies to PC-133 timing.

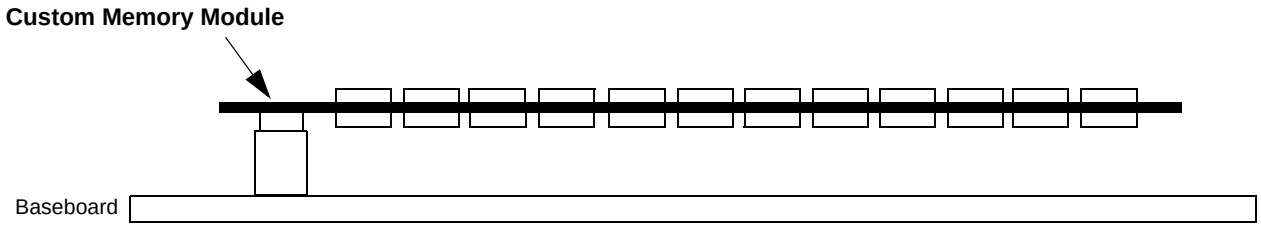


Figure 3-3. Custom Memory Module Topology (Side View)

Memory capacities are offered in **128-MB**, **256-MB**, **512-MB**, **1-GB**, **2-GB**, and **4-GB** capacities (see *Table 2-2* on page 2-3). USPII*e*-USB memory design includes Error Correction Code (ECC). A single bit error in a 64-bit word is corrected without loss of a cycle.

In designing the memory subsystem, considerable attention was paid to minimizing overall power consumption. The typical active power consumption of a USPII*e*-USB with a 1-GB memory module is 23 watts (see *Table 2-9* on page 2-13 for other power requirements).



Caution: Because of the *VME Specification* requiring a 0.8-inch interboard separation (see *Figure 1-1* on page 1-5) between VME slots, only one Memory Module can be installed onto a USPII*e*-USB Baseboard (*stacking is not supported*).

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

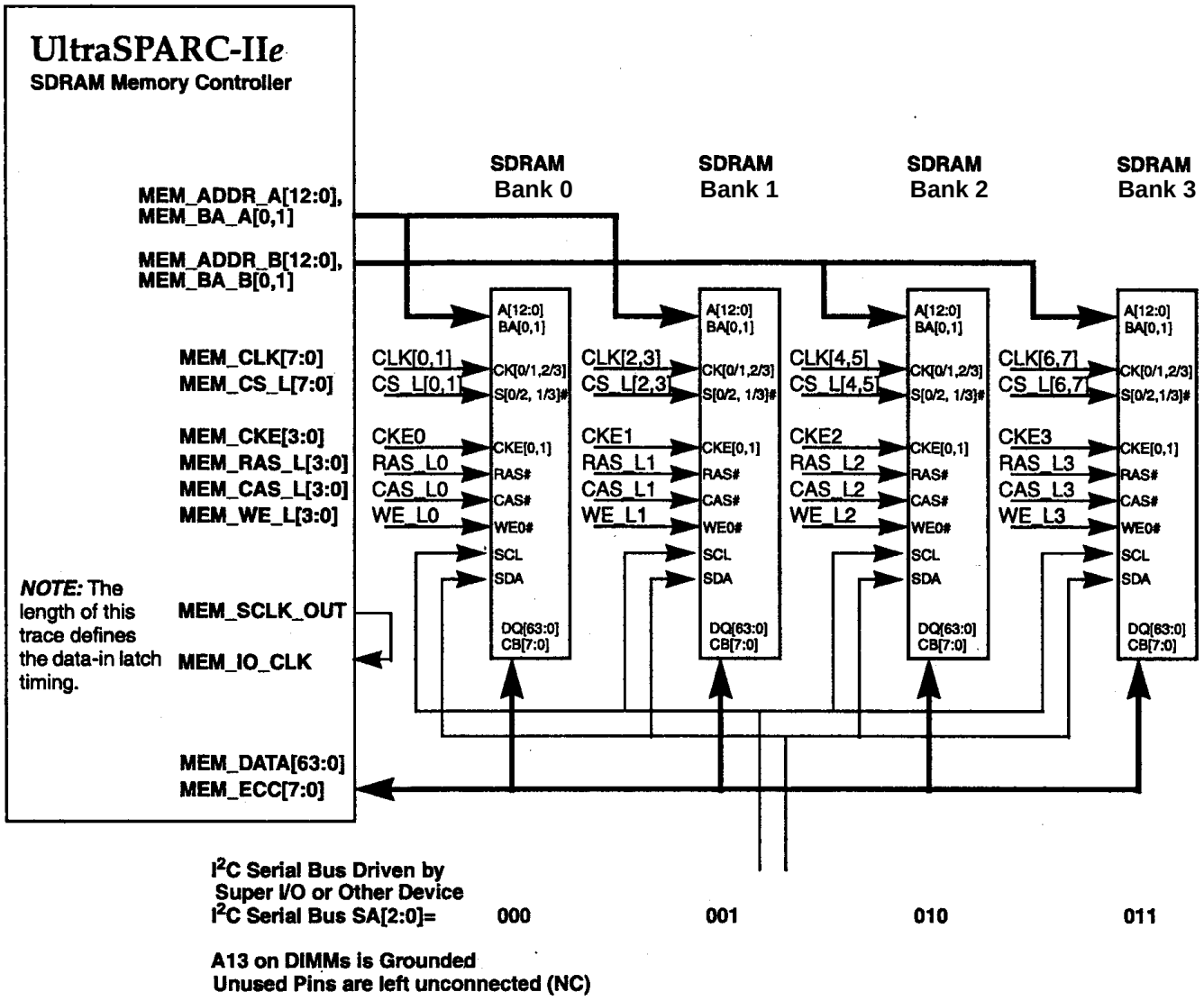


Figure 3-4. SDRAM Memory Subsystem

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

3.2 PMC Carrier Board

The PMC Carrier Board supports two (USPII*e*-USB/**2P2)** or three (USPII*e*-USB/**2P3**) PMC Module Cards in the second slot of the product configuration (see Appendix C, “Front Panel Diagrams” and Appendix D, “Board Diagrams”.

In addition to the standard PMC I/O, 64 bits of configurable User I/O are provided from the VME P2 connector directly to the PMC 1 and PMC 2 Module slot positions. All 64 bits may be routed to PMC 1, leaving 0 bits of User I/O for PMC 2. Alternatively, 32 bits may be routed to PMC 1 and 32 bits to PMC 2. In the latter case, PMC 1 will utilize the upper VME P2 signals, VME P2 A[32..17] and VME P2 C[32..17], while PMC 2 will utilize the lower VME P2 signals, VME P2 A[16..1] and VME P2 C[16..1]. The signals are available on the J1004 connector of PMC 1 and the J1104 connector of PMC 2. If all 64 bits of User I/O are routed to PMC 1, it utilizes all 64 signals of the VME P2 connector. In this case, all 64 signals are available on the J1004 connector of PMC 1.



Note: User I/O is directed to PMC 1 and PMC 2 Modules through solder-bead configurations (see *Table B-8* on page B-12).

3.3 OpenBoot PROM

The OpenBoot PROM (OBP) can be accessed through the Ebus2. OBP code is contained in Flash Memory and provides the following functionality:

- Runs start-up diagnostic tests.
- Initializes the host machine.
- Reads non-volatile RAM (NVRAM) and executes the boot sequence. The Diagnostic Executive or standalone programs can also be executed.
- Includes the abbreviated system monitor. Entry into the system monitor is signified by the “`ok`” prompt. If a boot attempt fails, the OBP tries to start the abbreviated system monitor.
- Supplies program code for the FORTH Toolkit; the on-board diagnostics contain the FORTH Toolkit and the FORTH language interpreter. Entry into the FORTH Toolkit is signified by the “`ok`” prompt.

For more information on the OBP please refer to the *OpenBoot Command Reference* from Sun Microsystems and to the Themis *USPIIe Software Manual*.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Operation Section

Chapter 4

Universe II Description

4.1 Features

Tundra's Universe II (CA91C142B) interfaces the local 32-bit PCI bus to the VMEbus. The following lists some of the Universe II's features on the USPII*e*-USB board:

- 33 MHz, 32-bit PCI bus interface
- Fully compliant, high performance 64-bit VMEbus interface
- Integral FIFOs buffer with multiple transactions from the PCI bus to the VMEbus and from the VMEbus to the PCI (both directions)
- Programmable DMA controller with linked list support
- A broad range of VMEbus address and data transfer modes:
  - — A32/A24/A16 master and slave transfer, except for A64 and A40
  - — D64/D32/D16/D08 master and slave transfer, except for MD32
  - — MBLT, BLT, ADOH, RMW, LOCK, and location monitors
- Support for full VMEbus System Controller
- Nine user programmable slave images on the VMEbus and the PCI bus ports
- Seven interrupt lines
- Auto initialization for the slave-only applications

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

- Programmable registers from both the VMEbus and the PCI bus
- Support for four mailbox registers
- Support for four location monitors
- Support for eight semaphores
- Support for RMW (Read, Modify, Write) cycles and lock cycles

This chapter is intended to outline the VMEbus to PCI Bus interface on the USPII*e*-USB. If more detailed information is need, please refer to the *Tundra Universe II User's Manual*, Spring 1998.



Note: All registers on the Universe II are little-endian.

4.2 VMEbus Interface

4.2.1 VMEbus Configuration

The following lists the initial configuration of the VMEbus system:

- VMEbus First Slot Detector
- Two methods of Auto Slot ID
- Register Access at the power up

4.2.2 Universe II as the VMEbus Slave

The Universe II's VMEbus Slave Channel supports all of the addressing and data transfer modes which are documented in the VME64 specification. The Universe II does not support the A64 mode and the modes intended to augment the 3U applications, i.e., A40 and MD32. The Universe II becomes a slave when one of its eight programmed slave images or register images are accessed by a VMEbus master. It is not implied that the Universe II cannot reflect a cycle on the VMEbus and access itself, as it is capable of doing so. Depending on the programmed values of the VMEbus slave images, the incoming write transaction from the VMEbus may be treated as either posted or coupled (refer to Section 4.3, "Slave Image Programming," on page 4-9). If the post write operation is selected, the data is written to a

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Posted Write Receive FIFO (RXFIFO) and the VMEbus master receives the data acknowledgment from the Universe II. The Universe II transfers the write data from the RXFIFO without the involvement of the initiating VMEbus master (refer to “Posted Writes” on page 2-15 of the Universe II manual for a complete explanation of this operation). If the coupled cycle operation is selected, the transaction is completed on the PCI bus first, and the data acknowledgment is sent to the VMEbus master. With the coupled cycle, the VMEbus is not available to other masters while the PCI bus is executing the transaction.

Read transactions may either be pre-fetched or coupled. A pre-fetched read is initiated when enabled by the user and a VMEbus master requests a block read transaction (BLT or MBLT). When the Universe II receives a request for the block transfer, it begins to fill its Read Data FIFO (RDFIFO) using burst transactions from the PCI bus resource. The initiating VMEbus master then obtains its block read data from the RDFIFO of the Universe II rather than from the PCI resources directly.

A RMW cycle allows a VMEbus master to read from a VMEbus slave and then write to the same resource without releasing the bus between the two operations. Each one of the Universe II slave images can be programmed to map RMW cycles to the PCI Locked cycles. RMW cycles are not supported with the unaligned or D24 Cycles.

In order to support the VMEbus broadcast capability, Universe II has four location monitors. The location monitor’s image consists of a 4Kbyte image in A32, A24, or A16 space on the VMEbus. If the Location Monitor is enabled, an access to a Location Monitor would cause the PCI Master Interface to issue an interrupt.

The Universe II supports the VMEbus lock commands as they are described in the VME64 Specification. The ADOH cycles are used to execute the lock command with a special AM code. A locked resource can not be accessed by any other resource as long as the VMEbus master has the bus ownership. If Target-Abort or Master-Abort occurs during a locked transaction on the PCI bus, the Universe II will relinquish its lock on the bus, in accordance with the PCI Specification.

4.2.3 Universe II as the VMEbus Master

The Universe II becomes the VMEbus master when the VMEbus Master Interface is internally requested by the Interrupt Channel, the PCI Bus Target Channel, or the DMA channels. The Interrupt Channel always has the highest priority over the other two channels and will request the VMEbus Master Interface when it receives an enabled VMEbus interrupt request.

The PCI Bus Target Channel and the DMA Channel compete for the VMEbus Master Interface and are awarded it in a fair manner. There are several methods available for the user to configure the relative priority that the DMA channel and the PCI Bus

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Target Channel have over the VMEbus Master Interface. The PCI Target Channel requests the VMEbus Master Interface when:

- the TXFIFO contains a completed transaction
- there is a coupled cycle request.

The DMA Channel requests the VMEbus Master Interface when:

- the DMAFIFO has 64 bytes available when reading from the VMEbus
- the DMAFIFO has 64 bytes in its FIFO when writing to the VMEbus
- the DMA block is complete.

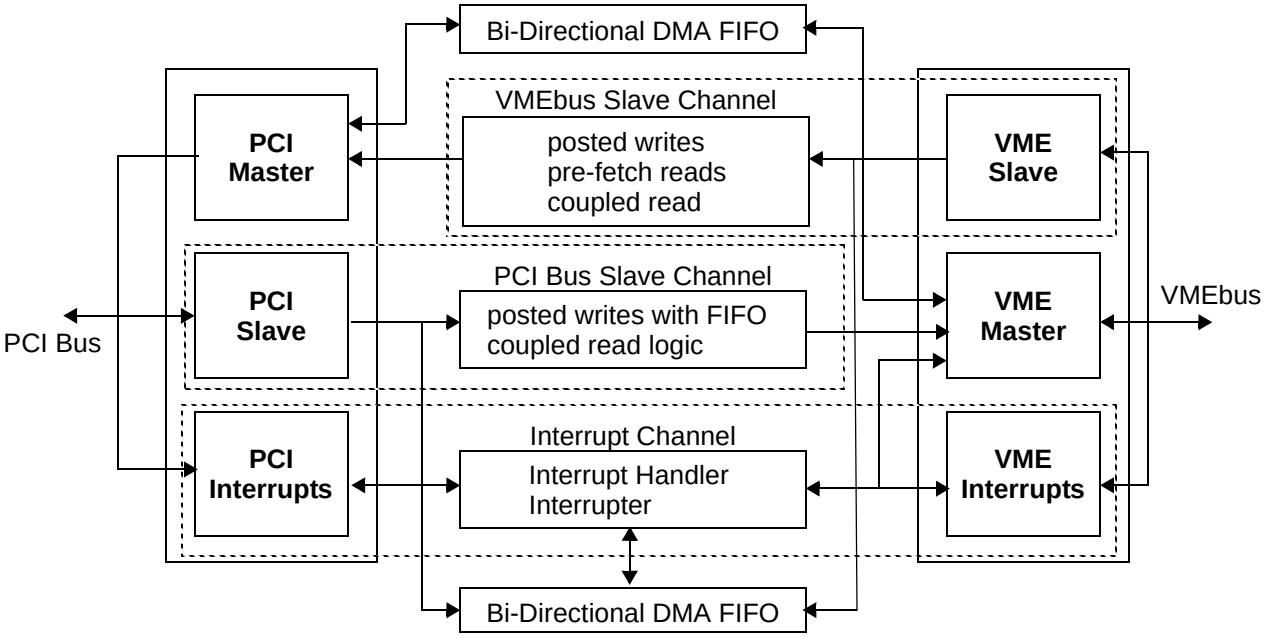


Figure 4-1. Universe II Architectural Diagram

The Universe II's VMEbus Master Interface supports all of the addressing and data transfer modes as specified by the VME64 specification. The Universe II does not support the A64 mode and modes intended to augment the 3U applications, i.e., A40 and MD32. The Universe II is compatible with all the VMEbus modules that conform to pre-VME64 specification. The Universe II as the VMEbus Master supports RMW and ADOH. It accepts BERR* (active low) and DTACK* as cycle terminations from the VMEbus, but does not accept the RETRY* as a termination from the VMEbus Slave. DTACK* indicates the successful completion of a transaction. The Universe II utilizes the ADOH cycle to implement the VMEbus Lock command allowing a PCI bus master to lock the VMEbus resources.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

4.2.4 VMEbus First Slot Detector

As defined by the VME64 specification, the Universe II samples the BG3IN* right after the reset to determine if the USPII*e*-USB resides in slot 1. If the BG3IN* is sampled low right after the reset, the USPII*e*-USB board becomes the SYSCON. Otherwise the SYSCON Module of the Universe II is disabled. The software can set or clear the SYSCON bit of the MISC_CTL register of the Universe II. The definition of the MISC_CTL register is provided in *Table 4-1* on page 4-5. The offset of this register is 0x404.

Table 4-1. Universe II Miscellaneous Control Register (MISC_CTL)[a]

BIts	Name	Description	Reset State	Access
[31:28]	VBTO	VMEbus Time-out: 0000 = Disable; 0001 = 16 μs; 0010 = 32 μs; 0011 = 64 μs; 0100 = 128 μs; 0101 = 256 μs; 0110 = 512 μs; 0111 = 1024 μs; Others = RESERVED	0011	R/W
26	VARB	VMEbus Arbitration Mode: 0 = Round Robin; 1 = Priority	0	R/W
[25:24]	VARBTO	VMEbus Arbitration Time-out 00 = Disable Timer; 01 = 16 μs (minimum value of 8 μs, due to the 8 μs clock granularity); 10 = 256 μs; others - RESERVED	01	R/W
23	SW_LST	PCI Reset: 0 = no effect; 1 = initiate PCI bus LRST*	0	W
22	SW_SYSRST	Software VMEbus SYSRESET: 0 = no effect; 1 = Initiate VMEbus SYSRST	0	W
20	BI	BI- Mode: 0 = Universe II is not in BI-mode; 1 = Universe II is in BI mode	Power-up Option	R/W
19	ENGBI	Enable Global BI-mode Initiator: 0 = Assertion of VIRQ1 ignored; 1 = Assertion of VIRQ1 puts the Universe II in BI-mode	0	R/W
18	RESCIND	Unused on the Universe II	1	R/W

Note: Footnotes are described at the end of *Table 4-1* on page 4-6.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Table 4-1. Universe II Miscellaneous Control Register (MISC_CTL)[a] (Continued)

BIts	Name	Description	Reset State	Access
17	SYSCON	SYSCON: 0 = Universe II is not a VMEbus System Controller; 1 = Universe II is a VMEbus System Contoller	Power-up Option	R/W
16	V64AUTO	VME64 Auto ID: Write: 0 = no effect; 1 = Initiate sequence This bit initiates the Universe II VME64 Auto ID Slave participation.	Power-up Option	R/W

a—All unspecified bits in this table are RESERVED for the Universe II. Reading the bits results in an undefined state; writing to these bits should be 0.

When the Universe II is configured as the System Controller, it provides the following functions on the VMEbus:

— A 16MHz Clock Driver

— An Arbitration Module

— A bus timer

— An IACK Daisy Chain Driver (DCD).

The USPII*e*-USB supports Round-Robin arbitration. The VMEbus arbitrator time out is also controlled by the MISC_CTL register described above. The timer may be set to either 16 µs, 256 µs, or disabled. The default setting is 16 µs. The arbitration timer has a granularity of 8 µs; setting the timer to 16 µs means the timer may expire in as little as 8 µs or as much as 24 µs. It should also be noted that disabling the arbitration timer implies that the Universe II will not recover from an access error. Disabling the arbitration timer is not recommended.

4.2.4.1 Automatic Slot Identification

The Universe II supports two types of Auto ID functionality:

- Auto Slot ID as described by the VME64 specification
- Proprietary Method which is developed by Tundra

Refer to “Auto Slot ID: VME64 Specified”, page 2-24, and “Auto-ID: A Proprietary Tundra Method”, on page 2-25 of the Universe II Manual for more information.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

4.2.4.2 Register Access at Power Up

Register access at power up is used in a system where either the Universe II is independent of the local CPU or a CPU is not present. Since the Universe II and the UltraSPARC-II*e* are present on the USPII*e*-USB, register access at power up is not supported.

4.2.5 Universe II's Hardware Power-Up Options

The Universe II power up options are determined right after the PWRRST* based on the level of VMEbus Address VA[31..1] and VMEbus Data VD[31..27]. See *Table 4-2* below for the Universe II's power up options.

The Universe II is automatically configured at power up to operate in the default configuration listed in *Table 4-2*. It should be noted that all power up options are latched only at the positive edge of PWRRST*; they are loaded when SYSRST*, PWRRST*, and RST* are negated.

Table 4-2. Universe II Power-Up Options

Option	Register	Field	Default	Pins
VMEbus Register Access Slave Image	VRAI_CTL	EN	Disabled	VA[31]
		VAS	A16	VA[30..29]
	VRAI_BS	BS	0x00	VA[28..21]
VMEbus CR/CSR Slave Image	VCSR_CTL	LAS[0][a]	Memory	VA[20]
	VCSR_TO	TO	0x00	VA[19..15]
Auto-ID	MISC_STAT	DY4AUTO	Disabled	VD[30]
	MISC_CTL	V64AUTO	Disabled	VD[29]
	VINT_EN	SW_INT	0	
	VINT_STAT	SW_INT	0	
	VINT_MAP1	SW_INT	000	
BI-Mod	MISC_CTL	BI	Disabled	VD[28]
AUTO_SYSCON Detect	MISC_CTL	SYSCON	Enabled	VBG3IN*

Note: Footnotes are described at the end of *Table 4-2* on page 4-8.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Table 4-2. Universe II Power-Up Options (Continued)

Option	Register	Field	Default	Pins
SYSFAIL* Assertion	VCSR_SET	SYSFAIL	Asserted	VD[27]
	VCSR_CLR	SYSFAIL	--	--
PCI Target IMAGE	LSI0_CTL	EN	Disabled	VA[13]
		LAS[0]	Memory	VA[12]
		VAS	A16	VA[11..10]
	LSI0_BS	BS	0x0	VA[9..6]
	LSI0_BD	BD	0x0	VA[5..2]
PCI Bus Size[b]	MISC_STAT	LCLSIZE	32-bit	REQ64*
PCI CSR Image Space	PCI_CSR	BM	Disabled	VA[14]
PCI Register Access	PCI_BS0 PCI_BS1	SPACE	Refer to: *Table 4-3* and *Table 4-4*.	VA[1]
PCI Bus Size[c]	MISC_STAT	LCLSIZE	32-bit	REQ64*
PCI CSR Image Size	PCI_CSR	BM	disabled	VA[14]

a—The LAS field will enable the PCI_CSR registers IOS or MS field if the EN FIELD of the LSIO_CTL register is set.

b—As per PCI 2.1 Specification, the PCI Bus Size is loaded on any RST* event.

c—Following the PCI 2.1 Specification, the PCI Bus Size is loaded on any RST* event.

The PCI Configuration Base Address 0 and Base Address 1 Registers' offsets are 0x010 and 0x014, respectively. The registers specify the 4KB aligned base address of the 4 KB Universe II register space on PCI. The power-up options determine if the registers are mapped into Memory or I/O space.

.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Table 4-3. PCI Configuration Base Address 0 Register (PCI_BS0)[a]

BIts	Name	Description	Reset State	Ac-cess
[31:12]	BS	Base Address	0	R/W
00	SPACE	PCI Bus Address Space: 0 = Memory; 1 = I/O	Power-up Options	R

a—All other bits are Read 0.

Table 4-4. PCI Configuration Base Address 1 Register (PCI_BS1)[a]

BIts	Name	Description	Reset State	Ac-cess
[31:12]	BS	Base Address	0	R/W
00	SPACE	PCI Bus Address Space: 0 = Memory; 1 = I/O	Power-up Options	R

a—All other bits are Read 0.

4.3 Slave Image Programming

The Universe II recognizes two types of accesses on its bus interfaces: accesses destined for the other bus and accesses decoded for its own register space.

4.3.1 VME Slave Images

A VMEbus slave image is used to access the resources of the PCI bus when the Universe II is not the VMEbus master. The user may control the type of accesses by programming specific attributes of the VMEbus slave image. The Universe II will only accept accesses to the VMEbus from within the programmed limits of the VMEbus slave image.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Note: The Bus Master Enable (BM) bit of the PCI_CS register must be set in order for the image to accept posted writes from an external VMEbus master. If this bit is cleared while there is data in the VMEbus Slave Posted Write FIFO, the data will be written to the PCI bus. No further data is accepted into this FIFO until the bit is set.

4.3.1.1 VMEbus Fields

Before the Universe II responds to a VMEbus Master (other than itself), the address must lie between the base and bound addresses. Also, the address modified must match the modifier specified by the address space, access mode, and type fields. Descriptions of the VMEbus fields for VMEbus Slave Images are presented in *Table 4-5* on page 4-10.

The Universe II's **eight** VMEbus slave images (0-7) are bounded by A32 space. Slave images 0 and 5 have a 4 KB resolution. Typically, these images would be used as A16 images since they provided the finest granularity. Slave images 1 to 3 and 6 to 8 have a 64 KB resolution. The maximum image size is 4 GB.

Table 4-5. VMEbus Fields for VMEbus Slave Image

Field	Register Bits	Description
base	BS[31:12] or BS[31:16] in VSIx_BS	Multiples of 4 or 64 KBytes (base to bound: maximum of 4 GB)
bound	BD[31:12] or BD[31:16] in VSIx_BD	
address space	VAS in VSIx_CTL	A16, A24, A32, User 1, User 2
mode	SUPER in VSIx_CTL	Supervisor and /or non-privileged
type	PGm in VSIx_CTL	Program and/or data

Warning: The address space of a VMEbus slave image must not overlap with the address space for the Universe II's control and status registers.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

4.3.1.2 PCI Bus Fields

The PCI bus fields specifies the mapping of a VMEbus transaction to the appropriate PCI bus transaction and allows users to translate a VMEbus address to a different address on the PCI bus. The translation of VMEbus transactions beyond 4 GB results in a wrap-around to the low portion of the address range.

Table 4-6. PCI Bus Fields for VMEbus Slave Image

Field	Register Bits	Description
Translation Offset	TO[31:12] or TO[31:16] in VSIx_TO	Offsets VMEbus slave address to a selected PCI address
Address space	LAS in VSIx_CTL	Memory, I/O, Configuration
RMW	LLRMW in VSIx_CTL	RMW enable bit

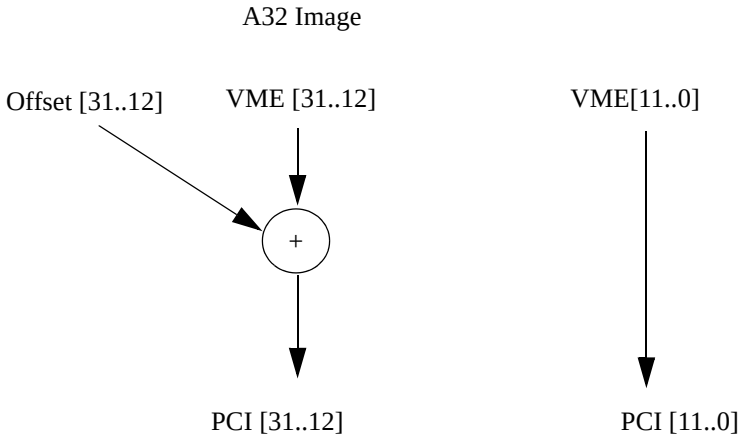


Figure 4-2. Address Translation for VMEbus to PCI Bus Transfers

4.3.1.3 Control Fields

A VMEbus slave image is enabled using the EN bit of the control field. The control field also specifies how reads and writes are processed: either as a coupled transfer or a posted write. At power up, all images are disabled and configured for coupled reads and writes.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Table 4-7. Control Fields for VMEbus Slave Image

Field	Register Bits	Description
image enable	EN in VSIx_CTL	enable bit
posted write	PWEN in VSIx_CTL	posted write enable bit
prefetched read	PREN in VSIx_CTL	prefetched read enable bit
enable PCI64	LD64EN in VSIx_CTL	enables 64-bit PIC bus transactions

Note: For a VMEbus slave image to respond to an incoming cycle, the PCI Master Interface must be enabled (bit BM in the PCI_CSR register).

4.3.2 PCI Bus Target Images

The Universe II accepts accesses from the PCI bus with specific programmed PCI target images that open windows to the VMEbus and control the type of access to the VMEbus. There are eight (0-7) standard PCI target images and one special PCI target image. The special PCI target image may be used for A16 and A24 transaction, freeing the other 8 images for standard A32 transactions.

4.3.2.1 PCI Bus Fields

Decoding for VMEbus accesses is based on the address and command information produced by a PCI bus master. The PCI Target Interface claims a cycle if there is an address match and if the command matches certain criteria.

The PCI target images are A32-capable only. For accesses other than A32 the Special PCI Target Image may be used (refer to Section 4.3.2.4, “Special PCI Target Image,” on page 4-15). Of the eight standard PCI target images, the first and fifth (PCI target images 0 and 4) have a 4KB resolution. PCI target images 1 to 3 and 5 to 7 have a 64-KB resolution.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Table 4-8. PCI Bus Fields for PCI Bus Target Image

Field	Register Bits	Description
base	BS[31:12] or BS[31:16] in LSIx_BS	Multiples of 4 or 64 KBytes (base to bound: maximum of 4 GB)
bound	BD[31:12] or BD[31:16] in LSIx_BD	
address space	LAS in LSIx_CTL	Memory or I/O

Warning: The address space of a PCI bus slave image must not overlap with the address space for the Universe II's control and status registers.

4.3.2.2 VMEbus Fields

The VMEbus fields cause the Universe II to generate the appropriate VMEbus address, AM code, and cycle type, allowing PCI transactions to be mapped to a VMEbus transaction. It is possible to use invalid combinations, such as block transfers in A16 space. This may cause illegal transactions on the VMEbus. All accesses beyond the 4-GB limit will wrap around to the low address range.

.

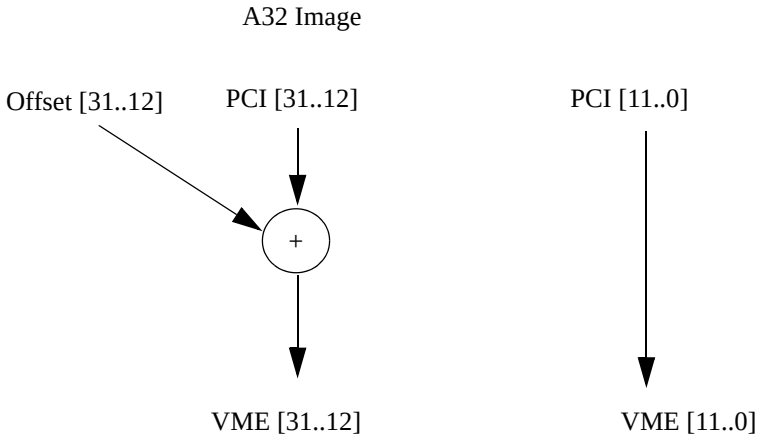


Figure 4-3. Address Translation for PCI Bus to VMEbus Transfers

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Table 4-9. PCI Bus Fields for PCI Bus Target Images

Field	Register Bits	Description
base	BS[31:12] or BS[31:16] in LSIx_BS	Translates PCI Bus Address to VMEbus Address
bound	BD[31:12] or BD[31:16] in LSIx_BD	8, 16, 32, or 64 bits
address space	LAS in LSIx_CTL	A16, A24, A32, User 1, User 2
mode	SUPER in LSIx_CTL	Supervisor or non-privileged
type	PGM in LSIx_CTL	Program or data
cycle	VCT in LSIx_CTL	Single or Block

4.3.2.3 Control Fields

Through the control fields, the user specifies how **writes** are processed and enables a PCI target image. The PCI target image is enabled by setting the EN bit.

Posted **writes** are performed when the PWEN bit is set and the particular PCI target image is accessed. Posted writes are only decoded within PCI Memory space. Access from other memory spaces are performed with coupled cycles, regardless of the setting of the PWEN bit.

Table 4-10. Control Fields for PCI Bus Target Image

Field	Register Bits	Description
image enable	EN in LSIx_CTL	enable bit
posted write	PWEN in LSIx_CTL	posted write enable bit



Note: For a VMEbus slave image to respond to an incoming cycle, the PCI Master Interface must be enabled (bit BM in the PCI_CSR register).

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

4.3.2.4 Special PCI Target Image

A special PCI target image is provided to expedite A16 and A24 transactions. The other eight, standard, PCI target images are typically programmed to access A32 space. The special PCI target image is a 64 MB space, located either within memory or I/O space, that is decoded using PCI address lines [31:26]. Its base address is aligned on 64-MB boundaries and no offsets are provided. Therefore, PCI address information is mapped directly to the VMEbus. The special PCI target image has a lower priority than any other PCI target image.

The 64-MB space is divided into four (4), 16-MB spaces that are selected using AD[25:16]. For each region, the upper 64 KB map to VMEbus A16 space, while the remaining portion map to VMEbus A24 space. The addressing of this slave image is depicted in *Figure 4-2* on page 4-11.

Table 4-11. PCI Bus Fields for Special PCI Bus Target Image

Field	Register Bits	Description
base	BS[05]	64 MB aligned base address for the image
address space	LAS	Places Image in Memory or I/O
maximum data width	VDW	separately set each region for 16 or 32 bits
mode	SUPER	separately set each region for supervisor or non-privileged
type	PGM	Program or data
cycle	VCT	Separately sets each region as program or data

Table 4-12. Control Fields for Special PCI Bus Target Image

Field	Register Bits	Description
image enable	EN	enable bit
posted write	PWEN	posted write enable bit

The special PCI target image register is described *Table 4-13*.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Table 4-13. Special PCI Target Image Register (Offset 188)

Bits	Name	Type	Reset State	Description
31	EN	R/W	0	Image Enable 0 = Disable, 1 = Enable
30	PWEN	R/W	0	Posted Write Enable 0 = Disable, 1 = Enable
29:24	Reserved			
23:20	VDW [3..0]	R/W	0	VMEbus Maximum Datawidth. Each of the four bits specifies a data width for the corresponding 16 MB regions. The lower order bits correspond to the lower order address regions. 0 = 16 bit, 1 = 32 bit
19:16	Reserved			
15:12	PGM [3..0]	R/W	0	Program/Data AM Code Each of the four bits specifies Program/Data AM code for the corresponding 16 mB region. The lower order bits correspond to the lower order address regions. 0 = Data, 1 = Program
11:8	SUPER [3..0]	R/W	0	Supervisor/User AM Code Each of the four bits specifies Supervisor/User AM code for the corresponding 16 MB region. Lower order bits correspond to the lower address regions. 0 = Non-Privileged, 1 = Supervisor
07-02	BS [5..0]	R/W	0	Base Address Specifies a 64 MB aligned base address for this 64 MB image
01	Reserved			
00	LAS	R/W	0	PCI Bus Address Space 0 = PCI Bus Memory Space, 1 = PCI Bus I/O Space

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

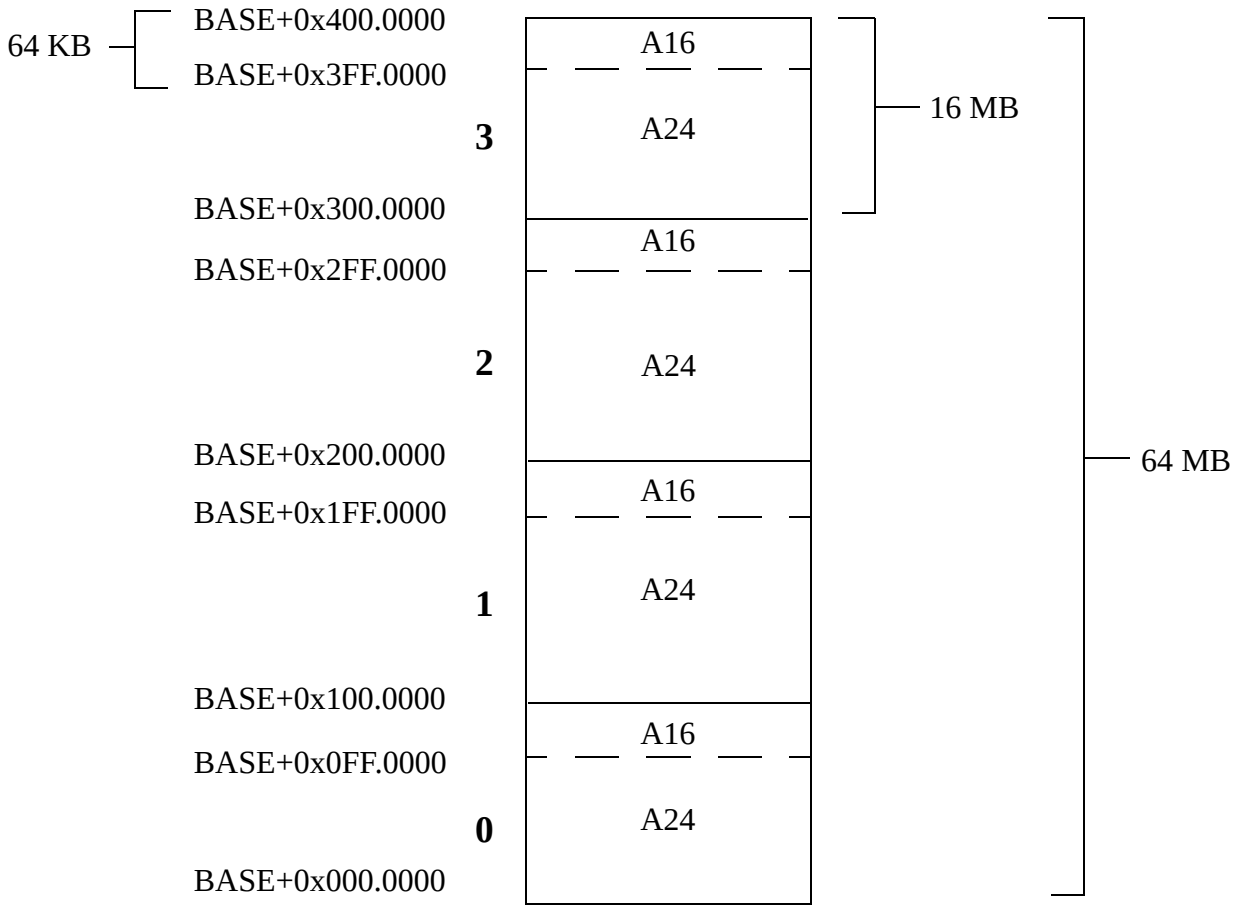


Figure 4-4. Memory Mapping in the Special PCI Target Image

4.4 Universe II's Interrupt and Interrupt Handler

4.4.1 VME and PCI Interrupters

For the VMEbus, the interrupt source can be mapped to any of the VMEbus interrupt output pins such as VIRQ*[7..0]. If a hardware and software source are assigned to the same VMEbus VIRQ*n pin, the software source always has higher priority. Interrupt sources mapped to the PCI bus interrupts are generated via the PCI Interrupt pin, INT*0.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

For the VMEbus interrupt outputs, the Universe II interrupter provides an 8-bit STATUS/ID to a VMEbus interrupt handler. Optionally, the Universe II generates an internal interrupt to signal that the interrupt vector has been provided.

Interrupts mapped to the PCI bus interrupt output pin (INT*0) are serviced by the PCI Interrupt Controller. The UltraSPARC-II*e* determines which interrupt sources are active by reading the interrupt status register in the Universe II. The interrupt is negated after being serviced by the UltraSPARC-II*e*.

4.4.2 VMEbus Interrupt Handling

A VMEbus interrupt causes the Universe II to issue a normal VMEbus IACK cycle and to generate the specified interrupt output. When the IACK cycle is completed, the Universe II relinquishes the VMEbus. The interrupt vector is read by the PCI resource servicing the interrupt output. Hardware and internal interrupts are RORA. Software interrupts are ROAK.

4.4.3 Universe II's Mailbox Registers

Universe II contains four 32-bit mailbox registers that provide an additional communication path between the PCI bus and the VMEbus. The mailboxes support read and write accesses from either bus. They can be enabled to generate interrupts on either bus whenever written to; and are accessed from the same address spaces and in the same method as other Universe II registers.

4.4.4 Universe II's Semaphores

The Universe II contains two general purpose semaphore registers such as SEMA0 and SEMA1; each register contains four semaphores. To obtain the ownership of a semaphore, a processor writes a logic one to the semaphore bit and a unique pattern to the associated tag field; if a subsequent read of the tag field returns the same pattern, then the processor has gained the ownership of the semaphore. In order to release the semaphore, the processor writes a value of 0 to it.

4.4.5 Programmable Slave Images on the VMEbus and PCI bus

There are two types of accesses that the Universe II recognizes on its bus interfaces: accesses for its own register space and accesses destined elsewhere.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

For the VME Slave Images, the Universe II accepts accesses from the VMEbus within specific programmed slave images. Each one of the VMEbus slave images opens a window to the resources on the PCI bus, and through the specific attributes, the VMEbus slave images allow the user to control the type of access to the PCI resources. The VMEbus slave images are divided into VMEbus, PCI bus, and Control fields (refer to Section 4.3, "Slave Image Programming," on page 4-9).

For the PCI Slave Images, the Universe II accepts accesses from the PCI bus with the specific programmed PCI target images. Each one of the PCI bus slave images opens a window to the resources on the VMEbus, and it allows the user to control the type of access to the VMEbus resources. The PCI bus slave images are divided into VMEbus, PCI bus, and control fields. There is one special PCI target image that is separate from the VMEbus, PCI bus, and the control fields (refer to Section 4.3, "Slave Image Programming," on page 4-9).

4.4.6 DMA Controller

The Universe II utilizes an internal DMA controller for high performance data transfer between the VMEbus and the PCI bus. Universe II's parameters for the DMA transfer are software configurable. DMA operations between the source and destination bus are decoupled via the use of a single bidirectional FIFO (DMAFIFO).

There are two modes of operation for the DMA: Linked List Mode and Direct Mode. In Linked List Mode, the Universe II loads the DMA registers from PCI memory and executes the transfers described by these registers. In the direct mode, the PCI master directly programs the DMA registers.

The DMA controller also utilizes the command packet. A command packet is a block of DMA registers stored in PCI memory. A command packet may be linked to another command packet so that when the DMA has finished the operations described by one command packet, the DMA controller can automatically move on to the next command packet in the linked-list of command packets (refer to "DMA Controller" on page 2-77 of the *Universe II User's Manual*).

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Operation Section

Chapter 5

Programmable Logic Device

5.1 Introduction

The Programmable Logic Device or PLD resides on the Ebus of the Sun Rio I/O Controller on the USPII*e*-USB Baseboard (see *Figure 2-1* on page 2-2). It provides the following functions:

- Implements the reset logic of the USPII*e*-USB
- Implements an extensive boot address decoder and mapping control of the flashes
- Provides miscellaneous registers to control the behavior of the USPII*e*-USB
- Implements a 2-level Watchdog
- Implements power management and thermal management
- Implements miscellaneous features like:
  - **a.** VME slot-ID detection
  - **b.** VME sysreset management

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

5.2 Flash Mapping and Boot Control

Flash mapping is controlled by Jumper Pins JP2701, JP2702, and JP2703 (see *Table B-1* on page B-3).

Write accesses to the Flash memory can be enabled or disabled using Jumper Pins JP2201, JP2202, and JP2203.

Selection of the boot device (FLASH0, FLASH1, FLASH2, or ROMBO connector) is controlled by the combined settings of Jumper Pins JP2201 and JP2202 (see *Table B-4* on page B-5).

5.3 PLD registers

The PLD implements the following registers:

Table 5-1. PLD Register Address Map

Register	Register Name	Offset Address	Description
0	pld_rev	0x1FF.F120.0000	Revision and ID of the base_Usp2e_PLD
1	flash_status	0x1FF.F120.0002	Boot address space mapping
2	vme_slot_id	0x1FF.F120.0003	Usp2e VME id status register
3	vme_reset_mode	0x1FF.F120.0004	Usp2e VME sysreset/system controller setting
4	patch_status	0x1FF.F120.0005	OBP patch setting
5	EBus_CS_MUX	0x1FF.F120.0006	EBus CS signal selection
6	Voltage_status	0x1FF.F120.0007	Voltage status
7	TTY/KBM_config	0x1FF.F120.0008	TTY ports and Keyboard/Mouse setting (Front panel versus P2)
8	SCSI_A_STATUS	0x1FF.F120.0009	SCSI-A termination setting and status
9	misc	0x1FF.F120.000a	User LED, soft alarm, and thermal shutdown.
10	watchdog 1 counter	0x1FF.F120.0010	Watchdog 1 counter loaded value
11	watchdog 1 Limit	0x1FF.F120.0014	Watchdog 1 limiter loaded value

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Table 5-1. PLD Register Address Map (Continued)

Register	Register Name	Offset Address	Description
12	watchdog 1 status	0x1FF.F120.0018	Watchdog 1 status
13	watchdog 2 counter	0x1FF.F120.0020	Watchdog 2 counter loaded value
14	watchdog 2 Limit	0x1FF.F120.0024	Watchdog 2 limiter loaded value
15	watchdog 2 status	0x1FF.F120.0028	Watchdog 2 status
16	watchdog int mask	0x1FF.F120.0040	Watchdog interrupt mask
17	semaphore status	0x1FF.F120.00F0	Semaphore status and requester flag
18	semaphore request1	0x1FF.F120.00F1	requester1's image of semaphore
19	semaphore request2	0x1FF.F120.00F2	requester2's image of semaphore
20	semaphore request3	0x1FF.F120.00F3	requester3's image of semaphore
21	semaphore request4	0x1FF.F120.00F4	requester4's image of semaphore
22	semaphore request5	0x1FF.F120.00F5	requester5's image of semaphore
23	semaphore request6	0x1FF.F120.00F6	requester6's image of semaphore
24	semaphore request7	0x1FF.F120.00F7	requester7's image of semaphore

5.4 2-Level Watchdog

A 2-level watchdog is implemented in the PLD. The states of the watchdog are "normal", "warning", "coping", and "failed." Each watchdog may be programmed to expire within the range of 0.1 seconds to approximately 6500 seconds and contains a 16-bit counter register, a 16-bit limit register, and an 8-bit status register. The counter register and the status register are read-only while the limit register is read/write. Refer to the *USPIIe-USB Software Manual* for a description of the Watchdog Registers.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com



Note: The 2-level watchdog implemented in the PLD is entirely separate from the internal watchdog of the UltraSPARC-II*e*. For more information on the watchdog implemented in the UltraSPARC-II*e* refer to the UltraSPARC-II*e User's Manual*, published by SUN Microelectronics (SME).

When no watchdogs have expired, the USPII*e*-USB is in a "normal" state. When the level 1 watchdog expires, a maskable interrupt is sent to the Ichip. The USPII*e*-USB is considered to be in a "warning" state. Upon expiration, the level-2 watchdog issues a non-maskable power-on-reset (POR) interrupt to the UltraSPARC-IIe processor. This signal has the same effect as an "Abort" button assertion and will terminate the active job. When this occurs, the board is considered to be in a "coping" state.

Upon expiration, a higher-order watchdog will reset a lower-order watchdog; i.e., the expiration of watchdog 2 resets watchdog 1 to its initial programmed state.

5.5 Power management

The USPII*e*-USB uses several voltage sources in order to operate. 5V, 3.3V, and Vdd-core (CPU) are monitored by the SMS44 voltage monitor/controller, which generates a `power-ok` signal to the PLD only if the three voltage sources are within tolerance.

If the CPU temperature shutdown option is enabled (PLD control-register 10 and SB 2702), the Vdd-core power supply can be shut down by the PLD when the CPU junction temperature exceeds the preset limit. By setting the appropriate bit in the PLD control register, software can also shut down the Vdd-core power supply.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

5.6 Temperature management

The PLD is involved in the temperature management of the board, although an external temperature monitor IC chip is used.

The temperature sensor/monitor is composed of the I^2C W83782D connected to a sensor (DIODE) located in the UltraSPARC-II*e* CPU. A temperature threshold can be defined by software. If the CPU junction temperature exceeds the programmed thresholds, W83782D generates an over-temperature indicator signal to the PLD.

If the CPU thermal shutdown option is enabled, the PLD will generate an over-temperature interrupt to the Ichip, assert a `hi-temp-trip` signal to the VME P2 bus, and turn off CPU core power.

[See *USPIIe*-USB *Software Manual*, Chapter 3, "Temperature Monitoring", for more details.]

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Operation Section

Chapter 6

Resets

6.1 Overview

This chapter presents a brief discussion of the reset structure of the USPII*e*-USB. The various types of resets, some possible reset sources, and reset effects are explained.

Resets are used to force all or part of the system into a known state. A Reset is defined as any action or signal that places the UltraSPARC-II*e* in Reset, Error, or Debug State (RED_State). This state will be entered under any of the following conditions:

- A Trap is taken when:
  - — Trap_Level = Max_Trap_Level - 1
- One of the reset request signals (POR, XIR, WDR) becomes active
- A reset request, SIR, is issued when the Trap_Level < Max_Trap_Level (if Trap_Level = Max_Trap_Level, the UltraSPARC-II*e* enters an error_state)
- *Internal_processor_error* exception or *catastrophic_error exception* occurs
- The setting of PSTATE.RED by system software

The RED_state is indicated by the PSTATE.RED bit being set. For more information on the RED_state consult Section 17.3, RED_state, of the *UltraSPARC-IIe User's Manual*, published by Sun Microsystems.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

The USPII*e*-USB reset tree uses the UltraSPARC-II*e* CPU in conjunction with the power monitor (SMS44), PLD, and the Universe II VMEbus Interface ASIC. The PLD receives the `power-ok` signal from the SMS44, and receives input from the push-button reset to set the `B_POR` bit in the `reset_control_register` (*Table 6-1* on page 6-6). When any of the system voltages are out of their preset ranges, `power_ok` will be deasserted, which in turn will place the UltraSPARC-II*e* and the system in a reset state until all voltages are with their specified ranges.

The PLD also receives input from the Push-Button `Reset`. When the PLD receives this signal it issues a Push-Button POR (Power-On-Reset) to the UltraSPARC-II*e*. The UltraSPARC-II*e* will then place the system in a reset state.

The system, or part of the system, may also be reset by a Watchdog Reset (WDR) or a Software-Initiated Reset (SIR). These resets originate within the UltraSPARC-II*e* core and are only observed by the processor core. Depending on the conditions and type of reset, the processor may propagate the reset throughout the system (as in the case of a POR) or reset part of the system; i.e., the processor core itself.



Note: Unlike other UltraSPARC-based systems, the UltraSPARC-II*e* does not support a wake-up reset for power management.

6.2 UltraSPARC-IIe Reset Request Signals

The reset request signals accepted by the UltraSPARC-II*e* on the USPII*e*-USB board are explained in this section. The signals are: System_Reset and Power-On Reset (POR), initiated when power is applied to the system or when a systemwide reset is needed; Externally Initiated Reset (XIR), initiated in response to a signal external to the UltraSPARC-II*e* processor generally indicating a critical system event; Watchdog Reset (WDR), initiated in response to the error_state; and Software Initiated Reset (SIR), initiated by software with the SIR command.

System_Reset, POR, and XIR are received by the UltraSPARC-II*e* from the PLD, while WDR and SIR are internally generated by the UltraSPARC-II*e* and affect only the processor core. Reset priorities, from highest to lowest are: System_Reset and POR, XIR, WDR, and SIR.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

6.2.1 System_Reset and P-Reset

System_Reset (Power-On Reset) input or P(ushbutton)-Reset input to the UltraSPARC-II*e* CPU is a Power-On Reset (POR) for processor and board reset. When POR is active, all other resets and traps are ignored. POR initiates the power-on sequence of the processor and firmware.

The UltraSPARC-II*e* CPU will propagate this reset to all of the subsystems of the USPII*e*-USB, through the Intel 21154 PCI Bridge and through the Advanced PCI Bridge (APB) to all other devices connected to the secondary side of the PCI bridges.

6.2.2 Externally Initiated Reset (XIR)

An XIR has a higher priority than all other resets except System_Reset and POR, and is initiated by a source external to the UltraSPARC-II*e*, such as an external component. It does *not* propagate a reset outside the CPU.

XIR does not cause a systemwide reset. It preserves the existing state of all registers on the board with the exception of UltraSPARC-II*e* registers. If the UltraSPARC-II*e* is in an error_state, XIR brings it to a RED_state.

6.2.3 Watchdog Reset (WDR)

On the USPII*e*-USB, a Watchdog Reset (WDR) is generated in response to the error_state of the UltraSPARC-II*e*. It is generated internally to the UltraSPARC-II*e* core. The UltraSPARC-II*e* will enter an error_state when a trap occurs and Trap_Level = Max_Trap_Level - 1. A WDR performs a system reset; all pending and in-progress hardware operations are cancelled or aborted. Hardware and firmware registers are unchanged from before the WDR occurred, but may be in an inconsistent state as some operations have been aborted. If the processor is in error_state, a WDR places it in RED_state.

Note that a WDR initiated internal to the processor is different than the 2-Level Watchdog implemented in the PLD of the USPII*e*-USB. For further explanation of the 2-Level Watchdog, see Section 6.3.4, “2-Level Watchdog Resets,” on page 6-5.

6.2.4 Software Initiated Reset (SIR)

A Software Initiated Reset (SIR) is initiated by an SIR instruction from supervisory software. It is initiated within the UltraSPARC-II*e* core itself and affects only the UltraSPARC-II*e*. An SIR is not propagated to the I/O or external system.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

6.3 Reset Sources

The UltraSPARC-II*e* accepts three reset signals from the PLD: System_Reset, P-Reset, and XIR. System_Reset, P-Reset, and POR propagate from the processor to the entire board. XIR does not propagate outside the processor.

POR can be generated from the push-button on the front panel, from on-board power management, from VMEbus reset, and from a 2-Level Watchdog reset. POR can also be initiated by software.

XIR can be generated from Level-2 Watchdog or initiated by software.

6.3.1 Push-Button Reset

Push-Button Reset is activated by pressing the push-button on the front panel of the USPII*e*-USB. This activates the Push_Button_POR input to the PLD, which propagates the signal as a POR to the UltraSPARC-II*e*, which then resets the processor and board. When a Push-Button Reset is initiated, the B_POR in the Reset_Control_Register (*Table 6-1* on page 6-6) will be set until software clears it. This is done to allow software to detect the source of the reset. The POR bit will not be set.

6.3.2 Power Management Resets

The on-board power management system, in conjunction with the PLD, generates a POR for the USPII*e*-USB during the power-on period. The power-management circuitry continuously monitors the 5V, 3.3V, and CPU Vdd-core voltages. If any voltage source (1.7V, 3.3V, or 5V) drops below the preset value (typically 10-percent below nominal value), the `power-ok` input to the PLD will be deasserted, generating a POR that resets the processor and the board.

6.3.3 VMEbus Resets

A system reset from the VMEbus is received by the Universe II ASIC through the VME P1 bus connector. The Universe II asserts LOCAL_RESET to the PLD (this depends on the setting in the PLD `vme_reset_mode` control register; see *Table 5-1* on page 5-2). If the incoming VME system reset is allowed to reset the USPII*e*-USB system, the PLD may assert `sys_reset` to the CPU, which propagates a reset to the entire board.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

An incoming VMEbus reset may be enabled or disabled through the setting of jumper **JP1601**. If JP1601 is ON, the USPII*e*-USB can see the reset from the VMEbus. If JP1601 is OFF or left open, resets from the VMEbus will be ignored. The incoming `VMESYS` reset is controlled further by the `vme_reset_mode` control register in the PLD.

Outgoing VMEbus resets may also be enabled and disabled by setting jumper **JP1501**. If JP1501 is ON, a reset of the USPII*e*-USB will be propagated from the Universe II distributed to the VMEbus. If JP1501 is OFF or left open, a reset of the USPII*e*-USB will not be propagated to the VMEbus.

Software may initiate a VMEbus Reset by writing to the `VME_Software_Reset` address located at 0x1FF.F110.0001. A software VMEbus reset will reset only the VMEbus. No components on the USPII*e*-USB are effected by a software VMEbus reset.

6.3.4 2-Level Watchdog Resets

A 2-Level Watchdog reset, as explained in Section 5.4 on page 5-3, is implemented in the PLD. When the second watchdog in the PLD expires, the PLD asserts a POR to the UltraSPARC-II*e*. This signal initiates a POR in the processor, which propagates throughout the system.



Note: This 2-Level Watchdog is different from a Watchdog implemented internally on the UltraSPARC-II*e*. Refer to “Watchdog Reset (WDR)”, page 6-3, for more information concerning the Watchdog Reset implemented internally on the UltraSPARC-II*e*.

6.3.5 Software POR

Software may initiate a reset equivalent to a Power-On-Reset (POR) by setting the SOFT_POR bit in the UltraSPARC-II*e* Reset_Control Register (see *Table 6-1* on page 6-6). This bit will remain set until the software clears it, to allow software to detect the source of the reset.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

6.3.6 Software XIR

Software may initiate a reset equivalent to an Externally-Initiated-Reset (XIR) by setting the SOFT_XIR bit in the UltraSPARC-II*e* Reset_Control Register (*Table 6-1* below). This bit will remain set until software clears it, to allow software to detect the source of the reset.

6.4 UltraSPARC-IIe Reset_Control_Register

The UltraSPARC-II*e* `reset_control_register` indicates the source of a reset and provides control of software reset generation. It is located at 0x1FE.0000.F020.



Note: Internal to the UltraSPARC-II*e* are the Watch Dog Reset (WDR) and Software Initiated Reset (SIR). These two resets are initiated within the processor core and affect only the processor.

Table 6-1. UltraSPARC-IIe Reset_Control_Register

Field	Bits	Value	Description	Type
Reserved	63:32	0	Reserved	R0
POR	31	*[a]	Set if the last reset was due to the assertion of SYS_RESET_L	R/W1C
SOFT_POR	30	*	Setting to 1 causes a POR reset; stays set until software clears it	R/W
SOFT_XIR	29	*	Setting to 1 causes an XIR trap; stays set until software clears it	R/W
B_POR	28	*	Set if the last reset was due to the assertion of P_RESET_L	R/W1C
B_XIR	27	*	Set if the last reset was due to the assertion of an X_Reset_L	R/W1C
Reserved	26:0	*	Reserved	R0

a—The highest priority reset source has its bit set. Only the bits marked with "*" are set.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Appendix A

Connector Pinouts, LEDs, Switches

This appendix provides connector pinouts for the user interfaces on the USPII*e*-USB as well as descriptions of LEDs and switches. The Baseboard, PMC Carrier Board, Paddle Boards (Standard and Multiple I/O), and Memory Module connector pinouts are each presented as individual sections. For a diagram of the Front Panel I/O available on each board, refer to Appendix C, “Front Panel Diagrams”.

A.1 Baseboard VME P1

- Connector Type: 5-row VME64 (see *Figure A-1* and *Table A-1*, page -2)

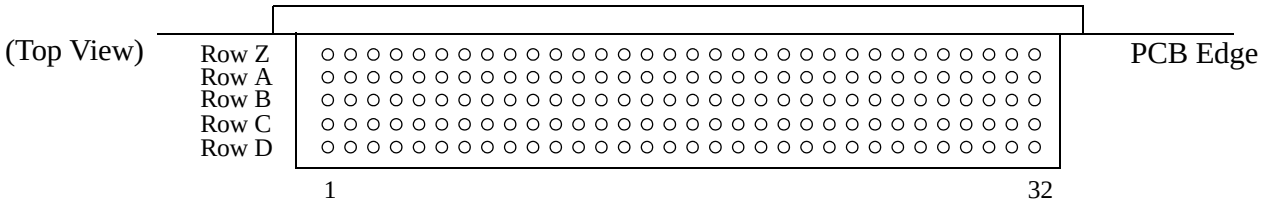


Figure A-1. Baseboard VME P1 Connector Orientation

Note: In *Table A-1*
- an **asterisk** (*) indicates active low
- **(–)** and **(+)** indicate one member of a signal pair
- A **(1)** indicates pins that are defined in the VME64*x* specification, but not used
- A **(2)** indicates pins that are reserved in the VME64*x* specification, but not used

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Table A-1. Baseboard VME P1 Pinouts

Pin	Row Z Signal	Row A Signal	Row B Signal	Row C Signal	Row D Signal
1	MPR (1)	VME D00	VME BBSY	VME D08	VCC
2	GND	VME D01	VME BCLR	VME D09	GND
3	MCLK (1)	VME D02	VME ACFAIL	VME D10	+V1(1)
4	GND	VME D03	VME BGIN0	VME D11	+V2(1)
5	MSD (1)	VME D04	VME BGOUT0	VME D12	Reserved(2)
6	GND	VME D05	VME BGIN1	VME D13	-V1(1)
7	MMD (1)	VME D06	VME BGOUT1	VME D14	-V2(1)
8	GND	VME D07	VME BGIN2	VME D15	Reserved(2)
9	MCTL (1)	GND	VME BGOUT2	GND	GAP*
10	GND	VME SYSCLK	VME BGIN3	VME SYSFAIL	GA0*
11	RESP* (1)	GND	VME BGOUT3	VME BERR	GA1*
12	GND	VME DS1	VME BR0	VME SYSRESET	+3.3V(1)
13	Reserved (2)	VME DS0	VME BR1	VME WORD	GA2*
14	GND	VME WRITE	VME BR2	VME AM5	+3.3V(1)
15	Reserved (2)	GND	VME BR3	VME A23	GA3*
16	GND	VME DTACK	VME AM0	VME A22	+3.3V(1)
17	Reserved (2)	GND	VME AM1	VME A21	GA4*
18	GND	VME AS	VME AM2	VME A20	+3.3V(1)
19	Reserved (2)	GND	VME AM3	VME A19	Reserved (2)
20	GND	VME IACK	GND	VME A18	+3.3V(1)
21	Reserved (2)	VME IACKIN	Not Connected	VME A17	Reserved (2)
22	GND	VME IACKOUT	Not Connected	VME A16	+3.3V(1)
23	Reserved (2)	VME AM04	GND	VME A15	Reserved (2)
24	GND	VME A07	VME IRQ7	VME A14	+3.3V(1)
25	Reserved (2)	VME A06	VME IRQ6	VME A13	Reserved (2)
26	GND	VME A05	VME IRQ5	VME A12	+3.3V(1)
27	Reserved (2)	VME A04	VME IRQ4	VME A11	LI/I*(1)
28	GND	VME A03	VME IRQ3	VME A10	+3.3V(1)
29	Reserved (2)	VME A02	VME IRQ2	VME A09	LI/O*(1)
30	GND	VME A01	VME IRQ1	VME A08	+3.3V(1)
31	Reserved (2)	-12V	Not Connected	+12V	GND
32	GND	VCC	VCC	VCC	VCC

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

A.2 Baseboard VME P2

Serial Port A (TTYA), Serial Port B (TTYB), Serial Port C (TTYC), Serial Port D (TTYD), parallel port, SCSI Port A, and alarm signals are routed to the Baseboard VME P2 backplane (see *Figure A-2* and *Table A-2* on page A-4).

Note: In *Table A-2*,

- an **asterisk** (*) indicates an active low
- **(–)** and **(+)** indicate one member of a signal pair
- a **thick border** groups associated signals
- A **(1)** indicates pins that are defined in the VME64*x* specification, but not used
- A **(2)** indicates pins that are reserved in the VME64*x* specification, but not used

Additional VME P2 pinouts vary with the board configuration: Refer to Section 1.1, “Determine Board Type,” on page 1-1.

VME P2 also contains 3 unbuffered, active low, alarm output signals:

— POWER FAIL: Asserted on Power Failure

— HI TEMP: Asserted when critical temperature is reached

— SW ALARM: User-defined. Asserted on a write access to address 0x1ff.f110.0000. Refer to the USPII*e*-USB Software Manual.

The VME P2 is a VME64 connector type.

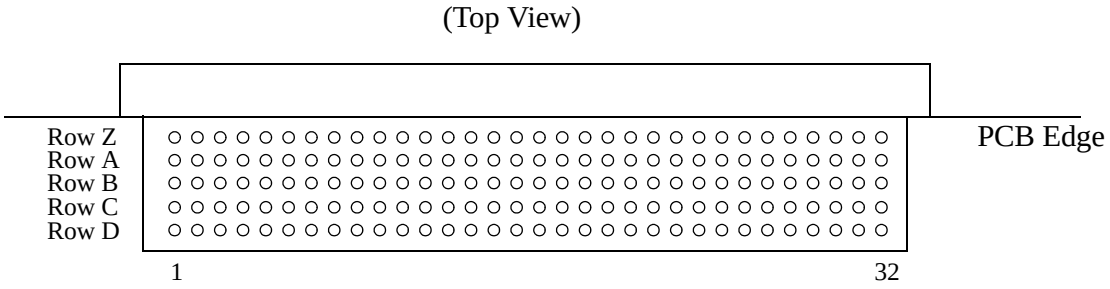


Figure A-2. Baseboard VME P2 Connector Orientation

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Table A-2. Baseboard VME P2 Connector Pinouts

Pin	Row Z Signal	Row A Signal	Row B Signal	Row C Signal	Row D Signal
1	**LP_Data7**	VCC	VCC	VCC	**LP_AFXN***
2	GND	**AC97_RST_L**	GND	**SCSI_P2-SENSING**[a]	**LP_PAPER_EMPTY**
3	**LP_Data6**	**AC97_SYNC_P2**	VME_RETRY(1)	**TermPwr**	**SCSI-DIFF-SENSE**
4	GND	**AC97_BCLK_P2**	VME_A[24]	**SCSI_A_ATN(–)**	**SCSI_A_ATN(+)**
5	**LP_Data5**	**AC97_DIN_P2**	VME_A[25]	**SCSI_A_BUSY(–)**	**SCSI_A_BUSY(+)**
6	GND	**AC97_DOUT_P2**	VME_A[26]	**SCSI_A_ACK(–)**	**SCSI_A_ACK(+)**
7	**LP_Data4**	**USB2_D_P**	VME_A[27]	**SCSI_A_RST(–)**	**SCSI_A_RST(+)**
8	GND	**USB2_D_N**	VME_A[28]	**SCSI_A_MSG(–)**	**SCSI_A_MSG(+)**
9	**LP_Data3**	GND	VME_A[29]	**SCSI_A_SEL(–)**	**SCSI_A_SEL(+)**
10	GND	**PS2_KB_CLK_P2**	VME_A[30]	**SCSI_A_CD(–)**	**SCSI_A_CD(+)**
11	**LP_Data2**	**PS2_KB_D_P2**	VME_A[31]	**SCSI_A_REQ(–)**	**SCSI_A_REQ(+)**
12	GND	**PS2_MS_CLK_P2**	GND	**SCSI_A_IO(–)**	**SCSI_A_IO(+)**
13	**LP_Data1**	**PS2_MS_D_P2**	VCC	**SCSI_A_D[0](–)**	**SCSI_A_D[0](+)**
14	GND	**SSER_TXD_C_P2**	VME_D[16]	**SCSI_A_D[1](–)**	**SCSI_A_D[1](+)**
15	**LP_Data0**	**SSER_RXD_C_P2**	VME_D[17]	**SCSI_A_D[2](–)**	**SCSI_A_D[2](+)**
16	GND	**SSER_TXD_D_P2**	VME_D[18]	**SCSI_A_D[3](–)**	**SCSI_A_D[3](+)**
17	**LP_Busy***	**SSER_RXD_D_P2**	VME_D[19]	**SCSI_A_D[4](–)**	**SCSI_A_D[4](+)**
18	GND	**SSER_TXD_A_P2**	VME_D[20]	**SCSI_A_D[5](–)**	**SCSI_A_D[5](+)**
19	**LP_ack***	**SSER_RXD_A_P2**	VME_D[21]	**SCSI_A_D[6](–)**	**SCSI_A_D[6](+)**
20	GND	**SSER_TXD_B_P2**	VME_D[22]	**SCSI_A_D[7](–)**	**SCSI_A_D[7](+)**
21	**LP_Init***	**SSER_RXD_B_P2**	VME_D[23]	**SCSI_A_PAR[0](–)**	**SCSI_A_PAR[0](+)**
22	GND	**SSER_CTS_B_P2**	GND	**SCSI_A_D[8](–)**	**SCSI_A_D[8](+)**
23	**LP_Error***	**SSER_RTS_B_P2**	VME_D[24]	**SCSI_A_D[9](–)**	**SCSI_A_D[9](+)**
24	GND	**SSER_DTR_B_P2**	VME_D[25]	**SCSI_A_D[10](–)**	**SCSI_A_D[10](+)**
25		**SSER_DCD_B_P2**	VME_D[26]	**SCSI_A_D[11](–)**	**SCSI_A_D[11](+)**
26	GND	**SSER_DSR_B_P2**	VME_D[27]	**SCSI_A_D[12](–)**	**SCSI_A_D[12](+)**
27		**SSER_RI_B_P2**	VME_D[28]	**SCSI_A_D[13](–)**	**SCSI_A_D[13](+)**
28	GND	Pwr_Fail/ **PP_Select_In_L**	VME_D[29]	**SCSI_A_D[14](–)**	**SCSI_A_D[14](+)**
29		Hi_Temp_Trip/**PP_Select**	VME_D[30]	**SCSI_A_D[15](–)**	**SCSI_A_D[15](+)**
30	GND	Sw_alarm/ **PP_Strobe***	VME_D[31]	**SCSI_A_PAR[1](–)**	**SCSI_A_PAR[1](+)**
31		GND	GND	VCC	GND
32	GND	VCC	VCC	VCC	VCC

a—SCSI_P2-SENSING is part of the automatic SCSI termination logic; the SCSI A P2 signal will be forced to ground by the mating SCSI connector when attached. This will disable the active onboard SCSI terminator on the P2 side.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

A.3 Baseboard

A.3.1 SCSI A and B

- Connector Type: Honda Dual SCSI-2 (80 MB/sec) Connector, 68 Pin, 0.8 mm Pitch
- Connector Part Number: HDRA-E68WILFDT-IEC-SL

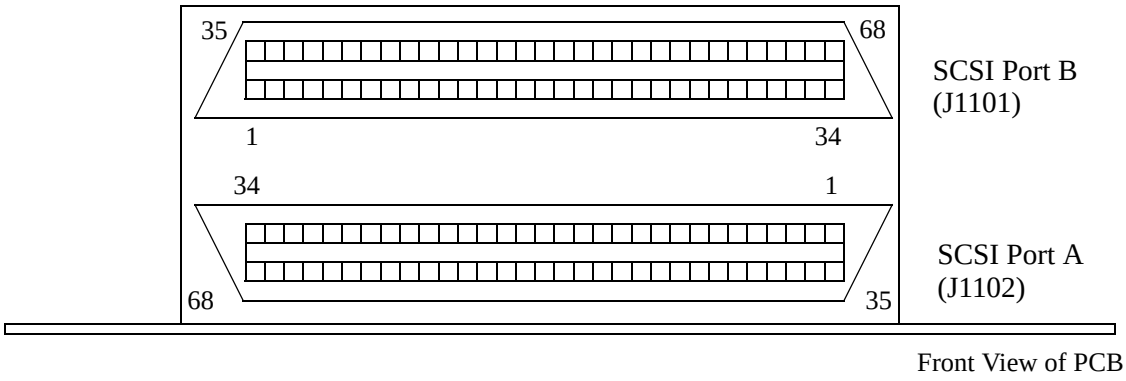


Figure A-3. Baseboard SCSI A and B Connector Orientation

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Table A-3. SCSI Ports A and B Connector Pin Signals

Pin	Signal	Description	Pin	Signal	Description
1	+DB(12)	+ Data 12	35	–DB(12)	–Data 12
2	+DB(13)	+ Data 13	36	–DB(13)	–Data 13
3	+DB(14)	+ Data 14	37	–DB(14)	–Data 14
4	+DB(15)	+ Data 15	38	–DB(15)	–Data 15
5	+DB(P1)	+ Parity 1	39	–DB(P1)	–Parity 1
6	+DB(0)	+ Data 0	40	–DB(0)	–Data 0
7	+DB(1)	+ Data 1	41	–DB(1)	–Data 1
8	+DB(2)	+ Data 2	42	–DB(2)	–Data 2
9	+DB(3)	+ Data 3	43	–DB(3)	–Data 3
10	+DB(4)	+ Data 4	44	–DB(4)	–Data 4
11	+DB(5)	+ Data 5	45	–DB(5)	–Data 5
12	+DB(6)	+ Data 6	46	–DB(6)	–Data 6
13	+DB(7)	+ Data 7	47	–DB(7)	–Data 7
14	+DB(P0)	+ Parity 0	48	–DB(P0)	–Parity 0
15	GND	Ground	49	GND	Ground
16	Diff Sense	Sense Differential	50	GND	Ground
17	TermPower	Termination Power	51	TermPower	Termination Power
18	TermPower	Termination Power	52	TermPower	Termination Power
19	Open	*Not Connected*	53	Open	*Not Connected*
20	SCSI Sense	Sense Cable	54	GND	Ground
21	+ATN	+ Attention	55	–ATN	–Attention
22	GND	Ground	56	GND	Ground
23	+BSY	+ Busy	57	–BSY	–Busy
24	+ACK	+ Acknowledge	58	–ACK	–Acknowledge
25	+RST	+ Reset	59	–RST	–Reset
26	+MSG	+ Message	60	–MSG	–Message
27	+SEL	+ Select	61	–SEL	–Select
28	+CD	+ Command	62	–CD	–Command
29	+REQ	+ Request	63	–REQ	–Request
30	+I/O	+ Input/Output	64	–I/O	–Input/Output
31	+DB(8)	+ Data 8	65	–DB(8)	–Data 8
32	+DB(9)	+ Data 9	66	–DB(9)	–Data 9
33	+DB(10)	+ Data 10	67	–DB(10)	–Data 10
34	+DB(11)	+ Data 11	68	–DB(11)	–Data 11

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

A.3.2 Ethernet Port A

- Connector Type: RJ45 TPE
- Connector Part Number: STEWART-SS-6488S-A-NF

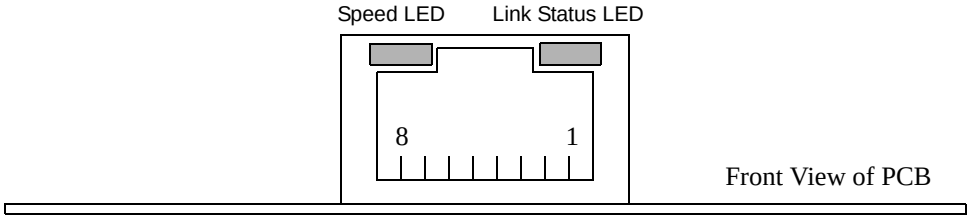


Figure A-4. Ethernet A Connector Orientation

Table A-4. RJ45 Ethernet A Pinout

Pin	Signal Name
1	TXD+
2	TXD-
3	RXD+
4	TXGND
5	TXGND
6	RXD-
7	RXGND
8	RXGND

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

A.3.3 Combination PS/2–USB Connector

- Connector Type: 8-Pin Mini-DIN
- Connector Part Number: AMP-749179-1

The mini-DIN-8 connector (marked **KEYBD/MOUSE**) on the Baseboard front panel supports both a PS/2 keyboard/mouse port and dual USB (USB-0, USB-1) ports. Either option is selected by configuring five solder beads (SB3502 through SB3506; see *Table 1-2* on page 1-3 in Chapter 1, "USPIIe-USB Installation", and *Table B-6* on page B-9, Appendix B, ”DIP-Switch, Jumper-Pin, and Solder-Bead Configurations”).

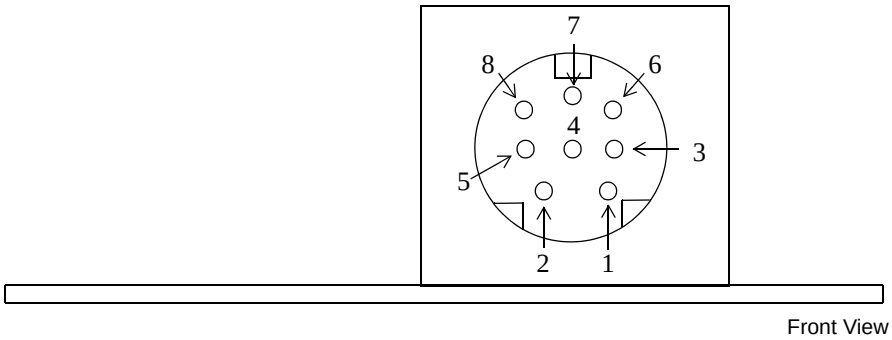


Figure A-5. Front-Panel Mini-DIN Connector

Table A-5. 8-Pin Mini-DIN/PS/2–USB Pinouts

Pin	USB Signal[a]	PS/2 KB/M Signal[a]
1	GND	GND
2	GND	GND
3	VCC	VCC
4	USB1_D_P (USB-1	PS2_MS_DAT 18
5	USB1_D_N (USB-1)	PS2_KBD_CLK 18
6	USB0_D_P (USB-0)	PS2_KBD_DAT 18
7	USB0_D_N (USB-0)	PS2_MS_CLK 18
8	VCC	VCC

a—Signals are dependant on SB3503–SB3506 settings (see *Table B-6*, page B-9).

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

A.3.4 Serial Port A (RS232) and B (RS232/422)

Caution: Note the location of **pin 1** on this port. Connectors must match wires to pin numbers called out in *Figure A-6* and *Table A-6*, below.

- Connector: 2 stacked Micro-DB15
- Part No.: ITT-MDS30PE-Z10-VR22

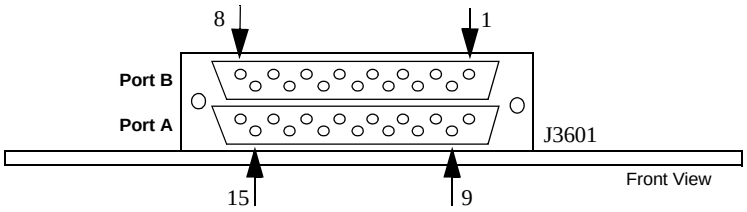


Figure A-6. Front-Panel Serial Ports A and B

Table A-6. Serial Port A and B Connector Pinouts[a]

PC board is marked:	Port A Pin[b]	Signal Name: Port A (RS232)	Signal Name: Port B (RS232/422)	Port B Pin[b]	*PC board is marked:*
B1	1	NC	RTS_B_P	1	**A1**
	2	NC	RXD_B_P	2	
	3	NC	TXD_B_P	3	
	4	GND	GND	4	
	5	**A_DTR_FP**	*DTR_B_N*	5	
	6	**A_TXD_FP**	*TXD_B_N*	6	
	7	**A_RXD_FP**	*RXD_B_N*	7	
B8	8	**A_DCD_FP**	*DCD_B_N*	8	**A8**
B9	9	NC	CTS_B_P	9	**A9**
	10	NC	DTR_B_P	10	
	11	NC	DCD_B_P	11	
	12	NC	NC	12	
	13	**A_CTS_FP**	*CTS_B_N*	13	
	14	**A_RTS_FP**	*RTS_B_N*	14	
B15	15	NC	NC	15	**A15**

a—Boldface signals are used for RS232 Port A; italic signals are used for RS232 Port B. At the end of the signal code, N = negative and P = positive.

b—***Important:*** The A and B associated with Serial Port connector pins on PC boards (Rev **Y** and Rev **B**) should not be confused with corresponding Serial Ports A and B. Port A pins are marked with a B instead of an A. Port B pins are marked with an A instead of a B.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

A.3.5 PMC Module Slot 0

PMC Module slot 0 has no I/O through the VME P2 connector of the Baseboard. The Baseboard connector used for installation is shown in *Figure A-7*.

- Connector Type: 64 Pin, Female, 10mm, Dual Row
- Connector Manufacturer: AMP
- Manufacturer's Part Number: 120528-1

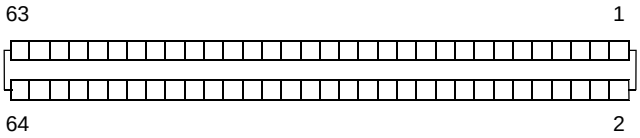


Figure A-7. PMC Module Slot 0 Connector

A.3.6 LEDs

The following LEDs are located on the Front Panel of the Baseboard (see Appendix C, "Front Panel Diagrams"):

- VME Status LEDs: Reset, Fail, VME Master, and VME Slave
- System Status LEDs: User, Shutdown, Power OK, and Enable

Table A-7. Color Interpretation of Front-Panel LEDs

Type	LED	Color	Type	Interpretation
VME Status	Reset	Red	Static	• VME system reset
	Fail	Orange	Static	• VME system failure
	Master [a]	Yellow	Static	• Master VME access
	Slave	Green	Static	• Slave VME access
System Status	User	Red	Static	• Defined by user
	Shutdown	Orange	Static	• USPIIe-USB system is shutting down
	Power OK	Yellow	Static	• System power is operational
	Enable[b]	Green	Static	• System is up

a—If the VME Master LED is ON, the USPIIe-USB currently owns the VME bus. This does not mean that the USPIIe-USB is accessing the VME bus, however. If the USPIIe-USB is set to VME RWD (Release When Done) mode, it releases VME ownership after each VME cycle. This is accomplished by de-asserting the BBSY signal. If the LED is ON, setting the USPIIe-USB to VME ROR (Release On Request) mode can also mean that the USPIIe-USB owns the VME bus, but is not accessing it. Setting the USPIIe-USB in VME RWD mode increases VME performance, since an arbitration phase is not needed for each VME cycle. But it can also have a deep impact on others boards in the VME chassis. Setting the system to ROR or RWD mode is done through an OBP environment variable (see the Themis *USPIIe Software Manual*, P/N 110102-023).

b—This LED is turned ON only when OBP boot is completed.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

A.3.7 Push-Button RESET

A push-button RESET switch is located on the Front Panel of the Baseboard, and is accessible by inserting an object the size of a paper clip. The RESET switch will initiate a POR Reset to the UltraSPARC-II*e*, which is propagated throughout the USPII*e*-USB. See Section 6.3.1, “Push-Button Reset,” on page 6-4 for details.

A.4 PMC Carrier Board

The PMC Carrier Board occupies the second slot position on the USPII*e*-USB/**2P2** and USPII*e*-USB/**2P3**.

Components on the USPII*e*-USB/**2P2** include:

- PMC Module slot 1
- PMC Module slot 2
- Serial (TTY) Port E (RS232)
- Serial (TTY) Port F (RS232)
- Ethernet Port B
- Audio Line-in or Mic-in
- Audio Line-out or Headphones-out
- User-defined rotary switch
- I^2C signals available as P2 option

Components on the USPII*e*-USB/**2P3** include:

- PMC Module slot 1
- PMC Module slot 2
- PMC Module slot 3

For a diagram of the PMC Carrier Board front panel, refer to Appendix C, “Front Panel Diagrams”.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

A.4.1 PMC Carrier Board VME P1 Connector

The VME P1 connector (see *Table A-8* on page A-13) provides daisy-chaining of IACK and BG signals. There is no need to jumper those signals manually for the position occupied by the PMC Carrier Board.

- Connector Type: VME64

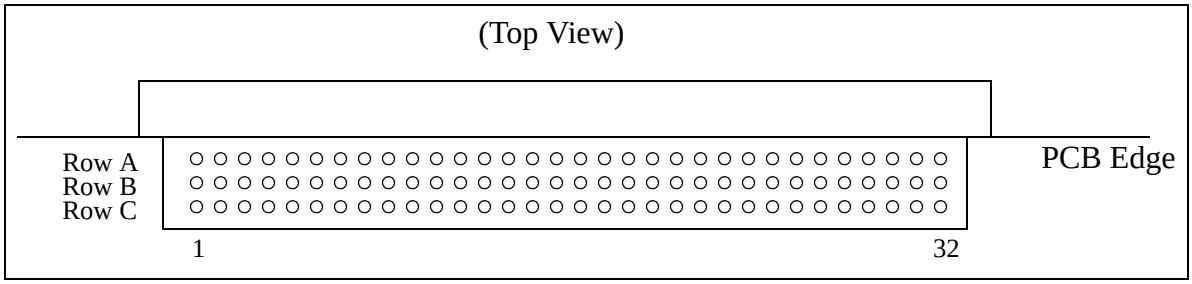


Figure A-8. PMC Carrier Board VME P1 Connector Orientation

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Table A-8. PMC Carrier Board VME P1 Pinouts

Pin	Row A Signal Name	Row B Signal Name	Row C Signal Name
1	NC	NC	NC
2	NC	NC	NC
3	NC	NC	NC
4	NC	DAISY_CHAIN_BG0*	NC
5	NC	DAISY_CHAIN_BG0*	NC
6	NC	DAISY_CHAIN_BG1*	NC
7	NC	DAISY_CHAIN_BG1*	NC
8	NC	DAISY_CHAIN_BG2*	NC
9	GND	DAISY_CHAIN_BG2*	GND
10	NC	DAISY_CHAIN_BG3*	NC
11	GND	DAISY_CHAIN_BG3*	NC
12	NC	NC	NC
13	NC	NC	NC
14	NC	NC	NC
15	GND	NC	NC
16	NC	NC	NC
17	GND	NC	NC
18	NC	NC	NC
19	GND	NC	NC
20	NC	GND	NC
21	DAISY_CHAIN_IACK*	NC	NC
22	DAISY_CHAIN_IACK*	NC	NC
23	NC	GND	NC
24	NC	NC	NC
25	NC	NC	NC
26	NC	NC	NC
27	NC	NC	NC
28	NC	NC	NC
29	NC	NC	NC
30	NC	NC	NC
31	-12V	NC	+12V
32	VCC	VCC	VCC

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

A.4.2 PMC Carrier Board VME P2 Connector

The VME P2 connector (see *Figure A-9* and *Table A-9* on page A-15) of the PMC Carrier Board transmits 64 user-defined signals through rows **A** and **C**, all from a combination of signals (solder-bead switchable) from PMC Module slots 1 and 2, Serial Ports E (TTY E) and F (TTY F), the front-panel User Rotary Switch, and the I^2C bus (see *Table B-14* in Appendix B, ”DIP-Switch, Jumper-Pin, and Solder-Bead Configurations” for details).

- Connector Type: VME64

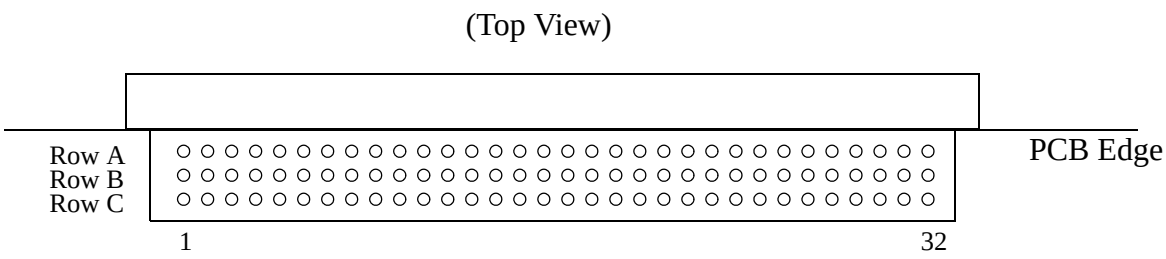


Figure A-9. PMC Board VME P2 Connector

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Table A-9. PMC Carrier Board VME P2 Pinout

Pin	Row A Signal Name	Row B Signal Name	Row C Signal Name
1	User-switchable[a]	VCC	User-switchable[a]
2	User-switchable[a]	GND	User-switchable[a]
3	User-switchable[a]	NC	User-switchable[a]
4	User-switchable[a]	NC	User-switchable[a]
5	User-switchable[a]	NC	User-switchable[a]
6	User-switchable[a]	NC	User-switchable[a]
7	User-switchable[a]	NC	User-switchable[a]
8	User-switchable[a]	NC	User-switchable[a]
9	User-switchable[a]	NC	User-switchable[a]
10	User-switchable[a]	NC	User-switchable[a]
11	User-switchable[a]	NC	User-switchable[a]
12	User-switchable[a]	GND	User-switchable[a]
13	User-switchable[a]	VCC	User-switchable[a]
14	User-switchable[a]	NC	User-switchable[a]
15	User-switchable[a]	NC	User-switchable[a]
16	User-switchable[a]	NC	User-switchable[a]
17	PMC1_IO34	NC	PMC1_IO33
18	PMC1_IO36	NC	PMC1_IO35
19	PMC1_IO38	NC	PMC1_IO37
20	PMC1_IO40	NC	PMC1_IO39
21	PMC1_IO42	NC	PMC1_IO41
22	PMC1_IO44	GND	PMC1_IO43
23	PMC1_IO46	NC	PMC1_IO45
24	PMC1_IO48	NC	PMC1_IO47
25	PMC1_IO50	NC	PMC1_IO49
26	PMC1_IO52	NC	PMC1_IO51
27	PMC1_IO54	NC	PMC1_IO53
28	PMC1_IO56	NC	PMC1_IO55
29	PMC1_IO58	NC	PMC1_IO57
30	PMC1_IO60	NC	PMC1_IO59
31	PMC1_IO62	GND	PMC1_IO61
32	PMC1_IO64	VCC	PMC1_IO63

a—See *Table B-14* on page B-17, Appendix B, “DIP-Switch, Jumper-Pin, and Solder-Bead Configurations”.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

A.4.3 PMC Module Slot User I/O

This section provides the pinouts of the 64 PMC User I/O signals that can be brought from PMC Module **slot 1** and **slot 2** to the VME P2 connector of the PMC Carrier Board.

Note: PMC Module **slot 3** has no I/O through the VME P2 connector of the PMC Carrier Board.

Three **solder-bead-selectable** configurations are possible:

1. 32 user signals from PMC Slot 1 (connector J1004), and the following I/O signals: Serial Ports E and F, I^2C, and User-Programmable Rotary Switch. *This is the default configuration*.
2. 64 user signals from PMC Slot 1 (connector J1004), and none from Slot 2.
3. 32 user signals from PMC Slot 1 (connector J1004) and 32 from Slot 2 (connector J1104).

Both PMC Carrier Slot 1, Slot 2, and Slot 3 use the connector type illustrated in *Figure A-10*, below.

- Connector Type: 64-Pin, Female, 10mm, Dual Row
- Connector Manufacturer: AMP
- Manufacturer's Part Number: 120528-1

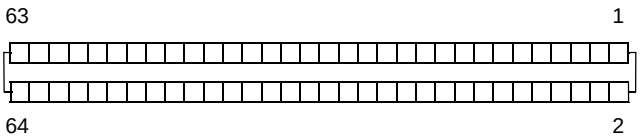


Figure A-10. PMC Carrier Board User I/O Connector

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

A.4.3.1 PMC Module Slot 1: 64-Bit User I/O Configuration

Table A-10. PMC Carrier Slot 1 with 64 Bits of User I/O

PMC Pin (J1004)	VME P2 Signal	PMC Pin (J1004)	VME P2 Signal
1	PMC IO C1	2	PMC IO A1
3	PMC IO C2	4	PMC IO A2
5	PMC IO C3	6	PMC IO A3
7	PMC IO C4	8	PMC IO A4
9	PMC IO C5	10	PMC IO A5
11	PMC IO C6	12	PMC IO A6
13	PMC IO C7	14	PMC IO A7
15	PMC IO C8	16	PMC IO A8
17	PMC IO C9	18	PMC IO A9
19	PMC IO C10	20	PMC IO A10
21	PMC IO C11	22	PMC IO A11
23	PMC IO C12	24	PMC IO A12
25	PMC IO C13	26	PMC IO A13
27	PMC IO C14	28	PMC IO A14
29	PMC IO C15	30	PMC IO A15
31	PMC IO C16	32	PMC IO A16
33	PMC IO C17	34	PMC IO A17
35	PMC IO C18	36	PMC IO A18
37	PMC IO C19	38	PMC IO A19
39	PMC IO C20	40	PMC IO A20
41	PMC IO C21	42	PMC IO A21
43	PMC IO C22	44	PMC IO A22
45	PMC IO C23	46	PMC IO A23
47	PMC IO C24	48	PMC IO A24
49	PMC IO C25	50	PMC IO A25
51	PMC IO C26	52	PMC IO A26
53	PMC IO C27	54	PMC IO A27
55	PMC IO C28	56	PMC IO A28
57	PMC IO C29	58	PMC IO A29
59	PMC IO C30	60	PMC IO A30
61	PMC IO C31	62	PMC IO A31
63	PMC IO C32	64	PMC IO A32

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

A.4.3.2 PMC Module Slot 1: 32-Bit User I/O Configuration

Table A-11. PMC Carrier Slot 1 with 32 Bits of User I/O

PMC Pin (J1004)	VME P2 Signal	PMC Pin (J1004)	VME P2 Signal
1	NC	2	NC
3	NC	4	NC
5	NC	6	NC
7	NC	8	NC
9	NC	10	NC
11	NC	12	NC
13	NC	14	NC
15	NC	16	NC
17	NC	18	NC
19	NC	20	NC
21	NC	22	NC
23	NC	24	NC
25	NC	26	NC
27	NC	28	NC
29	NC	30	NC
31	NC	32	NC
33	PMC IO C17	34	PMC IO A17
35	PMC IO C18	36	PMC IO A18
37	PMC IO C19	38	PMC IO A19
39	PMC IO C20	40	PMC IO A20
41	PMC IO C21	42	PMC IO A21
43	PMC IO C22	44	PMC IO A22
45	PMC IO C23	46	PMC IO A23
47	PMC IO C24	48	PMC IO A24
49	PMC IO C25	50	PMC IO A25
51	PMC IO C26	52	PMC IO A26
53	PMC IO C27	54	PMC IO A27
55	PMC IO C28	56	PMC IO A28
57	PMC IO C29	58	PMC IO A29
59	PMC IO C30	60	PMC IO A30
61	PMC IO C31	62	PMC IO A31
63	PMC IO C32	64	PMC IO A32

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

A.4.3.3 PMC Module Slot 2: 32-Bit User I/O Configuration

Table A-12. PMC Carrier Slot 2 with 32 Bits of User I/O

PMC Pin (J1104)	VME P2 Signal	PMC Pin (J1104)	VME P2 Signal
1	NC	2	NC
3	NC	4	NC
5	NC	6	NC
7	NC	8	NC
9	NC	10	NC
11	NC	12	NC
13	NC	14	NC
15	NC	16	NC
17	NC	18	NC
19	NC	20	NC
21	NC	22	NC
23	NC	24	NC
25	NC	26	NC
27	NC	28	NC
29	NC	30	NC
31	NC	32	NC
33	PMC IO C1	34	PMC IO A1
35	PMC IO C2	36	PMC IO A2
37	PMC IO C3	38	PMC IO A3
39	PMC IO C4	40	PMC IO A4
41	PMC IO C5	42	PMC IO A5
43	PMC IO C6	44	PMC IO A6
45	PMC IO C7	46	PMC IO A7
47	PMC IO C8	48	PMC IO A8
49	PMC IO C9	50	PMC IO A9
51	PMC IO C10	52	PMC IO A10
53	PMC IO C11	54	PMC IO A11
55	PMC IO C12	56	PMC IO A12
57	PMC IO C13	58	PMC IO A13
59	PMC IO C14	60	PMC IO A14
61	PMC IO C15	62	PMC IO A15
63	PMC IO C16	64	PMC IO A16

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

A.4.3.4 PMC Module Slot 3: 0-Bit User I/O Configuration

Table A-13. PMC Carrier Slot 3 with 0 Bits of User I/O

PMC Pin (J1204)	VME P2 Signal	PMC Pin (J1204)	VME P2 Signal
1	*Not available*	2	*Not available*
3	*Not available*	4	*Not available*
5	*Not available*	6	*Not available*
7	*Not available*	8	*Not available*
9	*Not available*	10	*Not available*
11	*Not available*	12	*Not available*
13	*Not available*	14	*Not available*
15	*Not available*	16	*Not available*
17	*Not available*	18	*Not available*
19	*Not available*	20	*Not available*
21	*Not available*	22	*Not available*
23	*Not available*	24	*Not available*
25	*Not available*	26	*Not available*
27	*Not available*	28	*Not available*
29	*Not available*	30	*Not available*
31	*Not available*	32	*Not available*
33	*Not available*	34	*Not available*
35	*Not available*	36	*Not available*
37	*Not available*	38	*Not available*
39	*Not available*	40	*Not available*
41	*Not available*	42	*Not available*
43	*Not available*	44	*Not available*
45	*Not available*	46	*Not available*
47	*Not available*	48	*Not available*
49	*Not available*	50	*Not available*
51	*Not available*	52	*Not available*
53	*Not available*	54	*Not available*
55	*Not available*	56	*Not available*
57	*Not available*	58	*Not available*
59	*Not available*	60	*Not available*
61	*Not available*	62	*Not available*
63	*Not available*	64	*Not available*

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

A.4.4 Serial Ports E and F (RS232)

- Connector Type: Dual-stacked 9-pin Micro-DB9
- Part Number: ITT Cannon MDS18PE-Z10
- Themis Cable (optional): 108113

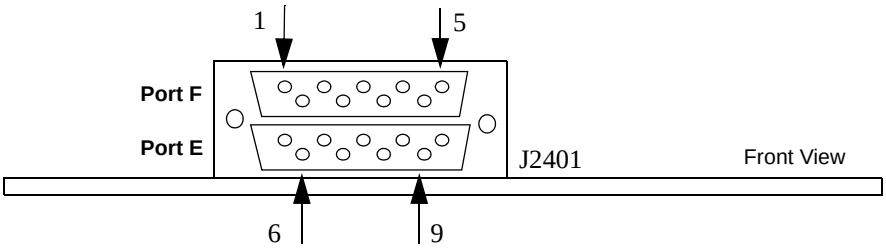


Figure A-11. Front-Panel Serial Ports E and F

Table A-14. Serial Port E and F Connector Pinout

PC board is marked:	Port E Pin[a]	Signal Name: TTY E Signal	Signal Name: Description	Signal Name: TTY F Signal	Port F Pin[a]	*PC board is marked:*
B1	1	DCD	Carrier Detect	DCD	1	**A1**
	2	RXD	Receive Data	RXD	2	
	3	TXD	Transmit Data	TXD	3	
	4	DTR	Data Terminal Ready	DTR	4	
B5	5	SIG GND	Signal Ground	SIG GND	5	**A5**
B6	6	DSR	Data Set Ready	DSR	6	**A6**
	7	RTS	Request to send	RTS	7	
	8	CTS	Clear to send	CTS	8	
B9	9	RI	Ring indicator	RI	9	**A9**

a—***Important:*** The A and B associated with Serial Port connector pins on PC boards (Rev **Y** and Rev **B**) are interpreted as follows: Port E pins are marked with a B. Port F pins are marked with an A.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

A.4.5 Ethernet Port B

- Connector Type: RJ45 TPE
- Connector Part Number: STEWART-SS-6488S-A-NF

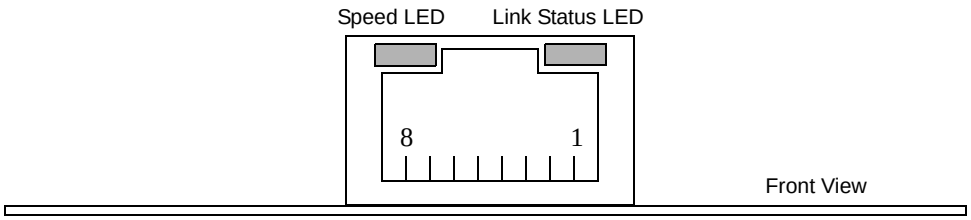


Figure A-12. Ethernet B Connector

Table A-15. RJ45 Ethernet B Pinout

Pin	Signal Name
1	TXD+
2	TXD-
3	RXD+
4	4T_D3P
5	4T_D3P
6	RXD-
7	4T_D4P
8	4T_D4P

A.4.6 Stereo Audio Connectors

- Connector Type: Mini Stereo Jack
- Connector Part Number: ASTRON AT-JY3540-050B

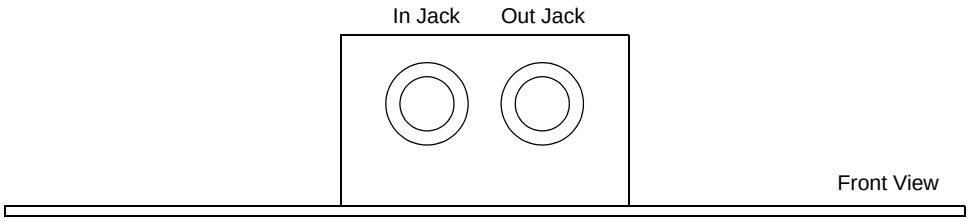


Figure A-13. Dual Stereo Audio Connector

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

A.5 Paddle Boards

The following paddle boards are connected to the back of the VME P2 connector backplane (see Table A-2, “Baseboard VME P2 Connector Pinouts,” on page 4).

A.5.1 Standard Paddle Board

The Standard Paddle Board (P/N 110094-030) attaches to the rear of the slot occupied by the USPII*e*-USB Baseboard on the VME P2 backplane (see *Figure 1-1* on page 1-5) and provides connection for:

- SCSI Port A (SE mode)
- Serial Port B (RS232)
- Power fail, software alarm, and high-temperature trip signals
- Polyswitch Vcc power fuse

[See the section entitled “Paddle Boards” on page D-1 for a more complete description.]

A.5.1.1 SCSI Port A Connector

- Connector Type: High-density, 68 Pin, Female, Shielded Subminiature-D (single-ended only)
- Connector Part Number: AMP 749069-7

When a SCSI device is attached to the USPII*e*-USB through the Standard Paddle Board, jumper-pin JP1801 must be **on** (see “SCSI Termination” on page 1-4 in Chapter 1, "USPIIe-USB Installation"). SCSI bus A will only operate in wide single-ended (SE) mode. See *Figure A-14* and *Table A-16* on page A-24, for SCSI Port A pinouts.

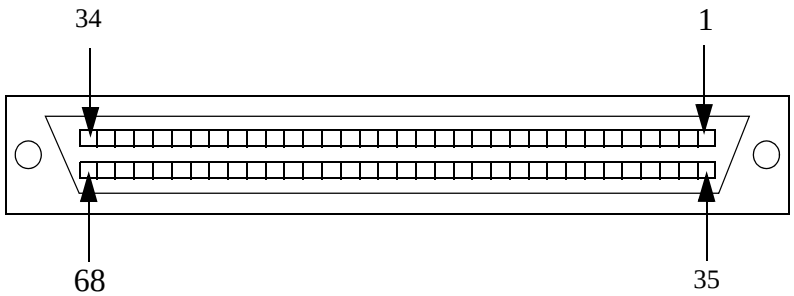


Figure A-14. Standard Paddle Board SCSI Connector

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

A.5.1.2 Serial (TTY) Port B Connector

- Connector Type: Sub-DB, 9-pin, Male, Right Angle
- Connector Part Number: AMP 747150-2

The exact signals available on the paddle board connector vary with the board configuration, as described in *Table 2-5* on page 2-10 in Chapter 2, "USPIIe-USB Specifications". See *Figure A-15* and *Table A-17* on page A-25 for pinout designations.

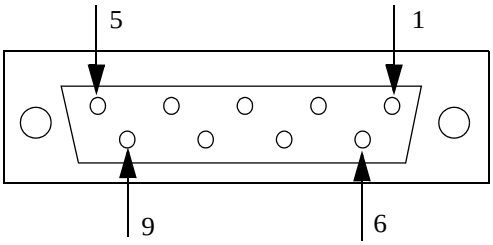


Figure A-15. Paddle Board Serial Port B Connector

Table A-16. Paddle Board SCSI Port A Connector Pinouts

Pin	Signal Name	Pin	Signal Name
1	GND	35	DAT12
2	GND	36	DAT13
3	GND	37	DAT14
4	GND	38	DAT15
5	GND	39	DPAR1
6	GND	40	DAT0
7	GND	41	DAT1
8	GND	42	DAT2
9	GND	43	DAT3
10	GND	44	DAT4
11	GND	45	DAT5
12	GND	46	DAT6
13	GND	47	DAT7
14	GND	48	DPAR0
15	GND	49	GND
16	GND	50	NC
17	TERPWR	51	TERPWR
18	TERPWR	52	TERPWR

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Table A-16. Paddle Board SCSI Port A Connector Pinouts (Continued)

Pin	Signal Name	Pin	Signal Name
19	*NC*	53	*NC*
20	SENSE[a]	54	GND
21	GND	55	ATN
22	GND	56	GND
23	GND	57	BUSY
24	GND	58	ACK
25	GND	59	RESET
26	GND	60	MSG
27	GND	61	SEL
28	GND	62	CD
29	GND	63	REQ
30	GND	64	IO
31	GND	65	DAT8
32	GND	66	DAT9
33	GND	67	DAT10
34	GND	68	DAT11

a—This is part of the automatic SCSI termination sensing logic. The SCSI P2 signal will be forced to ground by the mating SCSI connector when attached, thus disabling the on-board terminator (see *Figure 1-2*, page 1-6).

Table A-17. Paddle Board Serial Port B Connector Pinouts

Pin	Signal Name
1	DCD
2	RXD
3	TXD
4	DTR
5	GND
6	DSR
7	RTS
8	CTS
9	RI

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

A.5.2 Multiple I/O Paddle Board

As shown in *Figure A-16*, the Multiple-I/O Paddle Board (P/N 110778-001) provides I/O connection for:

- Ultra160 SCSI Port A (wide-LVD mode)
- Parallel Port (DB25)
- 4 Serial Ports: Port A (TTY-A), Port B (RS232), Port C (TTY-C), and Port D (TTY-D)
- Dual (2) USB Ports
- PS/2 Keyboard/Mouse Port (mini-DIN-8)
- Audio Line Out (stereo jack)
- Audio Line In (stereo jack)

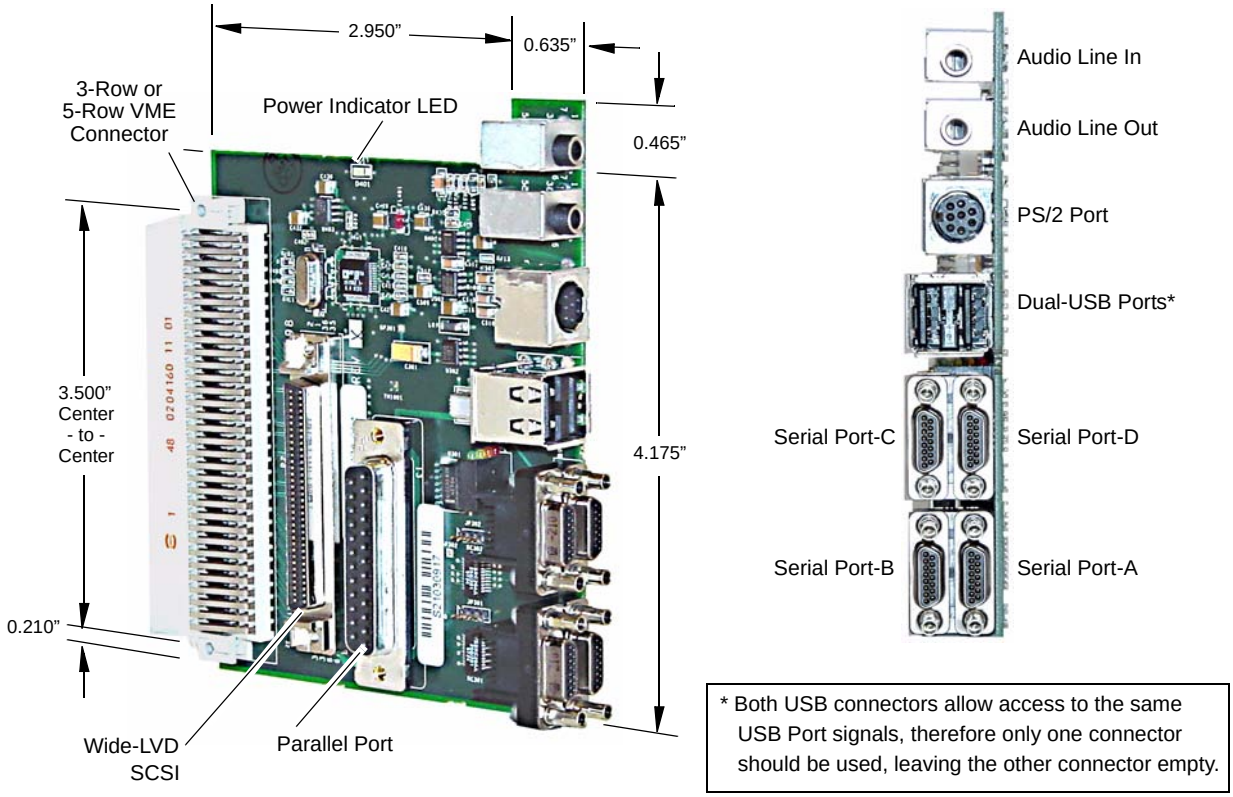


Figure A-16. USPIIe-USB Multiple-I/O Paddle Board

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

A.5.2.1 Ultra160 SCSI Port A (68-pin female)

See *Table A-3* on page A-6 for a list of pinout signals.

A.5.2.2 Parallel Port

The USPII*e*-USB does not support the parallel-port connector.

A.5.2.3 Serial Port A, C, and D (RS-232)

See *Table A-2* on page A-4 for a list of pinout signals.

A.5.2.4 Serial Port B (RS-232 with modem support)

See *Table A-2* on page A-4 for a list of pinout signals.

A.5.2.5 Dual USB Port

The USPII*e*-USB does not support the dual-USB-port connector on the Multiple-I/O Paddle Board.

A.5.2.6 PS/2 Keyboard/Mouse Port (mini-DIN-8)

See *Table A-5* on page A-8 for a list of pinout signals.

A.5.2.7 Stereo Audio Line Out and Line In

The stereo signals for the audio-out and audio-in lines (*Figure A-17*) are listed in *Table A-18* on page A-28.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

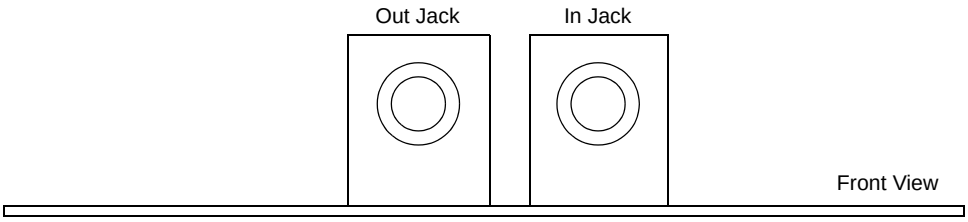


Figure A-17. Line Out/In Stereo Audio Connectors

Table A-18. Audio Signal Assignments

Component	Line Out	Line In
Tip	Left channel	Left channel
Ring (center)	Right channel	Right channel
Shield	Ground	Ground

A.6 Memory Module Connector

- Connector Type: 2-Part (Receptacle/Plug), 2-row, 200-pin, Board-to-Board (Receptacle is mounted on Baseboard)
- Connector Part Number: Molex 52760-2009 (R), 53481-2009 (P)

The custom Memory Module is installed onto the USPII*e*-USB Baseboard with one connector to attach it to the Baseboard (see *Figure A-18*).

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Caution: Because of the *VME Specification* requiring a 0.8-inch interboard separation (see *Figure 1-1* on page 1-5) between VME slots, only one Memory Module can be installed onto a USPIIe-USB Baseboard (*stacking not supported*).

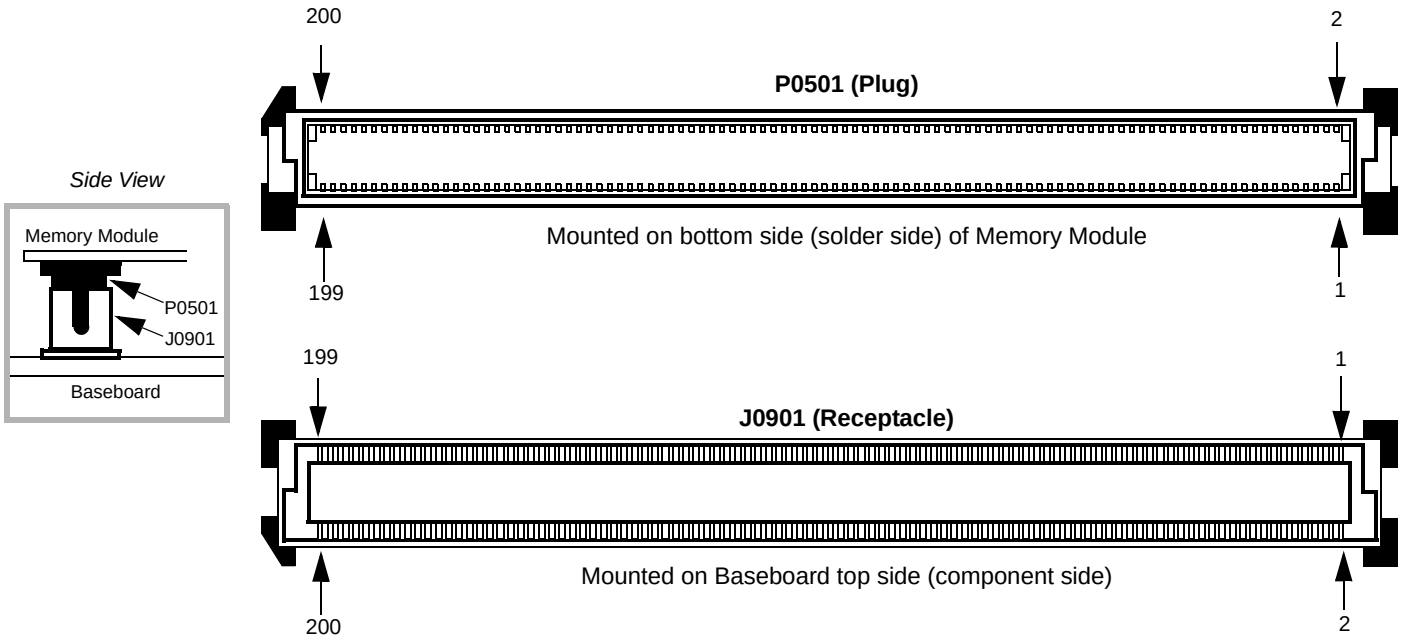


Figure A-18. Memory Module Baseboard Connectors (Receptacle & Plug)

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Appendix B

DIP-Switch, Jumper-Pin, and Solder-Bead Configurations

B.1 Overview

This appendix provides a summary of the DIP-switch, jumper-pin, and solder-bead configurations for all boards on the USPII*e*-USB. At the present time, there is only one **DIP switch**, which is contained on the PMC Carrier Board (top side). **Jumper pins** and DIP switches are considered "field-configurable" and may be altered by a user on site. **Solder beads** are considered "factory-configurable" and *must not be altered* by the user. If a solder bead requires re-configuration, contact Themis Customer Service.



Warning: Attempting to alter a solder-bead configuration could seriously damage the USPII*e*-USB.
DO NOT ATTEMPT TO ALTER SOLDER-BEAD CONFIGURATIONS.

B.2 Field-Configurable

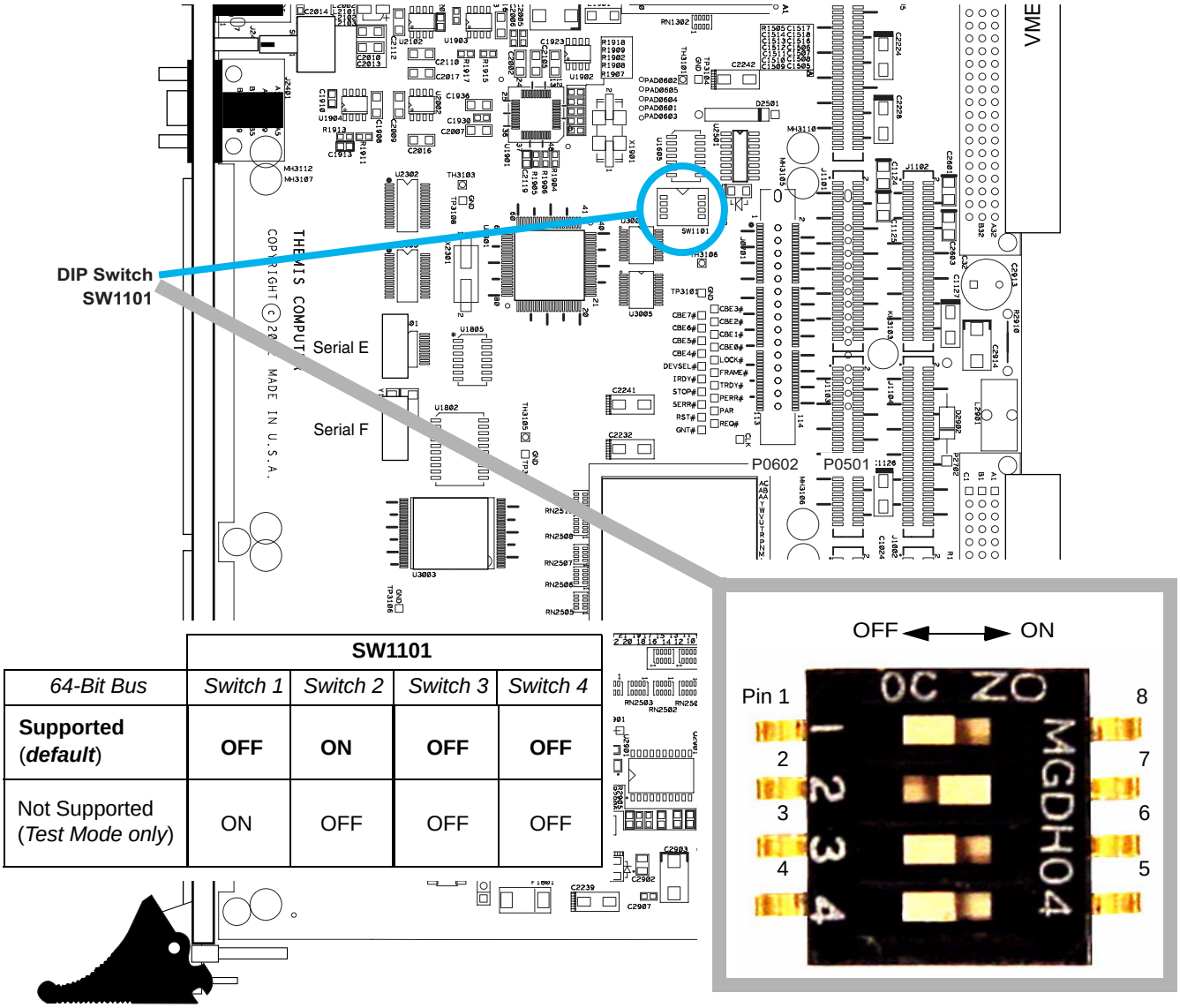
B.2.1 DIP Switch

The PMC Carrier Board contains a DIP switch (SW1101) with four independent ON/OFF switches (see *Figure B-1* on page B-2). Only switches 1 and 2 are used by the USPII*e*-USB; the location of SW1101 and its default switch settings are shown

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

in *Figure B-1*. To set a switch to the ON position, push the switch toward the ON direction with a pointed object (a pencil, for example); for OFF, push the switch in the opposite direction.

Note: Because of the small size of the DIP switch, it may be necessary to use a magnifying glass.



	SW1101			
64-Bit Bus	*Switch 1*	*Switch 2*	*Switch 3*	*Switch 4*
Supported (*default*)	**OFF**	**ON**	**OFF**	**OFF**
Not Supported (*Test Mode only*)	ON	OFF	OFF	OFF

Figure B-1. Location and Configuration of SW1101 (Top Side)

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

B.2.2 Baseboard Jumper Pins

Jumper pins are found only on the *top side (component side)* of the USPII*e*-USB Baseboard and are described in *Table B-1*.

In *Table B-1*, an **ON** jumper position means the jumper is installed, shorting the pins and completing the circuit. **OFF** means there is no jumper installed, hence the path between the pins is open, breaking the circuit.

Table B-1. Baseboard Jumper-Pin Settings (Top Side)

Jumper Pins	Jumper Position[a]	Description
JP1401 (see *Table B-2*, page B-4)	ON	Force Universe II to be the VME system controller (SYSCON).[b]
	OFF	Autosensing is enabled to determine the Universe II operating mode.
JP1402 (see *Table B-2*, page B-4)	Short 1–2	VME bus grant in (3) at input of the VME system controller is pulled up, forcing the USPII*e*-USB to be a non-system controller at power-up.
	Short 2–3	Setting the VME controller as the system controller is determined by JP1401.
JP1501	**ON**	Transmit system reset to VME SYSRST.
	OFF	DO NOT transmit system reset to VME SYSRST.
JP1601	**ON**	Enable the USPII*e*-USB to be receptive to the VME system reset (SYSRST).
	OFF	USPII*e*-USB will ignore any incoming VME system reset (SYSRST) signal.
JP1801 (see *Table B-3*, page B-5)	ON[c]	Force SCSI A into single-ended (SE) mode when a 3-row VME backplane is used, and connect SCSI A to VME P2.
	OFF	Allow autosense mode to determine if SCSI A bus is SE or differential mode.
JP2201	**ON**	Flash 0 is writable.
	OFF	Flash 0 is NOT writable.
JP2202	**ON**	Flash 1 is writable.
	OFF	Flash 1 is NOT writable.
JP2203	**ON**	Flash 2 is writable.
	OFF	Flash 2 is NOT writable.

Note: Footnotes are described at the end of *Table B-1* on page B-4.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Table B-1. Baseboard Jumper-Pin Settings (Top Side) (Continued)

Jumper Pins	Jumper Position[a]	Description
JP2701	**ON**	JP2701 and JP2702 determine the boot device (*see Table B-4, page B-5)*. *(JP2701 and JP2702 are configured together.)*
	OFF	
JP2702	**ON**	
	OFF	
JP2703	**ON**	Use the first bank in the Flash PROM.
	OFF	Use the second bank in the Flash PROM.
JP2704 to JP2706	**ON**	Select OBP patch execution during reset.
	OFF	*Reserved for Themis engineering use.*
JP3401	**ON**	Set TTYB to RS232 mode.
	OFF	Set TTYB to RS422 mode.
JP3701	Short 1–2	On-board PMC 0 Module does not support 64-bit PCI bus.
	Short 2–3	On-board PMC 0 Module supports 64-bit PCI bus.

a—Boldface = the default jumper position.

b—The Universe II operating mode (VME system controller vs. non-VME system controller) is determined by autosensing VME bus grant #3 during power-up. See Chapter 4, "Universe II Description".

c—When the USPIIe-USB is accessed through a 3-row VME backplane, only SE mode is supported, and a jumper must be installed on JP1801. If there are 1 or more SE-mode SCSI devices present on the SCSI bus, the entire bus will run in SE mode.

Table B-2. Combined JP1401/JP1402 Configurations

	JP1401 Jumper ON	**JP1401 Jumper OFF**
JP1402 Jumper 1-2 ON	Non-VME System Controller	Non-VME System Controller
JP1402 Jumper 2-3 ON	VME System Controller (SYSCON)	Autosensing mode

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Table B-3. SCSI A Access Definition

Baseboard SCSI A Port Access		Mode?	Auto-Sensed?	Install JP1801 Jumper?
Front Panel only		LVD[a] or SE[b]	YES (either LVD or SE mode)	NO
VME P2 Connector	3-row VME backplane	SE only	NO (see Appendix , *Table A-2*, page A-4)	YES
	5-row VME backplane[c]	LVD or SE	YES	NO
VME P2 Connector through Themis 3-row Paddle Board		SE only	NO	YES

a—Low-Voltage Differential.

b—Single-Ended.

c—5-row access requires Multiple I/O or custom Paddle Board.

Table B-4. Boot-Device Settings[a]

JP2702	JP2701	Boot Device
Jumper ON	**Jumper ON**	Flash 0 PROM
Jumper ON	Jumper OFF	Flash 1 PROM
Jumper OFF	Jumper ON	Flash 2 PROM
Jumper OFF	Jumper OFF	ROMBO

a—See also Tables 4-3 and 4-4 in Chapter 4 of the *USPIIe*-USB *Software Manual*.

Figure B-2 on page B-6 provides the location of the various jumpers on the USPII*e*-USB Baseboard. In *Figure B-2*, jumper pin 1 is identified with a **square** and a **triangle**.

B.2.3 Paddle Board Jumper Pins

There are no jumper pins on either of the USPII*e*-USB paddle boards (Standard or Multiple I/O).

B.2.4 PMC Carrier Board Jumper Pins

There are no jumper pins on the USPII*e*-USB PMC Carrier Board.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

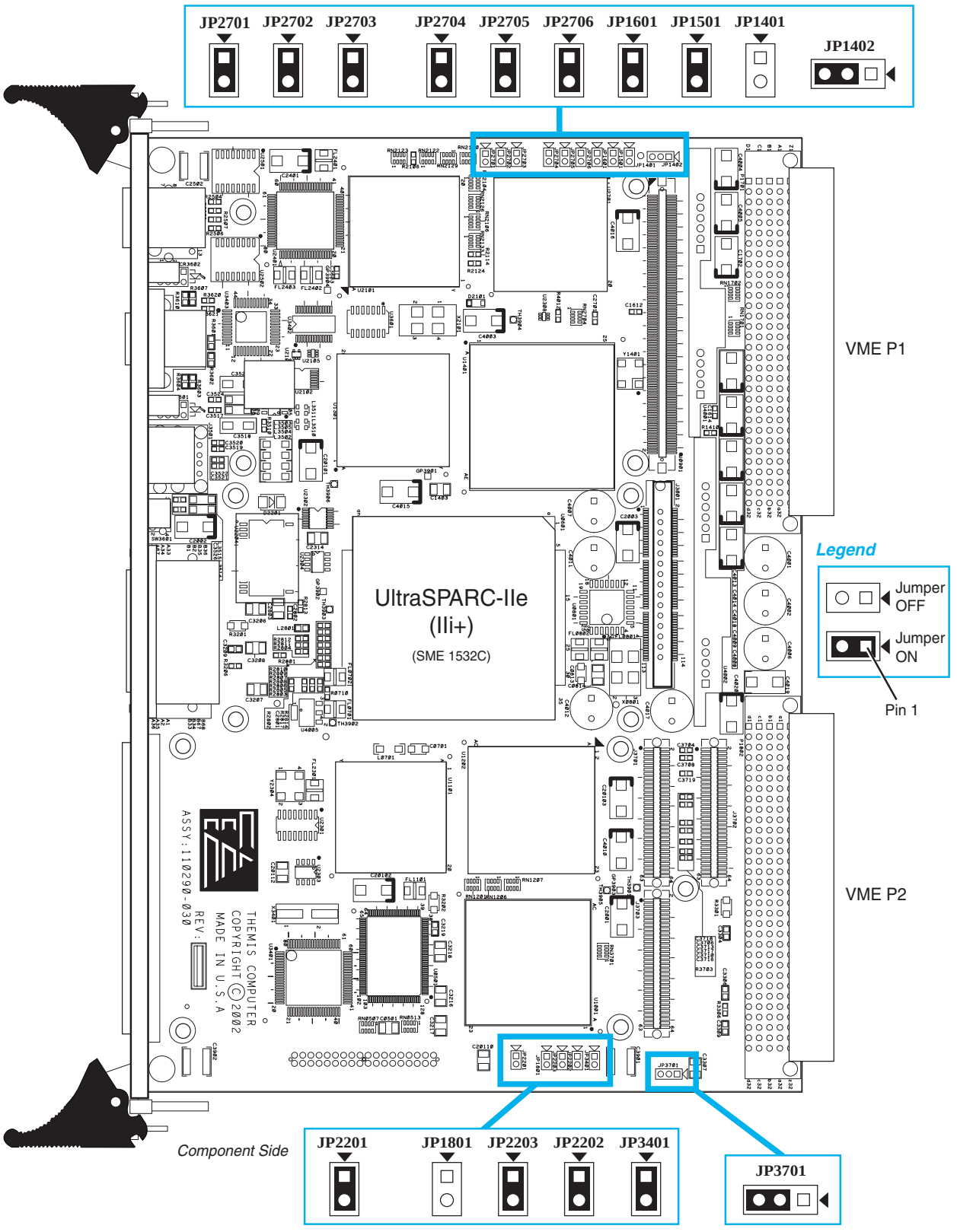


Figure B-2. Baseboard Jumper Locations (Top Side)

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

B.3 Factory-Configurable

B.3.1 Baseboard Solder Beads

Solder beads are found only on the *bottom side* (solder side) of the USPII*e*-USB Baseboard and are described in *Table B-5*.

In *Table B-5*, if no pin number is given, only **2** solder pins exist. If there are **3** solder pins, the two pins listed are shorted together. **Short** means a solder bead is installed, creating an electrical path between two contacts. **Open** means no solder bead is installed, hence the path between the contacts is open. *Figure B-3* on page B-10 provides the location of the baseboard solder beads. Remember that **pin 1** is indicated on the board by a **thick bar line**.



Caution: When dealing with a **3-pin** solder-bead switch, a solder bead will short only one set of pins, either 1–2 or 2–3.
If a solder bead shorts more than 2 pins, call Themis Customer Support.

Table B-5. Baseboard Solder-Bead Settings (Bottom Side)

Solder Bead	Setting[a]	Description
SB0501	Short 1–2	PWR_HEALTHY.
	Short 2–3	SCAN_TRST is driven by PLD
SB0801	Short	CPU CLK PLL (clock phase-locked loop) can be programmed (*normal mode*).
	Open	CPU clock generator serial load is disabled.
SB1201	**Short**	SCAN_TRST of non-Sun ASIC is driven by PWR_HEALTHY.
	Open	SCAN_TRST of non-Sun ASIC is not driven by PWR_HEALTHY.
SB1801	**Short 1–2**	Audio Codec 97 (AC97) signals are connected to the PCI extension.
	Short 2–3	Audio Codec 97 (AC97) signals are connected to the VME P2 connector.
SB1805 to SB1807	**Short 1–2**	Parallel port is connected to VME P2.
	Short 2–3	No parallel port on VME P2. High-temperature, software-alarm, and power-failure signals enabled on P2.
SB1810 to SB1813	**Short**	PS/2 signals are connected to VME P2.
	Open	PS/2 signals are not connected to VME P2.
SB2201 to SB2203	**Short 1–2**	Only 5V is connected to programming power of flash memory.
	Short 2–3	Only 12V is connected to programming power of flash memory.

Note: Footnotes are described at the end of *Table B-5* on page B-8.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Table B-5. Baseboard Solder-Bead Settings (Bottom Side) (Continued)

Solder Bead	Setting[a]	Description
SB2204	**Short 1–2**	TOD/NVRAM is M48T59.
	Short 2–3	TOD/NVRAM is M48T35.
SB2205	Short	TOD/NVRAM is M48T35.
	Open	TOD/NVRAM is M48T59.
SB2701	Short	The 3.3V standby signal is disabled (*battle mode*).
	Open	The 3.3V standby signal is enabled.
SB2702	Short	The Vdd-core standby signal is disabled (*battle mode*).
	Open	The Vdd-core standby signal is enabled.
SB2703	**Short 1–2**	*See Table B-7, page -9 (SB2703 and SB2705 are set together)*
	Short 2–3	
SB2704	Short	*Manufacturing use only.*
	Open	Disable PLD clock test.
SB2705	Short 1–2	*See Table B-7, page -9 (SB2703 and SB2705 are set together)*
	Short 2–3	
SB2706	Short 1–2	ROMBO_CS is not connected to Rombo connector.
	Short 2–3	ROMBO_CS is connected to Rombo connector.
SB3001	**Short**	PMC Carrier Board is connected to Baseboard.
	Open	TGA3D/3D+ Graphics Board is connected to Baseboard.
SB3202	Short 1–2	*Manufacturing use only.*
	Short 2–3	Setting is dependent on SCSI-B termination components installed.
SB3204	Short	*Manufacturing use only.*
	Open	Setting is dependent on SCSI-A termination components installed.
SB3501	**Short**	Serial ports A and B are connected to front panel (not connected to VME P2).
	Open	Serial ports A and B are connected to VME P2 (not connected to front panel).
SB3502[b]	Short	USB is indicated for the front-panel DIN (8-pin) connector.
	Open	PS/2 is indicated for the front-panel DIN (8-pin) connector.
SB3503[b] to SB3506	**Short 1–2**	PS/2 is enabled on the front-panel DIN (8-pin) connector.
	Short 2–3	USB-0 and USB-1 are enabled on the front-panel DIN (8-pin) connector.

a—Boldface = the default solder-bead position.

b—SB3502 through SB3506 must be set together.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Table B-6. Front-Panel DIN Settings

SB3502	SB3503 through SB3506	Front-Panel 8-Pin Mini-DIN Configuration	Comments
Open	**Short 1-2**	**PS/2 keyboard/mouse**	Accessible only through special split pigtail cable (*Themis 110104-001*) • 8-pin mini-DIN to 6-pin keyboard DIN and 6-pin mouse DIN
Open	Short 2-3	*Not Applicable*	
Short	Short 1-2	*Not Applicable*	
Short	**Short 2-3**	**USB-0 and USB-1 (USB0, USB1)**	Accessible only through special split pigtail cable (*Themis 110473-001*) • 8-pin mini-DIN to dual 4-pin USB

Table B-7. CPU Speed Settings

SB2703	SB2705	CPU Speed
Short 1-2	Short 1-2	650 MHz
Short 1-2	Short 2-3	600 MHz
Short 2-3	Short 1-2	550 MHz
Short 2-3	Short 2-3	*Not applicable*

B.3.2 Memory Module Solder Beads

There are no solder beads on the USPII*e*-USB Memory Module.

B.3.3 Paddle Board Solder Beads

There are no solder beads on either of the USPII*e*-USB paddle boards (Standard or Multiple I/O).

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

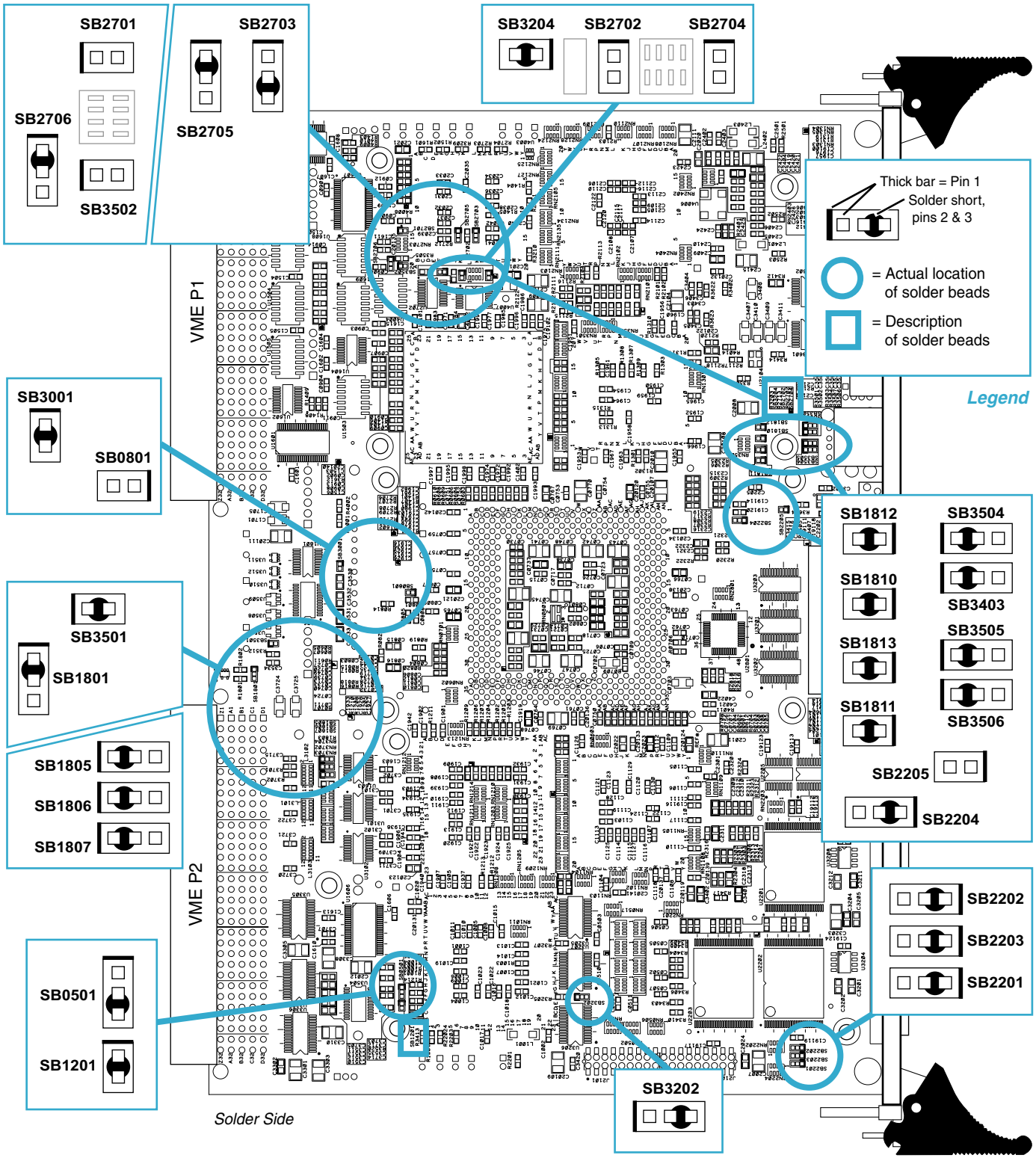


Figure B-3. Baseboard Solder-Bead Locations (Bottom Side)

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

B.3.4 PMC Carrier Board Solder Beads

Solder beads are found only on *the bottom side* of the USPII*e*-USB PMC Carrier Boards and are described in *Table B-8*.

Note: Solder beads are the same for both the 2P2 and 2P3 PMC Carrier Boards, with the exception that the audio interface is not supported on the 2P3 model, as indicated in *Table B-8*. Please note the boldface text indicating ***model 2P2 only***.

In *Table B-8*, if no pin number is given, only **2** solder pins exist. If there are **3 or more** solder pins, the two pins listed are shorted together. **Short** means a solder bead is installed, creating an electrical path between contacts. **Open** means no solder bead is installed, hence the path between the contacts is open.

Figure B-4 on page B-16, provides the location of the Carrier Board solder beads. Remember that **pin 1** is indicated on the board by a **dot** and/or a **thick bar line**.

Caution: When dealing with a **3- or 4-pin** solder-bead switch, a solder bead will short only one set of pins.
If a solder bead shorts more than 2 pins, call Themis Customer Support.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Table B-8. PMC Carrier Board Solder-Bead Settings (Both Sides)

Solder Bead	Setting[a]	Description
SB0901	**Short 1–2**	Required when the PMC Carrier Board (in the *second* VME slot) is directly connected to the Baseboard
	Short 2–3	Required when the PMC Carrier Board (in the *third* VME slot) is directly connected to the Graphics Board or the PMC Carrier Board in the *second* VME slot
SB0902	Short 1–2	Support 33-MHz PMC function.
	Short 2–3	Support 66-MHz PMC function.
SB0903	**Short 1–2**	Required when the PMC Carrier Board supports 5V VIO PMC modules
	Short 2–3	Required when the PMC Carrier Board supports 3.3V VIO PMC modules
SB1301	**Short 1–2**	Set Rio to Motherboard mode (PMC Carrier Board must be set to this mode)
	Short 2–3	Set Rio to Add-In mode *(factory use only*)
SB1302	**Short**	Assign Ethernet interupt to PCI interupt
	Open	Block Ethernet interupt *(factory use only*)
SB1801	Short	Disable 5-MHz I^2C clock
	Open	Enable 5-MHz I^2C clock
SB1802	Short	Audio interface configuration (see *Table B-9*, page B-13); USPIIe-USB **model 2P2** only
	Open	
SB1803	Short	Audio interface configuration (see *Table B-9*); USPIIe-USB **model 2P2** only
	Open	
SB1804	*Not used*	
SB2403 and SB2404	Short 1–2	Audio interface configuration (see *Table B-9*, page B-13); USPIIe-USB **model 2P2** only
	Short 2–3	
SB2407 and SB2408	Short 1–2	Audio interface configuration (see *Table B-9*, page B-13); USPIIe-USB **model 2P2** only
	Short 2–3	
SB2801 to SB2832	Short 1–4	VME P2 connector pinout configuration (see *Table B-10*, page B-14)
	Short 2–4	
	Short 3–4	
SB2833	Short	Board type selection (see *Table B-11*, page B-14)
	Open	

Note: Footnotes are described at the end of *Table B-8* on page B-13.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Table B-8. PMC Carrier Board Solder-Bead Settings (Both Sides) (Continued)

Solder Bead	Setting[a]	Description
SB2834	Short	PCB Revision settings indicator (see *Table B-12*, page B-14)
	Open	
SB2835	Short	VME P2 connector pinout configuration (see *Table B-10*, page B-14)
	Open	
SB2836	Short	VME P2 connector pinout configuration (see *Table B-10*, page B-14)
	Open	
SB2837	Short	PCB Revision settings indicator (see *Table B-12*, page B-14)
	Open	
SB2838	Short	PCB Revision settings indicator (see *Table B-12*, page B-14)
	Open	
SB2839	Short	Board type selection (see *Table B-11*, page B-14)
	Open	
SB2840	Short	Board type selection (see *Table B-11*, page B-14)
	Open	
SB3002	**Short**	Flash PROM selected is writable
	Open	Flash PROM selected is not writable
SB3003	**Short 1–2**	Enable 5V Flash programming voltage (Vpp)
	Short 2–3	Enable 12V Flash programming voltage (Vpp)

a—Boldface = the default solder-bead position. No boldface indicates there is no default.

Table B-9. Audio Input/Output Settings (2P2 Only)[a]

Solder Bead	Line In	Line Out	Microphone In	Head-phones
SB1802	**Open**		Short	
SB1803		**Open**		Short
SB2403 and SB2404		**Short 2–3**		Short 1–2
SB2407 and SB2408	**Short 2–3**		Short 1–2	

a—The 2P3 PMC Carrier Board does not provide Audio I/O.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Table B-10. VME P2 Connector Configuration (2P2 and 2P3)[a]

Definition (32 Pins)	SB2801 to SB2832	SB2835	SB2836
All PMC 1	Short 1–4	Short	Short
PMC 1 (16 pins) and PMC 2 (16 pins)	Short 3–4	**Open**	Short
PMC 1 (16 pins) and PMC Carrier I/O	**Short 2–4**		**Open**

a—See *Table B-13*, page B-15, and *Table B-14*, page B-17, for details. Dark shaded area indicates no preference.

Table B-11. PMC Carrier Board Selection Settings (2P2 and 2P3)

	SB2839	SB2840	SB2833
2 PMCs in First I/O slot (slot 2)	Short	Short	Short
3 PMCs in First I/O slot (slot 2)	Short	Short	*Open*
2 PMCs in Second I/O slot (slot 3)	Short	*Open*	Short
3 PMCs in Second I/O slot (slot 3)	Short	*Open*	*Open*
Reserved	*Open*	Short	Short
Reserved	*Open*	Short	*Open*
Reserved	*Open*	*Open*	Short
Reserved	*Open*	*Open*	*Open*

Table B-12. PCB Revision Settings

Revision	SB2834	SB2837	SB2838
A	Short	Short	Short
B	Short	Short	*Open*
C	Short	*Open*	Short
D	Short	*Open*	*Open*
E	*Open*	Short	Short
F	*Open*	Short	*Open*
Y	*Open*	*Open*	Short
X	*Open*	*Open*	*Open*

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

In *Table B-14* on page B-17, VME P2 pin signals are interpreted as follows:

Table B-13. VME P2 Pin Signal Interpretation

Signal	Interpretation
PMC1_IO*n*	The *n*th pin of PMC Module slot 1
PMC2_IO*n*	The *n*th pin of PMC Module slot 2
USR_SW1_*n*	The User Switch is equal to the value *n* (1, 2, 4, or 8)
SSER_E_*xyz*	The *xyz* signal of Serial Port E
SSER_F_*xyz*	The *xyz* signal of Serial Port F
I2C_*abc_xyz*	An I^2C bus signal (1.5A, Vcc Polyswitch fuse)

In *Table B-14*, bold lines outline the various functions available from the VME P2 connector according to the PMC Carrier Board solder-bead configuration; namely

- PMC Module slot 1
- PMC Module slot 2
- Serial Port E
- Serial Port F
- User Switch
- I^2C-bus signals

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

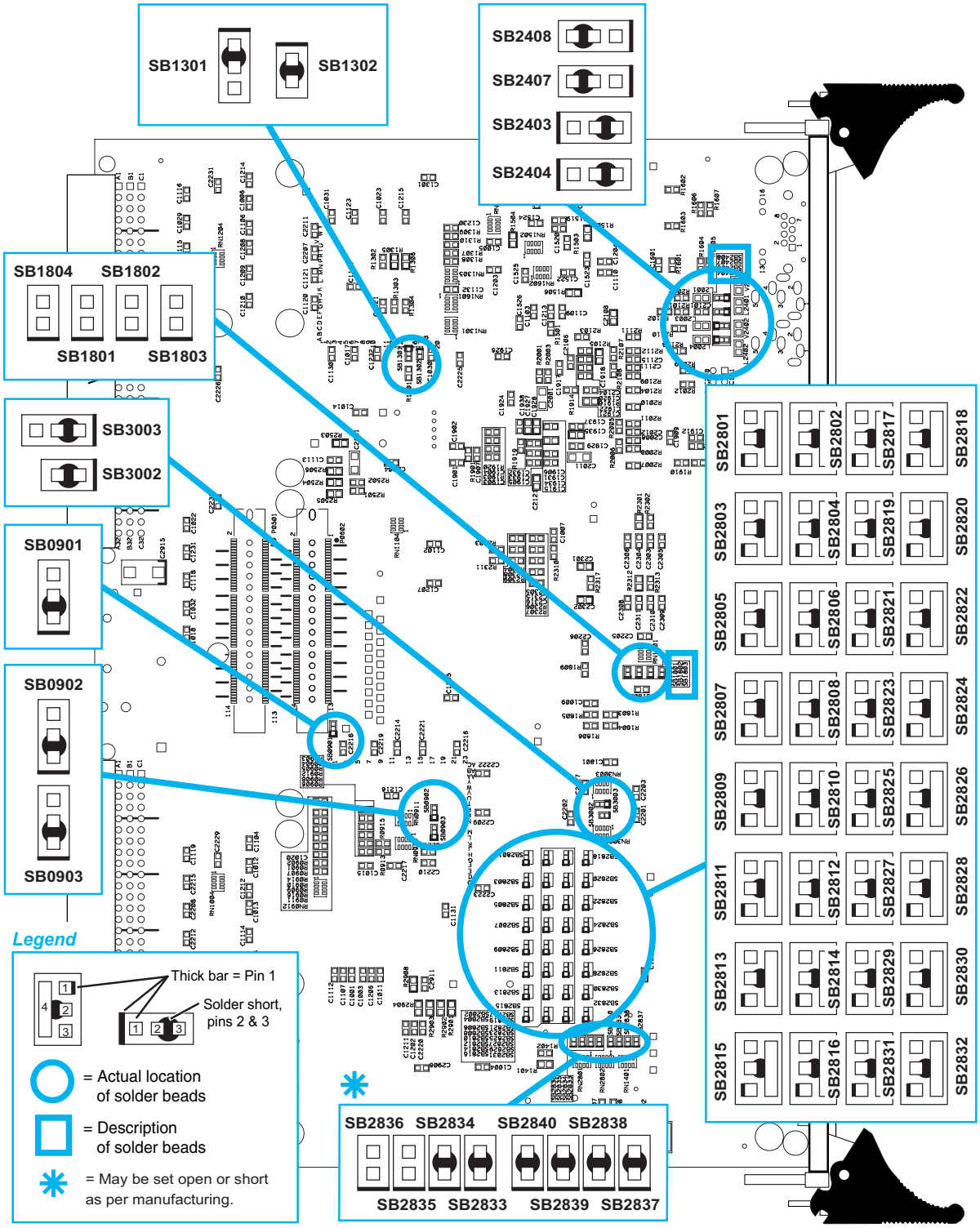


Figure B-4. PMC Carrier Board Solder-Bead Locations (Bottom Side)

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Table B-14. PMC Carrier Board VME P2 Connector SB2801–SB2832 Configuration [a]

VME P2 Connector Row A (see *Table A-9*)				**VME P2 Connector Row C** (see *Table A-9*)			
Pin	**Pin Signal with SB 1–4 Shorted**	**Pin Signal with SB 2–4 Shorted**	**Pin Signal with SB 3–4 Shorted**	**Pin**	**Pin Signal with SB 1–4 Shorted**	**Pin Signal with SB 2–4 Shorted**	**Pin Signal with SB 3–4 Shorted**
A1	PMC1_IO2	Ground	PMC2_IO34	C1	PMC1_IO1	Ground	PMC2_IO33
A2	PMC1_IO4	USR_SW1_8	PMC2_IO36	C2	PMC1_IO3	I2C_CON_SDA	PMC2_IO35
A3	PMC1_IO6	USR_SW1_4	PMC2_IO38	C3	PMC1_IO5	I2C_CON_SCL	PMC2_IO37
A4	PMC1_IO8	USR_SW1_2	PMC2_IO40	C4	PMC1_IO7	Ground	PMC2_IO39
A5	PMC1_IO10	USR_SW1_1	PMC2_IO42	C5	PMC1_IO9	I2C_BUF_VCC	PMC2_IO41
A6	PMC1_IO12	Ground	PMC2_IO44	C6	PMC1_IO11	—	PMC2_IO43
A7	PMC1_IO14	—	PMC2_IO46	C7	PMC1_IO13	—	PMC2_IO45
A8	PMC1_IO16	—	PMC2_IO48	C8	PMC1_IO15	—	PMC2_IO47
A9	PMC1_IO18	SSER_E_TXD	PMC2_IO50	C9	PMC1_IO17	SSER_F_TXD	PMC2_IO49
A10	PMC1_IO20	SSER_E_RXD	PMC2_IO52	C10	PMC1_IO19	SSER_F_RXD	PMC2_IO51
A11	PMC1_IO22	SSER_E_CTS	PMC2_IO54	C11	PMC1_IO21	SSER_F_CTS	PMC2_IO53
A12	PMC1_IO24	SSER_E_RTS	PMC2_IO56	C12	PMC1_IO23	SSER_F_RTS	PMC2_IO55
A13	PMC1_IO26	SSER_E_DTR	PMC2_IO58	C13	PMC1_IO25	SSER_F_DTR	PMC2_IO57
A14	PMC1_IO28	SSER_E_DCD	PMC2_IO60	C14	PMC1_IO27	SSER_F_DCD	PMC2_IO59
A15	PMC1_IO30	SSER_E_DSR	PMC2_IO62	C15	PMC1_IO29	SSER_F_DSR	PMC2_IO61
A16	PMC1_IO32	SSER_E_RI	PMC2_IO64	C16	PMC1_IO31	SSER_F_RI	PMC2_IO63
A17	PMC1_IO34			C17	PMC1_IO33		
A18	PMC1_IO36			C18	PMC1_IO35		
A19	PMC1_IO38			C19	PMC1_IO37		
A20	PMC1_IO40			C20	PMC1_IO39		
A21	PMC1_IO42			C21	PMC1_IO41		
A22	PMC1_IO44			C22	PMC1_IO43		
A23	PMC1_IO46			C23	PMC1_IO45		
A24	PMC1_IO48			C24	PMC1_IO47		
A25	PMC1_IO50			C25	PMC1_IO49		
A26	PMC1_IO52			C26	PMC1_IO51		
A27	PMC1_IO54			C27	PMC1_IO53		
A28	PMC1_IO56			C28	PMC1_IO55		
A29	PMC1_IO58			C29	PMC1_IO57		

Note: Footnotes are described at the end of *Table B-14* on page B-18.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Table B-14. PMC Carrier Board VME P2 Connector SB2801–SB2832 Configuration (Continued)[a]

VME P2 Connector Row A (see *Table A-9*)			
Pin	**Pin Signal with SB 1–4 Shorted**	**Pin Signal with SB 2–4 Shorted**	**Pin Signal with SB 3–4 Shorted**
A30	PMC1_IO60		
A31	PMC1_IO62		
A32	PMC1_IO64		

VME P2 Connector Row C (see *Table A-9*)			
Pin	**Pin Signal with SB 1–4 Shorted**	**Pin Signal with SB 2–4 Shorted**	**Pin Signal with SB 3–4 Shorted**
C30	PMC1_IO59		
C31	PMC1_IO61		
C32	PMC1_IO63		

a—Bold lines outline the various functions available from the VME P2 connector, as defined on page B-15.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Appendix C

Front Panel Diagrams

C.1 Introduction

This appendix contains diagrams of all front panels (faceplates) for each possible model configuration of the USPII*e*-USB. It is intended as a reference to the I/O and monitoring functions of the specific product. See *Table C-1* on page C-1 for a list of USPII*e*-USB models.

Caution: The PCI address of a PMC Module is not necessarily the same as the PMC Module slot number. To avoid confusion, each front-panel illustration in Appendix C has a table correlating PCI address with PMC Module slot.

Table C-1. USPII*e*-USB Model Configurations

Model	Baseboard	TGA3D/3D+ Graphics Board		PMC Carrier Board	
	VME Slot 1	VME Slot 2	VME Slot 3	2-PMC Slots VME Slot 2 or 3	3-PMC Slots VME Slot 2 or 3
USPII*e*-USB / 1	Yes				
USPII*e*-USB / 2G	Yes	Yes			
USPII*e*-USB / 3G2	Yes	Yes	Yes		
USPII*e*-USB / 3GP2	Yes	Yes		Yes (*VME Slot 3*)	
USPII*e*-USB / 3GP3	Yes	Yes			Yes (*VME Slot 3*)
USPII*e*-USB / 2P2	Yes			Yes (*VME Slot 2*)	
USPII*e*-USB / 2P3	Yes				Yes (*VME Slot 2*)

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

C.1.1 Front-Panel Dimensions

All front panels measure 264-mm (10.4”) high by 20-mm (0.8”)wide.

C.1.2 Ejector Handles

The USPII*e*-USB comes with Triple-E-type VME ejector handles. On special order, APW “snap-lock” and Elma IEEE P1101.10 VME64-type replacement handles can be installed.

C.1.2.1 VME64-type Handles Only

When VME64-type handles are installed, make sure to secure all ejector handles with the mating pins that are shipped with the system (see *Figure C-1*). Installation of mating pins between all handles assures that all boards will lock onto and release from the VME rack frame at the same time.

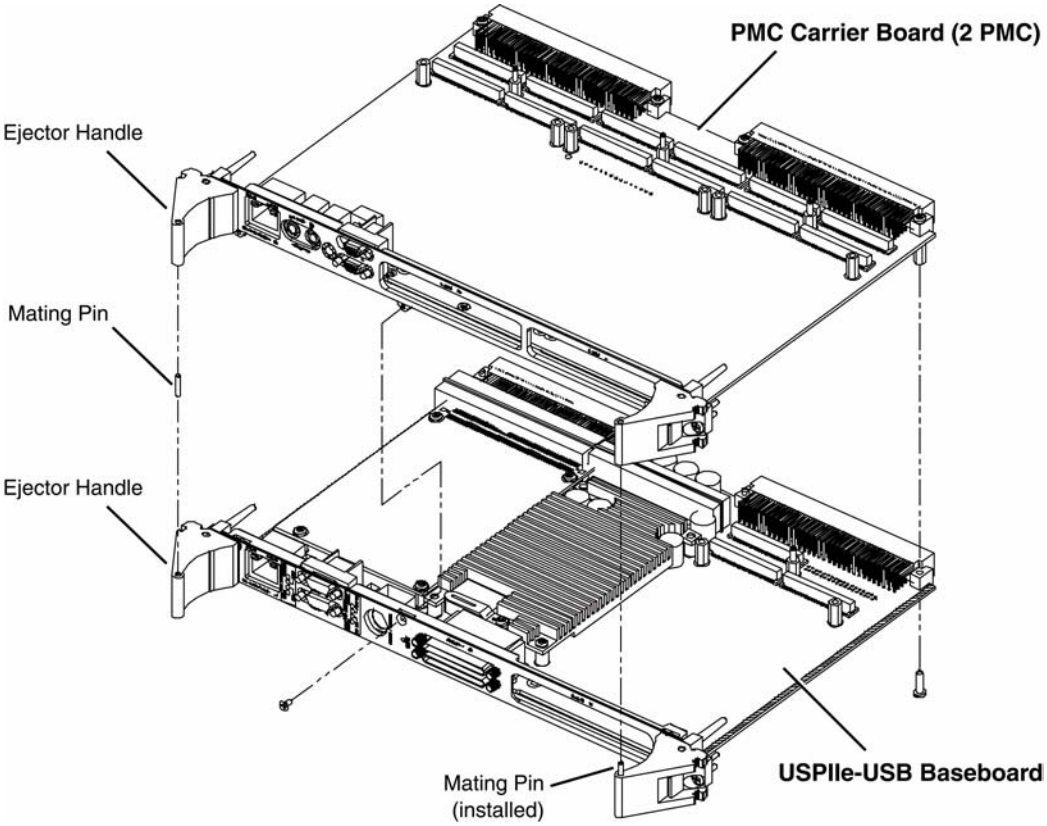


Figure C-1. Placement of Mating Pins on Elma Handles

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

C.1.3 PS/2 and USB Protocols

The USPII*e*-USB offers the option of choosing either PS/2 or USB protocol, accessed through a mini-DIN-8-type or dual-USB-type front-panel connector. This choice must be implemented by Themis before the Baseboard is shipped, since it involves the setting of multiple solder beads (see Appendix B, "DIP-Switch, Jumper-Pin, and Solder-Bead Configurations").

Table C-2 describes devices that are supported by these protocols.

Table C-2. PS/2 and USB Protocols and Connectors

Device Protocol (Solder-Bead Settings)	Type of Connector	
	Mini-DIN-8	**Dual-USB**
PS/2 (Keyboard/Mouse only)	*Adapter required:* DIN-8 → DIN-6, DIN-6 *Part: 110104-002*	
USB (Sun Keyboard/Mouse or any USB device)	*Adapter required:* DIN-8 → USB-0, USB-1 *Part: 110473-001*	• Standard USB cable for each port (keyboard, mouse, or USB device)

Important: If you require a dual-USB port instead of a mini-DIN-8 port on your Baseboard front panel, make sure to specify this at the time of your order.



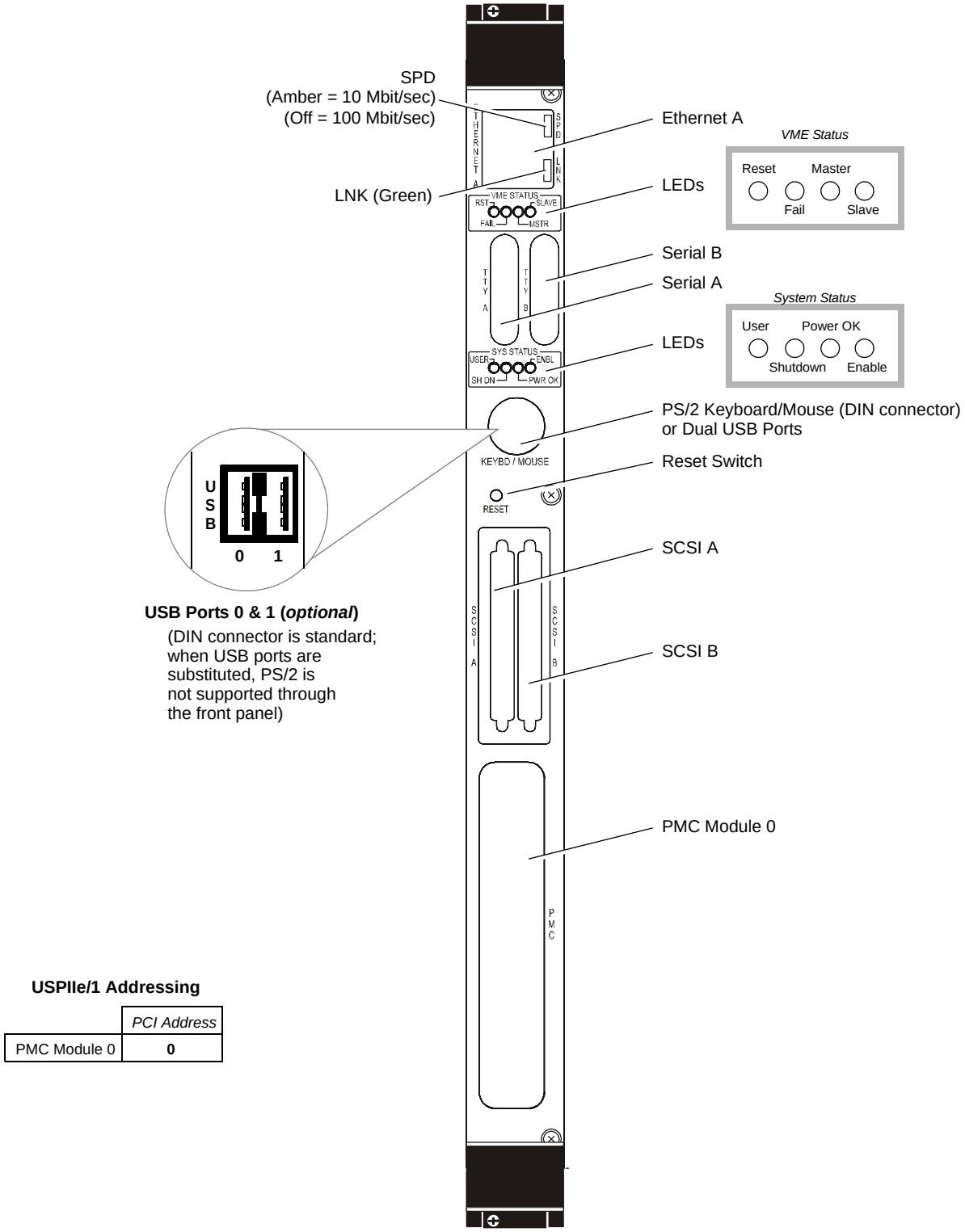
Note: The standard PS/2 keyboard/mouse connector on the Baseboard consists of a single 8-pin mini-DIN socket (see Section A.3.3, "Combination PS/2–USB Connector," on page A-8).
A dual-USB connector may be substituted for the mini-DIN connector by the customer at the time an order is placed for the USPII*e*-USB.

C.2 USPIIe-USB Front Panels

This section contains descriptive graphics of the front panels for each USPII*e*-USB model configuration listed in *Table C-1* on page C-1 (see *Figure C-2* on page C-4, through *Figure C-8* on page C-10).

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

C.2.1 USPIIe-USB/1 (Single VME Slot)



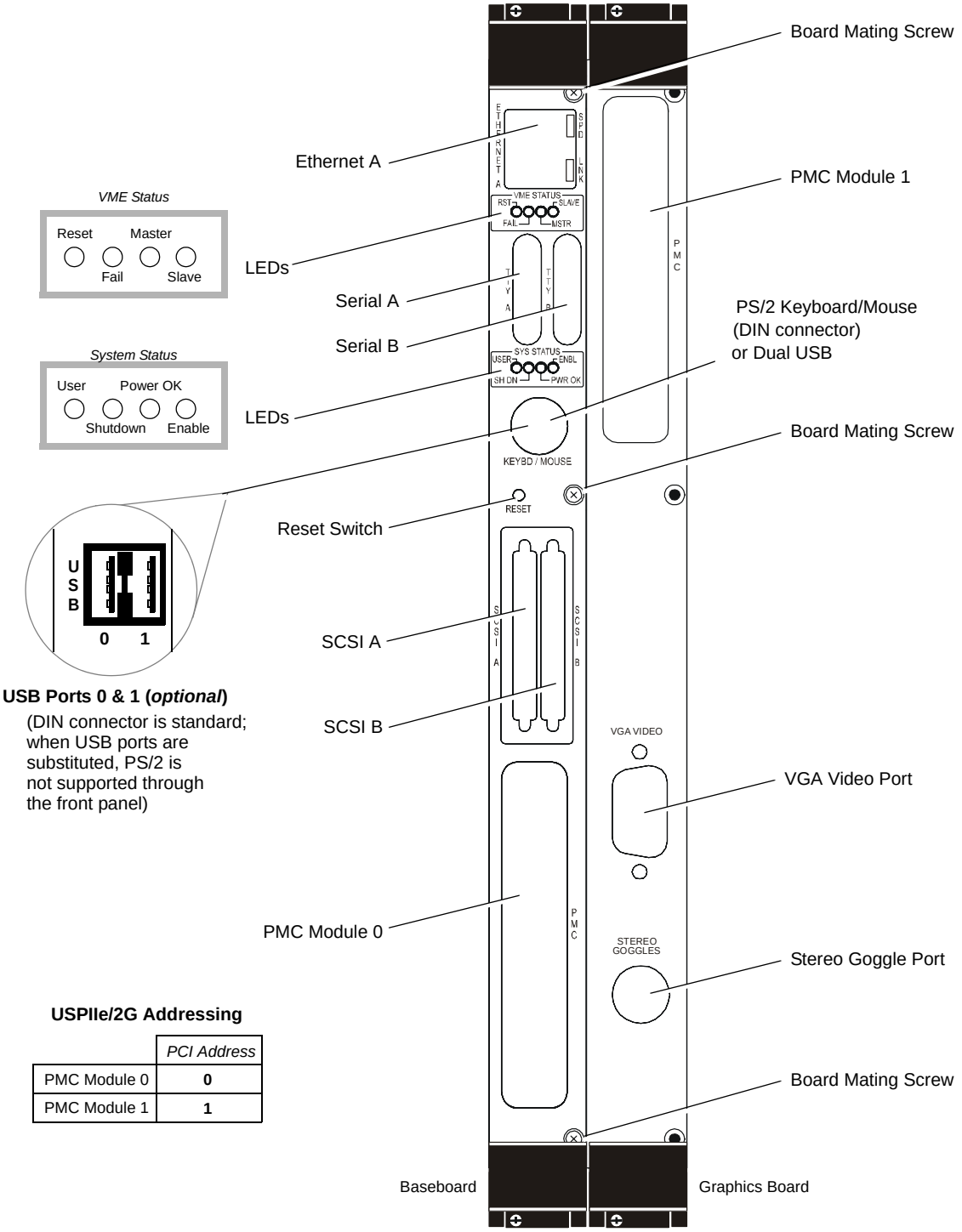
USPIIe/1 Addressing

	PCI Address
PMC Module 0	**0**

Figure C-2. Single-Slot Front Panel (Baseboard)

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

C.2.2 USPIIe-USB/2G—Baseboard & 1 Graphics Board (requires 2 VME slots)



USB Ports 0 & 1 (*optional*)

(DIN connector is standard; when USB ports are substituted, PS/2 is not supported through the front panel)

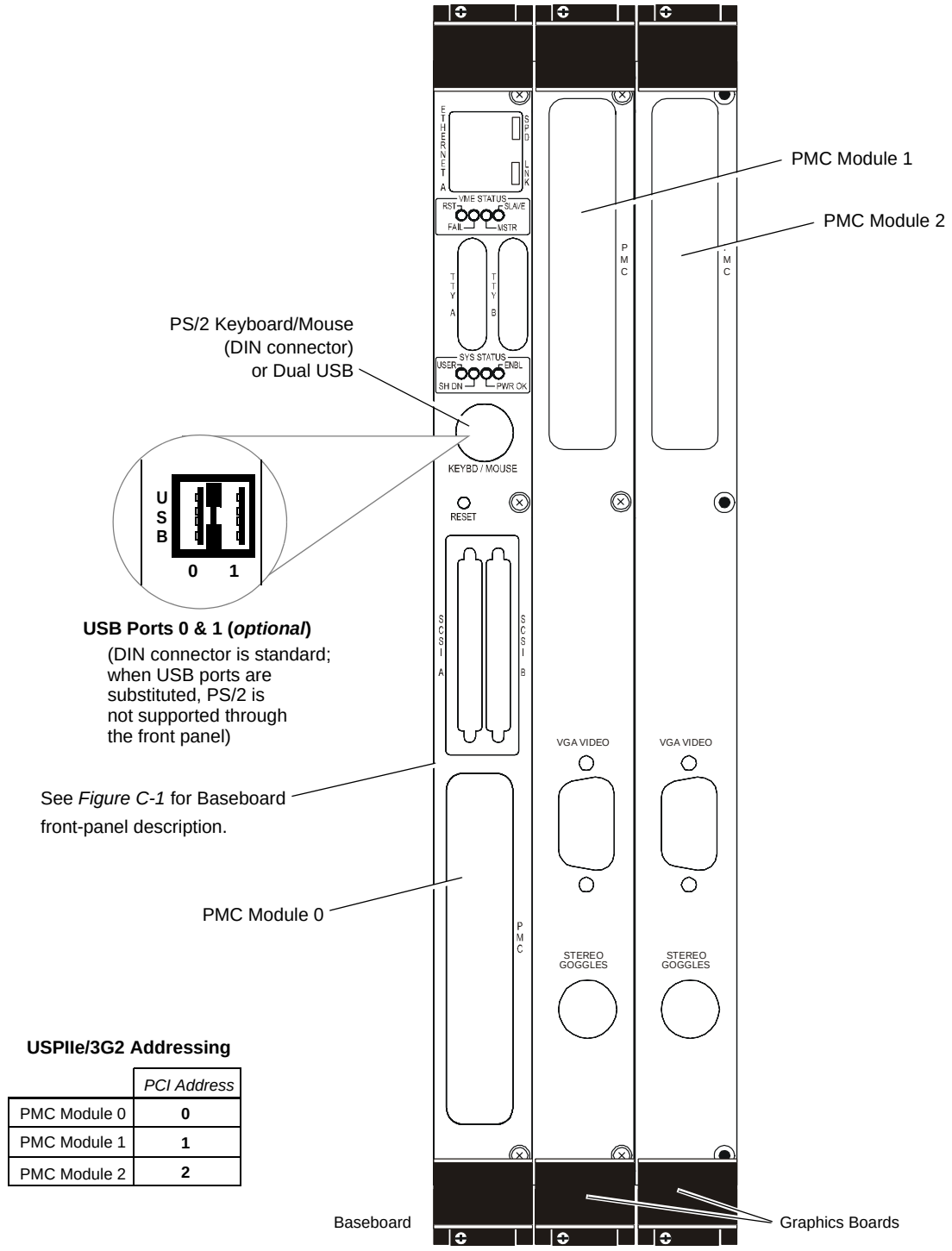
USPIIe/2G Addressing

	PCI Address
PMC Module 0	**0**
PMC Module 1	**1**

Figure C-3. 2-Slot Front Panels (Baseboard and Graphics Board)

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

C.2.3 USPIIe-USB/3G2—Baseboard & 2 Graphics Boards (requires 3 VME slots)



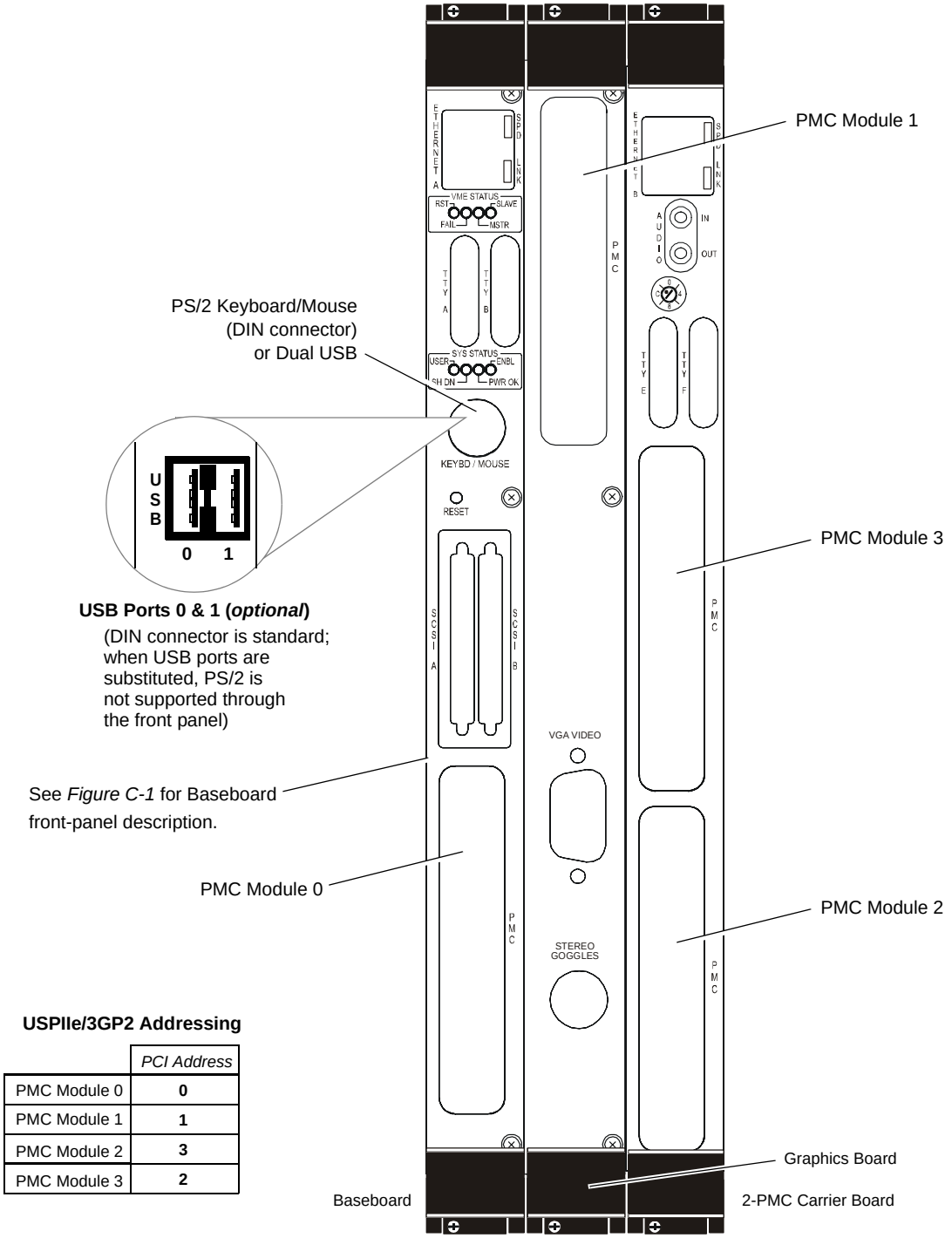
USPIIe/3G2 Addressing

	PCI Address
PMC Module 0	**0**
PMC Module 1	**1**
PMC Module 2	**2**

Figure C-4. 3-Slot Front Panels (Baseboard and 2 Graphics Boards)

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

C.2.4 USPIIe-USB/3GP2—Baseboard, 1 Graphics Board, and 2-PMC Carrier Boards (requires 3 VME slots)



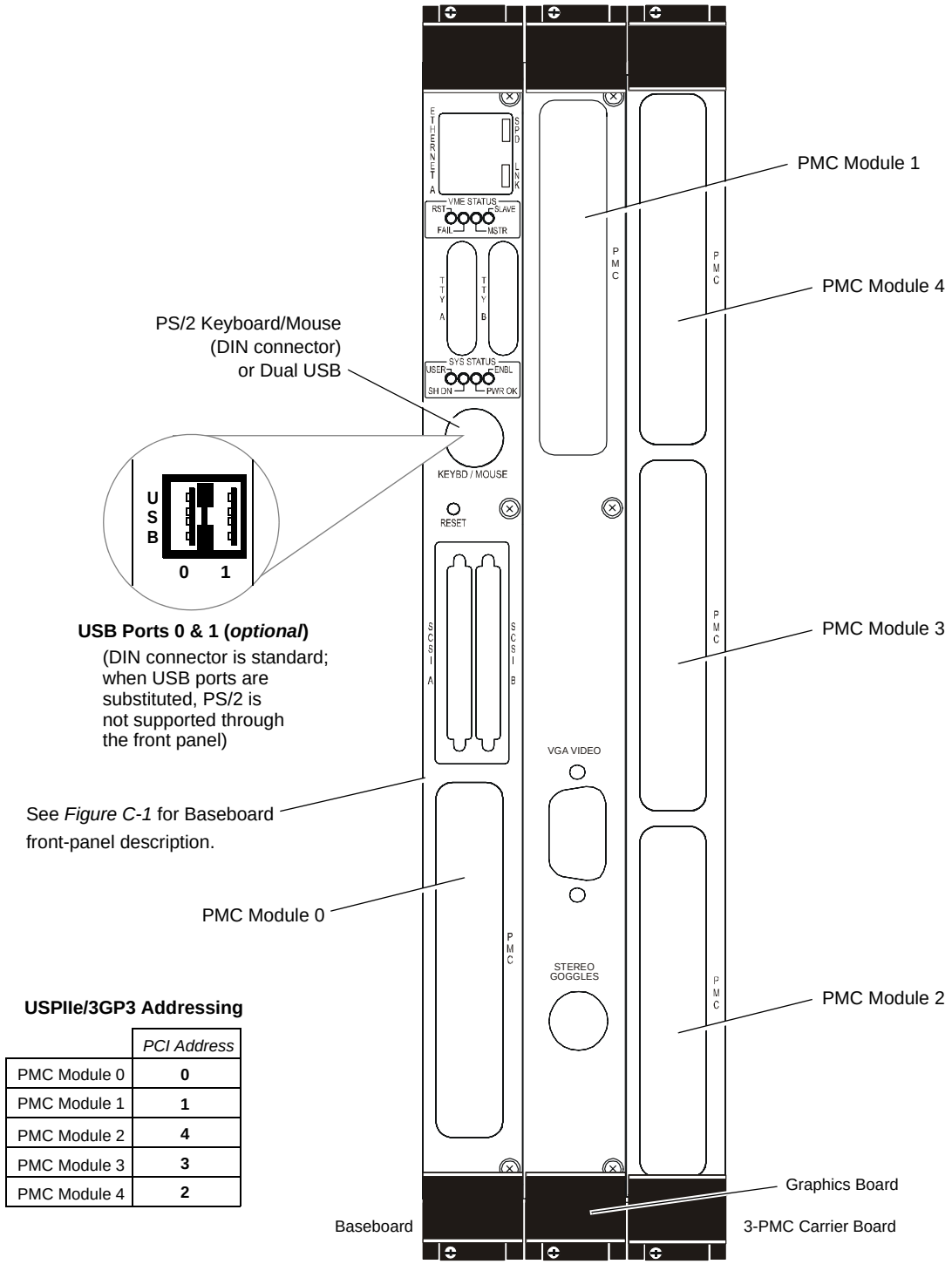
USPIIe/3GP2 Addressing

	PCI Address
PMC Module 0	**0**
PMC Module 1	**1**
PMC Module 2	**3**
PMC Module 3	**2**

Figure C-5. 3-Slot Front Panels (Baseboard, Graphics Board, and 2 PMC Carrier Boards)

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

C.2.5 USPIIe-USB/3GP3—Baseboard, 1 Graphics Board, and 3-PMC Carrier Boards (requires 3 VME slots)



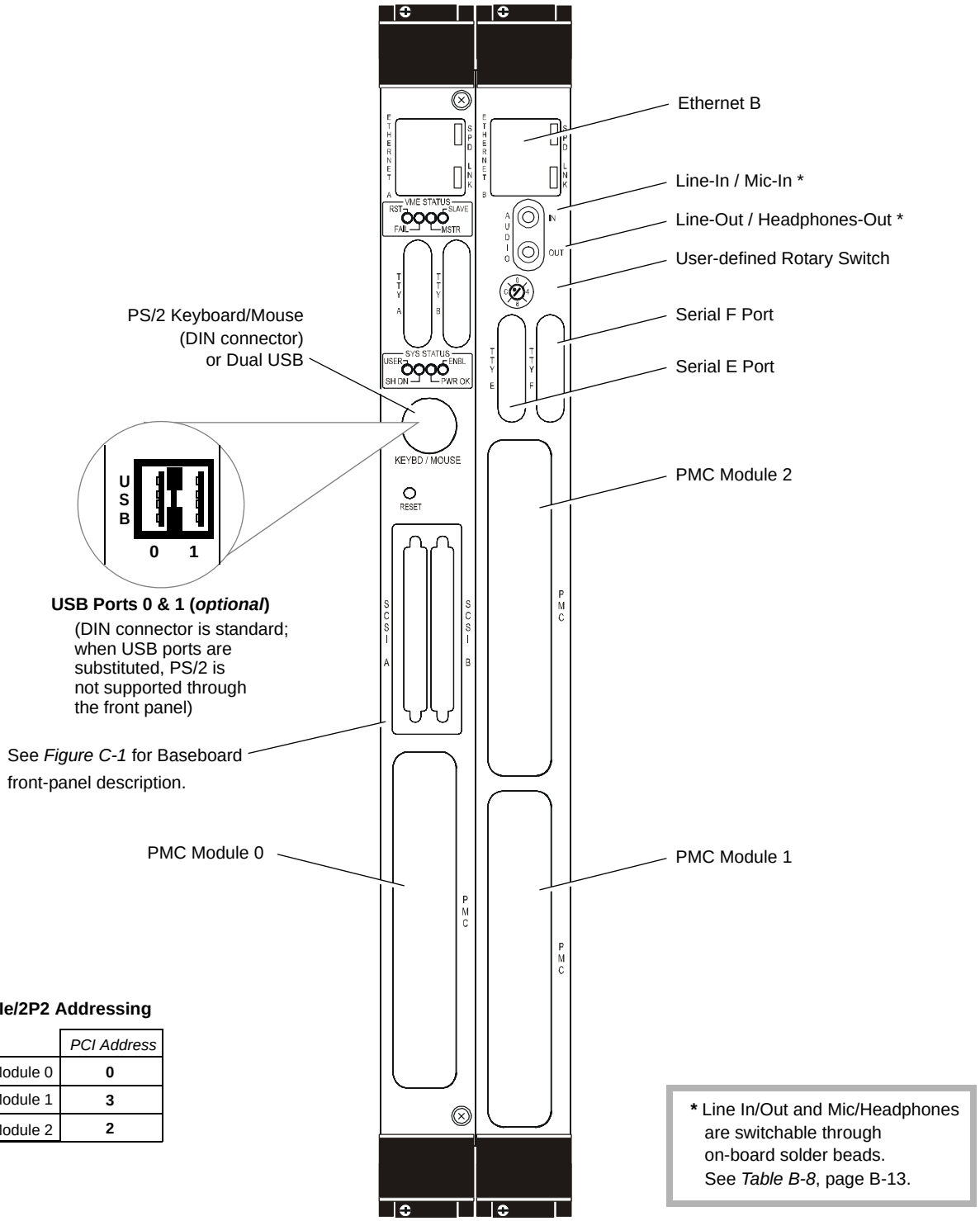
USPIIe/3GP3 Addressing

	PCI Address
PMC Module 0	**0**
PMC Module 1	**1**
PMC Module 2	**4**
PMC Module 3	**3**
PMC Module 4	**2**

Figure C-6. 3-Slot Front Panels (Baseboard, Graphics Board, and 3 PMC Carrier Boards)

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

C.2.6 USPII*e*-USB/2P2 (2 VME Slots)



USPIIe/2P2 Addressing

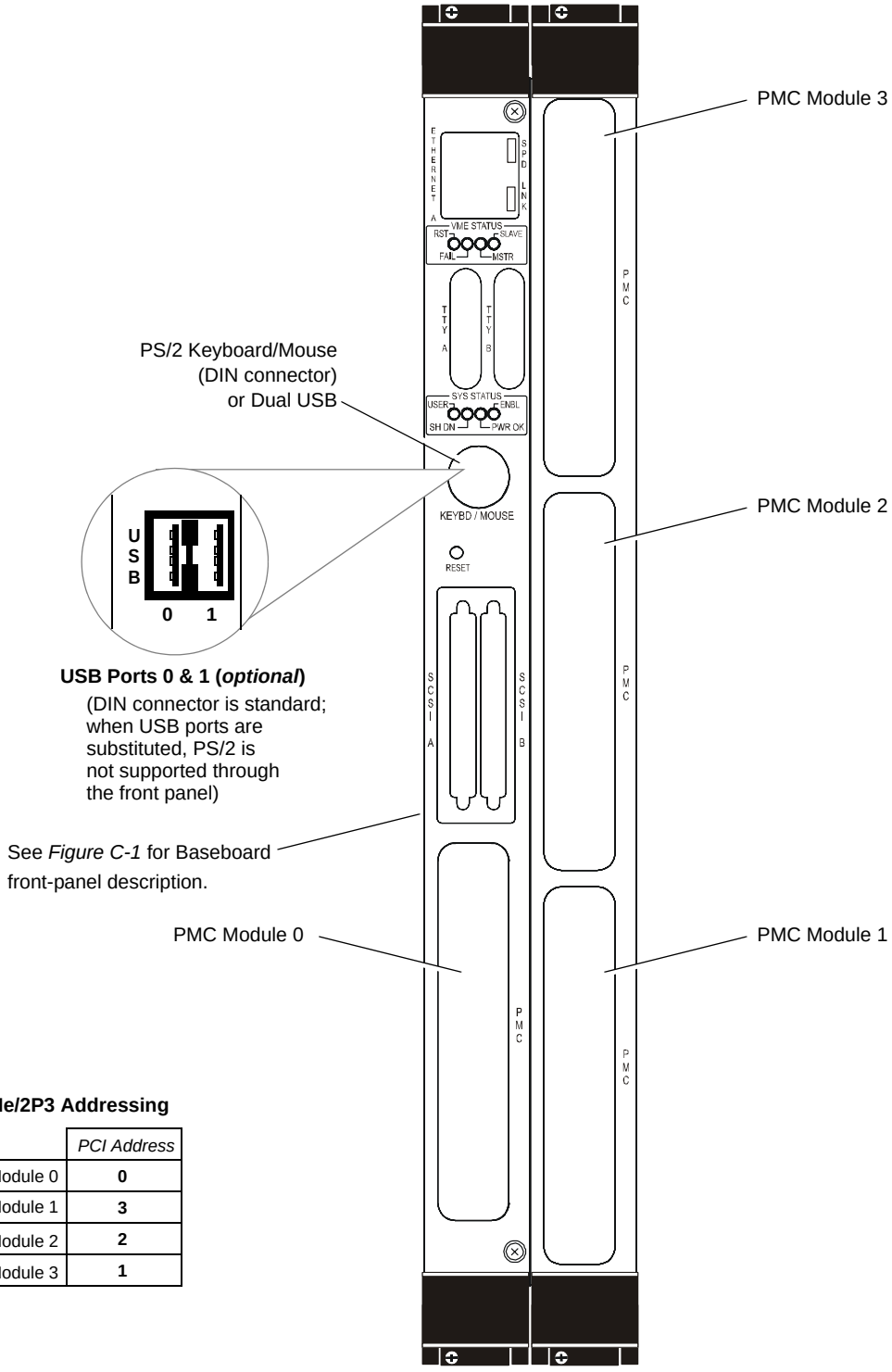
	PCI Address
PMC Module 0	**0**
PMC Module 1	**3**
PMC Module 2	**2**

***** Line In/Out and Mic/Headphones are switchable through on-board solder beads. See *Table B-8*, page B-13.

Figure C-7. Double-Slot Front Panels (Baseboard and 2 PMC Carrier Boards)

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

C.2.7 USPIIe-USB/2P3 (2 VME Slots)



USPIIe/2P3 Addressing

	PCI Address
PMC Module 0	**0**
PMC Module 1	**3**
PMC Module 2	**2**
PMC Module 3	**1**

Figure C-8. Double-Slot Front Panels (Baseboard and 3 PMC Carrier Boards)

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Appendix D

Board Diagrams

The following sections of this appendix contain diagrams of the various boards of the USPII*e*-USB. It is intended as a quick reference to component and connector identification. USPII*e*-USB boards included are:

- Baseboard
- PMC Carrier Board
- Paddle Boards (Standard and Multiple I/O)

See Appendix B, ”DIP-Switch, Jumper-Pin, and Solder-Bead Configurations”, for a description of jumper-pin configurations.

D.1 Baseboard

Figure D-1 on page D-2 identifies front-panel, major board-surface components, and connectors as seen from the top side of the Baseboard.

D.2 PMC Carrier Board

Figure D-2 on page D-3, and *Figure D-3* on page D-4, show major board-surface components and connectors as seen from the top side of the PMC Carrier Board.

D.3 Paddle Boards

Figure D-4 on page D-5, and *Figure D-5* on page D-6, identify the major connectors on the Standard and Multiple I/O Paddle Boards, as viewed from the I/O-connector side and the bottom side.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

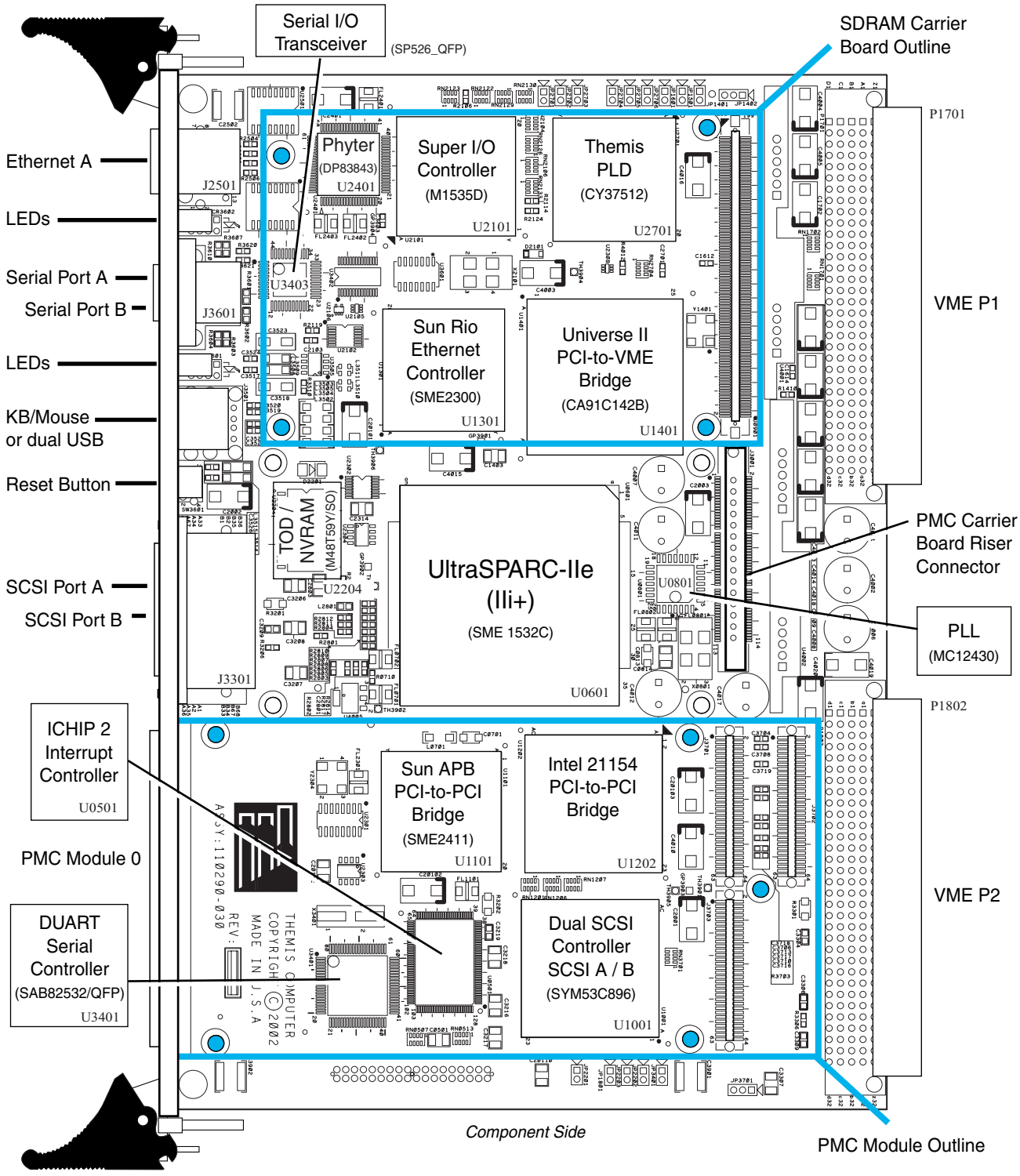


Figure D-1. Baseboard Front-Panel, Component, and Connector Diagram

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

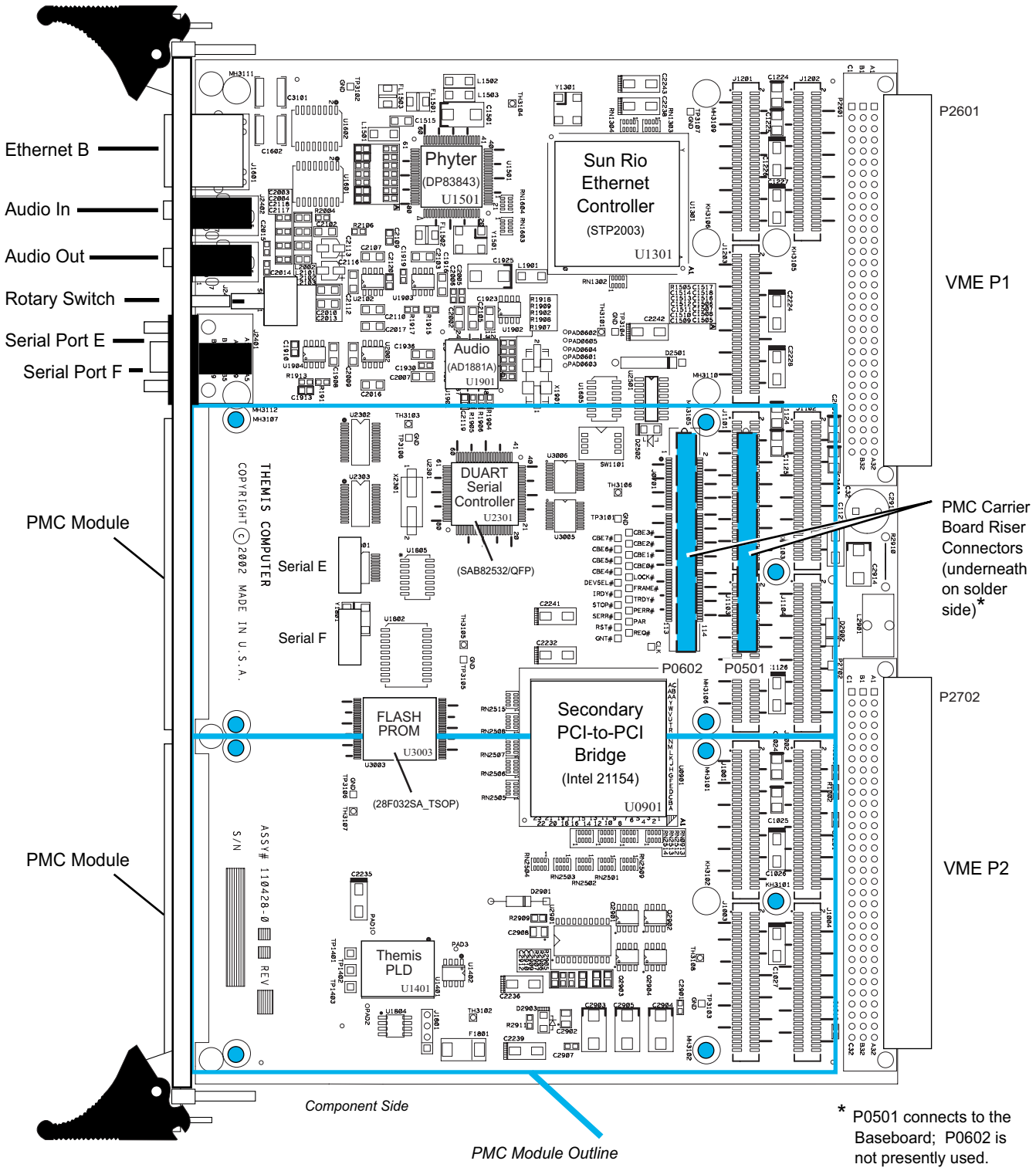


Figure D-2. USPIIe-USB/2P2 PMC Carrier Board Component and Connector Diagram

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

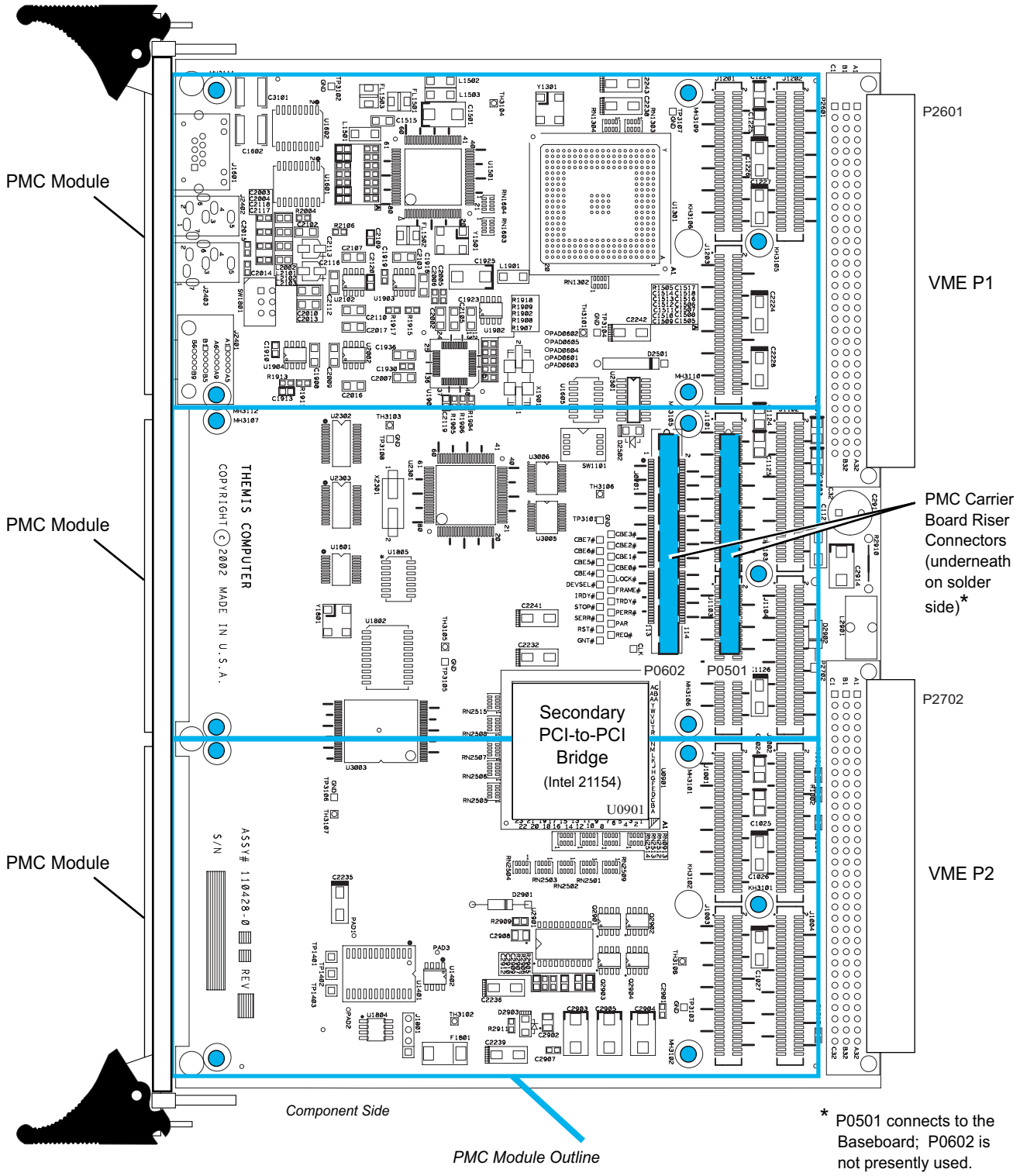
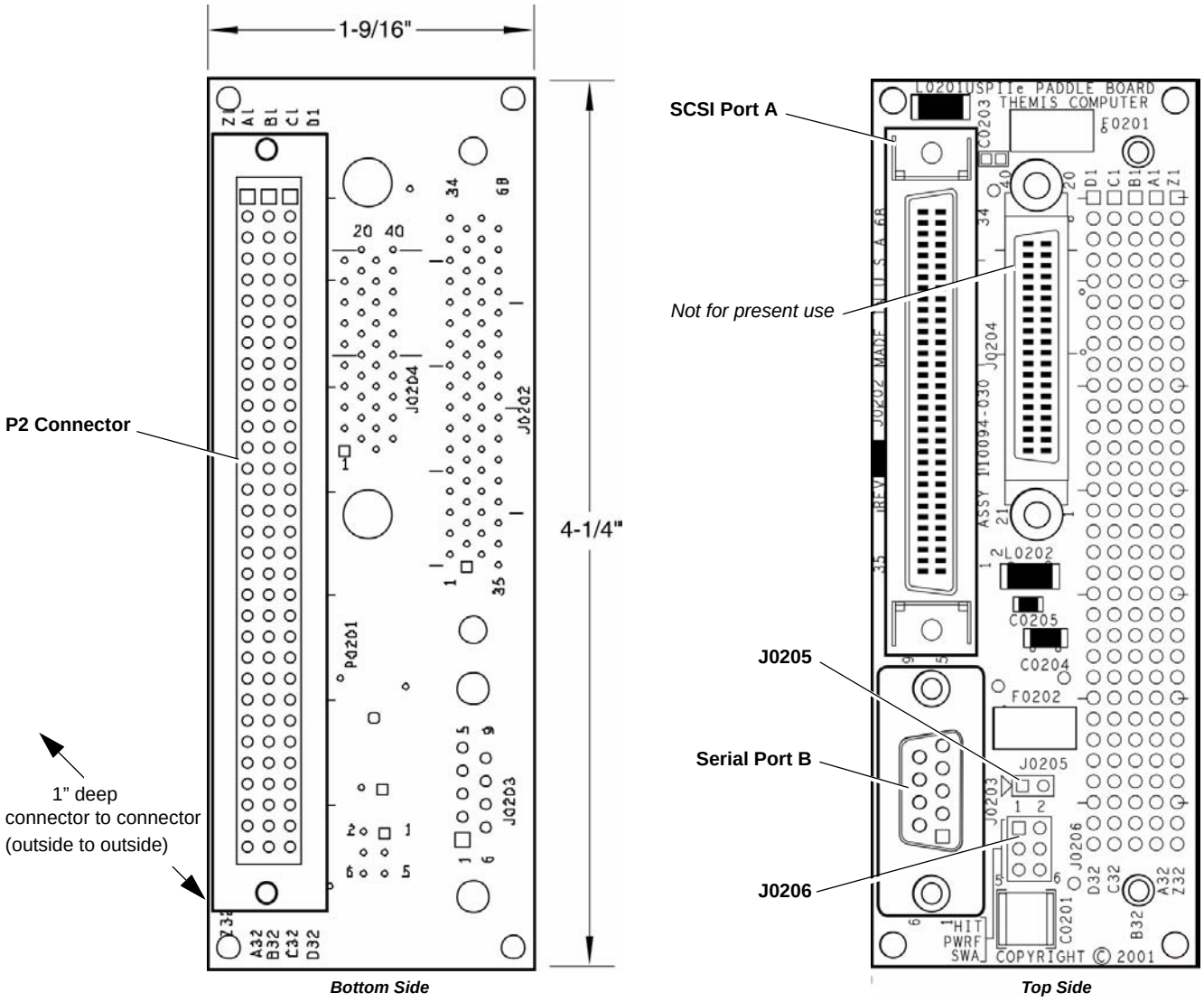


Figure D-3. USPII*e*-USB/2P3 PMC Carrier Board Component and Connector Diagram

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com



Note: Detailed measurements of the Paddle Board are given in *Figure 1-1*, page 1-5 (Chapter 1).

J0205: Pin 1 = 5V fused
Pin 2 = Ground

Figure D-4. Standard Paddle Board (P2 Connector and I/O Connector Sides)

Table D-1. Standard Paddle Board Connector J0206 Pinout

Pin	Function
1	High-temperature trip
2	GROUND
3	Power fail

Pin	Function
4	GROUND
5	Software alarm
6	GROUND

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Caution: Connect the Paddle Board to the **P2 connector** of the VME Backplane only. Connection to the P1 connector will cause malfunctions.

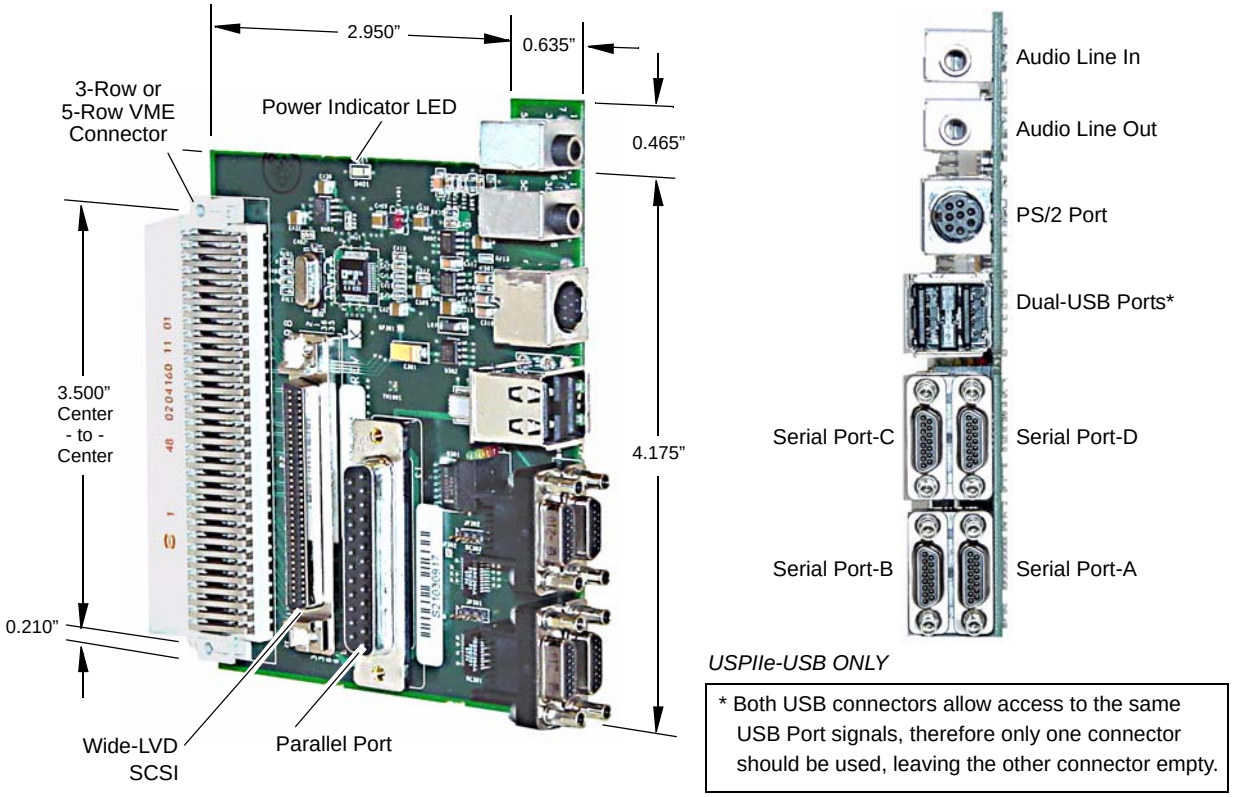


Figure D-5. Multiple I/O Paddle Board (Component and Connector Side)

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Appendix E

Glossary

The terminology used in this manual generally follows industry conventions. The following list defines the specific meanings of words and terms that *may* be used in this manual.

A16: Addressing on address line A[15..0], as specified in ANSI VME64 Specification.

A24: Addressing on address line A[23..0], as specified in ANSI VME64 Specification.

A32: Addressing on address line A[31..0], as specified in ANSI VME64 Specification.

A40: Addressing on address line A[39..0], as specified in ANSI VME64 Specification.

A64: Addressing on address line A[63..0], as specified in ANSI VME64 Specification.

APB: Advanced PCI Bridge

Arbitration: The process of assigning a resource to one of several requestors.

ASI: An abbreviation for “Address Space Identifier.”

Boot: The process of initializing the hardware to execute and run an operating System such as Solaris 0.

cPCI: Compact PCI. An adaptation of the PCI Specification for industrial and/or embedded applications requiring a more robust mechanical form factor than desktop PCI applications.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

CPI: Cycles per Instruction. The number of clock cycles required to execute one instruction.

CTS: Clear to send (DCE to DTE).

DCD (or CD): Data carrier detected (tone from a modem; DCE to DTE).

DCE: Data circuit-terminating/communications equipment (a modem, for example).

Device tree: The OBP probing process constructs a hierarchal representation of the hardware devices that are found on the bus, the host-bus being the root. The device tree includes several device nodes (PCI bus is a device-node).

DMA: Direct Memory Access. A facility of some architectures that allows a peripheral to read and write memory without intervention by the CPU. DMA is a limited form or bus mastering.

DSR: Data set ready (DCE to DTE).

DTE: Data terminal equipment (a computer, terminal, or printer, for example).

DTR: Data terminal ready (DTE to DCE).

DUART: Dual Universal Asynchronous Receiver/Transmitter. *See* UART

Firmware: This is software that stays with the hardware, usually in a PROM or similar device. Referred to as OBP in IEEE 1275 standards. Supported in the USPII*e* implementation, release versions 3.10.x and later. These versions come with the motherboard. The user may upgrade the OBP to a newer version if needed.

FPGA: Field-Programmable Gate Array. A gate array where the logic network can be programmed into the device after its manufacture. An FPGA consists of an array of logic elements, either gates or lookup table RAMs, flip-flops, and programmable interconnect wiring.

GBIC: GigaBit Interface Converter. A hardware module used to attach network devices to fiber-based transmission systems such as Fibre Channel and Gigabit Ethernet. The GBIC converts serial electrical signals to serial optical signals and vice versa.

GHz: Gigahertz (billions of cycles per second, 10^6 cps); unit of frequency.

GUI (Graphical User Interface): The use of pictures rather than words to represent both the input and the output of a program. A program with a GUI runs under some windowing systems.

HVD: High-Voltage Differential; usually shortened to Differential (see LVD).

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Hardware: On the USPII*e*, the CPU module, cables, and peripheral devices are typical examples of hardware.

may: A keyword indicating flexibility of choice with no implied preference.

LED: Light-Emitting Diode.

LVD: Low-Voltage Differential (Device).

IOM: I/O Module.

ISR: In-Service Reprogramming.

MHz: Megahertz (millions of cycles per second, 10^9 cps); unit of frequency.

MII: Medium Independent Interface.

MMU: Memory Management Unit.

NA or **N/A**: Not Applicable.

NC or **N/C**: No Connection.

NVRAMRC: Acronym for *N*on-*V*olatile *R*andom *A*ccess *M*emory *R*un *C*ommand. This refers to the executable OBP script that is written in the NVRAM. Other text information or binary data may exist in the NVRAM, but is not referred as NVRAMRC.

OBP: Acronym for *O*pen*B*oot *P*ROM. This refers to a program that consists of code executable by the UltraSPARC-II*e* CPU. The Code is responsible for initialization of the hardware and booting the system to bring up the Solaris operating system or another operating system such as VxWorks.

PCB: Printed Circuit Board.

PCI: Peripheral Component Interconnect (bus). A high-performance 32- or 64-bit bus with multiplexed address and data lines, as specified in the PCI Local Bus Specification, Revision 2.1, June 1, 1995. The internal bus on the Sun Microsystems UltraSPARC-II*e* is a PCI bus.

PHY: Physical transceiver or sublayer.

Physical Address: An address that maps to real physical memory or I/O device space.

PIO: Programmed I/O. A method of accessing devices under UNIX as special files (as opposed to mapping the physical address range to a process's virtual address space).

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

PLD: Programmable Logic Device.

PLL: Phase-Locked Loop. A feedback control system that automatically adjusts the phase of a locally generated signal to match the phase of an input signal.

PMC: PCI Mezzanine Card.

POR: Power-On Reset.

Probing: A process implemented in the firmware and software to identify onboard hardware devices and add-on cards on the PCI bus. The probing process creates the device-tree.

R0: An abbreviation used to indicate “Read Zero.” When software attempts to read an R0 area, zero will be returned. Writes to R0 are not permitted.

RC (RCK): Receiver clock input (external).

Read Cycle: A VMEbus cycle used to transfer 1, 2, 3, 4, or 8 bytes from a Slave to a Master.

Read-Modify-Write Cycle: A VMEbus cycle used to read from, and then write to, a Slave location without permitting any other Master to access that location during that cycle.

RED_state: The Reset, Error, and *D*ebug state of the UltraSPARC-II*e* processor. The UltraSPARC-II*e* enters the RED_state when PSTATE.RED=1. Refer to Chapter 6, "Resets", for more information.

RI: Ring indicator (ring tone detected; DCE to DTE)).

RIC: Reset, Interrupt, Clock.

RMW: Read, Modify, Write.

RTS: Ready/request to send (DTE to DCE).

RXD (or RD): Receive data (DCE to DTE).

SCSI: Small Computer System Interface.

SCTS: Secondary clear to send (DCE to DTE).

SDCD: Secondary data carrier detected (tone from a modem; DCE to DTE).

SDRAM: *S*ynchronous-*D*ynamic *R*andom *A*ccess *M*emory.

SE: Single-Ended (as in Single-Ended Differential SCSI).

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

SG: Signal ground.

SME: Sun Micro-Electronics.

SO-DIMM: Small-Outline Dual-Inline Memory Module.

Software: A collection of machine-readable information, instructions, data, and procedures that enable the computer to perform specific functions. Typically stored on electronic media.

Solaris: Sun Microsystems, Inc.'s version of the UNIX operating system. In addition to the core operating system, Solaris includes networking software, the Java Virtual Machine, the CDE/Desktop that includes an X11-based windowing environment, and a graphical user interface (GUI).

SRTS: Secondary ready to send (DTE to DCE).

SRXD: Secondary receive data (DCE to DTE).

STXD: Secondary transmit data (DTE to DCE).

TLB: Translation Lookaside Buffer. A hardware cache that contains copies of recently used translations. Separate TLBs reside both in the MMU and the IOM.

TSB: Translation Storage Buffer. A one-level, software data structure that maintains address translation information. Separate TSBs reside both in the MMU and the IOM.

TSOP: Thin Small-Outline Package. A very thin surface-mount chip package with gull-wing pins on the short sides. TSOPs are approximately a third of the thickness of SOJ chips.

TXD (or TD): Transmit data (DTE to DCE).

UART: Universal Asynchronous Receiver/Transmitter. An integrated circuit used for serial communications that contains a transmitter (parallel-to-serial converter) and a receiver (serial-to-parallel converter), each clocked separately.

Virtual Address: An address produced by a processor that maps all systemwide, programmable memory. Virtual addresses usually are translated by a combination of hardware and software to physical addresses, which can be used to access physical memory.

VME: Versa Module Europe. VME is a standard for chassis (rack) based industrial computer systems based on 32- or 64- bit system architectures.

Write Cycle: A VMEbus cycle used to transfer 1, 2, 3, 4 or 8 bytes from a Master to a Slave.

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Appendix F

VME Slot Configurations

The following foldout (see *Figure F-1* on page F-3) illustrates the slot configurations of all models of the USPII*e*-USB, including those with the TGA3D/3D+ Graphics Board and two versions of the PMC Carrier Board (either the 2-PMC Module version or the 3-PMC Module version). All models contain the USPII*e*-USB Baseboard.

Table F-1 summarizes all model configurations.

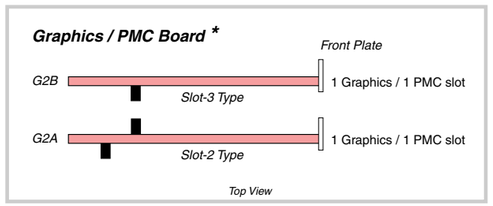
Table F-1. USPII*e*-USB Model Configurations

Model	Baseboard	TGA3D/3D+ Graphics Board		PMC Carrier Board	
	VME Slot 1	VME Slot 2	VME Slot 3	2-PMC Slots VME Slot 2 or 3	3-PMC Slots VME Slot 2 or 3
USPII*e*-USB / 1	Yes				
USPII*e*-USB / 2G	Yes	Yes			
USPII*e*-USB / 3G2	Yes	Yes	Yes		
USPII*e*-USB / 3GP2	Yes	Yes		Yes (*VME Slot 3*)	
USPII*e*-USB / 3GP3	Yes	Yes			Yes (*VME Slot 3*)
USPII*e*-USB / 2P2	Yes			Yes (*VME Slot 2*)	
USPII*e*-USB / 2P3	Yes				Yes (*VME Slot 2*)

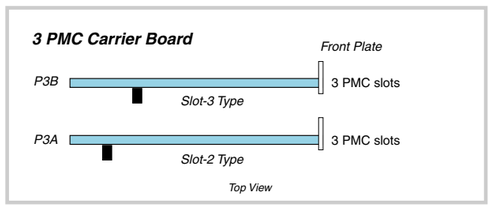
Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

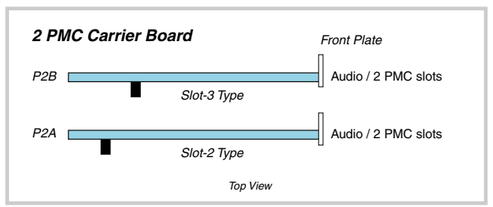
USPIIe-USB



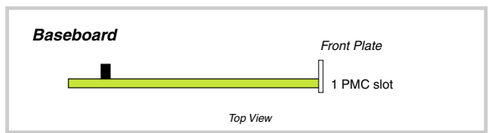
VME Slot 2 or 3



VME Slot 2 or 3



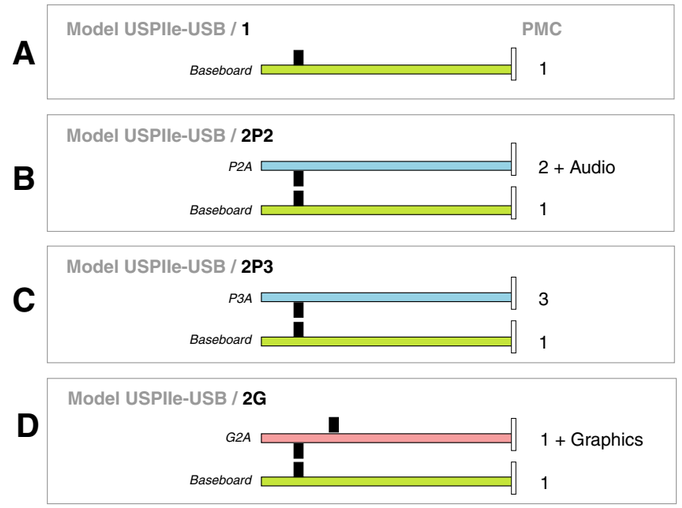
VME Slot 2 or 3

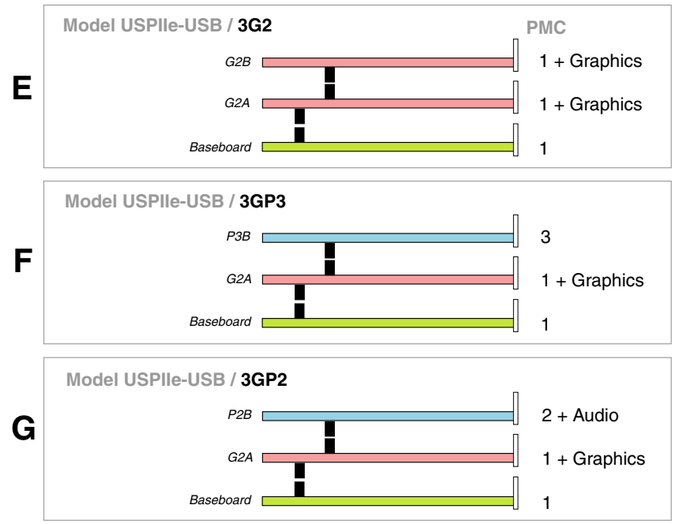


VME Slot 1

* Approved PMC Cards supported on Themis Graphics Board:
1 _____
2 _____
3 _____
4 _____

10/2002





VME Slots	1
PMC Cards	1
Graphics Cards	0
Audio I/O	0

VME Slots	2
PMC Cards	3
Graphics Cards	0
Audio I/O	1

VME Slots	2
PMC Cards	4
Graphics Cards	0
Audio I/O	0

VME Slots	2
PMC Cards	2
Graphics Cards	1
Audio I/O	0

VME Slots	3
PMC Cards	3
Graphics Cards	2
Audio I/O	0

VME Slots	3
PMC Cards	5
Graphics Cards	1
Audio I/O	0

VME Slots	3
PMC Cards	4
Graphics Cards	1
Audio I/O	1

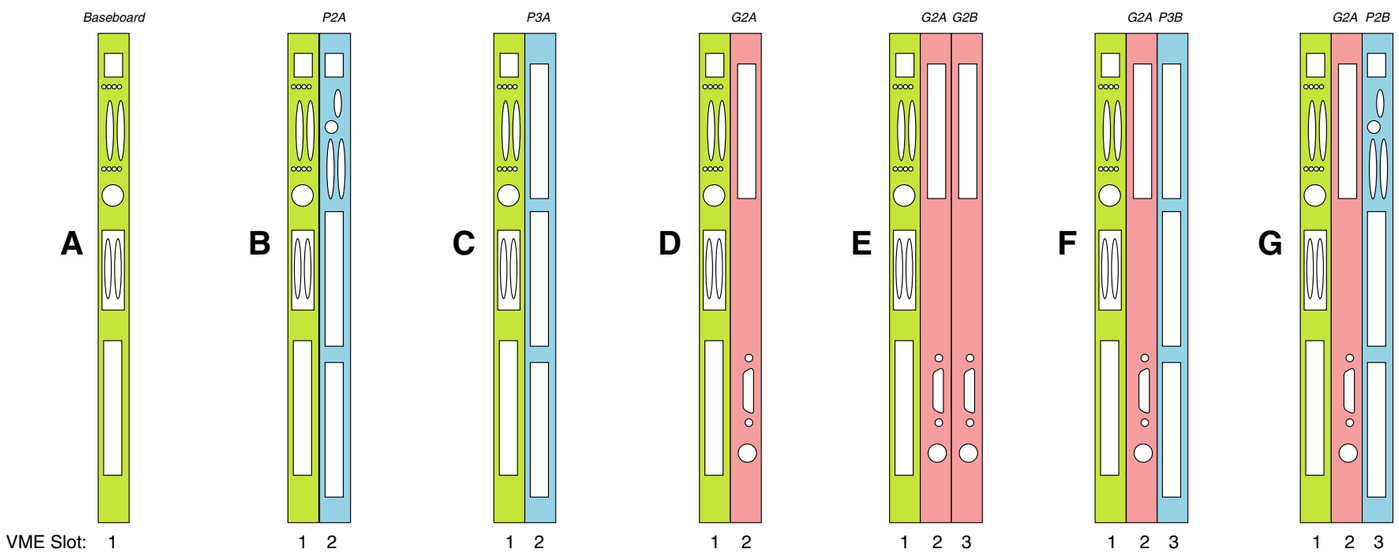


Figure F-1. USPIIe VME Slot Configurations

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Index

Numerics

10/100Base-T Ethernet *1-10*
2-Level Watchdog *5-1, 5-3, 6-5*
2P2 and 2P3 boards *A-11*
  diagram of 2P2 PMC Carrier Board (component and connector side) *D-3*
  diagram of 2P3 PMC Carrier Board (component and connector side) *D-4*
3.3V standby signal *B-8*
3-Slot front panels (baseboard, graphics board, and 2 PMC Carrier Boards) *C-7*
8-Pin Mini-DIN *A-8*

A

Acer Super I/O Controller *3-6*
address map
  PLD register *5-2*
Advanced PCI Bridge *3-4*
air flow *2-13*
altitude range *2-13*
APB. *See* Advanced PCI Bridge
audio
  connectors *A-22*
    paddleboard *A-28*
  headphones *2-6*
  Line In *2-6, 2-7*
  Line Out *2-6, 2-7*
  Mic In *2-6*
  solder-bead settings, PMC Carrier Board *B-13*
auxiliary functions *2-12*
  specifications *2-12*

B

back panel
  VMEbus P2 interface *2-3*
backplane
  jumper settings *2-8*
baseboard *A-5*
  back panel VMEbus P2 interface *2-3*
  diagram of, front-panel (component and connector side) *D-2*
  front panel *2-3*
  jumper pin locations, illustration of *B-6*
  jumper pins *B-3*
  SCSI A and B connectors *A-5*
  solder beads *B-7*
    illustration of locations *B-10*
    See also solder beads
  VME P1 connector *A-1*
  VME P1 connector pinouts *A-2*
  VME P2 connector *A-3*
  VME P2 connector pinout *A-4*
battery *3-6*
  replacement *1-14*
  TOD/NVRAM *1-14*
battle mode *B-8*
block diagram
  PMC Carrier Board *2-5*
  UltraSPARC-IIe CPU *3-2*
  USPIIe-USB Baseboard *2-2*
  See also diagrams
board diagram *D-6*
board type *1-1*
boot control *5-2*
boot-device settings, baseboard jumper pins *B-5*
bridges
  PCI-to-PCI *3-4*
bus fields, PCI *4-12*

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

C

cables
attaching *1-9*
cache *3-1*
CAS *3-7*
Chapter Overview *xx*
comment card *1-2*
configurations, USPIIE-USB *1-2*
connector pinouts *A-1*
console port (TTYA) *1-9*
control fields
PCI bus target images *4-14*
special PCI bus target image *4-15*
VMEbus slave images *4-12*
controller
Acer Super I/O *3-6*
DMA *4-19*
Seimens SAB 82532 *3-6*
Sun Rio I/O *3-5*
Symbios SCSI *3-5*
CPU *3-1*
speed settings *2-1*
solder beads *B-9*
customer comments *xviii*, *xxv*
customer support *xx*, *xxiv*

D

diagrams
2P3 PMC Carrier Board (component and connector side) *D-4*
2-slot front panels (baseboard and graphics board) *C-5*
3-slot front panels (baseboard and 2 graphics boards) *C-6*
3-slot front panels (baseboard, graphics board, and 2 PMC Carrier) *C-7*
3-slot front panels (baseboard, graphics board, and 3 PMC Carrier Boards) *C-8*
baseboard front panel (component, and connector side) *D-2*
double-slot front panels (baseboard and 2 PMC Carrier Boards) *C-9*
double-slot front panels (baseboard and 3 PMC Carrier Boards) *C-10*
Multiple I/O Paddle Board (component and connector side) *D-6*
single-slot front panel (baseboard) *C-4*
Standard Paddle Board (P2 connector and I/O connector sides) *D-5*
USPIIe-USB/2P2 PMC Carrier Board (component and connector side) *D-3*
dimensions
front panel *C-2*
DIN Settings *1-3*
DIP switches *B-1*
PMC Carrier Board *B-1*
illustration of *B-2*
DMA channel (Universe II) *4-3*
DMA controller *4-19*
DMAFIFO *4-4*

E

ECC. *See* Error Correction Code
ejector handles *C-2*
environmental specifications *2-13*
Error Correction Code (ECC) *3-7*
Ethernet *1-10*
Port A *2-3*
connector *A-7*
pinout *A-7*
Port B *2-6*
connector *A-22*
pinout *A-22*

F

fields
PCIbus *4-12*
VMEbus *4-13*
first slot detector *4-5*

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Flash
EPROM *3-6*
mapping *5-2*
memory *2-12*, *3-6*
FORTH toolkit *3-6*, *3-9*
front panel
baseboard I/O functions *2-3*
diagrams *C-4–C-10*
See also diagrams
dimensions *C-2*
DIN solder-bead settings *B-9*
LEDs *A-10*
PMC Carrier Board I/O *2-4–2-6*

G

getting started *xx*
glossary *E-1*
graphics board, TGA3D/3D+ *1-1*, *2-6*
model configurations *C-1*, *F-1*

H

handles
ejector *C-2*
Elma
placement of mating pins, illustration of *C-2*
VME64-type *C-2*
high-temperature trip signal *2-7*
humidity range *2-13*

I

I/O signals *1-12*
I/O subsystem *2-9*
specifications *2-10*
ICHIP-2 *3-3*
In case of difficulties *xxiv*
Intel 21154 PCI-to-PCI bridge *3-4*
intended audience *xix*
interrupt
Universe II *4-17*
interrupt controller *3-3*
interrupters
VME and PCI *4-17*

J

jumper pins *B-1*
baseboard *B-3*
boot-device settings *B-5*
combined JP1401/JP1402 configurations *B-4*
illustraton of jumper locations *B-6*
SCSI A access definition *B-5*
PMC Carrier Board *B-5*
jumper settings, backplane *2-8*

K

keyboard/mouse (PS/2 or USB) port *1-3*, *2-3*, *A-8*

L

LEDs *A-1*
front panel
color interpretation *A-10*
system status *2-12*
VME status *2-12*
lithium battery *1-14*, *3-6*
local 32-bit PCI bus *3-5*

M

mailbox registers, Universe II *4-18*
major components *3-1*
mating pins
on Elma handles, illustration of *C-2*
memory
configurations *2-3*
specifications *2-9*
subsystem *3-7*
memory mapping
special PCI target image *4-17*
memory module *2-3*
connector *A-28*, *A-29*
solder beads *B-9*

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Mini-DIN connector *1-3*, *A-8*
pinouts *A-8*
MISC_CTL *4-5*
Miscellaneous Control Register (Universe II). *See* MISC_CTL
miscellaneous I/O *1-12*
Multiple I/O Paddle Board *1-7*, *2-7*, *A-26*
See also paddle board, Multiple I/O

N

Non-Volatile RAM (NVRAM) *1-14*
NVRAM *1-14*, *3-6*
specifications *2-12*

O

OBP
commands *1-13*
environment variables *1-13*, *2-6*
to program the VME Interface *1-13*
See also OpenBoot PROM
OpenBoot Command *1-11*
OpenBoot PROM *1-13*, *3-9*

P

paddle board *1-4*, *1-7*, *2-7*
connections *1-9*, *1-10*, *1-11*
illustration of board installed *1-5*
installation *1-7*
Multiple I/O *1-7*, *2-7*, *A-26*, *D-6*
connectors for *A-26–A-28*
illustration of *1-8*, *A-26*
SCSI Port A connector pinouts *A-24*
SCSI termination *1-4*
Serial Port B connector pinouts *A-25*
Standard *1-7*, *2-7*
board diagram (P2 connector and I/O connector sides) *D-5*
connector J0206 pinout *D-5*
connectors for *A-23–A-25*
parallel port (printer) *1-10*, *2-3*, *2-7*
PC-133 timing *3-7*
PCI
Configuration Base Address 0 Register (PCI_BS0) *4-9*
PCI bus *3-4*
fields *4-11*, *4-15*
fields for PCI bus target images *4-14*
fields for special PCI bus *4-15*
fields for target images *4-12*
memory mapping, special PCI target image *4-17*
special target image registers *4-16*
target channel (Universe II) *4-3*
target images *4-12*, *4-14*, *4-15*
control fields *4-14*
PCI_BS0. *See* PCI, Configuration Base Address 0 Register
PCI-to-PCI bridge *3-4*
Intel 21154 *3-4*
peripheral devices *1-9*
PLD *3-6*, *5-1*
registers *5-2*
PMC (Expansion) Module Slots *1-10*
PMC Carrier Board *2-4*, *3-9*, *A-11*
block diagram *2-5*
connector *A-12*
connector pintouts *A-13*
DIP switches *B-1*
illustration of *B-2*
jumper pins *B-5*
model configurations *xviii*
solder beads *B-11*
illustration of locations *B-16*
revision settings *B-14*
selection settings *B-14*
User I/O connectors *2-4–2-6*, *A-16*
VME P2 connector *A-14*
SB2801–SB2832 configuration *B-17*
VME P2 connector pinouts *A-15*
VME P2 connector SB2801–SB2832 configuration *B-15*

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

PMC Module
Module 0 *2-3*
Module 1 *2-6*
Module 2 *2-6*
Module 3 *2-6*
Slot 0 connector *A-10*
Slot 1, 32-Bit User I/O configuration *A-18*
Slot 1, 64-Bit User I/O configuration *A-17*
Slot 2, 32-Bit User I/O configuration *A-19*
Slot 3, 0-Bit User I/O configuration *A-20*
Polyswitch Vcc power fuse *2-7*
POR *6-2*, *6-4*, *6-5*
See also Power-On-Reset
power fail signal *2-7*
power management *5-4*
power requirements *2-13*
Power-On-Reset (POR) *5-4*, *6-2*, *6-5*
power-up options
Universe II *4-7*
P-Reset *6-3*, *6-4*
printer port *1-10*
processor
and memory subsystems *2-8*
specifications *2-8*
speeds *2-1*
UltraSPARC-IIe *3-1*
product registration *xxiv*
Programmable Logic Device. *See* PLD
protocols
PS/2 and USB *C-3*
PS/2–USB connector *1-3*, *A-8*
pinouts *A-8*
protocols *C-3*
push-button reset (P-Reset) *6-4*, *A-11*

R

RDFIFO *4-3*
reader comment card *1-2*
references, related *xxi*
register access at power up *4-7*
registering Your SPARC 5/64-2S2E *xxiv*
registers
MISC_CTL *4-5*
PLD *5-2*
special PCI target image *4-16*
registration, product *xxiv*
related references *xxi*
reset architecture *3-3*
resets *6-1*
control registers *6-6*
Externally Initiated Reset (XIR) *6-3*
power management *6-4*
priorities *6-2*
push-button (P-Reset) *6-4*, *A-11*
request signals *6-2*
Software Initiated Reset (SIR) *6-3*
software POR *6-5*
software XIR *6-6*
sources *6-4*
system and P-Reset *6-3*
VMEbus *6-4*
Watchdog (WDR) *6-3*
RIC. *See* USPIIe-USB Reset, Interrupt, and Clock
RJ45 *1-10*
RMW cycle *4-3*
Round-Robin arbitration *4-6*
RXFIFO *4-3*

S

SCSI
controller *1-4*
termination *1-4*, *1-6*
SCSI Ports
Port A *2-3*, *2-7*
connector *A-5*
paddle board connector *A-23*
paddle board connector pinouts *A-24*
Ultra3 LVD *2-3*
Port B
connector *A-5*
Ultra3 LVD *2-3*

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Ports A and B *1-11*
connector *A-5*
connector pin signals *A-6*
SDRAM memory subsystem *3-8*
Seimens SAB 82532 *3-6*
semaphores *4-18*
Serial (TTY) Ports
Port A *2-3, A-9*
connector pinouts *A-9*
Port B *2-3, 2-7, A-9*
connector pinouts *A-9*
paddle board connector *A-24*
paddle board connector pinouts *A-25*
Port C *2-3*
Port D *2-3*
Port E *2-4*
Port F *2-4*
Ports A and B *1-9*
connector *A-9*
connector pinouts *A-9*
Ports C and D *1-9*
Ports E and F *1-10, A-21*
connector *A-21*
connector pinouts *A-21*
SGS Thomson Microelectronics *3-6*
signals
high-temperature trip *2-3*
power fail *2-3*
SIR *6-2*
slave images *4-9*
slot configurations
diagram of VME *F-3*
VME *F-1*
software alarm signal *2-7*
software XIR *6-6*
solder beads *B-1*
baseboard *B-7*
illustration of *B-10*
CPU speed settings *B-9*
front-panel DIN settings *B-9*
memory module *B-9*
PMC Carrier Board *B-11*
audio I/O settings *B-13*
illustration of *B-16*
revision settings *B-14*
selection settings *B-14*
selectable configurations, PMC module slot User I/O *A-16*
VME P2 connector *B-14*
VME P2 pin signal interpretation *B-15*
SPARC V9 *3-1*
specifications
auxiliary functions *2-12*
environmental *2-13*
I/O subsystem *2-10*
memory *2-9*
processor *2-8*
USPIIe-USB *2-1*
Standard Paddle Board. *See* paddle board, Standard
Status LEDs
System *A-10*
VME *A-10*
stereo jack *2-7*
Sun documents *xxiii*
Sun Rio I/O controller *3-5*
switches *A-1*
Symbios SCSI controller *3-5*
SYSCON *4-5, B-3*
SYSRST, VME *1-13*
system controller (Universe II) *4-6*
system reset *6-2, 6-4*
system specifications *2-8*
system status LEDs *A-10*

T

target images
PCI bus *4-12, 4-14*
special PCI *4-15*
temperature
management *5-5*
range *2-13*

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

sensor *2-12*
subsystem *5-5*
TGA3D/3D+ *2-6*
model configurations *xviii*, *1-1*, *C-1*, *F-1*
Time-of-Day (TOD) clock. *See* TOD
TOD *1-14*, *3-6*
TOD/NVRAM battery *1-14*, *3-6*
traps *6-1*
Tundra Universe II *3-5*, *4-1*
TXFIFO *4-4*

U

UltraSPARC-IIe
CPU block diagram *3-2*
processor *3-1*
reset control register *6-6*
Universe II *3-5*
architectural diagram *4-4*
automatic slot identification *4-6*
features *4-1*
hardware power-up options *4-7*
interrupt and interrupt handler *4-17*
mailbox registers *4-18*
Miscellaneous Control Register (MISC_CTL) *4-5*
semaphores *4-18*
SYSCON Module *4-5*
system controller *4-6*
VME and PCI interrupters *4-17*
VMEbus interrupt handling *4-18*
Unpacking the USPIIe *xix*
USB
connector *A-8*
pinouts *A-8*
USB Ports
Port 2 *1-12*
Ports 0 and 1 *1-11*
user-defined rotary switch *2-6*
USPIIe-USB
2P2 and 2P3 boards *A-11*
Advanced PCI Bridge (APB) *3-4*
baseboard *2-1*
block diagram *2-2*
configurations *1-2*
ejector handles *C-2*
model configurations *xviii*, *1-1*, *C-1*
paddle boards, Standard & Multiple I/O *2-7*
PCI I/O controller *3-5*
photo of *xvii*
reset architecture *3-3*
reset structure *6-1*
Reset, Interrupt, and Clock (RIC) *3-3*
slot configurations *F-1*
system specifications *2-8*

V

Vdd-core *B-8*
VME
slot configurations *F-1*
diagram of *F-3*
Status LEDs *A-10*
SYSRST *1-13*
system controller. *See* SYSCON
VME P1 connector *A-1*
pinouts *A-2*
PMC Carrier Board *A-12*
pinouts *A-13*
VME P2
connection *1-9*, *1-10*
connector *A-3*
connector pinouts *A-4*
signals, software alarm *2-3*
solder beads
pin signal interpretation *B-15*
VME P2 connector
PMC Carrier Board *A-14*
SB2801–SB2832 configuration *B-15*, *B-17*
solder-bead settings *B-14*
VME P2 connector pinouts
PMC Carrier Board *A-15*
VME64 specification *4-6*
VME64-type handles *C-2*

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

VMEbus *3-5*
address and data transfer modes (Universe II) *4-1*
arbitrator *4-6*
configuration *4-2*
fields *4-10*, *4-13*
for VMEbus slave images *4-10*
first slot detector *4-5*
interface *1-13*, *4-2*
interrupt handling *4-18*
lock commands *4-3*
master *4-10*
master interface *4-3*
resets *6-4*
slave channel *4-2*
slave images *4-9*
control fields *4-12*
system controller *3-5*
to PCI Bus interface *4-1*
voltage sensors *2-12*

W

warranty *xxiv*
Watchdog
2-Level *5-1*, *5-3*, *6-5*
PLD registers *5-2*
reset *6-2*, *6-3*
timers *2-12*
WDR *6-2*
Website Information *xxiv*

X

XIR *6-2*, *6-4*, *6-6*

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Place
Stamp
Here

Themis Computer
3185 Laurel View Court
Fremont, CA 94538
Attn: Publications Department

Fold here; tape at top to seal



Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Reader Comment Card

We welcome your comments and suggestions to help improve the *USPIIe-USB User Manual*. Please take time to let us know what you think about this manual.

- Information provided in the manual was complete.

  Agree___ Disagree___ Not Applicable___

- Information was well documented and easy to follow.

  Agree___ Disagree___ Not Applicable___

- Information was easily accessible.

  Agree___ Disagree___ Not Applicable___

- The manual was useful.

  Agree___ Disagree___ Not Applicable___

- Please write down any comments you may have about this manual, including how it can be improved:

  _____

  _____

  _____

  _____

  _____

  _____

  _____

  _____

  _____

Name: _____

Title: _____

Company: _____

Address: _____

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

Artisan Technology Group is an independent supplier of quality pre-owned equipment

Gold-standard solutions

Extend the life of your critical industrial, commercial, and military systems with our superior service and support.

We buy equipment

Planning to upgrade your current equipment? Have surplus equipment taking up shelf space? We'll give it a new home.

Learn more!

Visit us at **artisantg.com** for more info on price quotes, drivers, technical specifications, manuals, and documentation.

Artisan Scientific Corporation dba Artisan Technology Group is not an affiliate, representative, or authorized distributor for any manufacturer listed herein.

We're here to make your life easier. How can we help you today?

(217) 352-9330 | sales@artisantg.com | artisantg.com

ARTISAN® TECHNOLOGY GROUP