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TRENTON

DP2/DP2GX

5664-xxx

No. 87-005664-000 Revision G

TECHNICAL REFERENCE

Dual Pentium® II / III

PROCESSOR-BASED

SBC

AGP

CE

PCI INDUSTRIAL COMPUTERS

PCI LOCAL BUS

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Serial number from the label on the back of the board
Description of the failure

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Declaration of Conformity

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HANDLING PRECAUTIONS

WARNING: This product has components which may be damaged by electrostatic discharge.

To protect your single board computer (SBC) from electrostatic damage, be sure to observe the following precautions when handling or storing the board:

- Keep the SBC in its static-shielded bag until you are ready to perform your installation.
- Handle the SBC by its edges.
- Do not touch the I/O connector pins. Do not apply pressure or attach labels to the SBC.
- Use a grounded wrist strap at your workstation or ground yourself frequently by touching the metal chassis of the system before handling any components. The system must be plugged into an outlet that is connected to an earth ground.
- Use antistatic padding on all work surfaces.
- Avoid static-inducing carpeted areas.

SOLDER-SIDE COMPONENTS

This SBC has components on both sides of the PCB. It is important for you to observe the following precautions when handling or storing the board to prevent solder-side components from being damaged or broken off:

- Handle the board only by its edges.
- Store the board in padded shipping material or in an antistatic board rack.
- Do not place an unprotected board on a flat surface.

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INTRODUCTION

The DP2 full-featured PCI/ISA processors are single board computers (SBCs) which feature dual Pentium® II or Pentium III microprocessors, Intel® 440BX AGPset, 100MHz system and memory buses, Cirrus Logic Accelerated Graphics Port (AGP) video interface, SDRAM, PCI Local Bus, cache, floppy controller, dual EIDE (Ultra DMA/33) interface, PCI Ultra Wide SCSI controller, PCI 10/100Base-T Ethernet controller, 512MB memory support, two serial ports, parallel port, speaker port, mouse port and keyboard port on a single ISA-size card. These single-slot, high performance SBCs plug into PICMG® PCI/ISA passive backplanes and provide 100% PC compatibility for the system expansion slots.

The DP2GX models of this SBC feature the Intel 440GX AGPset supporting memory configurations up to 1GB.

MODELS

Model #	Model Name	Speed
DP2 (BX):		
Pentium III - Advanced Transfer Cache:		
5664-407-xM	DP2/850	850MHz
5664-406-xM	DP2/800	800MHz
5664-405-xM	DP2/750	750MHz
5664-404-xM	DP2/700	700MHz
5664-403-xM	DP2/650	650MHz
5664-402-xM	DP2/600E	600MHz
5664-401-xM	DP2/550E	550MHz
Pentium III - Discrete Cache:		
5664-303-xM	DP2/600	600MHz
5664-302-xM	DP2/550	550MHz
5664-301-xM	DP2/500	500MHz
5664-300-xM	DP2/450	450MHz

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MODELS (continued)

Model #	Model Name	Speed
DP2 (BX): (continued)		
Pentium II:		
5664-007-xM	DP2/450	450MHz
5664-006-xM	DP2/400	400MHz
5664-005-xM	DP2/350	350MHz
5664-003-xM	DP2/333	333MHz
DP2GX:		
Pentium III - Advanced Transfer Cache:		
5664-437-xM	DP2GX/850	850MHz
5664-436-xM	DP2GX/800	800MHz
5664-435-xM	DP2GX/750	750MHz
5664-434-xM	DP2GX/700	700MHz
5664-433-xM	DP2GX/650	650MHz
5664-432-xM	DP2GX/600E	600MHz
5664-431-xM	DP2GX/550E	550MHz
Pentium III - Discrete Cache:		
5664-333-xM	DP2GX/600	600MHz
5664-332-xM	DP2GX/550	550MHz
5664-331-xM	DP2GX/500	500MHz
5664-330-xM	DP2GX/450	450MHz
Pentium II:		
5664-037-xM	DP2GX/450	450MHz
5664-036-xM	DP2GX/400	400MHz
5664-035-xM	DP2GX/350	350MHz
5664-033-xM	DP2GX/333	333MHz

where xM indicates memory size (0M = 0MB memory, 8M = 8MB memory, etc.)

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FEATURES

- Pentium III microprocessors at 850MHz, 800MHz, 750MHz, 700MHz, 650MHz, 600EMHz, 600MHz, 550EMHz, 550MHz, 500MHz, 450MHz;

  or Pentium II microprocessors at 450MHz, 400MHz, 350MHz or 333MHz

- Intel 440BX AGPset with 100MHz system and memory buses, and PCI bandwidth greater than 100MB/second. 440GX AGPset also available.
- Dual microprocessors using Symmetric Multiprocessing (SMP)
- Accelerated Graphics Port (AGP) VGA on-board video interface
- DRAM error checking and correction (ECC) support
- PCI Local Bus supports off-board PCI option cards, PCI 10/100Base-T Ethernet controller and on-board PCI Ultra Wide SCSI controller - Adaptec AIC-7880
- Compatible with PCI Industrial Computer Manufacturers Group (PICMG) 2.0 Specification
- Supports up to 512MB of Synchronous DRAM (SDRAM) on-board; 440GX AGPset supports up to 1GB
- Floppy drive and dual PCI EIDE Ultra DMA/33 drive interface
- Two serial ports and one parallel port
- Automatic or manual peripheral configuration
- Watchdog timer
- System hardware monitor
- Supports 1M x 64 to 32M x 64 DIMMs for non-ECC configurations; supports 1M x 72 to 32M x 72 DIMMs for ECC configurations. 440GX configurations support up to 64M x 72 DIMMs.

- Shadow RAM for System BIOS and peripherals increases system speed and performance
- Full PC compatibility

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PROCESSOR

- Two Intel Pentium III microprocessors at 850MHz, 800MHz, 750MHz, 700MHz, 650MHz, 600EMHz, 600MHz, 550EMHz, 550MHz, 500MHz or 450MHz

  or two Intel Pentium II microprocessors at 450MHz, 400MHz, 350MHz or 333MHz

- Processors use the Slot 1 connector and Single Edge Contact Cartridge (SECC/SECC2) packaging

BUS INTERFACES

- ISA and PCI Local Bus compatible

DATA PATH

- DRAM/Memory - 64-bit
- ISA Bus - 16-bit
- PCI Bus - 32-bit
- Video - 64-bit

BUS SPEED - ISA

- 8.33MHz

BUS SPEED - PCI

- 33MHz

BUS SPEED - SYSTEM & MEMORY

- 100MHz for 850MHz, 800MHz, 750MHz, 700MHz, 650MHz, 600EMHz, 600MHz, 550EMHz, 550MHz, 500MHz, 450MHz, 400MHz or 350MHz
- 66MHz for 333MHz

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SYSTEM & MEMORY BUSES

The Intel 440BX/GX AGPset supports the system and memory buses at both 66MHz and 100MHz speeds. The 100MHz system and memory buses provide a higher bandwidth path for transferring data between main memory/chip set and the microprocessors. Bus speed is dependent on processor speed (see *Bus Speed - System & Memory* above).

DMA CHANNELS

The SBC is fully PC compatible with seven DMA channels, each supporting type F transfers.

INTERRUPTS

The SBC is fully PC compatible with interrupt steering for PCI plug and play compatibility.

BIOS (FLASH)

The BIOS is a Hi-Flex AMIBIOS with built-in advanced CMOS setup for system parameters, peripheral management for configuring on-board peripherals, PCI-to-PCI bridge support and PCI interrupt steering. The BIOS chip is a boot block Flash device - 28F002BX-T120. The BIOS may be upgraded from floppy disk by pressing **<Ctrl>** + **<Home>** *immediately* after reset or power-up with the floppy disk in drive A:. Custom BIOSs are available.

CACHE MEMORY

For Discrete Cache Pentium III processors, a 512K unified, non-blocking second level (L2) cache on the PCB of the SECC improves performance by reducing the average memory access time and providing fast access to recently used instructions and data. Performance is enhanced through a dedicated 64-bit cache bus. The speed of the L2 cache is half the processor core frequency. With a core

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frequency of 600MHz, the L2 cache bus runs at 300MHz. The processor chip also incorporates two separate 16K level one (L1) internal caches, one for instructions and one for data.

For Advanced Transfer Cache Pentium III processors, the processor includes an integrated on-die, 256K 8-way set associative level two (L2) cache. The L2 cache implements the new Advanced Transfer Cache architecture with a 256-bit wide bus. The processor also includes a 16K level one (L1) instruction cache and 16K L1 data cache. These cache arrays run at the full speed of the processor core.

DRAM MEMORY

The DRAM interface consists of two dual in-line memory module (DIMM) sockets and supports auto detection of memory up to 512MB of Synchronous DRAM (SDRAM) for the 440BX or up to 1GB of SDRAM for the 440GX. Minimum memory size is 8MB. The System BIOS automatically detects memory type, size and speed.

The SBC uses industry standard 64-bit or 72-bit wide gold finger DIMM DRAM in two 168-pin DIMM sockets.

NOTE: Memory can be installed in one or both DIMM sockets. If only one DIMM module is used, it must be populated in the top DIMM socket (Bank 1 - BK1). If two modules are used, they must be the same DIMM type, but may be different sizes (see table below). EDO DIMMs are not supported. All DIMMs must have gold contacts.

The SBC supports DIMM memory modules which are PC-100 compliant and have the following features:

- 168-pin DIMMs with gold-plated contacts
- 100MHz SDRAM
- Non-ECC (64-bit) or ECC (72-bit) memory
- 3.3 volt

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DRAM MEMORY (continued)

- Single or double-sided DIMMs in the sizes listed below
- Buffered or Registered configuration

DIMM Size	DIMM Type	Non-ECC	ECC
8MB	Unbuffered	1M x 64	1M x 72
16MB	Unbuffered	2M x 64	2M x 72
32MB	Unbuffered	4M x 64	4M x 72
64MB	Unbuffered	8M x 64	8M x 72
128MB	Unbuffered	16M x 64	16M x 72
256MB	Registered	32M x 64	32M x 72
512MB	Registered	64M x 64	64M x 72 *

* DP2GX models only

All memory components and DIMMs used with the SBC must be PC-100 compliant, which means that they comply with Intel's PC SDRAM specifications. These include the PC SDRAM Specification (memory component specific), the PC Unbuffered DIMM Specification, the PC Registered DIMM Specification and the PC Serial Presence Detect Specification.

MEMORY HOLE

The SBC supports a 1MB memory hole option at 512KB-640KB or 15MB-16MB.

ERROR CHECKING AND CORRECTION

The memory interface supports ECC modes via BIOS setting for multiple-bit error detection and detection of all errors confined to a single nibble.

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PCI LOCAL BUS INTERFACE

The SBC is fully compliant with the PCI Local Bus 2.1 Specification. It has optimized the PCI interface to allow the processor to sustain the highest possible bandwidth (greater than 100MB/sec sustained) and low latency of the PCI Bus. It supports PCI-to-PCI bridge technology, a pipelined snoop ahead feature and improved PCI to DRAM write-back policy. The PCI Local Bus interfaces to the on-board PCI Ultra Wide SCSI controller, to the PCI 10/100 Base-T Ethernet controller and to standard PCI option cards in the backplane. The PCI Local Bus interface to the backplane is compliant with the PCI Industrial Computer Manufacturers Group (PICMG) 2.0 Specification.

UNIVERSAL SERIAL BUS (USB)

The SBC supports two USB 1.0 ports for serial transfers at 12 or 1.5Mbit/sec. The Universal Serial Bus (USB) is an interface allowing for connectivity to many standard PC peripherals via an external port.

SYMMETRIC MULTIPROCESSING (SMP)

The dual Pentium II/III processor-based design allows the operating system to assign tasks on demand to the next available processor. SMP uses applications which are divided into threads which can run concurrently on any available processor. This improves performance of the application itself as well as the total throughput of the system.

CONCURRENT PCI

Concurrent PCI maximizes system performance with simultaneous CPU, PCI and AGP Bus activities. It includes multitransaction timing, enhanced write performance, a passive release mechanism and support for PCI 2.1 compliant delayed transactions.

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AGP VGA INTERFACE

The Cirrus Logic GD5465 video interface is an Accelerated Graphics Port (AGP) device with both 3D and 2D capabilities. AGP is designed to off-load the PCI Bus by allowing graphics data to move directly from system memory. The interface supports pixel resolutions up to 1600 x 1200 non-interlaced. The SBC provides 2MB of on-board Rambus® memory which provides a high-bandwidth solution. Software drivers for enhanced performance and resolution are available for most popular operating systems.

SYSTEM HARDWARE MONITOR

The system hardware monitoring system monitors system voltages, temperature and fan speeds.

The circuitry is based on National Semiconductor's LM80 and LM75. The LM80 monitors six system voltages, two fan speeds and the board ambient temperature. The LM80's interface to the companion LM75 temperature sensor monitors the temperature between the Pentium II/III cartridge and the SBC. All of the voltages, fan speeds and temperature measurements have associated programmable watchdog limits. When any of these programmed limits are exceeded, the monitor software can be used to notify the SBC. In addition, the externally available OS# signal can be used to notify external hardware of any over-temperature condition.

Fan speed monitoring can be configured to monitor two system fans.

The LM80 also monitors an external chassis intrusion switch via the system hardware monitor connector (P18).

A general purpose output (GPO) is also provided at the system hardware monitor connector. This signal can be used to provide a user-defined function.

The following system voltages are monitored by the LM80:

- -12 volts
- 3.3 volts provided by the on-board voltage regulator for components on the SBC

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- 3.3 volts backplane power used by the option slots
- +5 volts
- +12 volts
- 1.5 volt, VTT voltage used by processor's GTL+ bus

PCI 10/100BASE-T ETHERNET INTERFACE

The PCI Ethernet interface is implemented using an Intel 21143 and operates in 10Base-T and 100Base-TX Fast Ethernet modes. The interface is compliant with IEEE 802.3 and PCI Local Bus 2.0 and 2.1 Specifications.

The main components of the interface are:

- Intel 21143 for 10/100-Mb/s media access control (MAC) with SYM, a serial ROM port and a PCI Bus Master interface
- 100-Mb symbol-based PHY with a pass-through path
- Magnetics module for a 10/100-Mb/s magnetic connection
- Serial ROM for storing the Ethernet address and the interface configuration and control data
- RJ-45 connector on the SBC's I/O bracket for direct connection to the network. The connector requires a category 5 (CAT5) unshielded twisted-pair (UTP) 2-pair cable for a 100-Mb/s network connection or a category 3 (CAT3) or higher UTP 2-pair cable for a 10-Mb/s network connection.
- Link status and activity LEDs on the I/O bracket for status indication (See *Ethernet LEDs and Connector* later in this section.)

Software drivers are supplied for most popular operating systems. Loading instructions for the software drivers are on the driver diskette provided with the SBC.

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PCI ULTRA WIDE SCSI INTERFACE

The SCSI interface is a PCI Bus Master device which supports Ultra Wide SCSI data transfer up to 40MB per second and bursts data to the host at full PCI speeds. Active termination is provided with terminator voltage protected by self-resetting fuses. A jumper is provided to disable the termination. The SCSI controller is an Adaptec AIC-7880. Software drivers are available for most popular operating systems.

The Adaptec SCSISelect Configuration Utility allows you to view and/or change the default configuration settings for the Ultra Wide SCSI adapter. This utility is described in *Appendix C - SCSISelect Configuration Utility*.

PCI ENHANCED IDE ULTRA DMA/33 INTERFACE (DUAL)

Dual high performance PCI Bus Master EIDE interfaces are capable of supporting two IDE Type 4 disk drives each in a master/slave configuration. The interface supports Ultra DMA/33 with synchronous DMA mode transfers up to 33MB per second.

FLOPPY DRIVE INTERFACE

The SBC supports two floppy disk drives. Drives can be 360K to 2.88MB, in any combination.

SERIAL INTERFACE

Two high-speed FIFO (16C550) serial ports with independently programmable baud rates are supported. The IRQ for each serial port has BIOS selectable addressing.

ENHANCED PARALLEL INTERFACE

The SBC provides a PC/AT compatible bidirectional parallel port and supports enhanced parallel port (EPP) mode and extended

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capabilities port (ECP) mode. The ECP mode is IEEE 1284 compliant. The IRQ for the parallel port has BIOS selectable addressing.

PS/2 MOUSE INTERFACE

The SBC is compatible with a PS/2-type mouse. The mouse connection can be made by using either the PS/2 mouse header or the bracket mounted PS/2 mouse mini DIN connector. Mouse voltage is protected by a self-resetting fuse.

KEYBOARD INTERFACE

The SBC is compatible with an AT-type keyboard. The keyboard connection can be made by using either the keyboard header or the bracket mounted keyboard mini DIN connector. Keyboard voltage is protected by a self-resetting fuse.

WATCHDOG TIMER

The watchdog timer is a hardware timer which resets the SBC if the timer is not refreshed by software periodically. The timer is typically used to restart a system in which an application becomes hung on an external event. When the application is hung, it no longer refreshes the timer. The watchdog timer then times out and resets the SBC.

The watchdog timer has two levels of enable. First, the watchdog timer jumper must be moved to the "enabled" position, which puts the watchdog timer under software control.

The second level involves software control of the watchdog's timer retriggering. Bit 6 of the 82371EB GPOREG register at I/O address 437H must be set to a zero (0), which blocks the triggering clock to the watchdog timer circuit, thus scheduling a hardware reset in about 1.5 seconds.

To refresh the watchdog timer, the software in the application toggles bit 6 of the GPOREG register. First the bit must be set to a one

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(1) to clear the watchdog timer delay; then it must be set to a zero (0), which schedules a system reset in 1.5 seconds. Toggling bit 6 of the GPOREG must occur within a period of less than 1.5 seconds to insure that a system reset is not issued.

A set of watchdog timer software code and sample programs are available from Technical Support.

POWER FAIL DETECTION

A hardware reset is issued when on-board +5V voltage drops below 4.75 volts. In addition, if the 3.3V Monitor jumper (JU15) is enabled, a reset is issued if backplane 3.3V is below tolerance. (See *Configuration Jumpers* later in this section.)

BATTERY

A built-in lithium battery is provided, for ten years of data retention for CMOS memory.

POWER REQUIREMENTS

+5V @ 8.9 Amps maximum (850MHz)
+12V @ < 100 mAmps
-12V @ < 100 mAmps

TEMPERATURE/ENVIRONMENT

Operating Temperature: 0° C. to 60° C.
(0° C. to 50° C. for 550MHz and above)

Storage Temperature: - 40° C. to 70° C.

Humidity: 5% to 90% non-condensing

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MEAN TIME BETWEEN FAILURES (MTBF)

42,000 POH (Power-On Hours) at 40° C., per MIL-HDBK-217F

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CONFIGURATION JUMPERS

The setup of the configuration jumpers on the SBC is described below. * indicates the default value of each jumper.

NOTE: For two-position jumpers (3-post), "RIGHT" is toward the bracket end of the board; "LEFT" is toward the memory sockets.

Jumper	Description
JU7	Combo I/O (P5A) Speaker Connect (Also refer to JU18 - Combo I/O Reset Connect.) Install to connect speaker data signal to pin 8 of the Combo I/O connector (P5A). * Remove to disconnect.
JU8	Password Clear Install for one power-up cycle to reset the password to the default (null password). Remove for normal operation. *
JU9	CRT Type Select Install on the LEFT for a monochrome CRT. Install on the RIGHT for a color CRT. *
JU10/JU11	System Flash ROM Operational Modes The Flash ROM has two programmable sections: the Boot Block for "flashing" in the BIOS and the Main Block for the executable BIOS and PnP parameters. Normally only the Main Block is updated when a new BIOS is flashed into the system.

	JU10	JU11
Program All (Boot and Main)	Right	Right
Normal PnP (Program Main Block)	Right *	Left *
Write Protect	Left	Left

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CONFIGURATION JUMPERS (continued)

Jumper	Description
JU12	CMOS Clear Install to clear. Remove to operate. *

NOTE: The CMOS Clear jumper works on power-up. To clear the CMOS, power down the system, install the jumper, then turn the power back on. CMOS is cleared during the POST routines. Then power down the system again and remove the jumper before the next power-up.

JU13	SCSI Termination Enable Install to disable on-board active termination for the SCSI interface. Remove to enable active termination. *
JU14	Fan Speed Monitor This jumper *must* be removed (disabled).
JU15	3.3V Monitor Enable Install to enable the 3.3V monitor. Remove to disable the monitor. *

NOTE: JU15 enables the 3.3 volt monitor, which monitors the 3.3V power plane of the backplane. This voltage is routed to the SBC via the PICMG connector. The monitor generates a RESET to the SBC if 3.3V is below tolerance. If your system does *not* supply 3.3V to the backplane, this jumper *must* be removed (disabled).

JU16	Watchdog Timer Install on the LEFT for normal reset operation. * Install on the RIGHT to enable watchdog timer operation.

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CONFIGURATION JUMPERS (continued)

Jumper	Description
JU17	Interrupt 12 (IRQ12) Select Install to dedicate IRQ12 to the PS/2 mouse. * Remove to make IRQ12 available for system use.
JU18	Combo I/O (P5A) Reset Connect (Also refer to JU7 - Combo I/O Speaker Connect.) Install to connect reset data signal to pin 1 of the Combo I/O connector (P5A). * Remove to disconnect.
JU19	SCSI Activity LED Enable Install to light the hard drive LED for SCSI drive activity. * Remove if you do not have a SCSI drive (i.e., the SCSI controller is not being used).
JU20	Dual Processor Enable Install for dual processor operation. * Remove for single processor operation.

CPU Speed Jumpers

There are four jumpers (W3, W4, W5 and W6) which must be set correctly to allow the SBC to take full advantage of the speed of the Pentium II/III microprocessor. These jumpers must be set as specified on the following page.

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CONFIGURATION JUMPERS (continued)

CPU Speed Jumpers

CPU Speed	Synthesizer Frequency	Jumpers W4*	W3	W6	W5
850MHz	100MHz	In	Out	In	Out
800MHz	100MHz	Out	In	In	Out
750MHz	100MHz	Out	Out	Out	In
700MHz	100MHz	Out	In	Out	In
650MHz	100MHz	Out	Out	In	In
600MHz	100MHz	Out	In	In	In
550MHz	100MHz	In	Out	Out	Out
500MHz	100MHz	In	In	Out	Out
450MHz	100MHz	In	Out	In	Out
400MHz	100MHz	In	In	In	Out
350MHz	100MHz	In	Out	Out	In
333MHz	66MHz	In	In	Out	Out

* **NOTE:** In revision E-B-03 and earlier, W4 was hard-wired in an "In" position.

ETHERNET LEDS AND CONNECTOR

The Ethernet interface has two LEDs for status indication and an RJ-45 network connector.

LED/Connector	Description
Link Status LED	Green LED which indicates the link status.
	On — The Ethernet interface has a valid link on the network connection and is ready for normal operation. (10Base-T link or 100Base-TX link)
	Off — The Ethernet interface did not find a valid link on the network connection. Transmit and receive are not possible.

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ETHERNET LEDS AND CONNECTOR (continued)

LED/Connector	Description
Activity LED	Red LED which indicates the transmit or receive activity for the 10Base-T or 100Base-TX network connection. On — A packet is being transmitted or received. Off — There is no network activity.
RJ-45 Network Connector	The RJ-45 network connector requires a category 5 (CAT5) unshielded twisted-pair (UTP) 2-pair cable for a 100-Mb/s network connection or a category 3 (CAT3) or higher UTP 2-pair cable for a 10-Mb/s network connection.

SYSTEM BIOS SETUP UTILITIES

The System BIOS is a Hi-Flex AMIBIOS with ROM-resident setup utilities. The following Setup utilities are selectable from the AMIBIOS Hi-Flex Setup Utility Menu:

- Standard CMOS Setup
- Advanced CMOS Setup
- Advanced Chipset Setup
- Power Management Setup
- PCI/Plug and Play Setup
- Peripheral Setup
- Auto-Detect Hard Disks
- Change User Password
- Change Supervisor Password

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- Auto Configuration with Optimal Settings
- Auto Configuration with Fail Safe Settings
- Save Settings and Exit
- Exit Without Saving

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CONNECTORS

NOTE: Pin 1 on the connectors is indicated by the square pad on the PCB.

P2 - Keylock Connector
5 pin single row header, Amp #640456-5

PIN	SIGNAL
1	LED Power
2	Key
3	Gnd
4	Keylock Data
5	Gnd

P3 - Floppy Drive Connector
34 pin dual row header, Robinson Nugent #IDH-34LP-S3-TR

PIN	SIGNAL	PIN	SIGNAL
1	Gnd	2	N-RPM
3	Gnd	4	NC
5	Gnd	6	D-Rate0
7	Gnd	8	P-Index
9	Gnd	10	N-Motoron 1
11	Gnd	12	N-Drive Sel2
13	Gnd	14	N-Drive Sel1
15	Gnd	16	N-Motoron 2
17	Gnd	18	N-Dir
19	Gnd	20	N-Stop Step
21	Gnd	22	N-Write Data
23	Gnd	24	N-Write Gate
25	Gnd	26	P-Track 0
27	Gnd	28	P-Write Protect
29	Gnd	30	N-Read Data
31	Gnd	32	N-Side Select
33	Gnd	34	Disk Chng

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P4 - Keyboard Connector
6 pin mini DIN, Kycon #KMDG-6S-BS-PS

PIN	SIGNAL
1	Kbd Data
2	Reserved
3	Gnd
4	Kbd Power (+5V fused) with self-resetting fuse
5	Kbd Clock
6	Reserved

P4A - Keyboard Header
5 pin single row header, Amp #640456-5

PIN	SIGNAL
1	Kbd Clock
2	Kbd Data
3	Key
4	Kbd Gnd
5	Kbd Power (+5V fused) with self-resetting fuse

P5 - Speaker Port Connector
4 pin single row header, Amp #640456-4

PIN	SIGNAL
1	Speaker Data
2	Key
3	Gnd
4	+5V

P5A - Combo I/O Connector
8 pin single row header, Amp #640456-8

PIN	SIGNAL
1	Reset (See JU18 in the *Configuration Jumpers* section.)
2	Gnd
3	NC

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P5A - Combo I/O Connector (continued)

PIN	SIGNAL
4	Kbd Clock
5	Kbd Data
6	Kbd Lock Data
7	Kbd Power (+5V fused) with self-resetting fuse
8	Speaker Data

P6 - Serial Port 1 Connector

10 pin dual row header, 3M #30310-6002HB

PIN	SIGNAL	PIN	SIGNAL
1	Carrier Detect	2	Data Set Ready-I
3	Receive Data-I	4	Request to Send-O
5	Transmit Data-O	6	Clear to Send-I
7	Data Terminal Ready-O	8	Ring Indicator-I
9	Signal Gnd	10	NC

P7 - Serial Port 2 Connector

10 pin dual row header, 3M #30310-6002HB

PIN	SIGNAL	PIN	SIGNAL
1	Carrier Detect	2	Data Set Ready-I
3	Receive Data-I	4	Request to Send-O
5	Transmit Data-O	6	Clear to Send-I
7	Data Terminal Ready-O	8	Ring Indicator-I
9	Signal Gnd	10	NC

P8 - Parallel Port Connector

26 pin dual row header, 3M #30326-6002HB

PIN	SIGNAL	PIN	SIGNAL
1	Strobe	2	Auto Feed XT
3	Data Bit 0	4	Error
5	Data Bit 1	6	Init
7	Data Bit 2	8	Slct In

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P8 - Parallel Port Connector (continued)

PIN	SIGNAL	PIN	SIGNAL
9	Data Bit 3	10	Gnd
11	Data Bit 4	12	Gnd
13	Data Bit 5	14	Gnd
15	Data Bit 6	16	Gnd
17	Data Bit 7	18	Gnd
19	ACK	20	Gnd
21	Busy	22	Gnd
23	Paper End	24	Gnd
25	Slct	26	NC

P9 - PS/2 Mouse Connector

6 pin mini DIN, Kycon #KMDG-6S-BS-PS

PIN	SIGNAL
1	Ms Data
2	Reserved
3	Gnd
4	Kbd Power (+5V fused) with self-resetting fuse
5	Ms Clock
6	Reserved

P9A - PS/2 Mouse Header

6 pin single row header, Amp #640456-6

PIN	SIGNAL
1	Ms Data
2	Reserved
3	Kbd Gnd
4	Kbd Power (+5V fused) with self-resetting fuse
5	Ms Clock
6	Reserved

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P10 - External Reset Connector
2 pin header, Amp #640456-2

PIN	SIGNAL
1	Negative External Reset
2	Gnd

P11 - Primary IDE Hard Drive Connector
40 pin dual row header, Robinson Nugent #IDH-40LP-S3-TR

PIN	SIGNAL	PIN	SIGNAL
1	Reset	2	Gnd
3	Data 7	4	Data 8
5	Data 6	6	Data 9
7	Data 5	8	Data 10
9	Data 4	10	Data 11
11	Data 3	12	Data 12
13	Data 2	14	Data 13
15	Data 1	16	Data 14
17	Data 0	18	Data 15
19	Gnd	20	NC
21	DRQ 0	22	Gnd
23	IOW	24	Gnd
25	IOR	26	Gnd
27	IORDY	28	+5V
29	DACK 0	30	Gnd
31	IRQ 14	32	IOCS16
33	Add 1	34	Gnd
35	Add 0	36	Add 2
37	CS 1P	38	CS 3P
39	IDEACTP	40	Gnd

P11A - Secondary IDE Hard Drive Connector
40 pin dual row header, Robinson Nugent #IDH-40LP-S3-TR

PIN	SIGNAL	PIN	SIGNAL
1	Reset	2	Gnd
3	Data 7	4	Data 8

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P11A - Secondary IDE Hard Drive Connector (continued)

PIN	SIGNAL	PIN	SIGNAL
5	Data 6	6	Data 9
7	Data 5	8	Data 10
9	Data 4	10	Data 11
11	Data 3	12	Data 12
13	Data 2	14	Data 13
15	Data 1	16	Data 14
17	Data 0	18	Data 15
19	Gnd	20	NC
21	DRQ 1	22	Gnd
23	IOW	24	Gnd
25	IOR	26	Gnd
27	IORDY	28	+5V
29	DACK 1	30	Gnd
31	MIRQ 0	32	IOCS16
33	Add 1	34	Gnd
35	Add 0	36	Add 2
37	CS 1S	38	CS 3S
39	IDEACTS	40	Gnd

P12 - Hard Drive LED Connector

4 pin single row header, Amp #640456-4

(This connector is used for both IDE and SCSI drives. See JU19 in the *Configuration Jumpers* section.)

PIN	SIGNAL
1	+5V Pullup
2	Light
3	Light
4	+5V Pullup

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P13 - PCI Ultra Wide SCSI Controller Connector

50/68 high density SCSI connector, Amp #749069-7

PIN	SIGNAL	PIN	SIGNAL
1	Gnd	35	SCZDB12
2	Gnd	36	SCZDB13
3	Gnd	37	SCZDB14
4	Gnd	38	SCZDB15
5	Gnd	39	SCZDBPH
6	Gnd	40	SCZDB0
7	Gnd	41	SCZDB1
8	Gnd	42	SCZDB2
9	Gnd	43	SCZDB3
10	Gnd	44	SCZDB4
11	Gnd	45	SCZDB5
12	Gnd	46	SCZDB6
13	Gnd	47	SCZDB7
14	Gnd	48	SCZDBP
15	Gnd	49	Gnd
16	Gnd	50	Gnd
17	TERMPWR	51	TERMPWR
18	TERMPWR	52	TERMPWR
20	Gnd	54	Gnd
21	Gnd	55	SCZATN
22	Gnd	56	Gnd
23	Gnd	57	SCZBSY
24	Gnd	58	SCZACK
25	Gnd	59	SCZRST
26	Gnd	60	SCZMSG
27	Gnd	61	SCZSEL
28	Gnd	62	SCZCD
29	Gnd	63	SCZREQ
30	Gnd	64	SCZIO
31	Gnd	65	SCZDB8
32	Gnd	66	SCZDB9
33	Gnd	67	SCZDB10
34	WIDEPS	68	SCZDB11

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P15 - PCI SVGA Interface Connector
15 pin VGA connector, Amp #748390-5

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
		6	Gnd		
1	Red			11	NC
		7	Gnd		
2	Green			12	EEDI
		8	Gnd		
3	Blue			13	HSYNC
		9	NC		
4	NC			14	VSYNC
		10	Gnd		
5	Gnd			15	EECS

P16 - PCI 10/100Base-T Ethernet Connector
8 pin shielded RJ-45 connector, Molex #43202-8110

PIN	SIGNAL
1	TD+
2	TD-
3	RX+
4	NC
5	NC
6	RX-
7	NC
8	NC

P17 - Universal Serial Bus (USB) Connector
8 pin dual row header, Molex #702-46-0821
(+5V fused with self-resetting fuses)

PIN	SIGNAL	PIN	SIGNAL
1	+5V-USB0	2	+5V-USB1
3	USB0-	4	USB1-
5	USB0+	6	USB1+
7	Gnd-USB0	8	Gnd-USB1

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P18 - System Hardware Monitor Connector
6 pin single row header, Amp #640456-6

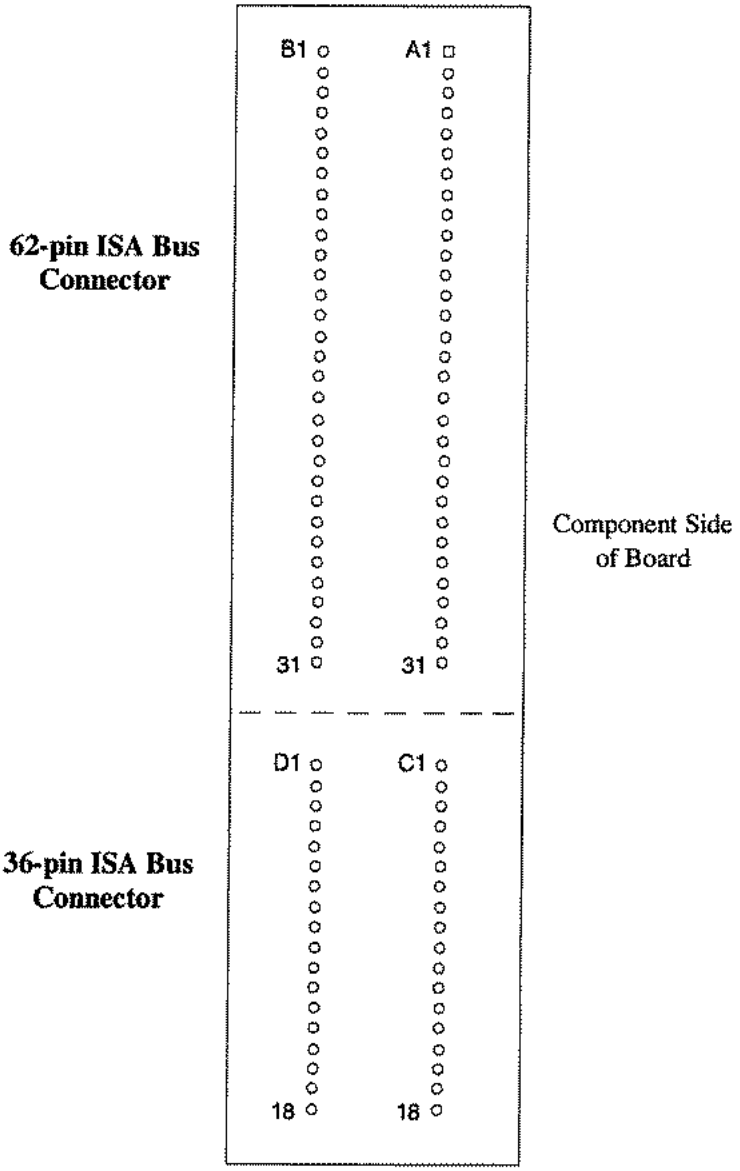
PIN	SIGNAL
1	Gnd
2	GPO (General Purpose Output)
3	CI (Chassis Intrusion Input)
4	FAN1 (Fan 1 Tachometer Input)
5	FAN2 (Fan 2 Tachometer Input)
6	OS# (Temperature Sense Output)

P19 - CPU Fan
3 pin single row header, Molex #22-23-2031

PIN	SIGNAL
1	Gnd
2	+12V
3	FanTach

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ISA BUS PIN NUMBERING



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ISA BUS PIN ASSIGNMENTS

The following figures summarize pin assignments for the Industry Standard Architecture (ISA) Bus connectors.

I/O Pin	Signal Name	I/O
A1	IOCHK#	I
A2	D7	I/O
A3	D6	I/O
A4	D5	I/O
A5	D4	I/O
A6	D3	I/O
A7	D2	I/O
A8	D1	I/O
A9	D0	I/O
A10	CHRDY	I
A11	AEN	O
A12	SA19	I/O
A13	SA18	I/O
A14	SA17	I/O
A15	SA16	I/O
A16	SA15	I/O
A17	SA14	I/O
A18	SA13	I/O
A19	SA12	I/O
A20	SA11	I/O
A21	SA10	I/O
A22	SA9	I/O
A23	SA8	I/O
A24	SA7	I/O
A25	SA6	I/O
A26	SA5	I/O
A27	SA4	I/O
A28	SA3	I/O
A29	SA2	I/O
A30	SA1	I/O
A31	SA0	I/O

I/O Pin	Signal Name	I/O
B1	Gnd	Ground
B2	RESDRV	O
B3	+5V	Power
B4	IRQ9	I
B5	-5V	Power
B6	DRQ2	I
B7	-12V	Power
B8	NOWS#	I
B9	+12V	Power
B10	Gnd	Ground
B11	SMWTC#	O
B12	SMRDC#	O
B13	IOWC#	I/O
B14	IORC#	I/O
B15	DAK3#	O
B16	DRQ3	I
B17	DAK1#	O
B18	DRQ1	I
B19	REFRESH#	I/O
B20	BCLK	O
B21	IRQ7	I
B22	IRQ6	I
B23	IRQ5	I
B24	IRQ4	I
B25	IRQ3	I
B26	DAK2#	O
B27	T-C	O
B28	BALE	O
B29	+5V	Power
B30	OSC	O
B31	Gnd	Ground

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ISA BUS PIN ASSIGNMENTS (continued)

I/O Pin	Signal Name	I/O
C1	SBHE#	I/O
C2	LA23	I/O
C3	LA22	I/O
C4	LA21	I/O
C5	LA20	I/O
C6	LA19	I/O
C7	LA18	I/O
C8	LA17	I/O
C9	MRDC#	I/O
C10	MWTC#	I/O
C11	D8	I/O
C12	D9	I/O
C13	D10	I/O
C14	D11	I/O
C15	D12	I/O
C16	D13	I/O
C17	D14	I/O
C18	D15	I/O

I/O Pin	Signal Name	I/O
D1	M16#	I
D2	IO16#	I
D3	IRQ10	I
D4	IRQ11	I
D5	IRQ12	I
D6	IRQ15	I
D7	IRQ14	I
D8	DAK0#	O
D9	DRQ0	I
D10	DAK5#	O
D11	DRQ5	I
D12	DAK6#	O
D13	DRQ6	I
D14	DAK7#	O
D15	DRQ7	I
D16	+5V	Power
D17	Master16#	I
D18	Gnd	Ground

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ISA BUS SIGNAL DESCRIPTIONS

The following is a description of the ISA Bus signals. All signal lines are TTL-compatible.

AEN (O)

Address Enable (AEN) is used to degate the microprocessor and other devices from the I/O channel to allow DMA transfers to take place. When this line is active, the DMA controller has control of the address bus, the data-bus Read command lines (memory and I/O), and the Write command lines (memory and I/O).

BALE (O) (Buffered)

Address Latch Enable (BALE) is provided by the bus controller and is used on the system board to latch valid addresses and memory decodes from the microprocessor. It is available to the I/O channel as an indicator of a valid microprocessor or DMA address (when used with AEN). Microprocessor addresses SA[19::0] are latched with the falling edge of BALE. BALE is forced high during DMA cycles.

BCLK (O)

BCLK is the system clock. The clock has a 50% duty cycle. This signal should only be used for synchronization. It is not intended for uses requiring a fixed frequency.

CHRDY (I)

I/O Channel Ready (CHRDY) is pulled low (not ready) by a memory or I/O device to lengthen I/O or memory cycles. Any slow device using this line should drive it low immediately upon detecting its valid address and a Read or Write command. Machine cycles are extended by an integral number of clock cycles. This signal should be held low for no more than 2.5 microseconds.

D[15::0] (I/O)

Data signals D[15::0] provide bus bits 15 through 0 for the microprocessor, memory, and I/O devices. D15 is the most-significant bit and D0 is the least-significant bit. All 8-bit devices on the I/O channel should use D[7::0] for communications to the microprocessor. The 16-bit devices will use D[15::0]. To support 8-bit devices, the data on D[15::8] will be gated to D[7::0] during 8-bit transfers to these devices. 16-bit microprocessor transfers to 8-bit devices will be converted to two 8-bit transfers.

DAK[7::5]#, DAK[3::0]# (O)

DMA Acknowledge DAK[7::5]# and DAK[3::0]# are used to acknowledge DMA requests DRQ[7::5] and DRQ[3::0]. They are active low.

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DRQ[7::5], DRQ[3::0] (I)

DMA Requests DRQ[7::5] and DRQ[3::0] are asynchronous channel requests used by peripheral devices and the I/O channel microprocessors to gain DMA service (or control of the system). They are prioritized, with DRQ0 having the highest priority and DRQ7 having the lowest. A request is generated by bringing a DRQ line to an active level. A DRQ line must be held high until the corresponding DMA Request Acknowledge (DAK) line goes active. DRQ[3::0] will perform 8-bit DMA transfers; DRQ[7::5] will perform 16-bit transfers.

IO16# (I)

I/O 16-bit Chip Select (IO16#) signals the system board that the present data transfer is a 16-bit, 1 wait-state, I/O cycle. It is derived from an address decode. IO16# is active low and should be driven with an open collector or tri-state driver capable of sinking 20 mAmps.

IOCHK# (I)

I/O Channel Check (IOCHK#) provides the system board with parity (error) information about memory or devices on the I/O channel. When this signal is active, it indicates an uncorrectable system error.

IORC# (I/O)

I/O Read (IORC#) instructs an I/O device to drive its data onto the data bus. It may be driven by the system microprocessor or DMA controller, or by a microprocessor or DMA controller resident on the I/O channel. This signal is active low.

IOWC# (I/O)

I/O Write (IOWC#) instructs an I/O device to read the data on the data bus. It may be driven by any microprocessor or DMA controller in the system. This signal is active low.

IRQ[15::14], IRQ[12::9], IRQ[7::3] (I)

Interrupt Requests IRQ[15::14], IRQ[12::9] and IRQ[7::3] are used to signal the microprocessor that an I/O device needs attention. The interrupt requests are prioritized, with IRQ[15::14] and IRQ[12::9] having the highest priority (IRQ9 is the highest) and IRQ[7::3] having the lowest priority (IRQ7 is the lowest). An interrupt request is generated when an IRQ line is raised from low to high. The line must be held high until the microprocessor acknowledges the interrupt request (Interrupt Service routine).

LA[23::17] (I/O)

These signals (unlatched) are used to address memory and I/O devices within the system. They give the system up to 16MB of addressability. These signals are valid when BALE is high. LA[23::17] are not latched during microprocessor cycles and therefore do not stay valid for the whole cycle. Their purpose is to generate memory decodes for 1 wait-state memory cycles. These decodes should be latched by I/O adapters on the falling edge of BALE. These signals

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also may be driven by other microprocessors or DMA controllers that reside on the I/O channel.

M16# (I)

M16# Chip Select signals the system board if the present data transfer is a 1 wait-state, 16-bit, memory cycle. It must be derived from the decode of LA[23::17]. M16# should be driven with an open collector or tri-state driver capable of sinking 20 mAmps.

Master16# (I)

Master16# is used with a DRQ line to gain control of the system. A processor or DMA controller on the I/O channel may issue a DRQ to a DMA channel in cascade mode and receive a DAK#. Upon receiving the DAK#, an I/O microprocessor may pull Master16# low, which will allow it to control the system address, data, and control lines (a condition known as tri-state). After Master16# is low, the I/O microprocessor must wait one system clock period before driving the address and data lines, and two clock periods before issuing a Read or Write command. If this signal is held low for more than 15 microseconds, system memory may be lost because of a lack of refresh.

NOWS# (I)

The No Wait State (NOWS#) signal tells the microprocessor that it can complete the present bus cycle without inserting any additional wait cycles. In order to run a memory cycle to a 16-bit device without wait cycles, NOWS# is derived from an address decode gated with a Read or Write command. In order to run a memory cycle to an 8-bit device with a minimum of two wait states, NOWS# should be driven active on system clock after the Read or Write command is active gated with the address decode for the device. Memory Read and Write commands to a 8-bit device are active on the falling edge of the system clock. NOWS# is active low and should be driven with an open collector or tri-state driver capable of sinking 20 mAmps.

OSC (O)

Oscillator (OSC) is a high-speed clock with a 70-nanosecond period (14.31818 MHz). This signal is not synchronous with the system clock. It has a 50% duty cycle.

REFRESH# (I/O)

The REFRESH# signal is used to indicate a refresh cycle and can be driven by a microprocessor on the I/O channel.

RESDRV (O)

Reset Drive (RESDRV) is used to reset or initialize system logic at power-up time or during a low line-voltage outage. This signal is active high.

SA[19::0] (I/O)

Address bits SA[19::0] are used to address memory and I/O devices within the system. These twenty address lines, in addition to LA[23::17], allow access

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of up to 16MB of memory. SA[19::0] are gated on the system bus when BALE is high and are latched on the falling edge of BALE. These signals are generated by the microprocessor or DMA Controller. They also may be driven by other microprocessors or DMA controllers that reside on the I/O channel.

SBHE# (I/O)

System Bus High Enable (SBHE#) indicates a transfer of data on the upper byte of the data bus, D[15::8]. 16-bit devices use SBHE# to condition data bus buffers tied to D[15::8].

SMRDC# (O), MRDC# (I/O)

These signals instruct the memory devices to drive data onto the data bus. SMRDC# is active only when the memory decode is within the low 1MB of memory space. MRDC# is active on all memory read cycles. MRDC# may be driven by any microprocessor or DMA controller in the system. SMRDC is derived from MRDC# and the decode of the low 1MB of memory. When a microprocessor on the I/O channel wishes to drive MRDC#, it must have the address lines valid on the bus for one system clock period before driving MRDC# active. Both signals are active low.

SMWTC# (O), MWTC# (I/O)

These signals instruct the memory devices to store the data present on the data bus. SMWTC# is active only when the memory decode is within the low 1MB of the memory space. MWTC# is active on all memory write cycles. MWTC# may be driven by any microprocessor or DMA controller in the system. SMWTC# is derived from MWTC# and the decode of the low 1MB of memory. When a microprocessor on the I/O channel wishes to drive MWTC#, it must have the address lines valid on the bus for one system clock period before driving MWTC# active. Both signals are active low.

T-C (O)

Terminal Count (T-C) provides a pulse when the terminal count for any DMA channel is reached.

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I/O ADDRESS MAP *

Hex Range	Device
000-01F	DMA Controller 1
020-03F	Interrupt Controller 1, Master
040-05F	Timer
060-06F	8042 (Keyboard)
070-07F	Realtime Clock, NMI (non-maskable interrupt) Mask
080-09F	DMA Page Register
0A0-0BF	Interrupt Controller 2
0C0-0DF	DMA Controller 2
0F0	Clear Math Coprocessor Busy
0F1	Reset Math Coprocessor
0F8-0FF	Math Coprocessor
1F0-1F8	Fixed Disk
200-207	Game I/O
278-27F	Parallel Printer Port 2
2F8-2FF	Serial Port 2
300-31F	Prototype Card
360-36F	Reserved
378-37F	Parallel Printer Port 1
380-38F	SDLC, Bisynchronous 2
3A0-3AF	Bisynchronous 1
3B0-3BF	Monochrome Display and Printer Adapter
3C0-3CF	Reserved
3D0-3DF	Color/Graphics Monitor Adapter
3F0-3F7	Diskette Controller
3F8-3FF	Serial Port 1

INTERRUPT ASSIGNMENTS *

Interrupt	Description
IRQ0	Timer Output 0
IRQ1	Keyboard (Output Buffer Full)
IRQ2	Interrupt 8 through 15
IRQ3	Serial Port 2
IRQ4	Serial Port 1
IRQ5	Parallel Port 2
IRQ6	Diskette Controller
IRQ7	Parallel Port 1
IRQ8	Realtime Clock Interrupt
IRQ9	Software Redirected to INT 0AH (IRQ2)
IRQ10	Unassigned
IRQ11	Unassigned
IRQ12	PS/2 Mouse
IRQ13	Coprocessor
IRQ14	Fixed Disk Controller
IRQ15	Unassigned (may be assigned by the system to the secondary IDE)

* These are typical parameters, which may not reflect your current system.

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PCI LOCAL BUS

PCI OVERVIEW

The PCI (Peripheral Component Interconnect) Local Bus is a high performance, 32-bit or 64-bit bus with multiplexed address and data lines. It is intended for use as an interconnect mechanism between highly integrated peripheral controller components, peripheral add-in boards and processor/memory systems.

The "local bus" moves peripheral functions with high bandwidth requirements closer to the system's processor bus and can produce substantial performance gains with graphical user interfaces (GUI's) and other high bandwidth functions (i.e., full motion video, SCSI, LAN's, etc.).

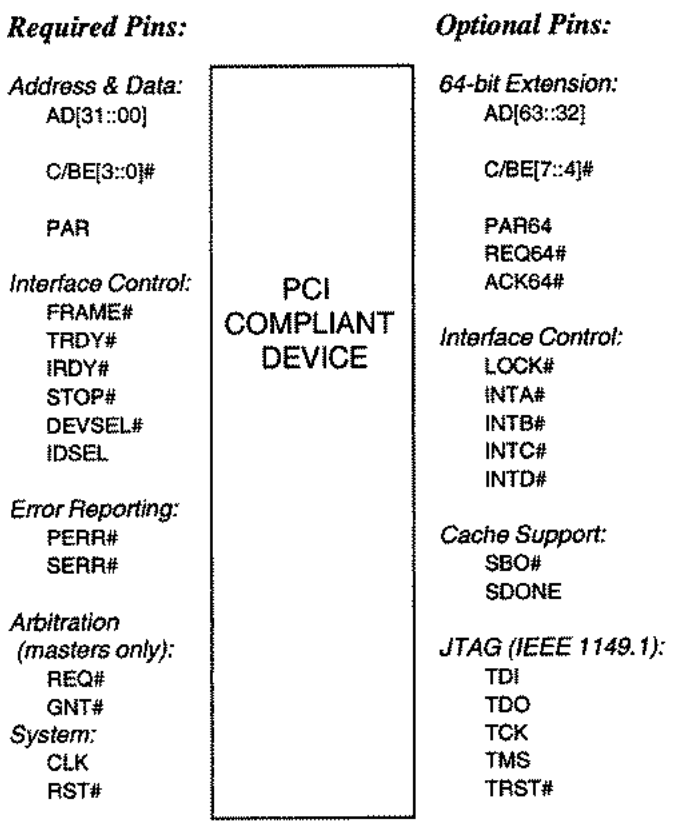
The PCI Local Bus accommodates future system requirements and is applicable across multiple platforms and architectures.

The PCI component and add-in card interface is processor independent, enabling an efficient transition to future processor generations, by bridges or by direct integration, and use with multiple processor architectures. Processor independence allows the PCI Local Bus to be optimized for I/O functions, enables concurrent operation of the local bus with the processor/memory subsystem, and accommodates multiple high performance peripherals in addition to graphics. Movement to enhanced video and multimedia displays and other high bandwidth I/O will continue to increase local bus bandwidth requirements. A transparent 64-bit extension of the 32-bit data and address buses is defined, doubling the bus bandwidth and offering forward and backward compatibility of 32-bit (132MB/s peak) and 64-bit (264MB/s peak) PCI Local Bus peripherals.

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PCI LOCAL BUS SIGNAL DEFINITION

The PCI interface requires a minimum of 47 pins for a target-only device and 49 pins for a master to handle data and addressing, interface control, arbitration and system functions. The diagram below shows the pins in functional groups, with required pins on the left side and optional pins on the right side.

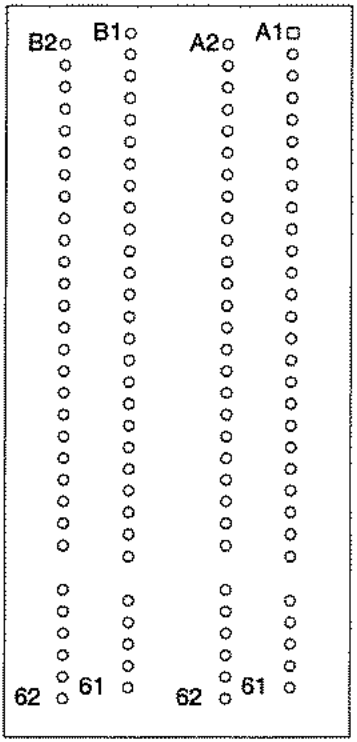


PCI Pin List

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PCI LOCAL BUS PIN NUMBERING

Component Side of Board



5-volt/32-bit PCI Connector

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PCI LOCAL BUS PIN ASSIGNMENTS

The PCI Local Bus specifies both 5-volt and 3.3-volt signaling environments. The bus pin assignments shown below are for the 5-volt connector. The 3.3-volt connector bus pin assignments are the same with the following exceptions:

* The pins noted as +V (I/O) are +5 volts or +3.3 volts, depending on which connector is being used.

† Pins B12, B13, A12 and A13 are Gnd (ground) on the 5-volt connector, but are Connector Keys on the 3.3-volt connector.

†† Pins B50, B51, A50 and A51 are Connectors Keys on the 5-volt connector, but are Gnd (ground) on the 3.3-volt connector.

I/O Pin	Signal Name
B1	-12V
B2	TCK
B3	Gnd
B4	TDO
B5	+5V
B6	+5V
B7	INTB#
B8	INTD#
B9	PRSNT1#
B10	Reserved
B11	PRSNT2#
B12	Gnd †
B13	Gnd †
B14	Reserved
B15	Gnd
B16	CLK
B17	Gnd
B18	REQ#
B19	+V (I/O) *
B20	AD31
B21	AD29
B22	Gnd

I/O Pin	Signal Name
A1	TRST#
A2	+12V
A3	TMS
A4	TDI
A5	+5V
A6	INTA#
A7	INTC#
A8	+5V
A9	Reserved
A10	+V (I/O) *
A11	Reserved
A12	Gnd †
A13	Gnd †
A14	Reserved
A15	RST#
A16	+V (I/O) *
A17	GNT#
A18	Gnd
A19	Reserved
A20	AD30
A21	+3.3V
A22	AD28

32-bit connector start

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PCI LOCAL BUS PIN ASSIGNMENTS (continued)

I/O Pin	Signal Name	I/O Pin	Signal Name	
B23	AD27	A23	AD26	
B24	AD25	A24	Gnd	
B25	+3.3V	A25	AD24	
B26	C/BE3#	A26	IDSEL	
B27	AD23	A27	+3.3V	
B28	Gnd	A28	AD22	
B29	AD21	A29	AD20	
B30	AD19	A30	Gnd	
B31	+3.3V	A31	AD18	
B32	AD17	A32	AD16	
B33	C/BE2#	A33	+3.3V	
B34	Gnd	A34	FRAME#	
B35	IRDY#	A35	Gnd	
B36	+3.3V	A36	TRDY#	
B37	DEVSEL#	A37	Gnd	
B38	Gnd	A38	STOP#	
B39	LOCK#	A39	+3.3V	
B40	PERR#	A40	SDONE	
B41	+3.3V	A41	SBO#	
B42	SERR#	A42	Gnd	
B43	+3.3V	A43	PAR	
B44	C/BE1#	A44	AD15	
B45	AD14	A45	+3.3V	
B46	Gnd	A46	AD13	
B47	AD12	A47	AD11	
B48	AD10	A48	Gnd	
B49	Gnd	A49	AD9	
B50	Connector Key ††	A50	Connector Key ††	5-volt key
B51	Connector Key ††	A51	Connector Key ††	5-volt key
B52	AD8	A52	C/BE0#	
B53	AD7	A53	+3.3V	
B54	+3.3V	A54	AD6	
B55	AD5	A55	AD4	
B56	AD3	A56	Gnd	
B57	Gnd	A57	AD2	
B58	AD1	A58	AD0	
B59	+V (I/O) *	A59	+V (I/O) *	
B60	ACK64#	A60	REQ64#	
B61	+5V	A61	+5V	
B62	+5V	A62	+5V	32-bit connector end

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PCI LOCAL BUS PIN ASSIGNMENTS (continued)

I/O Pin	Signal Name	I/O Pin	Signal Name	
	Connector Key		Connector Key	64-bit spacer
	Connector Key		Connector Key	64-bit spacer
B63	Reserved	A63	Gnd	64-bit connector start
B64	Gnd	A64	C/BE7#	
B65	C/BE6#	A65	C/BE5#	
B66	C/BE4#	A66	+V (I/O) *	
B67	Gnd	A67	PAR64	
B68	AD63	A68	AD62	
B69	AD61	A69	Gnd	
B70	+V (I/O) *	A70	AD60	
B71	AD59	A71	AD58	
B72	AD57	A72	Gnd	
B73	Gnd	A73	AD56	
B74	AD55	A74	AD54	
B75	AD53	A75	+V (I/O) *	
B76	Gnd	A76	AD52	
B77	AD51	A77	AD50	
B78	AD49	A78	Gnd	
B79	+V (I/O) *	A79	AD48	
B80	AD47	A80	AD46	
B81	AD45	A81	Gnd	
B82	Gnd	A82	AD44	
B83	AD43	A83	AD42	
B84	AD41	A84	+V (I/O) *	
B85	Gnd	A85	AD40	
B86	AD39	A86	AD38	
B87	AD37	A87	Gnd	
B88	+V (I/O) *	A88	AD36	
B89	AD35	A89	AD34	
B90	AD33	A90	Gnd	
B91	Gnd	A91	AD32	
B92	Reserved	A92	Reserved	
B93	Reserved	A93	Gnd	
B94	Gnd	A94	Reserved	64-bit connector end

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PCI LOCAL BUS SIGNAL DESCRIPTIONS

The PCI Local Bus signals are described below and may be categorized into the following functional groups:

- System Pins
- Address and Data Pins
- Interface Control Pins
- Arbitration Pins (Bus Masters Only)
- Error Reporting Pins
- Interrupt Pins (Optional)
- Cache Support Pins (Optional)
- 64-Bit Bus Extension Pins (Optional)
- JTAG/Boundary Scan Pins (Optional)

A # symbol at the end of a signal name indicates that the active state occurs when the signal is at a low voltage. When the # symbol is absent, the signal is active at a high voltage.

The following are descriptions of the PCI Local Bus signals.

ACK64# (optional)

Acknowledge 64-bit Transfer, when actively driven by the device that has positively decoded its address as the target of the current access, indicates the target is willing to transfer data using 64 bits. ACK64# has the same timing as DEVSEL#.

AD[31::00]

Address and Data are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. During the address phase, AD[31::00] contain a physical address (32 bits). During data phases, AD[07::00] contain the least significant byte (lsb) and AD[31::24] contain the most signficant byte (msb).

AD[63::32] (optional)

Address and Data are multiplexed on the same pins and provide 32 additional bits. During an address phase (when using the DAC command and when REQ64# is asserted), the upper 32 bits of a 64-bit address are transferred;

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otherwise, these bits are reserved but are stable and indeterminate. During a data phase, an additional 32 bits of data are transferred when REQ64# and ACK64# are both asserted.

C/BE[3::0]#

Bus Command and Byte Enables are multiplexed on the same PCI pins. During the address phase of a transaction, these pins define the bus command; during the data phase they are used as byte enables. The byte enables are valid for the entire data phase and determine which byte lanes carry meaningful data. C/BE0# applies to byte 0 (lsb) and C/BE3# applies to byte 3 (msb).

C/BE[7::4]# (optional)

Bus Command and Byte Enables are multiplexed on the same pins. During an address phase (when using the DAC command and when REQ64# is asserted), the actual bus command is transferred on C/BE[7::4]#; otherwise, these bits are reserved and indeterminate. During a data phase, C/BE[7::4]# are byte enables indicating which byte lanes carry meaningful data when REQ64# and ACK64# are both asserted. C/BE4# applies to byte 4 and C/BE7# applies to byte 7.

CLK

Clock provides timing for all transactions on PCI and is an input to every PCI device.

DEVSEL#

Device Select, when actively driven, indicates that the driving device has decoded its address as the target of the current access. As an input, DEVSEL# indicates whether any device on the bus has been selected.

FRAME#

Cycle Frame is an interface control pin which is driven by the current master to indicate the beginning and duration of an access. When FRAME# is asserted, data transfers continue; when it is deasserted, the transaction is in the final data phase.

GNT#

Grant indicates to the agent that access to the bus has been granted. This is a point to point signal. Every master has its own GNT#.

IDSEL

Initialization Device Select is used as a chip select during configuration read and write transactions.

INTA#, INTB#, INTC#, INTD# (optional)

Interrupts on PCI are optional and defined as "level sensitive," asserted low (negative true), using open drain output drivers. PCI defines one interrupt for

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a single function and up to four interrupt lines for a multi-function device or connector.

Interrupt A is used to request an interrupt. For a single function device, only INTA# may be used, while the other three interrupt lines have no meaning.

Interrupt B, Interrupt C and Interrupt D are used to request additional interrupts and only have meaning on a multi-function device.

IRDY#

Initiator Ready indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#. During a write, IRDY# indicates that valid data is present on AD[31::0]. During a read, it indicates that the master is prepared to accept data.

LOCK#

Lock indicates an operation that may require multiple transactions to complete. When LOCK# is asserted, non-exclusive transactions may proceed to an address that is not currently locked.

PAR

Parity is even parity across AD[31::00] and C/BE[3::0]#. Parity generation is required by all PCI agents. The master drives PAR for address and write data phases; the target drives PAR for read data phases.

PAR64 (optional)

Parity Upper DWORD is the even parity bit that protects AD[63::32] and C/BE[7::4]#. The master drives PAR64 for address and write data phases; the target drives PAR64 for read data phases.

PERR#

Parity Error is for the reporting of data parity errors during all PCI transactions except a Special Cycle. There are no special conditions when a data parity error may be lost or when reporting of an error may be delayed.

PRSNT1# and PRSNT2#

PRSNT1# and PRSNT2# are related to the connector only, not to other PCI components. They are used for two purposes: indicating that a board is physically present in the slot and providing information about the total power requirements of the board.

REQ#

Request indicates to the arbiter that this agent desires use of the bus. This is a point to point signal. Every master has its own REQ#.

REQ64# (optional)

Request 64-bit Transfer, when actively driven by the current bus master, indicates it desires to transfer data using 64 bits. REQ64# has the same timing as FRAME#. REQ64# has meaning at the end of reset.

RST#

Reset is used to bring PCI-specific registers, sequencers and signals to a consistent state.

SBO# (optional)

Snoop Backoff is an optional cache support pin which indicates a hit to a modified line when asserted. When SBO# is deasserted and SDONE is asserted, it indicates a "clean" snoop result.

SDONE (optional)

Snoop Done is an optional cache support pin which indicates the status of the snoop for the current access. When deasserted, it indicates the result of the snoop is still pending. When asserted, it indicates the snoop is complete.

SERR#

System Error is for reporting address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic. If an agent does not want a non-maskable interrupt (NMI) to be generated, a different reporting mechanism is required.

STOP#

Stop indicates that the current target is requesting the master to stop the current transaction.

TCK (optional)

Test Clock is used to clock state information and test data into and out of the device during operation of the TAP (Test Access Port).

TDI (optional)

Test Data Input is used to serially shift test data and test instructions into the device during TAP (Test Access Port) operation.

TDO (optional)

Test Data Output is used to serially shift test data and test instructions out of the device during TAP (Test Access Port) operation.

TMS (optional)

Test Mode Select is used to control the state of the TAP (Test Access Port) controller in the device.

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TRDY#

Target Ready indicates the target agent's (selected device's) ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. During a read, TRDY# indicates that valid data is present on AD[31::00]. During a write, it indicates that the target is prepared to accept data.

TRST# (optional)

Test Reset provides an asynchronous initialization of the TAP controller. This signal is optional in the IEEE Standard Test Access Port and Boundary Scan Architecture.

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BIOS OPERATION

Sections 3 through 8 of this manual describe the operation of the American Megatrends Hi-Flex AMIBIOS and the AMIBIOS Setup Utility. Refer to *Running AMIBIOS Setup* later in this section for standard Setup screens, options and defaults. The available Setup screens, options and defaults may vary if you have a custom BIOS.

When the system is powered on, AMIBIOS performs the Power-On Self Test (POST) routines. These routines are divided into two phases:

1) **System Test and Initialization**. Test and initialize system boards for normal operations.

2) **System Configuration Verification**. Compare defined configuration with hardware actually installed.

If an error is encountered during the diagnostic tests, the error is reported in one of two different ways. If the error occurs before the display device is initialized, a series of beeps is transmitted. If the error occurs after the display device is initialized, the error message is displayed on the screen. See *BIOS Errors* later in this section for more information on error handling.

The following are some of the Power-On Self Tests (POST's) which are performed when the system is powered on:

- CMOS Checksum Calculation
- Keyboard Controller Test
- CMOS Shutdown Register Test
- 8254 Timer Test
- Memory Refresh Test
- Display Memory Read/Write Test
- Display Type Verification
- Entering Protected Mode

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- Memory Size Calculation
- Conventional and Extended Memory Test
- DMA Controller Tests
- Keyboard Test
- System Configuration Verification and Setup

NOTE: When you perform a warm boot by pressing **<Ctrl> + <Alt> + <Del>**, all memory tests are bypassed.

AMIBIOS checks all system and cache memory and reports them on both the initial AMIBIOS screen and the AMIBIOS System Configuration screen which appears after POST is completed. AMIBIOS attempts to initialize the peripheral devices by verifying the validity of the system setup information stored in the system CMOS RAM. (See the *Running AMIBIOS Setup* section of this manual.) If AMIBIOS detects a fault, the screen displays the error condition(s) which has/have been detected. If no errors are detected, AMIBIOS attempts to load the system from any bootable device, such as a floppy disk or hard disk.

Normally, the only POST routine visible on the screen is the memory test. The following screen displays when the system is powered on:

```
AMIBIOS (C)1998 American Megatrends Inc.
TRENTON Technology Inc.


Hit DEL if you want to run SETUP
```

Initial Power-On Screen

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You have two options:

- Press **<Del>** to access the AMIBIOS Setup Utility.

  This option allows you to change various system parameters such as date and time, disk drives, etc. The *Running AMIBIOS Setup* section of this manual describes the options available.

  You may be requested to enter a password before gaining access to the AMIBIOS Setup Utility. (See *Password Entry* later in this section.)

  If you enter the correct password or no password is required, the AMIBIOS Setup Main Menu displays. (See *Running AMIBIOS Setup* later in this section.)

- Allow the bootup process to continue without invoking the AMIBIOS Setup Utility.

  In this case, after AMIBIOS loads the system, you may be requested to enter a password. (See *Password Entry* later in this section.)

Once the POST routines complete successfully, a screen displays showing the current configuration of your system, including processor type, base and extended memory amounts, floppy and hard drive types, display type and peripheral ports.

In systems with more than 1MB, AMIBIOS reports 384KB less RAM than it finds, because it accounts for the address space between 640K and 1024K which is unavailable to DOS. This space is used for video RAM, video BIOS, system BIOS and adapter ROMs.

Password Entry

The system may be configured so that the user is required to enter a password each time the system boots or whenever an attempt is made to enter AMIBIOS Setup. The password function may also be disabled so that the password prompt does not appear under any circumstances.

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The **Password Check** option in the Advanced CMOS Setup program allows you to specify when the password prompt displays: **Always** or only when **Setup** is attempted. The supervisor and user passwords may be changed using the **Change Supervisor Password** and **Change User Password** options on the AMIBIOS Setup Main Menu. If the passwords are null, the password prompt does not display at any time. A more detailed description of the password setup function may be found in the *Running AMIBIOS Setup* section of this manual.

When password checking is enabled, the following password prompt displays:

```
Enter CURRENT Password:
```

Type the password and press **<Enter>**.

NOTE: The null password is the system default and is in effect if a password has not been assigned or if the CMOS has been corrupted. In this case, the password prompt does not display. To set up passwords, you may use the **Change Supervisor Password** and **Change User Password** options on the AMIBIOS Setup Main Menu. (See the *Running AMIBIOS Setup* section of this manual.)

If an incorrect password is entered, the following screen displays:

```
Enter CURRENT Password: X
Enter CURRENT Password:
```

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You may try again to enter the correct password. If you enter the password incorrectly *three* times, the system responds in one of two different ways, depending on the value specified in the **Password Check** option on the Advanced CMOS Setup screen:

1) If the **Password Check** option is set to **Setup**, the system does not let you enter Setup, but does continue the booting process. You must reboot the system manually to retry entering the password.

2) If the **Password Check** option is set to **Always**, the system locks and you must reboot. After rebooting, you will be requested to enter the password.

Once the password has been entered correctly, you are allowed to continue.

BIOS Errors

If an error is encountered during the diagnostic checks performed when the system is powered on, the error is reported in one of two different ways:

1) If the error occurs before the display device is initialized, a series of beeps is transmitted.

2) If the error occurs after the display device is initialized, the screen displays the error message. In the case of a non-fatal error, a prompt to press the <F1> key may also appear on the screen.

Explanations of the beep codes and BIOS error messages may be found in *Appendix A - BIOS Messages*.

As the POST routines are performed, test codes are presented on Port 80H. These codes may be helpful as a diagnostic tool and are listed in *Appendix A - BIOS Messages*.

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If certain non-fatal error conditions occur, you are requested to run the AMIBIOS Setup Utility. The error messages are followed by this screen:

```
AMIBIOS (C)1998 American Megatrends Inc.
TRENTON Technology Inc.


RUN SETUP UTILITY
Press F1 to Resume
```

Press **<F1>**. You may be requested to enter a password before gaining access to the AMIBIOS Setup Utility. (See *Password Entry* earlier in this section.)

If you enter the correct password or no password is required, the AMIBIOS Setup Main Menu displays.

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RUNNING AMIBIOS SETUP

AMIBIOS Setup keeps a record of system parameters, such as date and time, disk drives, display type and other user-defined parameters. The Setup parameters reside in the Read Only Memory Basic Input/Output System (ROM BIOS) so that they are available each time the system is turned on. AMIBIOS Setup stores the information in the complementary metal oxide semiconductor (CMOS) memory. When the system is turned off, a backup battery retains system parameters in the CMOS memory.

Each time the system is powered on, it is configured with these values, unless the CMOS has been corrupted or is faulty. The AMIBIOS Setup Utility is resident in the ROM BIOS (Read Only Memory Basic Input/Output System) so that it is available each time the computer is turned on. If, for some reason, the CMOS becomes corrupted, the system is configured with the default values stored in this ROM file.

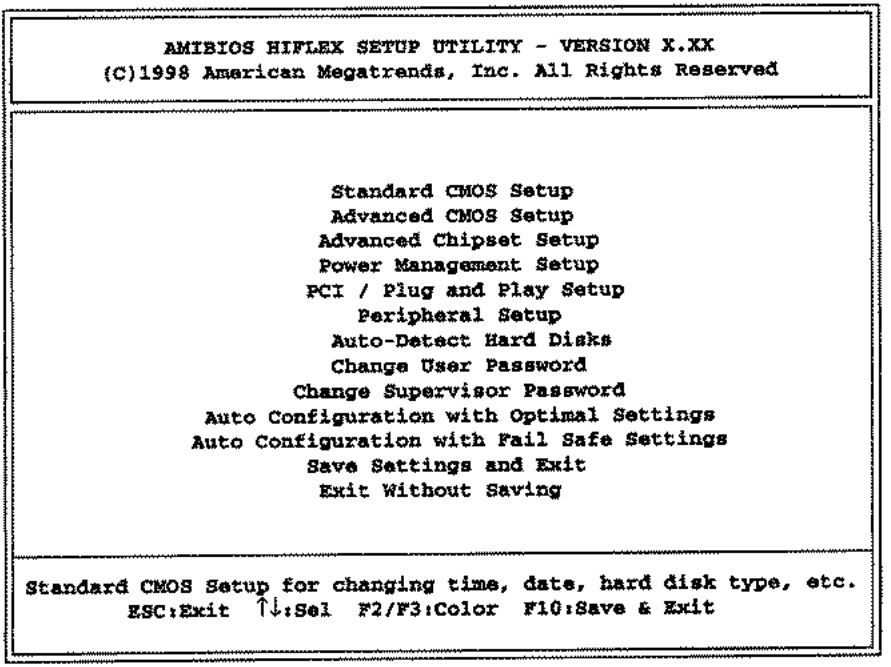
As soon as the system is turned on, the power-on diagnostic routines check memory, attempt to prepare peripheral devices for action, and offer you the option of pressing <Del> to run AMIBIOS Setup.

If certain non-fatal errors occur during the Power-On Self Test (POST) routines which are run when the system is turned on, you may be prompted to run AMIBIOS Setup by pressing <F1>.

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AMIBIOS SETUP MAIN MENU

When you press **<F1>** in response to an error message received during the POST routines or when you press the **<Del>** key to enter the AMIBIOS Setup Program, the following screen displays:



AMIBIOS Setup Main Menu

Use the **Down Arrow** key to highlight the desired option and press **<Enter>**.

- Select **Standard CMOS Setup** to make changes to Standard CMOS Setup parameters. The Setup program is described in the *Standard CMOS Setup* section of this manual. The following options may be changed:
  - Date/Time
  - Floppy Drive A:/Floppy Drive B: Types
  - Primary Master and Slave Disk Types

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- Secondary Master and Slave Disk Types
- Logical Block Address (LBA) Mode
- Block Mode
- PIO Mode
- 32Bit Mode
- Boot Sector Virus Protection

- Select **Advanced CMOS Setup** to make changes to Advanced CMOS Setup parameters. The Setup program is described in the *Advanced Setup* section of this manual. The following options may be changed:
  - Quick Boot
  - ARMD Emulation for IDE Devices
  - 1st Boot Device
  - 2nd Boot Device
  - 3rd Boot Device
  - Try Other Boot Devices
  - Initialize I2O Devices
  - Display Mode at Add-On ROM Init
  - Floppy Access Control
  - Hard Disk Access Control
  - S.M.A.R.T. for Hard Disks
  - BootUp Num-Lock
  - PS/2 Mouse Support
  - System Keyboard
  - Primary Display
  - Password Check
  - Parity Check

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- Boot to OS/2
- Internal Cache
- External Cache
- System BIOS Cacheable
- Cache Bus ECC
- Video and Adapter ROM Shadow

- Select **Advanced Chipset Setup** to make changes to Advanced Chipset Setup parameters. The Setup program is described in the *Advanced Setup* section of this manual. The following options may be changed:
  - USB Function
  - USB KB/Mouse Legacy Support
  - Port 64/60 Emulation
  - System Error Signal (SERR#)
  - Parity Error Signal (PERR#)
  - USWC Write Post
  - BX Master Latency Timer
  - Multi-Transaction Timer
  - PCI1 to PCI0 Access
  - DRAM Integrity Mode
  - DRAM Refresh Rate
  - Memory Hole
  - Graphics Aperture Size
  - AGP Multi-Transaction Timer
  - AGP Low-Priority Timer
  - AGP System Error Signal (SERR)
  - AGP Parity Error Response

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- 8bit and 16bit I/O Recovery Time
- PIIX4 System Error Signal (SERR#)
- USB Passive Release Enable
- PIIX4 Passive Release
- PIIX4 Delayed Transaction
- TypeF DMA Buffer Controls 1 and 2
- DMA-0, DMA-1, DMA-2, DMA-3, DMA-5, DMA-6 and DMA-7 Types

- Select **Power Management Setup** to make changes to Power Management Setup parameters. The Setup program is described in the *Power Management Setup* section of this manual. The following options may be changed:
  - ACPI Aware O/S
  - Power Management/APM
  - Power Button Function
  - Green PC Monitor Power State
  - Video Power Down Mode
  - Hard Disk Power Down Mode
  - Hard Disk Time Out
  - Power Saving Type
  - Standby/Suspend Timer Unit
  - Standby Time Out
  - Suspend Time Out
  - Slow Clock Ratio
  - Display Activity
  - Device 0 through Device 8 Monitor

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- Select **PCI/Plug and Play Setup** to make changes to PCI/Plug and Play Setup parameters. The Setup program is described in the *PCI/Plug and Play Setup* section of this manual. The following options may be changed:
    - On Board LAN
    - On Board Video
    - On Board SCSI
    - Plug and Play Aware O/S
    - PCI Latency Timer
    - PCI VGA Palette Snoop
    - PCI IDE BusMaster
    - OffBoard PCI IDE Card
    - OffBoard PCI IDE Primary and Secondary IRQs
    - DMA Channels 0, 1, 3, 5, 6 and 7
    - IRQ5 /IRQ9/IRQ10/IRQ11/IRQ15
    - Reserved Memory Size and Address
- Select **Peripheral Setup** to make changes to the Peripheral Setup parameters. The Setup program is described in the *Peripheral Setup* section of this manual. The following options may be changed:
    - OnBoard FDC
    - OnBoard Serial Port 1
    - OnBoard Serial Port 2
        - Receiver Polarity
        - Transmitter Polarity
    - OnBoard Parallel Port
        - Parallel Port Mode
        - EPP Version

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- Parallel Port IRQ
- Parallel Port DMA Channel

- OnBoard IDE

- Select **Auto-Detect Hard Disks** to have AMIBIOS automatically detect the type and parameters of each hard drive if you have IDE drive(s). This option is described later in this section.

- Select **Change User Password** to establish or change the password for the user. This function is described later in this section.

- Select **Change Supervisor Password** to establish or change the password for the supervisor. This function is described later in this section.

- Select **Auto Configuration with Optimal Settings** to load the Optimal default settings. These settings are best-case values which should provide the best performance characteristics. This function is described later in this section.

- Select **Auto Configuration with Fail Safe Settings** to load the Fail Safe default settings. These settings are more likely to configure a workable computer, but they may not provide optimal performance. This function is described later in this section.

- Select **Save Settings and Exit** to store your changes in the CMOS. The CMOS checksum is calculated and written to the CMOS. Control is then passed back to AMIBIOS and the booting process continues, using the new CMOS values. This function is described later in this section.

- Select **Exit Without Saving** to pass control back to the AMIBIOS *without* writing any changes to the CMOS. AMIBIOS continues with the booting process. This function is described later in this section.

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AUTO-DETECT HARD DISKS

The **Auto-Detect Hard Disks** option allows you to have AMIBIOS automatically detect the type of hard disk drive(s) in your system. The automatic detection functions only if you have IDE drives. The parameters are reported on the Standard CMOS Setup screen.

AMIBIOS searches first for the primary master and slave hard disk drives, then for the secondary master and slave drives. If it can access a drive, it reads the disk parameters. It then searches the AMIBIOS drive type table for matching parameters to determine the disk type and displays both the type and parameters on the screen. If no matching parameters are found in the table, AMIBIOS specifies the type as "User" and fills in the parameter values it found on the drive. If it cannot access the drive or if it is not an IDE drive, AMIBIOS times out and specifies that the disk drive is "Not Installed."

NOTE: The auto detect feature displays disk parameter values as established by the drive manufacturer. If the drive has been formatted using any other values, accepting the auto detect values will cause erratic behavior. You must either reformat the drive to meet the manufacturer's specifications or use Standard CMOS Setup to enter parameters which match the current format of the drive.

If you do not want to accept the hard disk type and its associated parameters as reported by AMIBIOS or if the drive is "Not Installed," you may use Standard CMOS Setup to set up the correct parameters for the drive.

Once the parameters are correct for all of the drives, you may exit from the Standard CMOS Setup screen and save the settings in the CMOS.

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CHANGE PASSWORD

AMIBIOS Setup has an optional password feature which can be configured so that a password must be entered each time the system boots or just when a user attempts to enter AMIBIOS Setup. (See the *Advanced CMOS Setup* section of this manual for information on how to enable the **Password Check** option.)

The **Change Supervisor Password** and **Change User Password** options on the AMIBIOS Setup Main Menu allow you to establish passwords, change the current passwords or disable the password prompts by entering null passwords. The passwords are stored in CMOS RAM.

The **Change User Password** function is accessible only if the supervisor password has been established previously. If you have signed on under the user password, you cannot change the supervisor password.

NOTE: The null password is the system default and is in effect if a password has not been assigned or if the CMOS has been corrupted. In this case, the "Enter CURRENT Password" prompt is bypassed when you boot the system, and you must establish a new password.

Change Supervisor Password

If you select the **Change Supervisor Password** option, the following window displays:

```
Enter new supervisor password: _
```

This is the message which displays before you have established a password, or if the last password entered was the null password. If a password has already been established, you are asked to enter the current password before being prompted to enter the new password.

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Type the new password and press **<Enter>**. The password cannot exceed six (6) characters in length. The screen does not display the characters as you type them.

After you have entered the new password, the following window displays:

```
Retype new supervisor password: _
```

Re-key the new password as described above.

If the password confirmation is miskeyed, AMIBIOS Setup displays the following message:

```
Incorrect password, press any key to continue
```

No retries are permitted; you must restart the procedure from the AMIBIOS Setup Main Menu.

If the password confirmation is entered correctly, the following message displays:

```
New supervisor password installed, press any key to continue
```

When you press any key, the screen returns to the AMIBIOS Setup Main Menu screen, which allows you to save the password change or exit from Setup without saving the new password. To save the new password in CMOS memory, be sure to select **Save Settings and Exit**.

If you save the changes when you exit AMIBIOS Setup, the password is stored in CMOS RAM. The next time the system boots, you are prompted for the password if the password function is present and is enabled. (See *Advanced CMOS Setup* later in this manual for an explanation of how to enable password checking.)

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NOTE: Be sure to keep a record of the new password each time it is changed. If you forget it, use the Password Clear jumper to reset it to the default (null password). See the *Specifications* section of this manual for details.

Change User Password

The **Change User Password** function is accessible only if the supervisor password has been established previously.

The **Change User Password** option is similar in functionality to the **Change Supervisor Password** and displays the same messages, except that "user" replaces "supervisor." If you have signed on under the user password, you cannot change the supervisor password.

Disabling the Password(s)

To *disable* password checking so that the password prompt does not appear under any circumstances, you may create null passwords using the **Change Supervisor Password** and **Change User Password** functions by pressing **<Enter>** without typing in a new password. You will be asked to confirm the password. Select **<Enter>** again and the following message displays:

```
Supervisor password disabled, press any key to continue
```

When you press any key, the screen returns to the AMIBIOS Setup Main Menu, which allows you to save the password change or exit from Setup without saving the null password. To save the null password(s) in CMOS memory, be sure to select **Save Settings and Exit**.

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AUTO CONFIGURATION OPTIONS

Each AMIBIOS Setup option has two default settings (Optimal and Fail Safe). These settings can be applied to all AMIBIOS Setup options when you select the appropriate auto configuration option from the AMIBIOS Setup Main Menu.

You can use these auto configuration options to quickly set the system configuration parameters which should provide the best performance characteristics, or you can select a group of settings which have a better chance of working when the system is having configuration-related problems.

Auto Configuration with Optimal Settings

This option allows you to load the Optimal default settings. These settings are best-case values which should provide the best performance characteristics. If CMOS RAM is corrupted, the Optimal settings are loaded automatically.

If you select the **Auto Configuration with Optimal Settings** option, the following window displays:

```
Load high performance settings (Y/N) ? N
```

You have two options:

- Press '**N**' and **<Enter>** to leave the current values in effect.
- Press '**Y**' and **<Enter>** to load the Optimal default settings.

Auto Configuration with Fail Safe Settings

This option allows you to load the Fail Safe default settings when you cannot boot your computer successfully. These settings are more likely to configure a workable computer. They may not provide optimal performance, but are the most stable settings. You may use this option as a diagnostic aid if your system is behaving

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erratically. Select the Fail Safe settings and then try to diagnose the problem after the computer boots.

If you select the **Auto Configuration with Fail Safe Settings** option, the following window displays:

```
Load failsafe settings (Y/N) ? N
```

You have two options:

- Press '**N**' and **<Enter>** to leave the current values in effect.
- Press '**Y**' and **<Enter>** to load the Fail Safe default settings.

SAVE SETTINGS AND EXIT

The features selected and configured in the Setup screens are stored in the CMOS when this option is selected. The CMOS checksum is calculated and written to the CMOS. Control is then passed back to the AMIBIOS and the booting process continues, using the new CMOS values.

If you select the **SAVE SETTINGS AND EXIT** option, the following window displays:

```
Save current settings and exit (Y/N) ? Y
```

You have two options:

- Press '**N**' and **<Enter>** to return to the AMIBIOS Setup Main Menu.
- Press '**Y**' and **<Enter>** to *save* the system parameters and continue with the booting process.

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EXIT WITHOUT SAVING

This option passes control back to AMIBIOS *without* writing any changes to the CMOS.

If you select the **EXIT WITHOUT SAVING** option, the following window displays:

```
Quit without saving the current settings (Y/N) ? N
```

You have two options:

- Press '**N**' and **<Enter>** to return to the AMIBIOS Setup Main Menu.
- Press '**Y**' and **<Enter>** to continue with the booting process *without* saving any system parameters.

KEY CONVENTIONS

Listed below is an explanation of the keys you may use for navigation and selection in the AMIBIOS Setup Utility:

Key	Task
<Esc>	Close the current operation and return to the previous level.
<Tab>	Move to the next field.
Arrow keys	Move to the next field in the desired direction.
<Enter>	Select the current item.
<F2>/<F3>	Change background and foreground colors.
<F10>	Save all changes made to Setup and exit from the AMIBIOS Setup Utility.
Plus key (+), <PgUp>	Increment a value.
Minus key (-), <PgDn>	Decrement a value.

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STANDARD CMOS SETUP

When you select **Standard CMOS Setup** from the AMIBIOS Setup Main Menu, the following Setup screen displays:

```
                AMIBIOS SETUP - STANDARD CMOS SETUP
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Date (mm/dd/yyyy): Mon Jan 01,1996              Base Memory: 640 KB
Time (hh/mm/ss):   12:30:00                     Extd Memory: 14 MB

Floppy Drive A:  1.44 MB 3 1/2
Floppy Drive B:  Not Installed
                                                LBA  Blk  PIO 32Bit
              Type     Size Cyln Head WPcom Sec Mode Mode Mode Mode
Pri Master : Auto                                              Off
Pri Slave  : Auto                                              Off
Sec Master : Auto                                              Off
Sec Slave  : Auto                                              Off

Boot Sector Virus Protection    Disabled

Month:  Jan - Dec                               ESC:Exit  ↓↑:Sel
  Day:   01 - 31                                PgUp/PgDn:Modify
 Year: 1901 - 2099                              F2/F3:Color
```

The Standard CMOS Setup Screen

When you display the Standard CMOS Setup screen, the format is similar to the sample shown above. If values display for all parameters, the Setup parameters have been defined previously. The available values for each option are displayed at the bottom of the screen when you tab or arrow into the field.

NOTE: The values on this screen do not necessarily reflect the values appropriate for your SBC. Refer to the explanations below for specific instructions about entering correct information.

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STANDARD CMOS OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not run the Standard CMOS Setup program yet. Once values have been defined, they display each time Standard CMOS Setup is run.

Date

The Setup screen displays the system option:

Date (mm/dd/yyyy): **Mon Jan 01, 1996**

The Help window displays allowable settings:

Month : Jan - Dec
Day : 01 - 31
Year : 1901 - 2099

There are three fields for entering the date. Use the left and right arrow keys or the tab key to move from one field to another; use the plus and minus (or PgUp and PgDn) keys to scroll through the allowable values for the field. As you scroll through the month, day or year field, the day of the week changes automatically to reflect the new date.

Time

The Setup screen displays the system option:

Time (hh/mm/ss): **00:00:00**

The Help window displays:

Time is 24 hour format:-
Hour:00-23 Minute:00-59 Second:00-59
(1:30AM = 01:30:00, 1:30PM = 13:30:00)

There are three fields for entering the time. Use the left and right arrow keys or the tab key to move from one field to another; use the

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plus and minus (or PgUp and PgDn) keys to scroll through the allowable values for the field.

Floppy Drive A:/Floppy Drive B:

The floppy drive type(s) in your system can be configured using these options.

The Setup screen displays the system options:

Floppy Drive A:	**1.44 MB 3-1/2**
Floppy Drive B:	**Not Installed**

Available options are:

Not Installed
360 KB 5-1/4
1.2 MB 5-1/4
720 KB 3-1/2
1.44 MB 3-1/2
2.88 MB 3-1/2

The **Not Installed** option can be used for diskless work stations.

Primary and Secondary Hard Disk Drives

The SBC supports up to four hard disk drives through a primary and secondary controller in a master/slave configuration. The primary controller uses I/O port addresses 1F0H through 1F7H, 3F6H and IRQ14. The secondary controller uses I/O port addresses 170H through 177H, 376H and IRQ15.

The AMIBIOS enhanced IDE (EIDE) interface can support IDE Type 4 disk drives. This EIDE interface allows disk drives greater than 528MB to be used.

The hard disk drives can be detected automatically by AMIBIOS (if they are IDE drives) or can be defined manually by the user, as described below.

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The Setup screen displays the system options:

Pri Master:	**Auto**
Pri Slave:	**Auto**
Sec Master:	**Auto**
Sec Slave:	**Auto**

The Help window displays:

1-46:	Predefined types
USER:	Enter parameters manually
AUTO:	Set parameters automatically on each boot
CD-ROM:	Use for ATAPI CD-ROM drives
Or press ENTER to set all HDD parameters automatically	

To set up the hard disk drive parameter(s), use the plus (+) key or PgDn key to scroll through the drive types to locate the correct type of disk drive(s) in your computer.

As you scroll through the disk types, the drive Type displays, along with values for size, cylinders, heads, write precompensation and sectors. Available predefined hard disk drive types are listed at the end of this section. If the parameters supplied by the manufacturer of your disk drive do not match any of these preprogrammed drive types, you may have AMIBIOS detect the drive type automatically (if it is an IDE drive), or you may select the **User** drive type to enter the parameters manually as described below.

Set the drive type to **CD-ROM** to boot from a CD-ROM drive.

Not Installed is available for use as an option. This option can be used for diskless work stations.

Automatic Detection of Drive Type

If any of the hard disks are IDE drives, AMIBIOS can automatically configure the drive type by detecting the IDE drive parameters and reporting them on the Standard CMOS Setup screen.

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You may invoke automatic detection of IDE drives in one of three ways:

- Press **Enter** when the cursor is in the **Type** field. AMIBIOS detects the drive type and parameters as requested. If the drive type is not defined in the drive type table, this option displays **User** as the drive type and displays the parameters which were detected by AMIBIOS. The detected drive type values may then be saved in the CMOS.
- Set the drive type to **Auto** to have AMIBIOS detect the drive type and parameters automatically *each time* the system is booted up. This option does not display the drive type on the Standard CMOS Setup screen, but does display it on the System Configuration screen shown after a successful bootup.
- Select the **Auto-Detect Hard Disks** option on the AMIBIOS Setup Main Menu to have AMIBIOS automatically detect the type and parameters of each hard drive and place the information into the Standard CMOS Setup screen. The detected drive type values may then be saved in the CMOS. This option is described in the *Running AMIBIOS Setup* section of the *System BIOS* chapter of this manual.

NOTE: The auto detect feature displays disk parameter values as established by the drive manufacturer. If the drive has been formatted using any other values, accepting the auto detect values will cause erratic behavior. You must either reformat the drive to meet the manufacturer's specifications or use the **User** type to enter parameters which match the current format of the drive.

User-Defined Drive Types

If the parameters supplied by the manufacturer of your disk drive do not match any of the preprogrammed drive types provided by AMIBIOS, you may enter the parameters manually.

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The user-defined parameters for each of the four drives may be different, which effectively allows four different user-definable hard disk types.

Scroll to the end of the drive type list to the **User** type. You can manually enter the Cyln, Head, WPcom and Sec parameters. The Size parameter is automatically calculated and displayed by the system based on the other parameters entered.

Use the arrow keys or tab key to move between fields. Once you have placed the cursor in a field, type in the correct value.

The following explains the drive parameters which you must enter for a drive type which is not in the list:

Type is the numeric designation for a drive with certain identification parameters.

Cylinders (Cyln) is the number of disk cylinders found in the specified drive type.

Heads (Head) is the number of disk heads found in the specified drive type.

Write Precompensation (WPcom) is the read delay circuitry which takes into account the timing differences between the inner and outer edges of the surface of the disk. The size of the sector gets progressively smaller as the track diameter diminishes. Yet each sector must still hold 512 bytes. Write precompensation circuitry on the hard disk compensates for the physical difference in sector size by boosting the write current for sectors on inner tracks. This parameter designates the track (cylinder) number where write precompensation begins.

Sectors (Sec) designates the number of disk sectors per track.

Size is the formatted capacity of the drive (in megabytes) based on the following formula:

# of heads x # of cylinders x # of sects/cyln x 512 bytes/sect

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IDE Drive Type Setup Options

For each of the four hard disk drives which is an IDE drive, the following options are also available for the drive:

Logical Block Addressing (LBA) Mode

This option allows you to enable IDE LBA (Logical Block Addressing) Mode for the specified primary or secondary IDE drive. Data is accessed by block addresses rather than by the traditional cylinder-head-sector format. This allows you to use drives larger than 528MB. In LBA mode, the maximum drive capacity supported is 8.4GB (gigabytes).

If **LBA Mode** is set to **On** and is supported by the hard disk drive, and if the drive is formatted, AMIBIOS enables LBA mode and translates the physical parameters of the drive to logical parameters. If a hard disk drive which supports LBA mode and has a capacity greater than 528MB was formatted with LBA mode *disabled*, AMIBIOS does *not* enable LBA mode even if the **LBA Mode** parameter is set to **On** in Standard CMOS Setup.

If **LBA Mode** is set to **Off**, AMIBIOS uses the physical parameters of the hard disk and does not translate parameters. The operating system which uses the parameter table then sees only 528MB of hard disk space even if the drive contains more than 528MB.

Available options are:

Off
On

Block (Blk) Mode

This option supports transfer of multiple sectors to and from the specified primary or secondary IDE drive.

Block mode boosts IDE drive performance by increasing the amount of data transferred during an interrupt. Block mode allows transfers

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of up to 64KB per interrupt, whereas only 512 bytes of data can be transferred per interrupt if block mode is not used.

If **Block Mode** is set to **On** and is supported by the IDE drive, AMIBIOS enables multi-sector transfers. AMIBIOS sets the number of sectors to be transferred per interrupt to the value returned by the "identify drive" command.

Available options are:

Off
On

Programmed I/O (PIO) Mode

IDE PIO mode programs timing cycles between the IDE drive and the programmable IDE controller. As the PIO mode increases, the cycle time decreases.

Set the **PIO Mode** option to **Auto** to have AMIBIOS select the PIO mode used by the IDE drive being configured. If you select a specific value for the PIO mode, you must make *absolutely* certain that you are selecting the PIO mode supported by the IDE drive being configured.

Available options are:

Auto	
0	3
1	4
2	5

32Bit Mode

Hard disk drives connected to the SBC via the ISA Bus transfer data 16 bits at a time. An IDE drive on the PCI Local Bus can use a 32-bit data path.

If the **32Bit Mode** parameter is set to **On**, AMIBIOS enables 32-bit data transfers. If the host controller does not support 32-bit transfer, this feature *must* be disabled.

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Available options are:

Off
On

Boot Sector Virus Protection

This option allows you to request AMIBIOS to issue a warning when any program or virus issues a Disk Format command or attempts to write to the boot sector of the hard disk drive.

The Setup screen displays the system option:

Boot Sector Virus Protection Disabled

Available options are:

Disabled
Enabled

If the **Boot Sector Virus Protection** option is set to **Enabled**, the following message displays when a write is attempted to the boot sector.

Boot Sector Write!!! Possible VIRUS: Continue (Y/N)?

Select **Y** or **N** as appropriate. You may have to select **N** several times to prevent the boot sector write.

The following message displays if any attempt is made to format any cylinder, head or sector of any hard disk drive via the BIOS INT 13 Hard Disk Drive Service:

Format!!! Possible VIRUS: Continue (Y/N)?

Select **Y** or **N** as appropriate. If you select **Y** to continue, formatting proceeds normally. If you do not want to continue formatting, you may have to select **N** several times, depending on how many retries are performed by the upper-level software. For example, DOS does at least five retries before the Format utility is actually terminated.

NOTE: You should *not* enable boot sector virus protection when formatting a hard drive.

The DOS hard disk Format utility does not use INT 13H function AH=05H to format the hard disk. It only verifies the hard disk using the INT 13H Verify function (AH=04H). The virus warning message is *not* displayed during DOS hard disk drive formatting.

Saving and Exiting

When you have made all desired changes to **Standard CMOS Setup**, press **<Esc>** to return to the AMIBIOS Setup Main Menu screen.

You may make changes to other Setup options before exiting from AMIBIOS Setup. You may save the changes you have just made or you may exit from Setup without saving your changes.

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ADVANCED CMOS SETUP

When you select **Advanced CMOS Setup** from the AMIBIOS Setup Main Menu, the following Setup screen displays:

```
        AMIBIOS SETUP - ADVANCED CMOS SETUP
    (C)1998 American Megatrends, Inc. All Rights Reserved

Quick Boot                          Disabled    Available Options:
Pri Master ARMD Emulated as         Auto          Disabled
Pri Slave ARMD Emulated as          Auto          Enabled
Sec Master ARMD Emulated as         Auto
Sec Slave ARMD Emulated as          Auto
1st Boot Device                     1st IDE-HDD
2nd Boot Device                     Floppy
3rd Boot Device                     ATAPI CDROM
Try Other Boot Devices              Yes
Initialize I2O Devices              Yes
Display Mode at Add-On ROM Init     Force BIOS
Floppy Access Control               Read-Write
Hard Disk Access Control            Read-Write
S.M.A.R.T. for Hard Disks           Disabled
BootUp Num-Lock                     On
PS/2 Mouse Support                  Enabled
System Keyboard                     Present
Primary Display                     VGA/EGA
Password Check                      Setup
Parity Check                        Enabled
Boot To OS/2                        No
Internal Cache                      WriteBack
External Cache                      WriteBack
System BIOS Cacheable               Enabled
Cache Bus ECC                       Enabled
C000,16k, Shadow                    Cached
C400,16k, Shadow                    Cached
C800,16k, Shadow                    Disabled
CC00,16k, Shadow                    Disabled
D000,16k, Shadow                    Disabled
D400,16k, Shadow                    Disabled    ESC:Exit  ↓↑:Sel
D800,16k, Shadow                    Disabled    PgUp/PgDn:Modify
DC00,16k, Shadow                    Disabled    F2/F3:Color
```

The Advanced CMOS Setup Screen

When you display the Advanced CMOS Setup screen, the format is similar to the sample shown above, except the screen displays only twenty options at a time. If you need to change other options, use the down arrow key to locate the appropriate option. The available

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values for each option are displayed on the right side of the screen when you tab or arrow into the field. If values display for all parameters, the Setup parameters have been defined previously.

NOTE: The values on this screen do not necessarily reflect the values appropriate for your SBC. Refer to the explanations below for specific instructions about entering correct information.

ADVANCED CMOS SETUP OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not run the Advanced CMOS Setup program yet. Once values have been defined, they display each time Advanced CMOS Setup is run.

Quick Boot

This option allows you to have the AMIBIOS boot quickly when the computer is powered on or go through more complete testing.

When this option is set to **Disabled**, AMIBIOS tests *all* system memory. It waits up to 40 seconds for a READY signal from the IDE hard disk drive. It waits for .5 seconds after sending a RESET signal to the IDE drive to allow the drive time to get ready again. It also checks whether the user has pressed the <Del> key and runs the AMIBIOS Setup program if the key has been pressed.

If the option is set to **Enabled**, AMIBIOS checks only the first 1MB of system memory. It does not wait up to 40 seconds for a READY signal from the IDE hard disk drive. If a READY signal is not received immediately, AMIBIOS does not configure the drive. It does not wait for .5 seconds after sending a RESET signal to the IDE drive to allow the IDE drive time to get ready again.

If you have set your system up for a quick boot, you cannot run AMIBIOS Setup at system boot, because there is no delay for the "Hit DEL if you want to run SETUP" message.

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The Setup screen displays the system option:

Quick Boot	**Disabled**

Available options are:

Disabled
Enabled

Primary/Secondary Master/Slave ARMD Emulation

These options specify the type of ARMD (ATAPI Removable Media Device) emulation used for a non-disk device attached to the specified IDE device.

If the option is set to **Auto**, AMIBIOS automatically determines the proper emulation type and will support particular storage devices with ATAPI interface. The default emulation types are Floppy for LS120, Hard Disk for MO and Hard Disk for IOMEGA Zip.

The Setup screen displays the system options:

Pri Master ARMD Emulated as	**Auto**
Pri Slave ARMD Emulated as	**Auto**
Sec Master ARMD Emulated as	**Auto**
Sec Slave ARMD Emulated as	**Auto**

Available options are:

Auto
Floppy
Hard Disk

1st Boot Device

This option specifies the device type of the first boot drive from which AMIBIOS attempts to boot after AMIBIOS post routines complete.

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The Setup screen displays the system option:

1st Boot Device	**1st IDE-HDD**

Available options are:

Disabled	Floppy	SCSI
1st IDE-HDD	ARMD-FDD	NETWORK
2nd IDE-HDD	ARMD-HDD	I2O
3rd IDE-HDD	ATAPI CDROM	
4th IDE-HDD		

2nd Boot Device/ 3rd Boot Device

These options specify the device types of the second and third boot drives from which AMIBIOS attempts to boot if it cannot boot from the device specified in the **1st Boot Device** option.

The Setup screen displays the system options:

2nd Boot Device	**Floppy**
3rd Boot Device	**ATAPI CDROM**

Available options are:

Disabled	Floppy
1st IDE-HDD	ARMD-FDD
2nd IDE-HDD	ARMD-HDD
3rd IDE-HDD	ATAPI CDROM
4th IDE-HDD	

Try Other Boot Devices

If AMIBIOS cannot find a boot drive among any of the drives specified in the **1st Boot Device**, **2nd Boot Device** and **3rd Boot Device** options, this option allows you to have AMIBIOS attempt to boot from any other drive in the system. If set to **No**, AMIBIOS will try to boot only from the boot devices specified in the previous three options.

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The Setup screen displays the system option:

Try Other Boot Devices **Yes**

Available options are:

No
Yes

Initialize I2O Devices

If this option is set to **Yes**, AMIBIOS initializes any attached I2O devices (processors or storage devices).

The Setup screen displays the system option:

Initialize I2O Devices **Yes**

Available options are:

No
Yes

Display Mode At Add-On ROM Init

This option specifies the system display mode which is set at the time the AMIBIOS post routines initialize an optional option ROM.

The Setup screen displays the system option:

Display Mode at Add-On ROM Init **Force BIOS**

Two options are available:

- Select **Force BIOS** to use the display mode currently being used by AMIBIOS.
- Select **Keep Current** to use the current display mode.

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Floppy Access Control

This option specifies the read/write access which is set when booting from a floppy drive. This option is effective only if the device is accessed through the BIOS.

The Setup screen displays the system option:

Floppy Access Control **Read-Write**

Available options are:

Read-Write
Read-Only

Hard Disk Access Control

This option specifies the read/write access which is set when booting from a hard disk drive. This option is effective only if the device is accessed through the BIOS.

The Setup screen displays the system option:

Hard Disk Access Control **Read-Write**

Available options are:

Read-Write
Read-Only

S.M.A.R.T. For Hard Disks

This option allows AMIBIOS to use the SMART (System Management and Reporting Technologies) protocol for reporting server system information over a network.

The Setup screen displays the system option:

S.M.A.R.T. for Hard Disks **Disabled**

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Available options are:

Disabled
Enabled

BootUp Num-Lock

This option enables you to turn off the Num-Lock option on the enhanced keyboard when the system is powered on. If Num-Lock is turned off, the arrow keys on the numeric keypad can be used, as well as the other set of arrow keys on the enhanced keyboard.

The Setup screen displays the system option:

BootUp Num-Lock **On**

Available options are:

Off
On

PS/2 Mouse Support

This option indicates whether or not a mouse is supported. If it is set to **Enabled**, AMIBIOS supports a PS/2-type mouse.

The Setup screen displays the system option:

PS/2 Mouse Support **Enabled**

Available options are:

Disabled
Enabled

System Keyboard

This option indicates whether or not a keyboard is attached to the computer.

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The Setup screen displays the system option:

System Keyboard	**Present**

Available options are:

Absent
Present

Primary Display

This option specifies the type of display monitor in the system. The **Absent** option can be used for network file servers.

The Setup screen displays the system option:

Primary Display	**VGA/EGA**

Available options are:

Absent
VGA/EGA
CGA 40 x 25
CGA 80 x 25
Mono (monochrome)

Password Check

This option determines when a password is required for access to the system.

The Setup screen displays the system option:

Password Check	**Setup**

Two options are available:

- Select **Setup** to have the password prompt appear only when an attempt is made to enter the AMIBIOS Setup program.
- Select **Always** to have the password prompt appear each time the system is powered on.

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NOTE: To *disable* password checking, a null password should be entered in the **Change Supervisor Password** or **Change User Password** function in the AMIBIOS Setup Main Menu. (See the *Running AMIBIOS Setup* section of this manual.) The null password is the system default and is in effect if a password has not been assigned or if the CMOS has been corrupted.

Parity Check

This option allows you to enable parity checking of all system memory.

The Setup screen displays the system option:

Parity Check **Enabled**

Available options are:

Disabled
Enabled

Boot To OS/2

This option should be set to **Yes** if you are running the IBM OS/2 operating system and using more than 64MB of system memory on the SBC.

The Setup screen displays the system option:

Boot To OS/2 **No**

Available options are:

No
Yes

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Internal Cache

This option specifies the caching algorithm used for L1 internal cache memory.

The Setup screen displays the system option:

Internal Cache **WriteBack**

Three options are available:

- Select **Disabled** to disable both L1 internal cache memory on the SBC and L2 secondary cache memory.
- Select **WriteThru** to use the write-through caching algorithm.
- Select **WriteBack** to use the write-back caching algorithm.

External Cache

This option specifies the caching algorithm used for L2 cache memory. If the **Internal Cache** option described above is set to **Disabled**, this option is *not* available for modification.

The Setup screen displays the system option:

External Cache **WriteBack**

Three options are available:

- Select **Disabled** to disable L2 cache memory.
- Select **WriteThru** to use the write-through caching algorithm.
- Select **WriteBack** to use the write-back caching algorithm.

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System BIOS Cacheable

The System BIOS, which is in the F000H memory segment, is automatically shadowed to RAM for faster execution. This option indicates that this memory segment can be read from or written to cache memory.

The Setup screen displays the system option:

System BIOS Cacheable **Enabled**

Available options are:

Disabled
Enabled

Cache Bus ECC

This option enables ECC on the secondary (L2) cache bus of the CPU. Some applications may experience slight performance degradation with ECC enabled.

The Setup screen displays the system option:

Cache Bus ECC **Enabled**

Available options are:

Disabled
Enabled

Video or Adapter ROM Shadow

ROM shadow is a technique in which BIOS code is copied from slower ROM to faster RAM. The BIOS is then executed from the RAM.

Each option allows for a segment of 16KB to be shadowed from ROM to RAM. If one of these options is enabled and there is BIOS code present in that particular segment, the BIOS is shadowed.

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Video BIOS shadowing may be done in two 16KB segments at C000H and C400H. Enabling shadowing can speed up the operation of a machine because RAM can be accessed more rapidly than ROM and the data bus is wider to RAM. The default setting for the video BIOS segments is **Cached**.

Other 16KB ROM segments may be shadowed in the memory area from C800H to E000H, depending upon preferences and system requirements. The ROM area that is not used by ISA adapter cards is allocated to PCI adapter cards.

The Setup screen displays the system option:

XXXX,16K Shadow **Cached**

where XXXX is the base address of the segment of memory to be shadowed.

Three options are available:

- Select **Enabled** to write the contents of the specified ROM area to the same address in system memory (RAM) for faster execution.
- Select **Cached** to write the contents of the specified ROM area to the same address in system memory (RAM), if an adapter ROM is using the ROM area. This also indicates that the contents of the RAM area can be read from and written to cache memory.
- Select **Disabled** if you do not want to copy the specified ROM area to RAM. The contents of the video ROM cannot be read from or written to cache memory.

Saving and Exiting

When you have made all desired changes to **Advanced CMOS Setup**, press **<Esc>** to return to the AMIBIOS Setup Main Menu screen.

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You may make changes to other Setup options before exiting from AMIBIOS Setup. You may save the changes you have just made or you may exit from Setup without saving your changes.

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ADVANCED CHIPSET SETUP

When you select **Advanced Chipset Setup** from the AMIBIOS Setup Main Menu, the following Setup screen displays:

```
        AMIBIOS SETUP - ADVANCED CHIPSET SETUP
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USB Function                        Enabled     Available Options:
USB KB/Mouse Legacy Support         Auto          Disabled
Port 64/60 Emulation                Disabled      Enabled
SERR#                               Disabled
PERR#                               Disabled
USWC Write Post                     Enabled
BX Master Latency Timer (Clks)      64
Multi-Trans Timer (Clks)            32
PCI1 to PCI0 Access                 Enabled
DRAM Integrity Mode                 None
DRAM Refresh Rate                   15.6 us
Memory Hole                         Disabled
Graphics Aperture Size              64MB
AGP Mlti-Trans Timer (AGP Clks)     32
AGP Low-Priority Timer (AGP Clks)16
AGP SERR                            Enabled
AGP Parity Error Response           Enabled
8bit I/O Recovery Time              Disabled
16bit I/O Recovery Time             Disabled
PIIX4 SERR#                         Disabled
USB Passive Release                 Enabled
PIIX4 Passive Release               Enabled
PIIX4 Delayed Transaction           Enabled
TypeF DMA Buffer Control1           Disabled
TypeF DMA Buffer Control2           Disabled
DMA-0 Type                          Normal ISA
DMA-1 Type                          Normal ISA
DMA-2 Type                          Normal ISA
DMA-3 Type                          Normal ISA
DMA-5 Type                          Normal ISA    ESC:Exit  ↓↑:Sel
SMA-6 Type                          Normal ISA    PgUp/PgDn:Modify
DMA-7 Type                          Normal ISA    F2/F3:Color
```

The Advanced Chipset Setup Screen

When you display the Advanced Chipset Setup screen, the format is similar to the sample shown above, except the screen displays only twenty options at a time. If you need to change other options, use the down arrow key to locate the appropriate option. The available

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values for each option are displayed on the right side of the screen when you tab or arrow into the field. If values display for all parameters, the Setup parameters have been defined previously.

NOTE: The values on this screen do not necessarily reflect the values appropriate for your SBC. Refer to the explanations below for specific instructions about entering correct information.

ADVANCED CHIPSET SETUP OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not run the Advanced Chipset Setup program yet. Once values have been defined, they display each time Advanced Chipset Setup is run.

NOTE: Do *not* change the values for the options on this screen unless you understand the impact on system operation. Depending on your system configuration, selection of other values may cause unreliable system operation.

USB Function

This option allows you to enable the Universal Serial Bus (USB).

If this option is set to **Disabled**, the **USB KB/Mouse Legacy Support** and **Port 64/60 Emulation** options are *not* available for modification.

The Setup screen displays the system option:

USB Function **Enabled**

Available options are:

Disabled
Enabled

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USB Keyboard/Mouse Legacy Support

This option allows you to enable support for older keyboards and mouse devices.

If the **USB Function** option is set to **Disabled**, this option is *not* available for modification.

The Setup screen displays the system option:

USB KB/Mouse Legacy Support **Auto**

Available options are:

Disabled
Keyboard
Auto
Keyb+Mouse

Port 64/60 Emulation

If the **USB Function** option is set to **Disabled**, this option is *not* available for modification.

The Setup screen displays the system option:

Port 64/60 Emulation **Disabled**

Available options are:

Disabled
Enabled

SERR#

This option enables the System Error (SERR#) signal on the bus.

The Setup screen displays the system option:

SERR# **Disabled**

Available options are:

Disabled
Enabled

PERR#

This option enables the Parity Error (PERR#) signal on the bus.

The Setup screen displays the system option:

PERR# **Disabled**

Available options are:

Disabled
Enabled

USWC Write Post

This option sets the status of Uncacheable, Speculatable, Write-Combined (USWC) posted writes to I/O.

The Setup screen displays the system option:

USWC Write Post **Enabled**

Available options are:

Disabled
Enabled

BX Master Latency Timer (Clks)

This option specifies the master latency timings (in PCI clocks) for devices on the SBC.

The Setup screen displays the system option:

BX Master Latency Timer (Clks) **64**

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Available options are:

Disabled	128
32	160
64	192
96	224

Multi-Transaction Timer (Clks)

This option specifies the multi-transaction latency timings (in PCI clocks) for devices on the SBC.

The Setup screen displays the system option:

Multi-Trans Timer (Clks) **32**

Available options are:

Disabled	128
32	160
64	192
96	224

PCI1 to PCI0 Access

This option enables access between two different PCI buses (PCI1 and PCI0).

The Setup screen displays the system option:

PCI1 to PCI0 Access **Enabled**

Available options are:

Disabled
Enabled

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DRAM Integrity Mode

This option allows you to set the type of system memory checking used in your system.

The Setup screen displays the system option:

DRAM Integrity Mode **None**

Three options are available:

- **None** - No error checking or error reporting is done.
- **EC** - Multibit errors are detected and reported as parity errors. Single-bit errors are corrected by the chipset. Corrected bits of data from memory are *not* written back to DRAM system memory.
- **ECC Hardware** - Multibit errors are detected and reported as parity errors. Single-bit errors are corrected by the chipset and are written back to DRAM system memory.

  If a soft (correctable) memory error occurs, writing the fixed data back to DRAM system memory will resolve the problem. Most DRAM errors are soft errors. If a hard (uncorrectable) error occurs, writing the fixed data back to DRAM system memory does not solve the problem. In this case, the second time the error occurs in the same location, a Parity Error is reported, indicating an uncorrectable error.

DRAM Refresh Rate

This option specifies the interval between refresh signals to DRAM system memory. Settings are in microseconds ("us").

The Setup screen displays the system option:

DRAM Refresh Rate **15.6 us**

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Available options are:

15.6 us
31.2 us
64.4 us
124.8 us
249.6 us

Memory Hole

This option may be used to specify an area in memory which cannot be addressed on the ISA Bus.

The Setup screen displays the system option:

Memory Hole **Disabled**

Available options are:

Disabled
512KB-640KB
15MB-16MB

Graphics Aperture Size

This option specifies the amount of system memory which can be used by the Accelerated Graphics Port (AGP).

The Setup screen displays the system option:

Graphics Aperture Size **64MB**

Available options are:

4 MB
8 MB
16MB
32MB
64MB
128 MB
256 MB

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AGP Multi-Transaction Timer (AGP Clks)

This option sets the AGP multi-transaction timer. The settings are in units of AGP clocks.

The Setup screen displays the system option:

AGP Mlti-Trans Timer (AGP Clks) 32

Available options are:

Disabled	128
32	160
64	192
96	224

AGP Low-Priority Timer (AGP Clks)

The Setup screen displays the system option:

AGP Low-Priority Timer (AGP Clks) 16

Available options are:

Disabled	80	176
16	96	192
32	112	208
48	128	224
64	144	240

AGP SERR

This option allows you to use a System Error (SERR#) signal for the AGP Bus.

The Setup screen displays the system option:

AGP SERR Enabled

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Available options are:

Disabled
Enabled

AGP Parity Error Response

This option enables the Accelerated Graphics Port (AGP) to respond to parity errors.

The Setup screen displays the system option:

AGP Parity Error Response **Enabled**

Available options are:

Disabled
Enabled

8 Bit I/O Recovery Time

This option specifies the length of the delay inserted between consecutive 8-bit I/O operations.

The Setup screen displays the system option:

8bit I/O Recovery Time **Disabled**

Available options are:

Disabled

8 Sysclk	4 Sysclk
1 Sysclk	5 Sysclk
2 Sysclk	6 Sysclk
3 Sysclk	7 Sysclk

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16 Bit I/O Recovery Time

This option specifies the length of the delay inserted between consecutive 16-bit I/O operations.

The Setup screen displays the system option:

16bit I/O Recovery Time **Disabled**

Available options are:

Disabled
3 Sysclk
1 Sysclk
2 Sysclk
4 Sysclk

PIIX4 SERR#

This option enables the System Error (SERR#) signal for the Intel PIIX4 chip.

The Setup screen displays the system option:

PIIX4 SERR# **Disabled**

Available options are:

Disabled
Enabled

USB Passive Release

This option enables passive release for the Universal Serial Bus (USB).

The Setup screen displays the system option:

USB Passive Release **Enabled**

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Available options are:

Disabled
Enabled

PIIX4 Passive Release

This option enables passive release for the Intel PIIX4 chip.

The Setup screen displays the system option:

PIIX4 Passive Release **Enabled**

Available options are:

Disabled
Enabled

PIIX Delayed Transaction

This option enables delayed transactions for the Intel PIIX4 chip.

The Setup screen displays the system option:

PIIX4 Delayed Transaction **Enabled**

Available options are:

Disabled
Enabled

Type F DMA Buffer Control1/Type FDMA Buffer Control2

These options specify the DMA channels where Type F buffer control is implemented.

The Setup screen displays the system options:

Type F DMA Buffer Control1 **Disabled**
Type F DMA Buffer Control2 **Disabled**

Available options are:

Channel-0	Disabled
Channel-1	Channel-5
Channel-2	Channel-6
Channel-3	Channel-7

DMA-0 through DMA-7 Type

The DMA-# Type options specify the bus on which the specified DMA channel can be used.

The Setup screen displays the system option:

DMA-# Type **Normal ISA**

where # is the DMA Channel number.

Available options are:

Normal ISA
PC/PCI
Distributed

Saving and Exiting

When you have made all desired changes to **Advanced Chipset Setup**, press **<Esc>** to return to the AMIBIOS Setup Main Menu screen.

You may make changes to other Setup options before exiting from AMIBIOS Setup. You may save the changes you have just made or you may exit from Setup without saving your changes.

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POWER MANAGEMENT SETUP

When you select **Power Management Setup** from the AMIBIOS Setup Main Menu, the following Setup screen displays:

```
        AMIBIOS SETUP - POWER MANAGEMENT SETUP
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ACPI Aware O/S                  No          Available Options:
Power Management/APM            Disabled      No
Power Button Function           On/Off        Yes
Green PC Monitor Power State    Stand By
Video Power Down Mode           Disabled
Hard Disk Power Down Mode       Disabled
Hard Disk Time Out (Minute)     Disabled
Power Saving Type               POS
Standby/Suspend Timer Unit      4 Min
Standby Time Out                Disabled
Suspend Time Out                Disabled
Slow Clock Ratio                50%-62.5%
Display Activity                Ignore
Device 6 (Serial port 1)        Ignore
Device 7 (Serial port 2)        Ignore
Device 8 (Parallel port)        Ignore
Device 5 (Floppy disk)          Ignore
Device 0 (Primary master IDE)   Ignore
Device 1 (Primary slave IDE)    Ignore      ESC:Exit  ↓↑:Sel
Device 2 (Secondary master IDE) Ignore      PgUp/PgDn:Modify
Device 3 (Secondary slave IDE)  Ignore      F2/F3:Color
```

The Power Management Setup Screen

When you display the Power Management Setup screen, the format is similar to the sample shown above, except the screen displays only twenty options at a time. If you need to change other options, use the down arrow key to locate the appropriate option. The available values for each option are displayed on the right side of the screen when you tab or arrow into the field. If values display for all parameters, the Setup parameters have been defined previously.

NOTE: The values on this screen do not necessarily reflect the values appropriate for your SBC. Refer to the explanations below for specific instructions about entering correct information.

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POWER MANAGEMENT SETUP OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not run the Power Management Setup program yet. Once values have been defined, they display each time Power Management Setup is run.

ACPI Aware O/S

This option indicates or not the operating system under which you are running complies with Intel's Advanced Configuration and Power Interface (ACPI) specification.

The Setup screen displays the system option:

ACPI Aware O/S **No**

Available options are:

No
Yes

Power Management/APM

This option allows you to enable Advanced Power Management (APM) on your system. If this option is disabled, you cannot change any other options on the Power Management Setup screen, except the **ACPI Aware O/S**.

The Setup screen displays the system option:

Power Management/APM **Disabled**

Available options are:

Disabled
Enabled

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Power Button Function

This option specifies how the power button mounted externally on the computer chassis is used.

The Setup screen displays the system option:

Power Button Function **On/Off**

Two options are available:

- Select **Suspend** to use the power button to place the computer into Suspend mode or Full On power mode.
- Select **On/Off** to use the power button to turn the computer on or off.

Green PC Monitor Power State

This option specifies the power management state, if any, which the Green PC-compliant video monitor enters after a specified period of display inactivity has expired. The period of inactivity before a monitor enters **Standby** mode is specified in the **Standby Time Out** option; the period of inactivity for **Suspend** mode is specified in the **Suspend Time Out** option.

The Setup screen displays the system option:

Green PC Monitor Power State **Stand By**

Available options are:

Stand By
Suspend
Off

Video Power Down Mode

If the video subsystem remains inactive for a specified period of time, AMIBIOS conserves power by placing the subsystem into the

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power management state specified in this option. The period of inactivity before the subsystem enters **Standby** mode is specified in the **Standby Time Out** option; the period of inactivity for **Suspend** mode is specified in the **Suspend Time Out** option.

The Setup screen displays the system option:

Video Power Down Mode **Disabled**

Available options are:

Disabled
Stand By
Suspend

Hard Disk Power Down Mode

If the hard disk drive remains inactive for a specified period of time, AMIBIOS conserves power by placing the drive into the power management state specified in this option. The period of inactivity before the drive is powered down is specified in the **Hard Disk Time Out** option.

The Setup screen displays the system option:

Hard Disk Power Down Mode **Disabled**

Available options are:

Disabled
Stand By
Suspend

Hard Disk Time Out (Minute)

This option specifies the length of time the AMIBIOS waits before turning off power to the hard disk drive if the drive remains inactive. When this period expires, the hard disk drive enters the power-conserving mode specified in the **Hard Disk Power Down Mode** option described above.

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The Setup screen displays the system option:

Hard Disk Time Out (Minute) **Disabled**

Available options are:

Disabled
1 through 15, in increments of 1 minute

Power Saving Type

The Setup screen displays the system option:

Power Saving Type **POS**

Available options are:

POS (Power On Suspend)
Sleep
Stop Clock
Deep Sleep

Standby/Suspend Timer Unit

This option specifies the unit of time used for the Standby and Suspend timeout periods.

The Setup screen displays the system option:

Standby/Suspend Timer Unit **4 Min**

Available options are:

32 secs
4 msec
4 min
4 sec

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Standby Time Out

This option specifies the length of the period of system inactivity when the computer is in full power-on mode before the computer is placed in Standby mode. In Standby mode, some power use is curtailed.

The default for this option depends on the value selected in the **Standby/Suspend Timer Unit** option.

The Setup screen displays the system option:

Standby Time Out **Disabled**

Available options are:

Disabled
32 through 4064, in increments of 32 (if the **Standby/Suspend Timer Unit** option is set to **32 secs**)
4 through 508, in increments of 4 (if the **Standby/Suspend Timer Unit** option is set to **4 msec**, **4 min** or **4 sec**)

Suspend Time Out

This option specifies the length of the period of system inactivity when the computer is already in Standby mode before the computer is placed in Suspend mode. In Suspend mode, nearly all power use is curtailed.

The default for this option depends on the value selected in the **Standby/Suspend Timer Unit** option.

The Setup screen displays the system option:

Suspend Time Out **Disabled**

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Available options are:

Disabled
32 through 4064, in increments of 32 (if the **Standby/Suspend Timer Unit** option is set to **32 secs**)
4 through 508, in increments of 4 (if the **Standby/Suspend Timer Unit** option is set to **4 msec**, **4 min** or **4 sec**)

Slow Clock Ratio

This option specifies the speed at which the system clock runs when the system is in Standby power saving mode. The settings are expressed as a percentage between the normal CPU clock speed and the CPU clock speed when the system is in the power-conserving state.

The Setup screen displays the system option:

Slow Clock Ratio **50%-62.5%**

Available options are:

0-12.5%
12.5%-25%
25%-37.5%
37.5%-50%
50%-62.5%
62.5%-75%
75%-87.5%

Display Activity

This option enables event monitoring on the video display. If the option is set to **Monitor** and the computer is in a power-saving mode, AMIBIOS watches for display activity. If any activity occurs, the computer enters the full power-on mode and AMIBIOS restarts the Standby and Suspend timeout timers.

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The Setup screen displays the system option:

Display Activity	**Ignore**

Available options are:

Ignore
Monitor

Device 0 through Device 8 Monitoring

These options allow you to enable event monitoring for your peripherals and hard disk drives. If an option is set to **Monitor** and the computer is in a power-saving mode, AMIBIOS watches for activity on the hardware interrupt request line (IRQ) for the specified device. If any activity occurs, the computer enters full power-on mode. AMIBIOS then restarts the Standby and Suspend timeout timers.

The Setup screen displays the system options:

Device 6 (Serial port 1)	**Ignore**
Device 7 (Serial port 2)	**Ignore**
Device 8 (Parallel port)	**Ignore**
Device 5 (Floppy disk)	**Ignore**
Device 0 (Primary master IDE)	**Ignore**
Device 1 (Primary slave IDE)	**Ignore**
Device 2 (Secondary master IDE)	**Ignore**
Device 3 (Secondary slave IDE)	**Ignore**

Available options are:

Ignore
Monitor

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Saving and Exiting

When you have made all desired changes to **Power Management Setup**, press **<Esc>** to return to the AMIBIOS Setup Main Menu screen.

You may make changes to other Setup options before exiting from AMIBIOS Setup. You may save the changes you have just made or you may exit from Setup without saving your changes.

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PCI/PLUG AND PLAY SETUP

When you select **PCI/Plug and Play Setup** from the AMIBIOS Setup Main Menu, the following Setup screen displays:

```
          AMIBIOS SETUP - PCI / PLUG AND PLAY SETUP
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On Board LAN                        Enabled     Available Options:
On Board Video                      Enabled       Disabled
On Board SCSI                       Enabled       Enabled
Plug and Play Aware O/S             No
PCI Latency Timer (PCI Clocks)      64
PCI VGA Palette Snoop               Disabled
PCI IDE BusMaster                   Disabled
OffBoard PCI IDE Card               Auto
OffBoard PCI IDE Primary IRQ        Disabled
OffBoard PCI IDE Secondary IRQ      Disabled
DMA Channel 0                       PnP
DMA Channel 1                       PnP
DMA Channel 3                       PnP
DMA Channel 5                       PnP
DMA Channel 6                       PnP
DMA Channel 7                       PnP
IRQ5                                PCI/PnP
IRQ9                                PCI/PnP
IRQ10                               PCI/PnP
IRQ11                               PCI/PnP
IRQ15                               PCI/PnP     ESC:Exit  ↓↑:Sel
Reserved Memory Size                Disabled    PgUp/PgDn:Modify
Reserved Memory Address             C8000       F2/F3:Color
```

The PCI / Plug and Play Setup Screen

When you display the PCI / Plug and Play Setup screen, the format is similar to the sample shown above, except the screen displays only twenty options at a time. If you need to change other options, use the down arrow key to locate the appropriate option. The available values for each option are displayed on the right side of the screen when you tab or arrow into the field. If values display for all parameters, the Setup parameters have been defined previously.

NOTE: The values on this screen do not necessarily reflect the values appropriate for your SBC. Refer to the explanations below for specific instructions about entering correct information.

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PCI/PLUG AND PLAY SETUP OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not run the PCI/Plug and Play Setup program yet. Once values have been defined, they display each time PCI/Plug and Play Setup is run.

On Board LAN

The Setup screen displays the system option:

On Board LAN	**Enabled**

Available options are:

Disabled
Enabled

On Board Video

The Setup screen displays the system option:

On Board Video	**Enabled**

Available options are:

Disabled
Enabled

On Board SCSI

The Setup screen displays the system option:

On Board SCSI	**Enabled**

Available options are:

Disabled
Enabled

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Plug and Play Aware O/S

This option indicates whether the operating system installed in the computer is Plug and Play-aware. AMIBIOS only detects and enables PnP ISA adapter cards which are required for system boot. The Windows 95 operating system is PnP-aware and detects and enables all other PnP-aware adapter cards. Set this option to **No** if the operating system (such as DOS, OS/2, Windows 3.x) does *not* use PnP.

NOTE: You *must* set this option correctly or PnP-aware adapter cards installed in your computer will not be configured properly.

The Setup screen displays the system option:

Plug and Play Aware O/S **No**

Available options are:

No
Yes

PCI Latency Timer (PCI Clocks)

This option specifies the latency of all PCI devices on the PCI Local Bus. The settings are in units equal to PCI clocks.

The Setup screen displays the system option:

PCI Latency Timer (PCI Clocks) **64**

Available options are:

32	160
64	192
96	224
128	248

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PCI VGA Palette Snoop

Palette snooping allows multiple VGA devices operating on different buses to handle data from the CPU on each set of palette registers on every video device, e.g. if there are two VGA devices in your system (one PCI and one ISA). Bit 5 of the command register in the PCI device configuration space is the VGA Palette Snoop bit (0 is disabled).

This option *must* be set to **Enabled** if any ISA adapter card installed in the system requires VGA palette snooping.

The Setup screen displays the system option:

PCI VGA Palette Snoop **Disabled**

Two options are available:

- **Disabled** - Data read and written by the CPU is only directed to the PCI VGA device's palette registers.
- **Enabled** - Data read and written by the CPU is directed to both the PCI VGA device's palette registers and the ISA VGA device's palette registers, permitting the palette registers of both devices to be identical.

PCI IDE BusMaster

This option specifies whether the IDE controller on the PCI Local Bus has bus mastering capability. AMIBIOS can perform bus master transfers using scatter/gather DMA on the PCI IDE interface. No special drivers are needed, but the IDE drive must support PCI bus mastering.

The Setup screen displays the system option:

PCI IDE BusMaster **Disabled**

Available options are:

Disabled
Enabled

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OffBoard PCI IDE Card

This option specifies the PCI expansion slot on the SBC where the off-board PCI IDE controller is installed, if any. If an off-board PCI IDE controller is used, the on-board IDE controller on the SBC is automatically disabled.

If **Auto** is selected, AMIBIOS automatically determines the correct setting for this option.

This option forces IRQ14 and IRQ15 to PCI slots on the PCI Local Bus. This is necessary to support non-compliant PCI IDE adapter cards.

If this option is set to **Auto**, the **OffBoard PCI IDE Primary IRQ** and **OffBoard PCI IDE Secondary IRQ** options may *not* be modified.

The Setup screen displays the system option:

OffBoard PCI IDE Card **Auto**

Available options are:

Auto
Slot1
Slot2
Slot3
Slot4
Slot5
Slot6

OffBoard PCI IDE Primary IRQ/Secondary IRQ

These options specify the PCI interrupts used by the primary and secondary IDE channels on the off-board PCI IDE controller.

If the **OffBoard PCI IDE Card** option described above is set to **Auto**, these options are *not* available.

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The Setup screen displays the system options:

OffBoard PCI IDE Primary IRQ	**Disabled**
OffBoard PCI IDE Secondary IRQ	**Disabled**

Available options are:

Disabled
INTA
INTB
INTC
INTD
Hardwired

DMA Channels 0, 1, 3, 5, 6 and 7

These options allow you to specify the bus type used by each DMA channel.

The Setup screen displays the system option:

DMA Channel #	**PnP**

where # is the DMA Channel number.

Available options are:

PnP
ISA/EISA

IRQ5/IRQ9/IRQ10/IRQ11/IRQ15

These options indicate whether or not the specified interrupt request (IRQ) is available for use by the system for PCI/Plug and Play features or is reserved for use by option cards on the ISA Bus. This allows you to specify IRQs for use by legacy ISA adapter cards.

The IRQ setup options indicate whether AMIBIOS should remove an IRQ from the pool of available IRQs passed to BIOS configurable devices. The available IRQ pool is determined by reading the ESCD

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NVRAM. If more IRQs must be removed from the pool, you can set the IRQ option to **ISA/EISA**. On-board I/O is configurable by AMIBIOS; the IRQs used by on-board I/O are configured as **PCI/PnP**.

The Setup screen displays the system option:

IRQ# **PCI/PnP**

where # is the number of the interrupt request (IRQ) available to the option specified (PCI or ISA).

Available options:

PCI/PnP
ISA/EISA

NOTE: If the **OnBoard IDE** option on the **Peripheral Setup** screen is set to **Secondary** or **Both**, IRQ15 is assigned by the system and is not available to the user.

Reserved Memory Size

This option specifies the size of the memory area reserved for legacy ISA adapter cards.

If this option is set to **Disabled**, the **Reserved Memory Address** option is *not* available for modification.

The Setup screen displays the system option:

Reserved Memory Size **Disabled**

Available options are:

Disabled
16K
32K
64K

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Reserved Memory Address

This option specifies the beginning address (in hexadecimal) of the ROM memory area reserved for use by legacy ISA adapter cards.

If the **Reserved Memory Size** option is set to **Disabled**, this option is *not* available for modification.

The Setup screen displays the system option:

Reserved Memory Address **C8000**

Available options are:

C0000	D0000
C4000	D4000
C8000	D8000
CC000	DC000

Saving and Exiting

When you have made all desired changes to **PCI/Plug and Play Setup**, press **<Esc>** to return to the AMIBIOS Setup Main Menu screen.

You may make changes to other Setup options before exiting from AMIBIOS Setup. You may save the changes you have just made or you may exit from Setup without saving your changes.

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PERIPHERAL SETUP

When you select the **Peripheral Setup** from the AMIBIOS Setup Main Menu, the following Setup screen displays:

```
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OnBoard FDC                     Auto        Available Options:
OnBoard Serial Port1            Auto          Auto
OnBoard Serial Port2            Auto          Disabled
    Receiver Polarity           Non-Inverted  Enabled
    Transmitter Polarity        Non-Inverted
OnBoard Parallel Port           Auto
  Parallel Port Mode            ECP
  EPP Version                   N/A
  Parallel Port IRQ             Auto
  Parallel Port DMA Channel     Auto
OnBoard IDE                     Both

                                            ESC:Exit  ↓↑:Sel
                                            PgUp/PgDn:Modify
                                            F2/F3:Color
```

The Peripheral Setup Screen

When you display the Peripheral Setup screen, the format is similar to the sample shown above. The available values for each option are displayed on the right side of the screen when you tab or arrow into the field. If values display for all parameters, the Setup parameters have been defined previously.

NOTE: The values on this screen do not necessarily reflect the values appropriate for your SBC. Refer to the explanations below for specific instructions about entering correct information.

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PERIPHERAL SETUP OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not run the Peripheral Setup program yet. Once values have been defined, they display each time Peripheral Setup is run.

The AMIBIOS allows automatic or manual setup of peripheral devices. The floppy drive controller, serial port, parallel port and IDE controller options on the **Peripheral Management** screen can each be set to **Auto**, which causes AMIBIOS to configure the peripherals automatically as described under each heading below.

When you set these options to values other than **Auto**, the values you set up manually are used by AMIBIOS when booting the system. AMIBIOS reports any I/O conflicts after displaying the BIOS Configuration Summary screen.

OnBoard FDC

The on-board floppy drive controller may be enabled or disabled using this option.

When this option is set to **Auto**, AMIBIOS attempts to enable any floppy drive controller on the ISA Bus. If no floppy controller is found on the ISA Bus, the on-board floppy controller is enabled.

The Setup screen displays the system option:

OnBoard FDC **Auto**

Available options are:

Auto
Disabled
Enabled

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OnBoard Serial Port 1/OnBoard Serial Port 2

Each of these options enables the specified serial port on the SBC and establishes the base I/O address for the port.

The Setup screen displays the system options:

OnBoard Serial Port1	**Auto**
OnBoard Serial Port2	**Auto**

Available options are:

Auto
Disabled
3F8H
2F8H
3E8H
2E8H

When this option is set to **Auto**, AMIBIOS also attempts to avoid address conflicts. If the off-board serial ports are configured to specific starting I/O ports via jumper settings, AMIBIOS configures the on-board serial ports to avoid conflicts.

AMIBIOS checks the ISA Bus for serial ports. Any off-board serial ports found on the ISA Bus are left at their assigned addresses. Serial Port 1, the first on-board serial port, is configured with the first available address and Serial Port 2, the second on-board serial port, is configured with the next available address. The default address assignment order is 3F8H, 2F8H, 3E8H, 2E8H. Note that this same assignment order is used by AMIBIOS to place the active serial port addresses in lower memory (BIOS data area) for configuration as logical COM devices.

After all addresses have been assigned, any remaining on-board serial ports are disabled.

For example, if there is one off-board serial port on the ISA Bus and its address is set to 2F8H, Serial Port 1 is assigned address 3F8H and Serial Port 2 is assigned address 3E8H. Configuration is then as follows:

COM1 - Serial Port 1 (at 3F8H)
COM2 - off-board serial port (at 2F8H)
COM3 - Serial Port 2 (at 3E8H)

If the **OnBoard Serial Port2** option is set to **Disabled**, the **Receiver Polarity** and **Transmitter Polarity** options are *not* available for modification.

Receiver Polarity

If the **OnBoard Serial Port2** option is set to **Disabled**, this option is *not* available for modification.

The Setup screen displays the system option:

Receiver Polarity **Non-Inverted**

Available options are:

Non-Inverted
Inverted

Transmitter Polarity

If the **OnBoard Serial Port2** option is set to **Disabled**, this option is *not* available for modification.

The Setup screen displays the system option:

Transmitter Polarity **Non-Inverted**

Available options are:

Non-Inverted
Inverted

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OnBoard Parallel Port

This option enables the parallel port on the SBC and establishes the base I/O address for the port.

The Setup screen displays the system option:

OnBoard Parallel Port **Auto**

Available options are:

Auto
Disabled
378
278
3BC

When this option is set to **Auto**, AMIBIOS checks the ISA Bus for off-board parallel ports. Any parallel ports found on the ISA Bus are left at their assigned addresses. The on-board Parallel Port is automatically configured with the first available address not used by an off-board parallel port. The default address assignment order is 3BCH, 378H, 278H. Note that this same assignment order is used by AMIBIOS to place the active parallel port addresses in lower memory (BIOS data area) for configuration as logical LPT devices.

Parallel Port Mode

This option specifies the parallel port mode. ECP and EPP are both bidirectional data transfer schemes which adhere to the IEEE P1284 specifications.

The Setup screen displays the system option:

Parallel Port Mode **ECP**

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Three options are available:

- **Normal** uses normal parallel port mode.
- **EPP** allows the parallel port to be used with devices which adhere to the Enhanced Parallel Port (EPP) specification. EPP uses the existing parallel port signals to provide asymmetric bidirectional data transfer driven by the host device.
- **ECP** allows the parallel port to be used with devices which adhere to the Extended Capabilities Port (ECP) specification. ECP uses the DMA protocol to achieve transfer rates of approximately 2.5MB/second. ECP provides symmetric bidirectional communication.

EPP Version

This option specifies the Enhanced Parallel Port (EPP) specification number which is used in the system. It is available only if the **Parallel Port Mode** option is set to **EPP**.

The Setup screen displays the system option:

EPP Version **N/A**

Available options are:

N/A
1.7
1.9

Parallel Port IRQ

This option specifies the interrupt request (IRQ) which is used by the parallel port.

The Setup screen displays the system option:

Parallel Port IRQ **Auto**

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Available options are:

Auto
5
7

Parallel Port DMA Channel

This option sets the DMA channel used by the parallel port. It is only available if the **Parallel Port Mode** option is set to **ECP**.

The Setup screen displays the system option:

Parallel Port Channel **Auto**

Available options are:

Auto
0
1
3

OnBoard IDE

This option specifies the on-board integrated drive electronics (IDE) controller channel(s) to be used.

The Setup screen displays the system option:

OnBoard IDE **Both**

Available options are:

Both
Disabled
Primary
Secondary

NOTE: If this option is set to **Secondary** or **Both**, the system assigns interrupt request 15 (IRQ15).

Saving and Exiting

When you have made all desired changes to **Peripheral Setup**, press **<Esc>** to return to the AMIBIOS Setup Main Menu screen.

You may make changes to other Setup options before exiting from AMIBIOS Setup. You may save the changes you have just made or you may exit from Setup without saving your changes.

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APPENDIX A - BIOS MESSAGES

BIOS BEEP CODES

Errors may occur during the POST (Power-On Self Test) routines which are performed each time the system is powered on.

Non-fatal errors are those which, in most cases, allow the system to continue the bootup process. The error message normally appears on the screen. See *BIOS Error Messages* later in this section for descriptions of these messages.

Fatal errors are those which will not allow the system to continue the bootup procedure.

These fatal errors are usually communicated through a series of audible beeps. Each error message has its own specific beep code, defined by the number of beeps following the error detection. The following table lists the errors which are communicated audibly.

All errors listed, *with the exception of #8*, are fatal errors.

Beep Count	Message	Description
1	Refresh Failure	The memory refresh circuitry of the processor board is faulty.
2	Parity Error	A parity error was detected in the base memory (the first block of 64KB) of the system.
3	Base 64KB Memory Failure	A memory failure occurred within the first 64KB of memory.
4	Timer Not Operational	A memory failure occurred within the first 64KB of memory, or Timer #1 on the processor board has failed to function properly.
5	Processor Error	The CPU (Central Processing Unit) on the processor board has generated an error.
6	8042 - Gate A20 Failure	The keyboard controller (8042) contains the Gate A20 switch which allows the CPU to operate in protected mode. This error message means that the BIOS is not able to switch the CPU into protected mode.
7	Processor Exception Interrupt Error	The CPU on the processor board has generated an exception interrupt.

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BIOS BEEP CODES (continued)

Beep Count	Message	Description
8	Display Memory Read/Write Error	The system video adaptor is either missing or its memory is faulty. **NOTE:** This is *not* a fatal error.
9	ROM Checksum Error	The ROM checksum value does not match the value encoded in the BIOS.
10	CMOS Shutdown Register Read/Write Error	The shutdown register for the CMOS RAM has failed.
11	Cache Memory Bad; Do Not Enable Cache	The cache memory test failed. Cache memory is disabled. *Do not press <Ctrl><Alt><Shift><+> to enable cache memory.*

BIOS ERROR MESSAGES

If a non-fatal error occurs during the POST routines performed each time the system is powered on, the error message will appear on the screen in the following format:

ERROR Message Line 1
ERROR Message Line 2
Press F1 to Resume

Note the error message and press the **<F1>** key to continue with the bootup procedure.

NOTE: If the "Wait for 'F1' If Any Error" option in the Advanced Setup portion of the BIOS Setup Program has been set to **Disabled**, the "Press F1 to Resume" prompt will not appear on the third line.

For most of the error messages, there is no ERROR Message Line 2. Generally, for those messages containing an ERROR Message Line 2, the text will be "RUN SETUP UTILITY." Pressing the **<F1>** key will invoke the BIOS Setup Utility.

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BIOS ERROR MESSAGES (continued)

A description of each error message appears below. The errors are listed in alphabetical order, not in the order in which they may occur.

Message	Description
8042 Gate-A20 Error	The gate-A20 portion of the keyboard controller (8042) has failed to operate correctly. Replace the 8042 chip.
Address Line Short!	An error has occurred in the address decoding circuitry of the processor board.
C: Drive Error	The BIOS is not receiving any response from hard disk drive C:. Check Standard Setup using the BIOS Setup Utility to see if the correct hard disk drive has been selected.
C: Drive Failure	The BIOS cannot get *any* response from hard disk drive C:. It may be necessary to replace the hard disk.
Cache Memory Bad, Do Not Enable Cache!	Cache memory is defective.
CH-2 Timer Error	Most AT standard system boards include two timers. An error with Timer #1 is a fatal error, explained in *BIOS Beep Codes* earlier in this section. If an error occurs with Timer #2, this error message appears.
CMOS Battery State Low	There is a battery in the system which is used for storing the CMOS values. This battery appears to be low in power and needs to be replaced.
CMOS Checksum Failure	After the CMOS values are saved, a checksum value is generated to provide for error checking. If the previous value is different from the value currently read, this error message appears. To correct the error, run the BIOS Setup Utility.
CMOS Display Type Mismatch	The type of video stored in CMOS does not match the type detected by the BIOS. Run the BIOS Setup Utility to correct the error.
CMOS Memory Size Mismatch	If the BIOS finds the amount of memory on the system board to be different from the amount stored in CMOS, this error message is generated. Run the BIOS Setup Utility to correct the error.
CMOS System Options Not Set	The values stored in the CMOS are either corrupt or nonexistent. Run the BIOS Setup Utility to correct the error.

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BIOS ERROR MESSAGES (continued)

Message	Description
CMOS Time & Date Not Set	Use Standard Setup in the BIOS Setup Utility to set the date and time of the CMOS.
D: Drive Error	The BIOS is not receiving any response from hard disk drive D:. Check Standard Setup using the BIOS Setup Utility to see if the correct hard disk drive has been selected.
D: Drive Failure	The BIOS cannot get *any* response from hard disk drive D:. It may be necessary to replace the hard disk.
Diskette Boot Failure	The disk used to boot up in floppy drive A: is corrupt, which means it cannot be used to boot up the system. Use another boot disk and follow the instructions on the screen.
Display Switch Not Proper	Some systems require that a video switch on the processor be set to either color or monochrome, depending upon the type of video being used. To correct this situation, set the switch properly after the system is powered off.
DMA Error	An error has occurred in the DMA controller on the processor board.
DMA #1 Error	An error has occurred in the first DMA channel on the processor board.
DMA #2 Error	An error has occurred in the second DMA channel on the processor board.
FDD Controller Failure	The BIOS is not able to communicate with the floppy disk drive controller. Check all appropriate connections after the system is powered off.
HDD Controller Failure	The BIOS is not able to communicate with the hard disk drive controller. Check all appropriate connections after the system is powered off.
INTR #1 Error	Interrupt channel #1 has failed the POST routine.
INTR #2 Error	Interrupt channel #2 has failed the POST routine.
Invalid Boot Diskette	The BIOS can read the disk in floppy drive A:, but it *cannot* boot up the system with it. Use another boot disk and follow the instructions on the screen.
KB/Interface Error	The BIOS has found an error with the keyboard connector on the processor board.

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BIOS ERROR MESSAGES (continued)

Message	Description
Keyboard Error	The BIOS has encountered a timing problem with the keyboard. The Keyboard option in the Standard Setup portion of the BIOS Setup Utility may be set to **Not Installed**, which will cause the BIOS to skip the keyboard POST routines.
Keyboard Is Locked... Unlock It	The keyboard lock on the system is engaged. It must be unlocked to continue the bootup procedure.
No ROM BASIC	This error occurs when a proper bootable sector cannot be found on either floppy disk drive A: or hard disk drive C:. The BIOS will try at this point to run ROM Basic, and the error message is generated when the BIOS does not find it.
Off Board Parity Error	The BIOS has encountered a parity error in memory installed on an adapter card in an I/O (Bus) expansion slot. The message appears as follows: OFF BOARD PARITY ERROR ADDR (HEX) = (XXXX) where XXXX is the address (in hexadecimal) at which the error has occurred. "Off Board" means that it is part of the memory installed via an expansion card in an I/O (Bus) slot, as opposed to memory attached directly to the processor board.
On Board Parity Error	The BIOS has encountered a parity error in memory installed on the processor board. The message appears as follows: ON BOARD PARITY ERROR ADDR (HEX) = (XXXX) where XXXX is the address (in hexadecimal) at which the error has occurred. "On Board" means that it is part of the memory attached directly to the processor board, as opposed to memory installed via an expansion card in an I/O (Bus) slot.
Parity Error ????	The BIOS has encountered a parity error with some memory in the system, but it is not able to determine the address of the error.

ISA BIOS NMI HANDLER MESSAGES

The ISA NMI (non-maskable interrupt) messages are described below.

Message	Description
Memory Parity Error	Memory failed. The message appears as follows: MEMORY PARITY ERROR AT XXXXX where XXXXX is the address (in hexadecimal) at which the error has occurred. If the memory location cannot be determined, the message is "Memory Parity Error ????"
I/O Card Parity Error	An expansion card failed. The message appears as follows: I/O PARITY ERROR AT XXXXX where XXXXX is the address (in hexadecimal) at which the error has occurred. If the address cannot be determined, the message is "I/O Card Parity Error ????"
DMA Bus Time-Out	A device has driven the bus signal for more than 7.8 microseconds.

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PORT 80 CODES

The following codes are presented on Port 80H as the BIOS performs its reset procedure.

Code	Description
Uncompressed Initialization Code Checkpoints:	
D0	NMI is disabled. Power-on delay starting. Initialization code checksum to be verified next.
D1	Initializing DMA controller, performing keyboard controller BAT test, starting memory refresh and entering 4GB flat mode next.
D3	Starting memory sizing next.
D4	Returning to real mode. Executing any OEM patches and setting stack next.
D5	Passing control to uncompressed code in shadow RAM at E000:0000H. Initialization code copied to segment 0 and control to be transferred to segment 0.
D6	Control in segment 0. Checking if <Ctrl>+<Home> was pressed and verifying system BIOS checksum. If <Ctrl>+<Home> was pressed or system BIOS checksum is bad, going to checkpoint code E0H next. Otherwise, going to checkpoint code D7H.
D7	Main BIOS runtime code to be decompressed and control to be passed to main BIOS in shadow RAM.
Boot Block Recovery Code Checkpoints:	
E0	Onboard floppy controller initialized, if any. Beginning base 512KB memory test next.
E1	Initializing interrupt vector table next.
E2	Initializing DMA and interrupt controllers next.
E6	Enabling floppy drive controller and timer IRQ's. Enabling internal cache memory.
ED	Initializing floppy drive.
EE	Looking for floppy diskette in drive A:. Reading first sector of diskette.
EF	Read error occurred while reading floppy drive in drive A:.
F0	Searching for AMIBOOT.ROM file in root directory.

PORT 80 CODES (continued)

Code	Description
F1	AMIBOOT.ROM file not in root directory.
F2	Reading and analyzing floppy diskette FAT to find clusters occupied by AMIBOOT.ROM file.
F3	Reading AMIBOOT.ROM file next, cluster by cluster.
F4	AMIBOOT.ROM file not correct size.
F5	Disabling internal cache memory next.
FB	Detecting type of flash ROM next.
FC	Erasing flash ROM next.
FD	Programming flash ROM next.
FF	Flash ROM programming successful. Restarting system BIOS next.
Runtime code is uncompressed in F000 shadow RAM.	
03	NMI is disabled. Checking for soft reset/power-on next.
05	BIOS stack has been built. Disabling cache memory next.
06	Uncompressing POST code next.
07	Initializing CPU and CPU data area next.
08	CMOS checksum calculation to be done next.
0A	CMOS checksum calculation done. Initializing CMOS status register for date and time next.
0B	CMOS status register initialized. Next, performing any required initialization before keyboard BAT command issued.
0C	Keyboard controller input buffer free. Issuing BAT command to keyboard controller next.
0E	Keyboard controller BAT command result verified. Performing any necessary initialization after keyboard controller BAT test next.
0F	Initialization after keyboard controller BAT command test done. Keyboard command byte to be written next.
10	Keyboard controller command byte is written. Issuing Pin 23,24 blocking/unblocking command next.

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PORT 80 CODES (continued)

Code	Description
11	Checking if <End> or <Ins> keys were pressed during power-on next. Initializing CMOS RAM if the "Initialize CMOS RAM in every boot" AMIBIOS POST option was set in AMIBCP or the <End> key was pressed.
12	Disabling DMA controllers 1 and 2 and interrupt controllers 1 and 2 next.
13	Video display disabled and port B initialized. Initializing chipset next.
14	8254 timer test to begin next.
19	8254 timer test over. Starting memory refresh test next.
1A	Memory refresh line is toggling. Checking 15 microsecond on/off time next.
23	Reading 8042 input port and disabling MEGAKEY Green PC feature next. Making BIOS code segment writable and performing any necessary configuration before initializing the interrupt vectors.
24	Configuration required before interrupt vector initialization complete. Interrupt vector initialization about to begin.
25	Interrupt vector initialization done. Clearing password if POST diagnostic switch is on.
27	Any initialization before setting video mode to be done next.
28	Initialization before setting video mode is complete. Configuring monochrome mode and color mode settings next.
2A	Bus initialization (system, static, output devices) to be done next, if present. (See end of Port 80H Codes for details of different buses.)
2B	Passing control to video ROM to perform any required configuration before video ROM test.
2C	All necessary processing before passing control to video ROM is done. Looking for video ROM next and passing control to it.
2D	Video ROM has returned control to BIOS POST. Performing any required processing after video ROM had control.
2E	Completed post-video ROM test processing. If EGA/VGA controller not found, performing display memory read/write test next.
2F	EGA/VGA controller not found. Display memory read/write test about to begin.

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PORT 80 CODES (continued)

Code	Description
30	Display memory read/write test passed. Looking for retrace checking next.
31	Display memory read/write test or retrace checking failed. Performing alternate display memory read/write test next.
32	Alternate display memory read/write test passed. Looking for alternate display retrace checking next.
34	Video display checking over. Setting display mode next.
37	Display mode set. Displaying power-on message next.
38	Initializing bus (input, IPL, general devices) next, if present. (See end of Port 80H Codes for details of different buses.)
39	Displaying bus initialization error messages. (See end of Port 80H Codes for details of different buses.)
3A	New cursor position read and saved. Displaying "Hit <DEL>" message next.
3B	"Hit <DEL>" message displayed. Protected mode memory test about to start.
40	Preparing descriptor tables next.
42	Descriptor tables prepared. Entering protected mode for memory test next.
43	Entered protected mode. Enabling interrupts for diagnostics mode next.
44	Interrupts enabled (if diagnostics switch is on). Initializing data to check memory wraparound at 0:0 next.
45	Data initialized. Checking for memory wraparound at 0:0 and finding total system memory size next.
46	Memory wraparound test done. Memory size calculation done. Writing patterns to test memory next.
47	Memory pattern written to extended memory. Writing patterns to base 640KB memory next.
48	Patterns written in base memory. Determining amount of memory below 1MB memory next.
49	Amount of memory below 1MB found and verified. Determining amount of memory above 1MB memory next.

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PORT 80 CODES (continued)

Code	Description
4B	Amount of memory above 1MB found and verified. Checking for soft reset and clearing memory below 1MB for soft reset next. (If power-on situation, going to checkpoint 4EH next.)
4C	Memory below 1MB has been cleared via soft reset. Clearing memory above 1MB next.
4D	Memory above 1MB has been cleared via soft reset. Saving memory size next. (Going to checkpoint 52H next.)
4E	Memory test started, but not as result of soft reset. Displaying first 64KB memory size next.
4F	Memory size display started. Display is updated during memory test. Performing sequential and random memory tests next.
50	Memory below 1MB has been tested and initialized. Adjusting displayed memory size for relocation and shadowing next.
51	Memory size display adjusted for relocation and shadowing. Testing memory above 1MB next.
52	Memory above 1MB has been tested and initialized. Saving memory size information next.
53	Memory size information and CPU registers are saved. Entering real mode next.
54	Shutdown was successful. CPU in real mode. Disabling Gate A20 line, parity and NMI next.
57	A20 address line, parity and NMI are disabled. Adjusting memory size depending on relocation and shadowing next.
58	Memory size adjusted for relocation and shadowing. Clearing "Hit <DEL>" message next.
59	"Hit <DEL>" message cleared. "Wait..." message displayed. Starting DMA and interrupt controller tests next.
60	DMA page register test passed. Performing DMA controller 1 base register test next.
62	DMA controller 1 base register test passed. Performing DMA controller 2 base register test next.
65	DMA controller_2 base register test passed. Programming DMA controllers 1 and 2 next.

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PORT 80 CODES (continued)

Code	Description
66	Completed programming DMA controllers 1 and 2. Initializing 8259 interrupt controller next.
67	Completed 8259 interrupt controller initialization.
7F	Extended NMI sources enabling in progress.
80	Keyboard test started. Clearing output buffer, checking for stuck keys. Issuing keyboard reset command next.
81	Keyboard reset error or stuck key found. Issuing keyboard controller interface test command next.
82	Keyboard controller interface test completed. Writing command byte and initializing circular buffer next.
83	Command byte written, global data initialization completed. Checking for locked key next.
84	Locked key checking over. Checking for memory size mismatch with CMOS RAM data next.
85	Memory size check done. Displaying soft error and checking for password or bypassing Setup next.
86	Password checked. Performing any required programming before Setup next.
87	Programming before Setup complete. Uncompressing Setup code and executing Setup utility next.
88	Returned from Setup program and screen is cleared. Performing any necessary programming after Setup next.
89	Programming after Setup complete. Displaying power-on screen message next.
8B	First screen message displayed. "Wait..." message displayed. Performing PS/2 mouse check and extended BIOS data area allocation check next.
8C	Programming Setup options next.
8D	Setup options are programmed. Resetting hard disk controller next.
8F	Hard disk controller reset done. Configuring floppy drive controller next.
91	Floppy drive controller configured. Configuring hard disk drive controller next.

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PORT 80 CODES (continued)

Code	Description
95	Initializing bus option ROM's from C800 next. (See end of Port 80H Codes for details of different buses.)
96	Initializing before passing control to adapter ROM at C800.
97	Initialization before C800 adapter ROM gains control completed. Adapter ROM check next.
98	Adapter ROM had control and has returned control to BIOS POST. Performing any required processing after option ROM returned control.
99	Any initialization required after option ROM test has completed. Configuring timer data area and printer base address next.
9A	Set timer and printer base addresses. Setting RS-232 base address next.
9B	Returned after setting RS-232 base address. Performing any required initialization before coprocessor test next.
9C	Required initialization before coprocessor test is over. Initializing coprocessor next.
9D	Coprocessor initialized. Performing any required initialization after coprocessor test next.
9E	Initialization after coprocessor test is complete. Checking extended key board, keyboard ID and Num Lock key next. Issuing keyboard ID command next.
A2	Displaying any soft errors next.
A3	Soft error display complete. Setting keyboard typematic rate next.
A4	Keyboard typematic rate set. Programming memory wait states next.
A5	Memory wait state programming over. Clearing screen and enabling parity and NMI next.
A7	NMI and parity enabled. Performing any initialization required before passing control to adapter ROM at E000H next.
A8	Initialization before passing control to adapter ROM at E000H completed. Passing control to adapter ROM at E000H next.
A9	Returned from E000 ROM control. Going to do any initialization required after E000 option ROM control.
AA	Initialization after E000H option ROM control completed. Displaying system configuration next.

PORT 80 CODES (continued)

Code	Description
AB	Uncompressing DMI data and executing DMI POST initialization next.
B0	System configuration is displayed.
B1	Copying any code to specific areas.
00	Copying of code to specific areas done. Passing control to INT 19H boot loader next.

The System BIOS passes control to the different buses at the following checkpoints to do various tasks:

Code	Description
2A	Initializing different bus system, static and output devices, if present.
38	Initializing bus input, IPL and general devices, if present.
39	Displaying bus initialization error messages, if any.
95	Initializing bus adapter ROM's from C8000H through D8000H.

ADDITIONAL BUS CHECKPOINTS

While control is in the different bus routines, additional checkpoints are output to Port 80H as WORD to identify the routines being executed. These are WORD checkpoints. The LOW BYTE of checkpoint is the system BIOS checkpoint where control is passed to the different bus routines, and the HIGH BYTE of checkpoint indicates that the routine is being executed in different buses.

The information included in the high and low bytes of these checkpoints is detailed on the next page.

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HIGH BYTE

The additional bus checkpoints listed above include the following information:

Bits	Description
Bits 7-4	0000 Function 0. Disable all devices on the bus. 0001 Function 1. Initialize static devices on the bus. 0010 Function 2. Initialize output dvices on the bus. 0011 Function 3. Initialize input devices on the bus. 0100 Function 4. Initialize IPL devices on the bus. 0101 Function 5. Initiate general devices on the bus. 0110 Function 6. Initialize error reporting on the bus. 0111 Function 7. Initialize add-on ROM's for all buses.
Bits 3-0	Specify the bus 0 Generic DIM Device Initialization Manager 1 Onboard system devices 2 ISA devices 3 EISA devices 4 ISA PnP devices 5 PCI devices

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APPENDIX B

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APPENDIX C

SCSISELECT CONFIGURATION UTILITY

INTRODUCTION

This appendix provides operating instructions for the Adaptec SCSISelect Configuration Utility, which allows you to view and change the configuration settings for the Adaptec SCSI adapter supplied on your single board computer (SBC). It also allows you to list the SCSI IDs of devices on the host adapter, format SCSI disk drives, and check drives for defects.

RUNNING THE CONFIGURATION UTILITY

To run the SCSISelect Configuration Utility, you must run the executable DOS program **cfg7880.exe**, which is provided with your SBC.

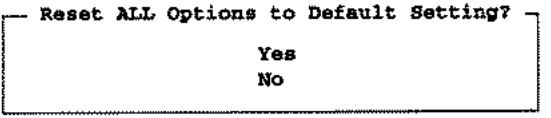
The configuration utility program may be run from your floppy drive or your hard drive. It is recommended that you run the program without any device drivers or TSRs loaded.

To select a line item for modification on any SCSISelect screen, use the arrow keys to move the cursor to the line item and then press **<Enter>**. The settings available for that line item display, with an asterisk (*) indicating the default value. Use the arrow keys to select the appropriate setting and press **<Enter>** to accept the setting and return to the setup screen. A line item might lead you to another screen with associated options. You can select the option(s) you wish to change as described above.

The SCSISelect screens, options and available settings are described later in this Appendix. The screens illustrated show the default settings for each line item. At any time during the SCSISelect session, you may press the **<F6>** key to reset to these default settings.

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If you select **<F6>**, the following message displays:

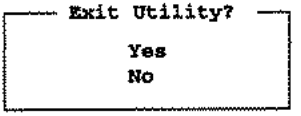


If you select **Yes**, *all* options revert to default settings. Any changes you have made previously will be lost, so be sure this is what you want to do before selecting this option.

EXITING SCSISELECT

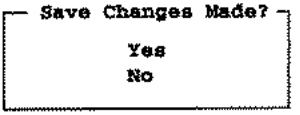
To exit from the SCSISelect utility, return to the **Options** Menu and press **<Esc>**.

If you have *not* made any changes to the adapter settings, the following message displays:

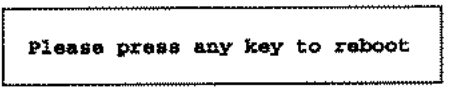


Select the appropriate response.

If you *have* made changes to the adapter settings, the following message displays:



If you do not want to save your changes, select **No** to exit from the utility. If you made changes to the adapter settings, select **Yes** to save your changes. The following message displays:

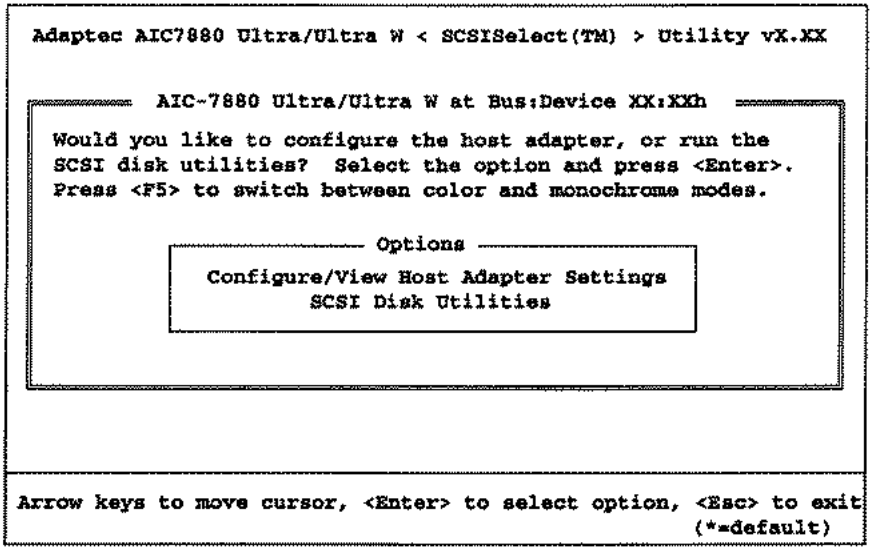


Press any key to reboot the computer. Any changes you made in SCSISelect take effect after the computer reboots.

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OPTIONS MENU

When you invoke the SCSISelect Configuration Utility, a screen similar to the following displays:



Options Screen

The two options available on this menu lead you to screens which allow you to view and/or change the adapter or device settings and to perform disk utility operations on these devices.

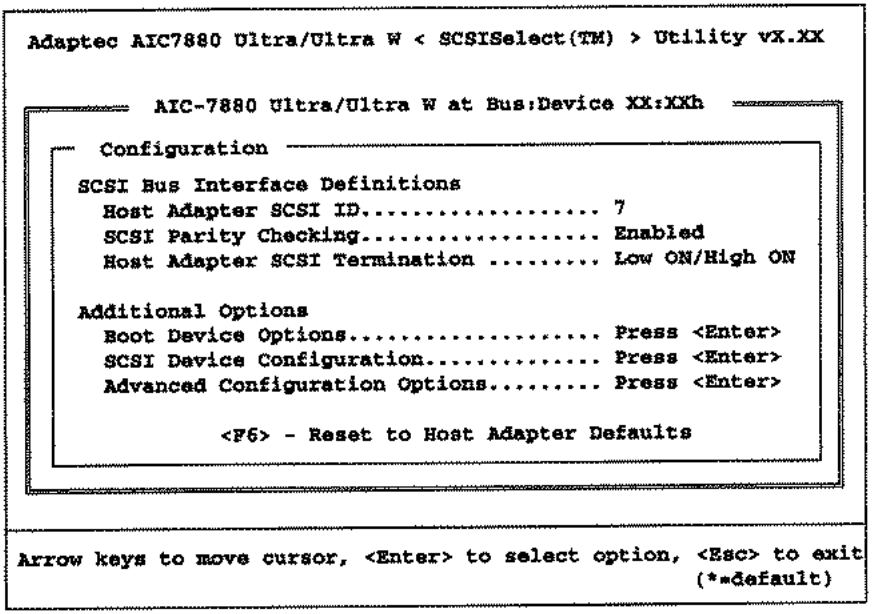
- Select **Configure/View Host Adapter Settings** to view and/or change the current settings for the host adapter and/or its devices.
- Select **SCSI Disk Utilities** to format disk drives attached to the host adapter or to check the disk drives for defects and reassign bad blocks.

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CONFIGURE/VIEW HOST ADAPTER SETTINGS

The **Configure/View Host Adapter** option displays the current settings for the SCSI bus interface and allows you to change these settings.

When you select this option from the **Options** Menu, a screen similar to the following displays:



Configure/View Host Adapter Settings Screen

The SCSI bus interface definitions displayed on this screen are described in the following pages. For additional options, you may:

- Select **Boot Device Options** to display and/or change boot device settings.
- Select **SCSI Device Configuration** to display and/or change the individual settings for the devices attached to the host adapter.
- Select **Advanced Configuration Options** to display and/or change the advanced configuration settings for the host adapter.

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Host Adapter SCSI ID

Each device on the SCSI bus, including the adapter, must have a unique SCSI ID. Allowable IDs are 0 through 7 on 8-bit adapters, and 0 through 15 on 16-bit adapters.

The SCSI ID serves two purposes:

1) It uniquely defines each SCSI device on the bus.
2) It determines which device controls the bus when two or more devices try to use the bus at the same time. For 8-bit devices, SCSI ID 7 has the highest priority and SCSI ID 0 has the lowest priority. For 16-bit devices, the priority of IDs is 7 through 0, then 15 through 8,with SCSI ID 7 having the highest priority and SCSI ID 8 having the lowest priority.

All adapters (8-bit and 16-bit) have a default SCSI ID of 7, which gives the host adapter the highest priority on the SCSI bus.

Available options are:

8-bit Adapters:
0 through 7

16-bit Adapters:
0 through 15

SCSI Parity Checking

Each adapter uses SCSI parity checking to verify the accuracy of data transfer on the SCSI bus. By default, parity checking is set to **Enabled**.

Most currently available SCSI devices support SCSI parity. However, if a device on the SCSI bus does *not* support SCSI parity, set the **SCSI Parity Checking** option to **Disabled**.

Available options are:

Enabled
Disabled

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Host Adapter SCSI Termination

A set of resistors, called *terminators*, must be either installed in or enabled on the first and last SCSI devices on each SCSI bus; otherwise, the devices will not operate properly.

Because the adapter is usually the SCSI device at one end of the bus, adapter termination for an 8-bit adapter is set to **Enabled** by default. If an 8-bit adapter is *not* at the end of the SCSI bus, set the **Host Adapter SCSI Termination** option to **Disabled**.

On 16-bit adapters, termination is enabled for both the low byte (bits 0-7) and the high byte (bits 8-15). The following table shows appropriate termination settings for a 16-bit adapter:

Description	Termination
Adapter is at end of SCSI bus; bus has only 8-bit devices or only 16-bit devices	Low ON/High ON (default)
Adapter is at end of SCSI bus; bus has both 8-bit and 16-bit devices. Last device must be 16-bit and be terminated.	Low ON/High ON
Adapter is *not* at end of SCSI bus; bus has only 16-bit devices	Low OFF/High OFF
Adapter is *not* at end of SCSI bus; bus has both 8-bit and 16-bit devices	Low OFF/High ON

Available options are:

8-bit Adapters:
- Enabled
- Disabled

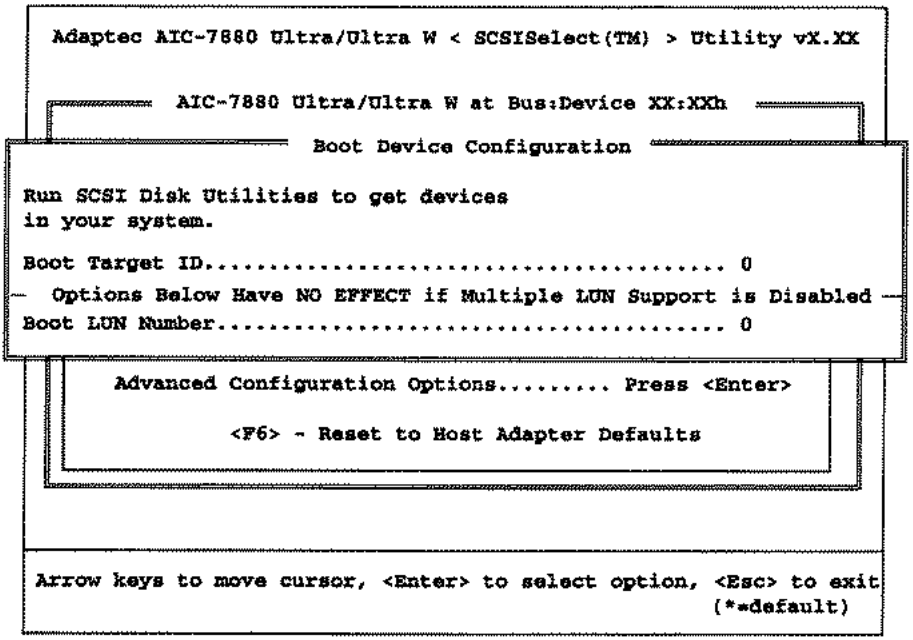
16-bit Adapters:
- Low ON/High ON
- Low OFF/High OFF
- Low OFF/High ON

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BOOT DEVICE OPTIONS

The **Boot Device Configuration** screen displays the current settings for the boot device and allows you to change these settings.

When you select **Boot Device Options** from the **Configuration** screen, a screen similar to the following displays:



Boot Device Configuration Screen

The Boot Device options (**Boot Target ID** and **Boot LUN Number**) let you specify the boot device. The default boot device is the device at SCSI ID 0 and logical unit number (LUN) 0.

Boot Target ID

This option allows you to specify a different boot device by selecting a different SCSI ID.

Available options are:

8-bit Adapters:
0 through 7

16-bit Adapters:
0 through 15

Boot LUN Number

If the boot device has multiple logical units, you must also specify the boot LUN.

Available options are:

0 through 7

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SCSI DEVICE CONFIGURATION

The **SCSI Device Configuration** screen displays the current settings for each SCSI ID and allows you to change these settings.

When you select this option from the **Configuration** screen, a screen similar to the following displays:

```
Adaptec AIC-7880 Ultra/Ultra W <SCSISelect(TM) > Utility vX.XX

SCSI Device ID                #0   #1   #2   #3   #4   #5   #6   #7

Initiate Sync Negotiation.. yes  yes  yes  yes  yes  yes  yes  yes
Maximum Sync Transfer Rate. 20.0 20.0 20.0 20.0 20.0 20.0 20.0 20.0
Enable Disconnection....... yes  yes  yes  yes  yes  yes  yes  yes
Initiate Wide Negotiation.. yes  yes  yes  yes  yes  yes  yes  yes
---- Options Listed Below Have NO EFFECT if the BIOS is Disabled ----
Send Start Unit Command.... no   no   no   no   no   no   no   no
Include in BIOS Scan....... yes  yes  yes  yes  yes  yes  yes  yes

SCSI Device ID                #8   #9   #10  #11  #12  #13  #14  #15

Initiate Sync Negotiation.. yes  yes  yes  yes  yes  yes  yes  yes
Maximum Sync Transfer Rate. 20.0 20.0 20.0 20.0 20.0 20.0 20.0 20.0
Enable Disconnection....... yes  yes  yes  yes  yes  yes  yes  yes
Initiate Wide Negotiation.. yes  yes  yes  yes  yes  yes  yes  yes
---- Options Listed Below Have NO EFFECT if the BIOS is Disabled ----
Send Start Unit Command.... no   no   no   no   no   no   no   no
Include in BIOS Scan....... yes  yes  yes  yes  yes  yes  yes  yes

Arrow keys to move cursor, <Enter> to select option, <Esc> to exit
                                                    (*=default)
```

SCSI Device ConfigurationScreen

The **SCSI Device Configuration** screen lists the current device settings for each SCSI ID, even if the ID is not assigned to a device.

If you do not know the SCSI ID of the device you want to configure, press **<Esc>** until the **Options** Menu displays, and then select the **SCSI Disk Utilities** option. A list of SCSI devices and their SCSI IDs displays. Note the ID of the device you want to configure and then return to the **SCSI Device Configuration** screen.

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SCSI DEVICE SETTINGS

The settings for each SCSI device on the SCSI bus can be modified individually as described below.

Initiate Sync Negotiation

Synchronous negotiation is a SCSI feature that allows the SCSI adapter and its attached SCSI devices to transfer data in synchronous mode. Synchronous data transfer is faster than asynchronous data transfer.

The **Initiate Sync Negotiation** setting determines whether the adapter initiates synchronous negotiation with the SCSI device. If this option is set to the default setting of **Yes**, the adapter initiates synchronous negotiation with the SCSI device. Normally, you should leave this option set to **Yes**, because most SCSI devices support synchronous negotiation, which allows for faster data transfer. If a device does not support synchronous negotiation, the adapter automatically transfers the data in asynchronous mode.

If you change the setting to **No**, the adapter does *not* initiate synchronous negotiation; however, the adapter always responds to synchronous negotiation if the SCSI device initiates it. If neither the adapter nor the SCSI device negotiates for synchronous data transfers, data is transferred in asynchronous mode.

Available options are:

Yes
No

Maximum Sync Transfer Rate

This setting determines the maximum synchronous data transfer rate that the adapter will negotiate with the device. The adapter automatically negotiates for the rate requested by the device. The allowable maximum rates are in megabytes.

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If the adapter is set *not* to negotiate for synchronous data transfer (i.e., if the **Initiate Sync Negotiation** option is set to **No**), the value selected here is the maximum rate at which the adapter accepts data from the device during negotiation. This is standard SCSI protocol.

If the **Support for Ultra SCSI Speed** option on the **Advanced Configuration Options** screen is disabled, the only values available for maximum sync transfer rate are those for 8-bit adapters (see below); in this case, the default is **20.0**. If **Support for Ultra SCSI Speed** is enabled, the values for 16-bit adapters are available and the default is **40.0**.

Available options are:

8-bit Adapters:
- 20.0
- 16.0
- 13.4
- 10.0

16-bit Adapters:
- 40.0
- 32.0
- 26.8
- 20.0

Enable Disconnection

This setting determines whether the adapter allows a SCSI device to disconnect from the SCSI bus (sometimes called Disconnect/Reconnect). Enabling disconnection allows the adapter to perform other operations on the SCSI bus while the SCSI device is temporarily disconnected.

When the **Enable Disconnection** option is set to the default setting of **Yes**, the SCSI device may disconnect from the SCSI bus. The SCSI device may choose not to disconnect, however, even if permitted by the adapter (this can usually be configured on the SCSI device). When this option is set to **No**, the SCSI device cannot disconnect from the SCSI bus.

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Leave the **Enable Disconnection** option set to **Yes** if the adapter connects to two or more SCSI devices. This optimizes SCSI bus performance. If the adapter connects to only one SCSI device, set this option to **No** to achieve slightly better performance.

Available options are:

Yes
No

Initiate Wide Negotiation

This option, which only displays for 16-bit adapters, lets the adapter initiate wide negotiation with a 16-bit SCSI device. The adapter will not attempt wide negotiation with 8-bit devices, so you can leave this option set to **Yes** even if the bus includes 8-bit devices.

Available options are:

Yes
No

Send Start Unit Command

This setting determines whether the adapter sends the Start Unit command (SCSI command 1B) to the SCSI device. The default setting for **Send Start Unit Command** is **No** (disabled).

Enabling this option reduces the load on a computer's power supply by allowing the adapter to turn on SCSI devices one by one when the computer boots; otherwise, all SCSI devices turn on at the same time. Before you enable this option for a device, make sure the AIC-7880 BIOS is enabled. Also, check the device documentation to make sure the device supports the command. On most devices, you must also change a switch or jumper setting on the device to enable the device to respond to the command.

If you enable **Send Start Unit Command** for more than one SCSI device, the adapter first sends the Start Unit command to the boot device specified in the **Boot Target ID** option of the **Boot Device**

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Configuration screen. When the boot device responds, Start Unit commands are sent to the remaining devices, beginning with the device with the lowest SCSI ID. The boot time varies depending on how long each drive takes to spin up.

Available options are:

Yes
No

Include in BIOS Scan

This option indicates whether or not the specified SCSI device should be included in a scan of the devices which is done during bootup. Setting this option to **No** for devices which are not attached saves time during bootup since the BIOS will not spend time checking for unassigned devices.

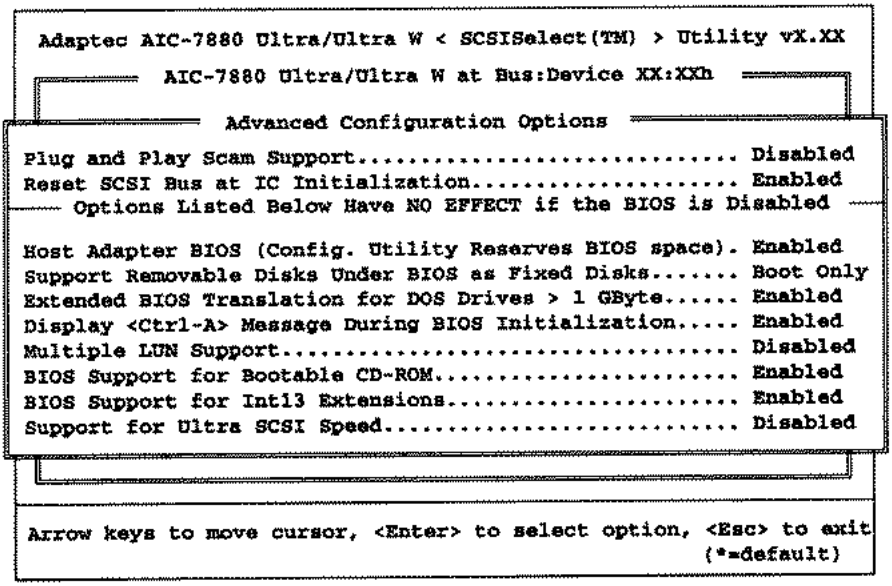
Available options are:

Yes
No

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ADVANCED CONFIGURATION OPTIONS

When you select **Advanced Configuration Options** from the **Configuration** Menu, the following screen displays:



Advanced Configuration Options Screen

The **Advanced Configuration Options** screen displays the current settings for the selected adapter and allows you to change these settings.

Plug and Play Scam Support

When this option is set to **Enabled**, it allows the adapter to automatically assign a SCSI ID to an attached SCSI device that supports SCAM-1 (SCSI Configured AutoMatically) protocol. Most non-SCAM devices tolerate SCAM protocol, so you can usually enable this option even if you have some non-SCAM devices. In rare cases, an old SCSI-1 device may not tolerate SCAM and may cause your computer to hang or operate erratically. If this happens, set the option back to **Disabled**.

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The default for this option is **Disabled**. When you attempt to change it to **Enabled**, the following informational message displays:

```
WARNING: 'Reset SCSI Bus at IC Initialization' cannot be DISABLED
         if 'Plug and Play Scam Support' is ENABLED.
         (Compliant to Scan Protocol)
```

Available options are:

Enabled
Disabled

Reset SCSI Bus at IC Initialization

The default for this option is **Enabled**. When the **Plug and Play Scam Support** option is set to **Enabled**, you *cannot* change this option to **Disabled**.

Available options are:

Enabled
Disabled

Host Adapter BIOS

This option enables or disables the AIC-7880 BIOS. The BIOS must be enabled if you want the computer to boot from a SCSI hard disk drive connected to the adapter. In addition, the BIOS must be enabled if you want to enable any of the following options:

- Support Removable Disks Under BIOS as Fixed Disks
- Extended BIOS Translation for DOS Drives > 1 GByte
- Multiple LUN Support
- BIOS Support for Bootable CD-ROM
- BIOS Support for Int 13 Extensions
- Support for Ultra SCSI Speed
- Send Start Unit SCSI Command

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If the devices on the SCSI bus are controlled by device drivers (and therefore do not need a BIOS), you can disable the AIC-7880 BIOS to free about 16KB of memory. This also shortens the boot time by up to 60 seconds.

Available options are:

Enabled
Disabled

Support Removable Disks Under BIOS as Fixed Disks

This setting controls which removable-media drives are supported by the AIC-7880 BIOS.

When you attempt to change the setting of this option, the following informational message displays:

```
WARNING:  Do not remove media from a removable media drive if
          it is under BIOS control.
```

Available options are:

- **Boot Only** - Only the removable-media drive designated as the boot device is treated as a hard disk drive. This is the default option.
- **All Disks** - All removable-media drives supported by the AIC-7880 BIOS are treated as hard drives. This setting has no effect on drives under NetWare, because NetWare automatically supports removable-media drives as fixed disks.
- **Disabled** - No removable-media drives running under DOS are treated as hard disk drives. In this situation, driver software is needed, because the drives are not controlled by the BIOS.

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Extended BIOS Translation for DOS Drives > 1 GByte

All current versions of MS-DOS are limited to 1024 cylinders per drive. The standard translation scheme for SCSI host adapters, using 64 heads and 32 sectors, provides a maximum accessible capacity of 1 GByte. To support disk drives larger than 1 GByte, the AIC-7880 BIOS includes an extended translation scheme that supports disk drives as large as 8 GBytes under MS-DOS.

This option is not available if the **Host Adapter BIOS** option is set to **Disabled**. The default for this option is **Enabled** and should *not* be changed. With extended translation enabled, drives handled by the AIC-7880 BIOS use extended translation if their formatted capacity is greater than 1 GByte, and drives smaller than 1 GByte use standard translation.

NOTE: If you decide to change the translation scheme, be sure to back up the disk drives first. All data is erased when you change from one translation scheme to another.

When you partition a disk larger than 1 GByte, use the MS-DOS *fdisk* utility as you normally would. Because the cylinder size increases up to 8MB under extended translation, the partition size you choose must be a multiple of 8MB. If you request a size that is not a multiple of 8MB, *fdisk* rounds up to the nearest whole multiple of 8MB.

Available options are:

Enabled
Disabled

Display <Ctrl-A> Message During BIOS Initialization

This option has no effect since the configuration utility is invoked using the cfg7880.exe program.

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Multiple LUN Support

This option allows the BIOS to support multiple logical units. Set this option to **Enabled** if any devices have multiple logical units.

Available options are:

Enabled
Disabled

BIOS Support for Bootable CD-ROM

To boot from a CD-ROM, this option must be set to **Enabled**. If you are booting from a hard disk or other device, make sure no bootable CD-ROM is installed, or set this option to **Disabled**.

Available options are:

Enabled
Disabled

BIOS Support for Int 13H Extensions

When this option is set to **Enabled**, the adapter BIOS supports El Torito Int 13H extensions, which are required for bootable CD-ROMs. You can disable this option if the boot device is not a CD-ROM, but it is not necessary to do so.

Available options are:

Enabled
Disabled

Support for Ultra SCSI Speed

This option should be set to **Enabled** if you want to use Ultra SCSI speeds with the AIC-7880.

Available options are:

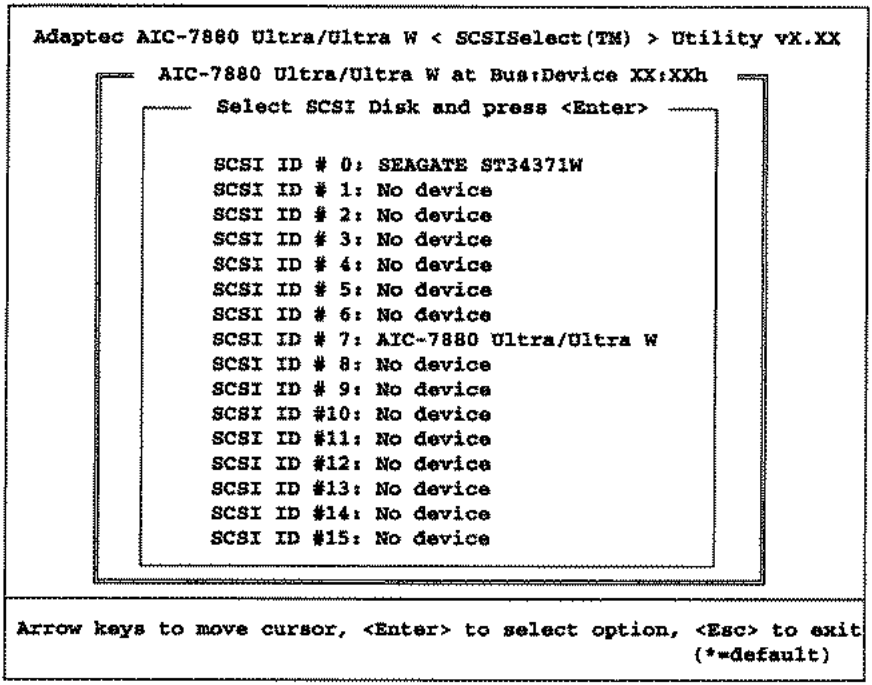
Enabled
Disabled

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SCSI DISK UTILITIES

The **SCSI Disk Utilities** screen allows you to format or verify a device on the SCSI bus.

When you select **SCSI Disk Utilities** from the **Options** Menu, SCSISelect scans the SCSI bus for SCSI devices and displays a screen similar to the following:



SCSI Disk Utilities Screen

This screen lists the SCSI IDs on the SCSI bus and the types of devices assigned to each ID. If your system has an Ultra Wide SCSI adapter, 16 devices display (IDs 0 through 15). If you have an 8-bit adapter, only IDs 0 through 7 display.

Select the device you wish to format or verify and press **<Enter>**. If the device has multiple logical units, a menu of LUNs displays. Select the LUN of the unit you want to format or verify and press **<Enter>**.

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The following menu displays:

```
Format Disk
Verify Disk Media
```

Format Disk

A disk must have a low-level format before you can use the operating system's partitioning and high-level formatting utilities, such as MS-DOS *fdisk* and *format*. Most SCSI drives are preformatted and need not be formatted again. If a drive is not preformatted, you can use SCSISelect to perform a low-level format on the drive. The formatting is compatible with most SCSI disk drives.

NOTE: A low-level format destroys all data on the drive. Be sure to back up your data before performing this operation. You *cannot* abort a low-level format once it starts.

When you select the **Format Disk** option, a prompt displays showing the SCSI ID, type and size of the device you have selected and asks you to confirm that you want to format the disk:

```
SCSI ID #0 : SEAGATE ST34371W
Capacity:    4148 MBytes

WARNING!!!  This drive is about to be low-level
formatted.  All data on the disk will be erased.

        Format Disk?
            Yes
            No
```

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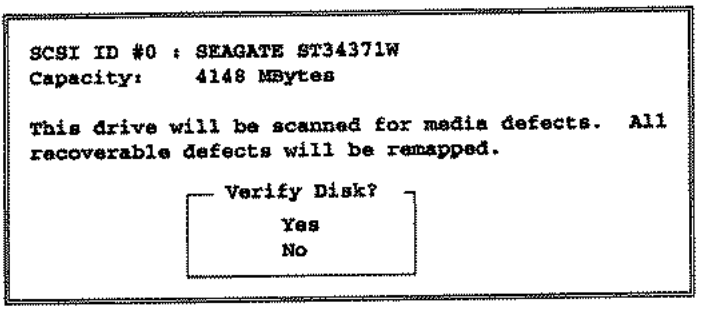
Two options are available:

- Select **Yes** to start formatting the disk immediately.
- Select **No** to cancel the format command *without* performing the format and return to the **SCSI Disk Utilities** screen.

Verify Disk Media

This option lets you scan a disk device for defects. If SCSISelect finds bad blocks, it prompts you to reassign them so they are no longer used.

When you select the **Verify Disk** option, a prompt displays showing the SCSI ID, type and size of the device you have selected and asks you to confirm that you want to verify the disk:



Two options are available:

- Select **Yes** to continue with the verify procedure and reassign bad blocks.

  If you choose to perform the verify, SCSISelect notifies you of bad blocks and prompts you to reassign them. You may press **<Esc>** at any time to stop the verification process.

- Select **No** to cancel the verify command *without* performing the verify and return to the **SCSI Disk Utilities** screen.

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Declaration of Conformity

APPLICATION OF COUNCIL DIRECTIVE(S)

89/336/EEC

Standard(s) to which Conformity is Declared:

EN55022: 1994/A2:1997, CLASS A
EN50082-2: 1995

Manufacturer:	TRENTON TECHNOLOGY Inc. 2350 Centennial Drive Gainesville, Georgia 30504 USA Phone: (770) 287-3100 Fax: (770) 287-3150
Type of Equipment:	PCI CPU Board
Model Name(s):	92-005664 (Also Known As: DP2/850, DP2/800, DP2/750, DP2/700, DP2/650, DP2/600E, DP2/600, DP2/550E, DP2/550, DP2/500, DP2/450, DP2/400, DP2/350 and DP2/333; DP2GX/850, DP2GX/800, DP2GX/750, DP2GX/700, DP2GX/650, DP2GX/600E, DP2GX/600, DP2GX/550E, DP2GX/550, DP2GX/500, DP2GX/450, DP2GX/400, DP2GX/350 and DP2GX/333)

I, the undersigned, hereby declare that the specified equipment conforms to the Directive(s) and Standard(s) listed above.

Signature:	
Name:	Stephen W. McReynolds
Title:	Engineering Manager
Date:	September 10, 2000

TRENTON

TRENTON Technology Inc.
2350 Centennial Drive • Gainesville, Georgia 30504
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