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XPT

S6090-xxx

TECHNICAL REFERENCE

Xeon™

PROCESSOR-BASED

SBC

CE

PCI INDUSTRIAL COMPUTERS PICMG

PCI LOCAL BUS

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Return company address and contact
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Serial number from the label on the back of the board
Description of the failure

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Declaration of Conformity

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HANDLING PRECAUTIONS

WARNING: This product has components which may be damaged by electrostatic discharge.

To protect your single board computer (SBC) from electrostatic damage, be sure to observe the following precautions when handling or storing the board:

- Keep the SBC in its static-shielded bag until you are ready to perform your installation.
- Handle the SBC by its edges.
- Do not touch the I/O connector pins. Do not apply pressure or attach labels to the SBC.
- Use a grounded wrist strap at your workstation or ground yourself frequently by touching the metal chassis of the system before handling any components. The system must be plugged into an outlet that is connected to an earth ground.
- Use antistatic padding on all work surfaces.
- Avoid static-inducing carpeted areas.

SOLDER-SIDE COMPONENTS

This SBC has components on both sides of the PCB. It is important for you to observe the following precautions when handling or storing the board to prevent solder-side components from being damaged or broken off:

- Handle the board only by its edges.
- Store the board in padded shipping material or in an anti-static board rack.
- Do not place an unprotected board on a flat surface.

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Before you Begin

INTRODUCTION

It is important to be aware of the system considerations listed below before installing your XPT SBC. Overall system performance may be affected by incorrect usage of these features.

DDR MEMORY

The XPT requires that at least two of the four memory sockets on the SBC must be populated. DIMMs *must* be installed in *pairs*, beginning with the sockets in Bank 1 (i.e., BK1A and BK1B), and must contain ECC registered PC1600 or PC2100 DIMMs. All DIMMs must be the same speed (PC1600 or PC2100). The modules within a pair *must* be the same size; however, if two pairs are used, each pair can contain a different size module. DIMM sizes can range from 128MB to 2GB each.

In addition, the DIMMs must have the following features:

- 184-pin with gold-plated contacts
- ECC (72-bit) memory
- Registered configuration
- x4 or x8 construction

POWER REQUIREMENTS

The following are typical values:

Processor Speed	+5V *	+12V **	+3.3V *	-12V *
2.8GHz	4.10 Amps	13.15 Amps	1.41 Amps	< 100 mAmps
2.4GHz	4.10 Amps	9.90 Amps	1.40 Amps	< 100 mAmps
2.0GHz	3.80 Amps	8.20 Amps	1.10 Amps	< 100 mAmps

* From backplane via PICMG connector.
** From ATX12V power supply or equivalent via P24 connector.

NOTE: The XPT requires an *additional* on-board power connector due to the power requirements of the Intel® Xeon™ processor. This 4-pin connector (P24) *requires* +12V from an external power supply that conforms to the ATX12V power specification. The external power supply *must* have a wattage rating of 250W or higher. The XPT also requires that +3.3V be applied to the backplane from the power supply.

HYPER-THREADING

The factory setting of the **HyperThreading** option in the system BIOS is **Disabled**.

Hyper-Threading improves overall performance in many systems designed for multi-processing, high-demand multi-tasking and multi-threaded applications. If you are using a system which can take advantage of Hyper-Threading technology, you may use the BIOS Setup Utility to change the setting of the **HyperThreading** option to **Enabled**. This option is found on the **CPU Configuration** screen in the *Advanced Setup* section of the BIOS Setup Utility.

Intel® recommends enabling Hyper-Threading on systems that use Microsoft® Windows® XP® or Linux® 2.4.x operating systems.

For systems which use applications and operating systems which cannot take advantage of Hyper-Threading technology, the **HyperThreading** option should remain **Disabled**. Intel recommends disabling Hyper-Threading when using the following operating systems: Microsoft Windows 98®, Windows NT®, Windows 2000®, Windows ME®, IBM® OS/2® and any version of Linux before revision 2.4.x. These operating systems are not optimized for Hyper-Threading technology and some applications may actually experience some performance degradation.

RATIO CMOS SETTING

The XPT SBC is set at the San Diego, CA 92123 factory to the correct processor speed before shipment, but if the CMOS settings have been corrupted or if you have used the JU12 jumper to clear CMOS, the Xeon processor may reset to the safe mode. The result is a reduction in execution speed which affects overall system performance. After clearing CMOS, you should always check the operating speed and reset it if necessary.

The **Ratio CMOS Setting** option in the BIOS Setup Utility allows you to reset the operating speed of the SBC to its correct value. This option is found on the **CPU Configuration** screen in the *Advanced Setup* section of the BIOS Setup Utility.

FOR MORE INFORMATION

For more information on any of these features, refer to the appropriate sections of the *XPT Technical Reference Manual* (#87-006093-000). The latest revision of this manual may be found on Chassis Plans' website - www.chassisplans.com.

Chapter 1 Specifications

INTRODUCTION

The XPT full-featured PCI/ISA processors are single board computers (SBCs) which feature dual Intel® Xeon™ microprocessors, 400/533MHz system and memory buses, ATI Technologies® video interface, support for 8GB DDR memory, PCI Local Bus, cache, floppy controller, dual EIDE (Ultra ATA/100) interfaces, Ultra320 Dual Channel SCSI controller, dual Gigabit Ethernet interfaces, two serial ports, parallel port, speaker port, mouse port and keyboard port. These high performance SBCs plug into PICMG® PCI/ISA and PCI-X backplanes and provide full PC compatibility for the system expansion slots. The XPT-NS model has all of the standard features of the XPT, except it does not include the Adaptec SCSI controller or the two Ultra320 SCSI ports.

MODELS

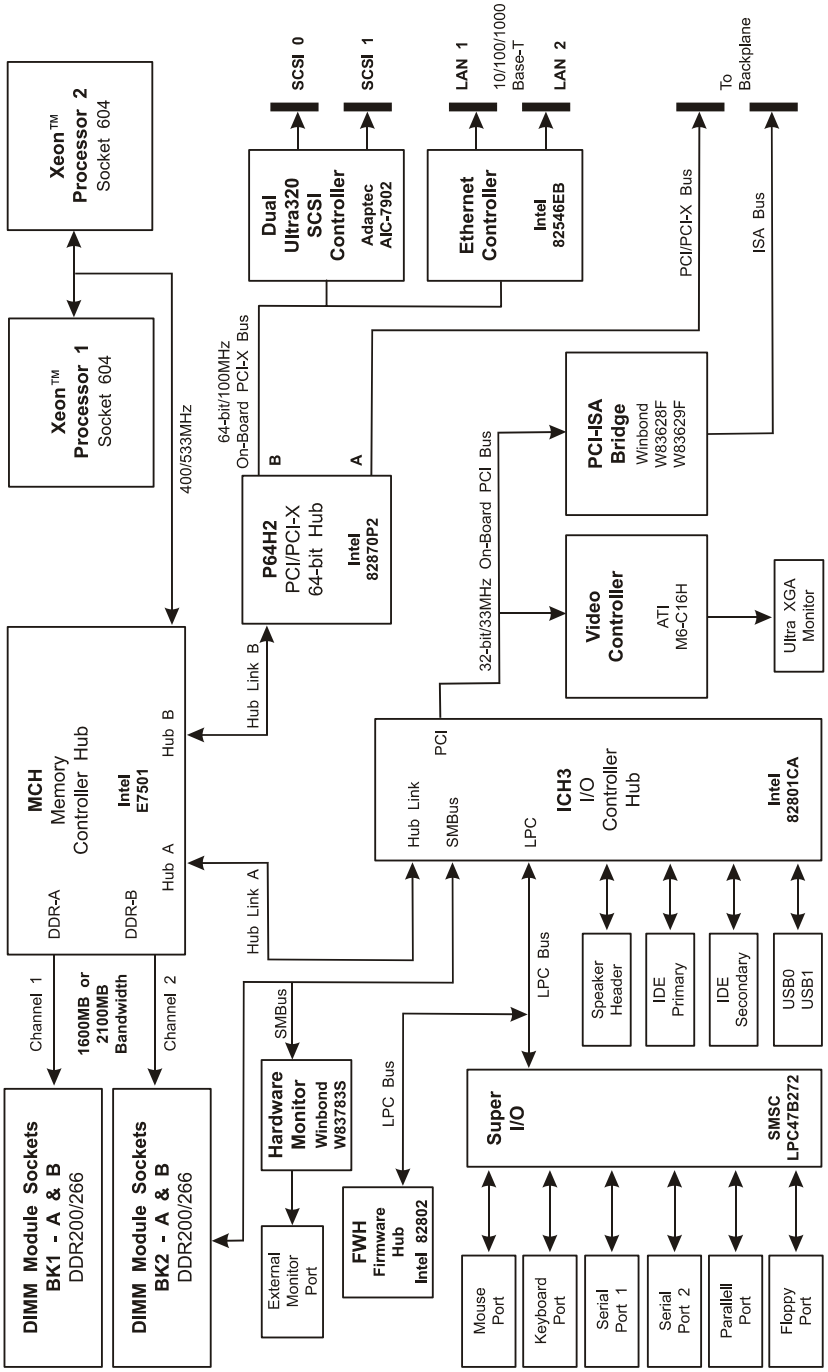
Model #	Model Name	Speed
Xeon Processor - 533MHz FSB/512K cache:		
S6090-108-xM	XPT/3.06	3.06GHz
S6090-107-xM	XPT/2.8E	2.8GHz
S6090-106-xM	XPT/2.66E	2.66GHz
S6090-104-xM	XPT/2.4E	2.4GHz
S6090-102-xM	XPT/2.0E	2.0GHz
Xeon Processor - 400MHz FSB/512K cache:		
S6090-007-xM	XPT/2.8	2.8GHz
S6090-006-xM	XPT/2.6	2.6GHz
S6090-004-xM	XPT/2.4	2.4GHz
S6090-003-xM	XPT/2.2	2.2GHz
S6090-002-xM	XPT/2.0A	2.0GHz
S6090-001-xM	XPT/1.8	1.8GHz
"No SCSI" Models:		
Xeon Processor - 533MHz FSB/512K cache:		
S6090-128-xM	XPT/3.06E-NS	3.06GHz
S6090-127-xM	XPT/2.8E-NS	2.8GHz
S6090-126-xM	XPT/2.66E-NS	2.66GHz
S6090-124-xM	XPT/2.4E-NS	2.4GHz
S6090-122-xM	XPT/2.0E-NS	2.0GHz
Xeon Processor - 400MHz FSB/512K cache:		
S6090-027-xM	XPT/2.8-NS	2.8GHz
S6090-026-xM	XPT/2.6-NS	2.6GHz
S6090-024-xM	XPT/2.4-NS	2.4GHz
S6090-023-xM	XPT/2.2-NS	2.2GHz
S6090-022-xM	XPT/2.0A-NS	2.0GHz
S6090-021-xM	XPT/1.8-NS	1.8GHz

where xM indicates memory size (0M = 0MB memory, 8M =8MB memory, etc.)

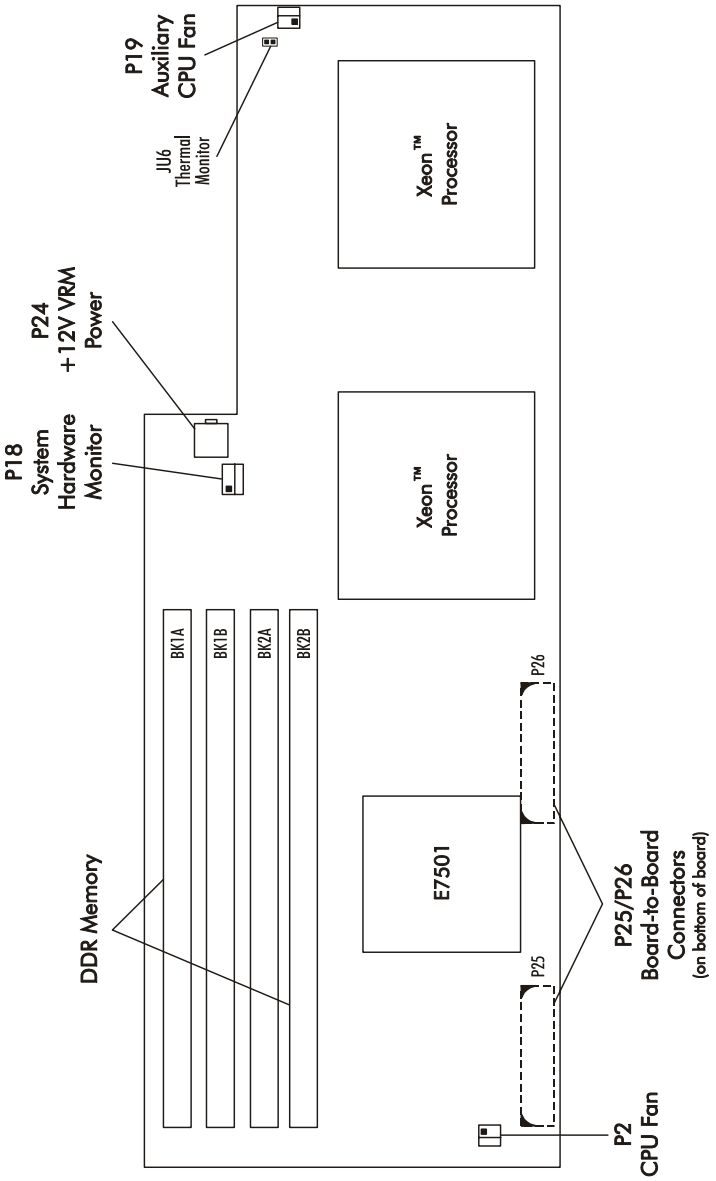
FEATURES

- Dual Intel® Xeon™ microprocessors
  - 2.8GHz, 2.66GHz, 2.4GHz or 2.0GHz with 512K cache and a 533MHz Front Side Bus
  - 2.8GHz, 2.6GHz, 2.4GHz, 2.2GHz, 2.0GHz or 1.8GHz with 512K cache and a 400MHz Front Side Bus
- Intel E7501 chipset with 400/533MHz system bus
- PCI-X Bus supports off-board PCI-X architectures of 64-bit/66MHz, 64-bit/100MHz or 64-bit/133MHz and off-board PCI architectures of 64-bit/66MHz, 64-bit/33MHz, 32-bit/66MHz or 32-bit/33MHz
- Ultra XGA on-board video interface (ATI Technologies®)
- Dual Ultra320 SCSI ports using an on-board Adaptec AIC-7902 controller
- Dual Ethernet interfaces for use with 10/100/1000Base-T networks
- Memory error checking and correction (ECC) support
- Compatible with PCI Industrial Computer Manufacturers Group (PICMG) 1.0 Specification
- Supports up to 8GB of Double Data Rate (DDR) on-board memory
- Floppy drive and dual PCI EIDE Ultra ATA/100 drive interfaces
- Two serial ports and one parallel port
- Dual Universal Serial Bus (USB) support
- Automatic or manual peripheral configuration
- Watchdog timer
- System hardware monitor
- Full PC compatibility

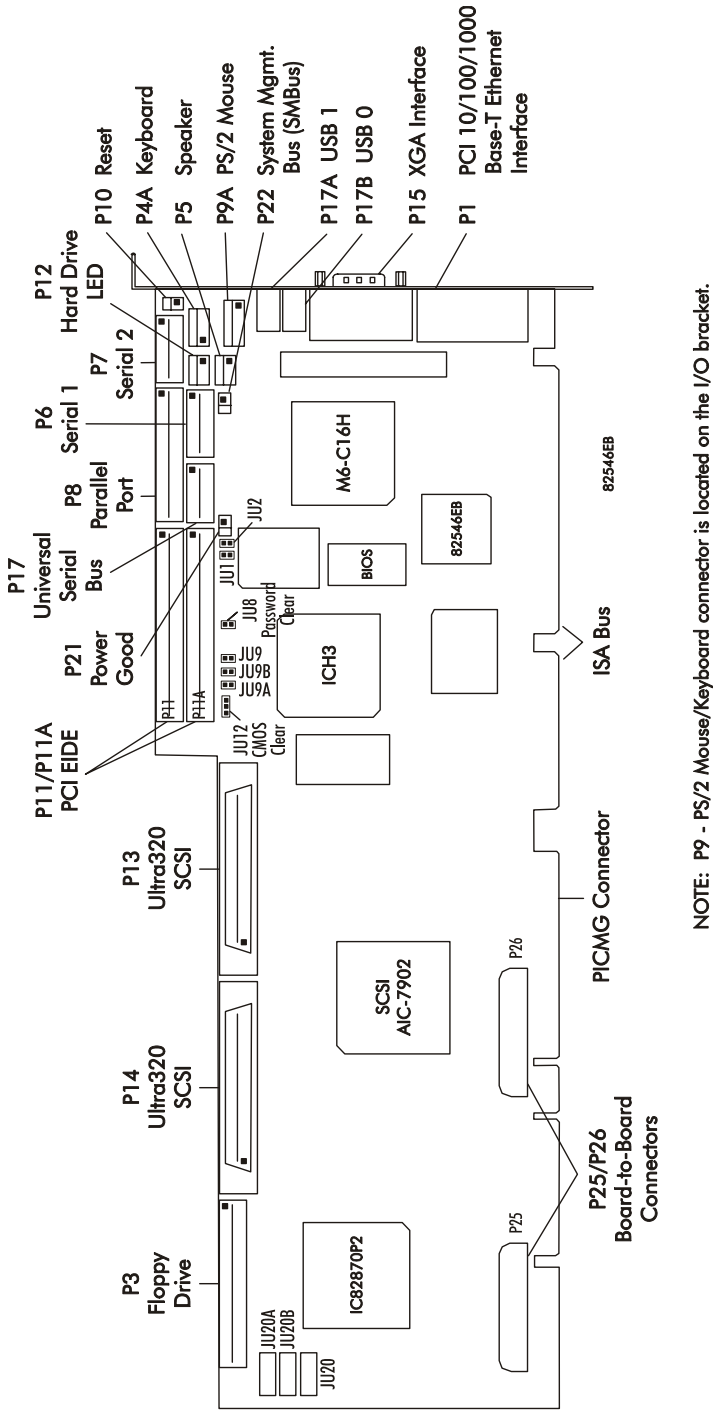
SBC BLOCK DIAGRAM



SBC PROCESSOR BOARD LAYOUT



SBC I/O BOARD LAYOUT



PROCESSORS

- Dual Intel® Xeon™ microprocessors
  - 2.8GHz, 2.66GHz, 2.4GHz or 2.0GHz with 512K cache and a 533MHz Front Side Bus
  - 2.8GHz, 2.6GHz, 2.4GHz, 2.2GHz, 2.0GHz or 1.8GHz with 512K cache and a 400MHz Front Side Bus
- Processors use the FC-mPGA2 packaging (604-pin)

NOTE: Xeon processors are shipped from the vendor as "fuse limited," indicating that they run up to the designated speed (e.g., 2.0GHz), but also have the ability to reset to a "safe mode" of 800MHz. The SBC is set at the Chassis Plans factory to the correct processor speed before shipment, but if the CMOS settings are corrupted or cleared, the Xeon processor may reset to the safe mode, resulting in a noticeable reduction in execution speed. In this event, the SBC must be reset to the correct operating speed using the **Ratio CMOS Setting** option on the **CPU Configuration** screen. See the *Advanced Setup* chapter of this manual for further details.

BUS INTERFACES ISA and PCI Local Bus compatible

DATA PATH DDR Memory - 64-bit

ISA Bus - 16-bit

PCI Bus - 32-bit or 64-bit

PCI-X Bus - 64-bit

Video - 32-bit

BUS SPEED - ISA 8.33MHz

BUS SPEED - PCI PCI - 33MHz or 66MHz
PCI-X - 66MHz, 100MHz or 133MHz

BUS SPEED - SYSTEM 400/533MHz Front Side Bus

MEMORY INTERFACE Dual Double Data Rate (DDR) memory channels for 3.2GB/s memory bandwidth

SYSTEM BUS The Intel E7501 chip set supports the system bus at 400MHz or 533MHz, which provides a higher bandwidth path for transferring data between main memory/chipset and the processor.

DMA CHANNELS The SBC is fully PC compatible with seven DMA channels, each supporting type F transfers.

INTERRUPTS The SBC is fully PC compatible with interrupt steering for PCI plug and play compatibility.

BIOS (FLASH)

The BIOS is an AMIBIOS8® with built-in advanced CMOS setup for system parameters, peripheral management for configuring on-board peripherals, PCI-to-PCI bridge support and PCI interrupt steering. The Flash BIOS resides in the Intel 82802 Firmware Hub (FWH). The BIOS may be upgraded from floppy disk by pressing **<Ctrl> + <Home>** immediately after reset or power-up with the floppy disk in drive A:. Custom BIOSs are available.

CACHE MEMORY

The processor includes integrated on-die, 512K 8-way set associative level two (L2) cache, which implements the Advanced Transfer Cache architecture. The processor also provides a 12K level one (L1) Execution Trace cache which includes an 8K L1 data cache. These cache arrays run at the full speed of the processor core.

NETBURST™ MICRO-ARCHITECTURE

NetBurst micro-architecture defines the techniques Intel uses to enhance the processor's execution of the BIOS, operating system and application software. These techniques include hyper pipelined technology, a rapid execution engine, advanced dynamic execution, enhanced floating point and multimedia unit and Streaming SIMD Extensions 2 (SSE2). The processor's system bus speed and memory cache are also part of the NetBurst micro-architecture.

Hyper pipelined technology doubles the pipeline depth inside the processor, which enables more instructions to be loaded, resulting in higher core frequencies. Advanced dynamic execution includes an improved speculative execution algorithm that minimizes processor instruction misdirects and results in faster instruction execution.

The rapid execution engine enables the two arithmetic logic units (ALUs) of the processor to operate at twice the core frequency. Many integer instructions can now execute in half the internal core clock period, resulting in improved software execution speeds.

NetBurst micro-architecture improvements in the floating point and multimedia unit include making the registers 128 bits wide and adding a separate register for moving data.

The SSE2 has 144 instructions which improve performance in secure transactions and multimedia processing. These instructions are used for double-precision floating point, SIMD integer and memory management improvements.

DDR MEMORY

The Double Data Rate (DDR) memory interface consists of two channels, each terminating at a pair of DIMM sockets, providing a total of four memory sockets. The SBC supports auto detection of up to 8GB of memory. The System BIOS automatically detects memory type, size and speed.

The SBC uses industry standard 72-bit wide gold finger PC1600 or PC2100 memory modules in four 184-pin sockets.

NOTE: At least two of the four memory sockets on the SBC must be populated. DIMMs *must* be installed in *pairs*, beginning with the sockets in Bank 1 (i.e., BK1A and BK1B), and must contain ECC registered PC1600 or PC2100 DIMMs. All DIMMs must be the same speed (PC1600 or PC2100). The modules within a pair *must* be the same size; however, if two pairs are used, each pair can contain a different size module.

DIMM sizes can range from 128MB to 2GB each. All memory modules must have gold contacts.

The SBC supports DIMMs which are PC1600/PC2100 compliant and have the following features:

- 184-pin with gold-plated contacts
- ECC (72-bit) memory
- Registered configuration
- x4 or x8 construction

The following DIMM sizes are supported:

DIMM Size	DIMM Type	ECC	Component Construction
128MB	Registered	16M x 72	x4, x8
256MB	Registered	32M x 72	x4, x8
512MB	Registered	64M x 72	x4, x8
1GB	Registered	128M x 72	x4, x8
2GB	Registered	256M x 72	x4, x8

ERROR CHECKING AND CORRECTION

The memory interface supports ECC modes via BIOS setting for multiple-bit error detection and correction of all errors confined to a single nibble.

PCI LOCAL BUS INTERFACE

The SBC is fully compliant with the PCI Local Bus 2.1 Specification. The SBC supports three independent PCI Bus interfaces: a 32-bit on-board PCI Bus interface (33MHz) and two 64-bit Secondary Bus interfaces (PCI Bus A and PCI Bus B). Secondary PCI Buses A and B each have four 1024-byte buffers for inbound read requests and a 1.5K buffer for inbound write transactions. An I/O cache is available that accommodates up to sixteen posted and non-posted inbound commands and up to sixteen outbound commands for completions and requests. Each secondary PCI Bus interface supports one outbound delayed transaction and up to four active and four pending inbound delayed transactions.

The SBC's on-board PCI Bus interface is 32 bits wide and runs at 33MHz. This bus supports the on-board video and PCI/ISA bridge interfaces.

Secondary PCI/PCI-X Bus A is 64 bits wide and supports off-board PCI/PCI-X architectures of 33MHz, 66MHz, 100MHz and 133MHz. This interface provides a sixteen-entry I/O cache and is routed off-board to drive PICMG compliant PCI/ISA and PCI-X backplanes.

Secondary PCI Bus B is 64 bits wide and runs at 100MHz. This bus is an on-board PCI-X bus interface that supports the SBC's dual Ultra320 SCSI controller and the dual 10/100/1000Base-T Ethernet controller, which enables full-speed Gigabit Ethernet capability.

The SBC supports Hub Interface 2.0-to-PCI bridge technology and PCI-to-ISA bridge technology. The SBC's high-speed primary Hub Interface and secondary PCI and PCI-X interfaces increase the connection speeds of external PCI devices and Ethernet LANs. The PCI/PCI-X interface to the backplane is compliant with the PCI Industrial Computer Manufacturers Group (PICMG) 1.0 Specification.

UNIVERSAL SERIAL BUS (USB)

The SBC supports two USB 1.1 ports for serial transfers at 12 or 1.5Mbit/sec. The Universal Serial Bus (USB) is an interface allowing for connectivity to many standard PC peripherals via an external port.

ULTRA XGA INTERFACE

The ATI Technologies M6-16H video controller enables 2D/3D video acceleration and provides 16MB of integrated video DDR memory. The video controller's DVI compliant 165MHz TMDS transmitter supports pixel resolutions from VGA (640 x 480) up to UXGA (1600 x 1200).

Software drivers are available for most popular operating systems.

SYSTEM HARDWARE MONITOR

The system hardware monitoring system monitors system voltages, temperature and fan speeds.

The circuitry is based on Winbond's W83783S hardware monitoring IC that is interfaced via the system's SMBus. System voltages of +12V, +5V, +3.3V, +2.5V and VCCORE (processor voltage) are monitored. Each of these voltages has programmable "high" and "low" watchdog limits. Also monitored is the fan speed associated with the processors' thermal solution. Optionally, the speed of a second system fan can be monitored via the Auxiliary CPU Fan connector. Programmable watchdog limits are also associated with fan speed RPMs. When any of these programmed limits are exceeded, monitor software can be used to report the out-of-limit condition.

The System Hardware Monitor connector (P18) provides an external interface for user functionality. Pin assignments for this connector are as follows:

Pin #/Definition	Description
Pin 1 - GND	System Ground
Pin 2 - GPO	General Purpose Output Active low open drain output. This multi-function output is controlled by the W38383S's configuration register at offset 40(h) and the control register at 4D(h). It can be used as a general-purpose output or programmed to provide a beep function that can be used as a watchdog warning signal. This output is open drain.

Pin 3 - CI	Chassis Intrusion Input Active low input from an external circuit, which can be used to indicate a chassis intrusion event. This input line is connected directly to the ICH's System Management Interface's INTRUDER# input. It can be set to disable the system if the chassis is open or can be used as a general-purpose input if intruder detection is not used.
Pin 4 - OVT	Over Temperature This active low, open drain output can be used to indicate that an over-temperature condition exists.

PCI ETHERNET INTERFACES (DUAL)

The dual PCI Ethernet interfaces are implemented using an Intel 82546EB Ethernet controller with two channels. These interfaces support Gigabit, 10Base-T and 100Base-TX Fast Ethernet modes. The interfaces are compliant with IEEE 802.3 and PCI Local Bus 2.1 Specifications.

The main components of each interface are:

- Intel 82546EB for 10/100/1000-Mb/s media access control (MAC) with SYM, a serial ROM port and a PCI Bus Master interface
- Serial ROM for storing the Ethernet address and the interface configuration and control data
- Integrated RJ-45/Magnetics module connector on the SBC's I/O bracket for direct connection to the network. The connector requires a category 5 (CAT5) unshielded twisted-pair (UTP) 2-pair cable for a 100-Mb/s network connection or a category3 (CAT3) or higher UTP 2-pair cable for a 10-Mb/s network connection. A category 5e (CAT5e) or higher UTP 2-pair cable is recommended for a 1000-Mb/s (Gigabit) network connection.
- Link status and activity LEDs on the I/O bracket for status indication (See *Ethernet LEDs and Connectors* later in this chapter.)

Software drivers are supplied for most popular operating systems.

HUB INTERFACE

The E7501 chipset utilizes a dedicated hub interface connection between the E7501 memory controller hub (MCH) and the I/O controller hub (ICH3). The purpose of the E7501 hub interface is to provide efficient, high-speed communication between chipset components in order to support high-speed I/O applications. It is a parity-protected, 1GB/s point-to-point hub interface and uses an 8-bit 66MHz base clock running at 8x.

PCI SCSI INTERFACES (DUAL)

The SCSI interfaces support Ultra320 SCSI data transfer using Adaptec's AIC-7902 SCSI controller, which supports SCSI data transfer up to 320MB per second. The interfaces support up to 15 SCSI devices, comply with the SPI-3 standard and are compatible with both single-ended and Low Voltage Differential (LVD) SCSI I/O.

Active termination is provided with terminator voltage protected by a self-resetting fuse. Jumpers are provided to disable the termination for Channels 0 and 1 (see the *Configuration Jumpers* section later in this chapter). Software drivers are available for most popular operating systems.

The Adaptec SCSISelect Configuration Utility allows you to view and/or change the default configuration settings for the Ultra320 SCSI adapter. You may press **<Ctrl> + <A>** to invoke the configuration utility.

PCI ENHANCED IDE INTERFACES (DUAL)

Dual high performance PCI Bus Master EIDE interfaces are capable of supporting two IDE disk drives each in a master/slave configuration. The interfaces support Ultra ATA/100 with synchronous ATA mode transfers up to 100MB per second. Ultra ATA/100 cables must be used with Ultra ATA/100 drives.

FLOPPY DRIVE INTERFACE

The SBC supports two floppy disk drives. Drives can be 360K to 2.88MB, in any combination.

SERIAL INTERFACE

Two high-speed FIFO (16C550) serial ports with independently programmable baud rates are supported. The IRQ for each serial port has BIOS selectable addressing.

ENHANCED PARALLEL INTERFACE

The SBC provides a PC/AT compatible bidirectional parallel port and supports enhanced parallel port (EPP) mode and extended capabilities port (ECP) mode. The ECP mode is IEEE 1284 compliant. The IRQ for the parallel port has BIOS selectable addressing.

PS/2 MOUSE INTERFACE

The SBC is compatible with a PS/2-type mouse. The mouse connection can be made by using either the PS/2 mouse header or the bracket mounted mouse/keyboard mini DIN connector. The mouse may be connected directly to the mini DIN connector or to the "mouse" side of the "Y" adapter. Mouse voltage is protected by a self-resetting fuse.

KEYBOARD INTERFACE

The SBC is compatible with an AT-type keyboard. The keyboard connection can be made by using either the keyboard header or the "keyboard" side of the "Y" adapter plugged into the bracket mounted mouse/keyboard mini DIN connector. Keyboard voltage is protected by a self-resetting fuse.

WATCHDOG TIMER

The watchdog timer is a hardware timer which resets the SBC if the timer is not refreshed by software periodically. The timer is typically used to restart a system in which an application becomes hung on an external event. When the application is hung, it no longer refreshes the timer. The watchdog timer then times out and resets the SBC.

The watchdog timer has programmable timeout periods of 30 mseconds, 10 seconds or 60 seconds. When enabled, the watchdog timer generates a system reset by deactivating the Power Good signal. Watchdog timer control is supplied via the ICH3 General Purpose I/O pins. The state of these GPIO signals are controlled by the GPIO Level Input or Output Register (GP_LVL). This 32-bit register is located at offset 0C(h) in the General Purpose I/O space at base address 500(h). Bits 19, 20 and 23 of this register are used for watchdog timer control. The register can also be accessed in byte mode; bits 23-16 reside at I/O address 50E(h).

The GP_LVL bit definitions are as follows:

Bit 19 - Watchdog Input (WDI)

When the watchdog timer is enabled, this bit must be toggled (0 to 1 or 1 to 0) within the selected watchdog timeout period. Failure to do so results in a system reset. This function is controlled by bit 19 of the GP_LVL register.

Bits 20 and 23 - Watchdog Select 0/Watchdog Select 1 (WDS0/WDS1)

These two bits of the GP_LVL register select the watchdog timeout period.

Timeout period options are as follows:

WDS1	WDS0	Timeout Period
0	0	30 mseconds
0	1	Disabled (power-on default)
1	0	10 seconds
1	1	60 seconds

The Watchdog Input (WDI) bit should be toggled immediately prior to changing the timeout period. Once the WDS1 and WDS0 bits have been set to select the desired timeout period, the WDI bit must be toggled within the selected period.

A set of watchdog timer software code and sample programs are available from Technical Support.

THERMAL MONITOR

The SBC's processor has a built-in thermal monitor feature designed to prevent processor failure at elevated operating temperature. The thermal monitor consists of an on-die temperature sensor and a fast-acting thermal control circuit (TCC).

The actual TCC activation point in a specific SBC application may vary as a function of processor loading, system case design, SBC location within a case and other factors. Critical temperature is determined by the processor and cannot be altered by the user.

When the TCC activates, the SBC's Thermal Throttling Activity LED turns on. Depending on the setting of the Thermal Throttling Activity LED jumper (JU6), the LED either goes off after the processor returns to normal temperature or remains on in a latched state to indicate that the processor's TCC has activated at least once. (See the *Configuration Jumpers* section later in this chapter for further explanation of the Thermal Throttling Activity LED jumper.)

Under normal operating conditions, the SBC's active cooling system generally prevents the TCC from activating.

COOLING FAN

A temperature switch mounted on the processor board near the I/O bracket monitors temperature and changes the fan speed based on sensed temperature. If the switch registers a temperature of 50° C., 12 volts is applied to the fan, causing the fan to operate at its maximum speed of 50CFM. For temperatures of less than 48° C., 8.7 volts is applied to the fan. This reduction in fan voltage causes the fan to operate at a much lower speed, ensuring proper SBC cooling and efficient cooling fan operation.

POWER FAIL DETECTION

A hardware reset is issued when any of the monitored voltages drops below its specified nominal low voltage limit.

The monitored voltages and their nominal low limits are listed below.

Monitored Voltage	Nominal Low Limit	Voltage Source
+5V	4.5 volts	System Power Supply
+3.3V	2.97 volts	System Power Supply
+1.2V	1.056 volts	On-Board Regulator
+1.25V	1.1 volt	On-Board Regulator
+2.5V	2.452 volts	On-Board Regulator

BATTERY

A built-in lithium battery is provided, for ten years of data retention for CMOS memory.

CAUTION: There is a danger of explosion if the battery is incorrectly replaced. Replace it only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

POWER REQUIREMENTS

The following are typical values:

Processor Speed	+5V *	+12V **	+3.3V *	-12V *
2.8GHz	4.10 Amps	13.15 Amps	1.41 Amps	< 100 mAmps
2.4GHz	4.10 Amps	9.90 Amps	1.40 Amps	< 100 mAmps
2.0GHz	3.80 Amps	8.20 Amps	1.10 Amps	< 100 mAmps

* From backplane via PICMG connector.
** From ATX12V power supply or equivalent via P24 connector.

NOTE: The XPT requires an *additional* on-board power connector due to the power requirements of the Intel® Xeon™ processor. This 4-pin connector (P24) *requires* +12V from an external power supply that conforms to the ATX12V power specification. The external power supply *must* have a wattage rating of 250W or higher. The XPT also requires that +3.3V be applied to the backplane from the power supply.

TEMPERATURE/ ENVIRONMENT

Operating Temperature: 0° C. to 45° C.

Storage Temperature: - 40° C. to 70° C.

Humidity: 5% to 90% non-condensing

UL RECOGNITION

This SBC is a UL recognized product listed in file #E208896.

This board was investigated and determined to be in compliance under the Bi-National Standard for Information Technology Equipment. This included the Electrical Business Equipment, UL 1950, Third Edition, and CAN/CSA C22.22 No. 950-95.

CONFIGURATION JUMPERS

The setup of the configuration jumpers on the SBC is described below. * indicates the default value of each jumper.

NOTE: For two-position jumpers (3-post), "RIGHT" is toward the bracket end of the board; "LEFT" is toward the memory sockets.

XPT PROCESSOR BOARD:

Jumper	Description
JU6	**Thermal Throttling Activity LED**

If the processor core gets to a critical temperature, it slows itself down to half its normal speed. This jumper sets the way in which the LED displays in response to this self-limiting mode.

Install for real-time activity. The LED lights only when the processor is operating in slow-power mode. *

Remove for latched activity. The LED lights and stays on once the processor has gone into slow-power mode.

NOTE: Critical temperature is determined by the processor and cannot be altered by the user.

XPT I/O BOARD:

Jumper	Description
JU1/JU2	**System Flash ROM Operational Modes**

The Flash ROM has two programmable sections: the Boot Block for “flashing” in the BIOS and the Main Block for the executable BIOS and PnP parameters. Normally only the Main Block is updated when a new BIOS is flashed into the system.

	JU1	JU2
All Blocks Write Enabled	Remove *	Remove *
Boot Block Write Protected	Install	Remove
Block 2-16 Write Protected	Remove	Install

JU8 **Password Clear**

Install for one power-up cycle to reset the password to the default (null password).
Remove for normal operation. *

CONFIGURATION JUMPERS (CONTINUED)

Jumper | Description

JU9/JU9A JU9B **SCSI Termination - Channel 0**

These three jumpers may be used to enable or disable on-board active termination for the Ultra320 SCSI interface - Channel 0.

	JU9	JU9A	JU9B
Enable active termination	Install*	Install*	Remove*
Disable active termination	Remove	Remove	Remove
Enable upper byte only	Remove	Install	Remove
Control via SCSI BIOS Utility	Remove	Remove	Install

JU12 **CMOS Clear**

Install on the RIGHT to clear.
Install on the LEFT to operate. *

NOTE: The CMOS Clear jumper works on power-up. To clear the CMOS, power down the system, install the jumper, then turn the power back on. Wait for at least two seconds and turn the power off. Then remove the jumper and turn the power on. When AMIBIOS displays the "CMOS Settings Wrong" message, press F1 to go into the BIOS Setup Utility, where you may reenter your desired BIOS settings, load optimal defaults or load failsafe defaults.

NOTE: If the CMOS settings are cleared, the processor may reset to the safe mode, resulting in a reduction in execution speed which affects overall system performance. After clearing CMOS, you should always check the operating speed and reset it if necessary. To reset the SBC to the correct operating speed, use the **Ratio CMOS Setting** option on the **CPU Configuration** screen. See the *Advanced Setup* chapter of this manual for further details.

JU20/JU20A JU20B **SCSI Termination - Channel 1**

These three jumpers may be used to enable or disable on-board active termination for the Ultra320 SCSI interface - Channel 1.

	JU20	JU20A	JU20B
Enable active termination	Install*	Install*	Remove*
Disable active termination	Remove	Remove	Remove
Enable upper byte only	Remove	Install	Remove
Control via SCSI BIOS Utility	Remove	Remove	Install

ETHERNET LEDS AND CONNECTORS

Each Ethernet interface has two LEDs for status indication and an RJ-45 network connector.

LED/Connector	Description
Activity LED	Green LED which indicates network activity. This is the lower LED on the LAN connector (i.e., toward the edge connectors).
Off	Indicates there is not a valid connection. Transmit and receive are not possible.
On (solid)	Indicates a link has successfully been established.
On (flashing)	Indicates network transmit or receive activity.
Speed LED	Yellow LED which identifies the connection speed. This is the upper LED on the LAN connector (i.e., toward the memory sockets).
Off	Indicates a 10Mb/s connection.
On (solid)	Indicates a 1000Mb/s connection.
On (flashing)	Indicates a 100Mb/s connection. The LED blinks twice per second.
RJ-45 Network Connector	The RJ-45 network connector requires a category 5 (CAT5) unshielded twisted-pair (UTP) 2-pair cable for a 100-Mb/s network connection or a category 3 (CAT3) or higher UTP 2-pair cable for a 10-Mb/s network connection. A category 5e (CAT5e) or higher UTP 2-pair cable is recommended for a 1000-Mb/s (Gigabit) network connection.

SYSTEM BIOS SETUP UTILITY

The System BIOS is an AMIBIOS with a ROM-resident setup utility. The BIOS Setup Utility allows you to select to the following categories of options:

- Main Menu
- Advanced Setup
- PCIPnP Setup
- Chipset Setup
- Boot Setup
- Security Setup
- Exit

Each of these options allows you to review and/or change various setup features of your system. Details are provided in the following chapters of this manual.

CONNECTORS

NOTE: Pin 1 on the connectors is indicated by the square pad on the PCB.

XPT PROCESSOR BOARD:

P2 - CPU Fan
3 pin single row header, Molex #22-23-2031

Pin	Signal
1	Gnd
2	+12V
3	FanTach

P18 - System Hardware Monitor Connector
4 pin single row header, Amp #640456-4

Pin	Signal
1	Gnd
2	GPO (General Purpose Output)
3	CI (Chassis Intrusion Input)
4	OVT (Over Temperature)

P19 - Auxiliary CPU Fan
3 pin single row header, Molex #22-23-2031

Pin	Signal
1	Gnd
2	+12V
3	FanTach

P24 - +12V VRM Power Input
4 pin mini-fit header, Molex #39-29-3046

Pin	Signal
1	Gnd
2	Gnd
3	+12V
4	+12V

CONNECTORS (CONTINUED)

XPT I/O BOARD:

P1 - 10/100/1000Base-T Ethernet Connectors - LAN1/LAN2
Dual RJ-45 connector, Amp/Tyco #1116353-4
Each individual RJ-45 connector is defined as follows:

Pin	Signal
1	TRP1+
2	TRP1-
3	TRP2+
4	TRP3+
5	TRP3-
6	TRP2-
7	TRP4+
8	TRP4-

P3 - Floppy Drive Connector
34 pin right angle connector, SAMTEC #ASP-104496-01

Pin	Signal	Pin	Signal
1	Gnd	2	N-RPM
3	Gnd	4	NC
5	Gnd	6	D-Rate0
7	Gnd	8	P-Index
9	Gnd	10	N-Motoron 1
11	Gnd	12	N-Drive Sel2
13	Gnd	14	N-Drive Sel1
15	Gnd	16	N-Motoron 2
17	Gnd	18	N-Dir
19	Gnd	20	N-Stop Step
21	Gnd	22	N-Write Data
23	Gnd	24	N-Write Gate
25	Gnd	26	P-Track 0
27	Gnd	28	P-Write Protect
29	Gnd	30	N-Read Data
31	Gnd	32	N-Side Select
33	Gnd	34	Disk Chng

P4A - Keyboard Header
5 pin single row header, Amp #640456-5

Pin	Signal
1	Kbd Clock
2	Kbd Data
3	Key
4	Kbd Gnd
5	Kbd Power (+5V fused) with self-resetting fuse

CONNECTORS (CONTINUED)

P5 - Speaker Port Connector
4 pin single row header, Amp #640456-4

Pin	Signal
1	Speaker Data
2	Key
3	Gnd
4	+5V

P6 - Serial Port 1 Connector
10 pin dual row header, Amp #103308-1

Pin	Signal	Pin	Signal
1	Carrier Detect	2	Data Set Ready-I
3	Receive Data-I	4	Request to Send-O
5	Transmit Data-O	6	Clear to Send-I
7	Data Terminal Ready-O	8	Ring Indicator-I
9	Signal Gnd	10	NC

P7 - Serial Port 2 Connector
10 pin dual row header, Amp #103308-1

Pin	Signal	Pin	Signal
1	Carrier Detect	2	Data Set Ready-I
3	Receive Data-I	4	Request to Send-O
5	Transmit Data-O	6	Clear to Send-I
7	Data Terminal Ready-O	8	Ring Indicator-I
9	Signal Gnd	10	NC

P8 - Parallel Port Connector
26 pin dual row header, Amp #103308-6

Pin	Signal	Pin	Signal
1	Strobe	2	Auto Feed XT
3	Data Bit 0	4	Error
5	Data Bit 1	6	Init
7	Data Bit 2	8	Slct In
9	Data Bit 3	10	Gnd
11	Data Bit 4	12	Gnd
13	Data Bit 5	14	Gnd
15	Data Bit 6	16	Gnd
17	Data Bit 7	18	Gnd
19	ACK	20	Gnd
21	Busy	22	Gnd
23	Paper End	24	Gnd
25	Slct	26	NC

CONNECTORS (CONTINUED)

P9 - PS/2 Mouse and Keyboard Connector
6 pin mini DIN, Singatron #2MJ-204-16000

Pin	Signal
1	Ms Data
2	Kbd Data
3	G nd
4	Power (+5V fused) with self-resetting fuse
5	Ms Clock
6	Kbd Clock

P9A - PS/2 Mouse Header
6 pin single row header, Amp #640456-6

Pin	Signal
1	Ms Data
2	Reserved
3	Gnd
4	Power (+5V fused) with self-resetting fuse
5	Ms Clock
6	Reserved

P10 - External Reset Connector
2 pin single row header, Amp #640456-2

Pin	Signal
1	External Reset In (Low Active)
2	Gnd

P11 - Primary IDE Hard Drive Connector
40 pin dual row header, 3M #30340-6002HB

Pin	Signal	Pin	Signal
1	Reset	2	Gnd
3	Data 7	4	Data 8
5	Data 6	6	Data 9
7	Data 5	8	Data 10
9	Data 4	10	Data 11
11	Data 3	12	Data 12
13	Data 2	14	Data 13
15	Data 1	16	Data 14
17	Data 0	18	Data 15
19	Gnd	20	NC
21	DRQ 0	22	Gnd
23	IOW	24	Gnd
25	IOR	26	Gnd
27	IORDY	28	SELPDP
29	DACK 0	30	Gnd

CONNECTORS (CONTINUED)

P11 - Primary IDE Hard Drive Connector (continued)

Pin	Signal	Pin	Signal
31	IRQ 14	32	NC
33	Add 1	34	PCBL DET *
35	Add 0	36	Add 2
37	CS 1P	38	CS 3P
39	IDEACTP	40	Gnd

* For ATA/66 and ATA/100 drives, which should be set for Cable Select for proper speed operation. If other drives are detected, pin definition is Gnd.

P11A - Secondary IDE Hard Drive Connector
40 pin dual row header, 3M #30340-6002HB

Pin	Signal	Pin	Signal
1	Reset	2	Gnd
3	Data 7	4	Data 8
5	Data 6	6	Data 9
7	Data 5	8	Data 10
9	Data 4	10	Data 11
11	Data 3	12	Data 12
13	Data 2	14	Data 13
15	Data 1	16	Data 14
17	Data 0	18	Data 15
19	Gnd	20	NC
21	DRQ 1	22	Gnd
23	IOW	24	Gnd
25	IOR	26	Gnd
27	IORDY	28	SELPDS
29	DACK 1	30	Gnd
31	IRQ 15	32	NC
33	Add 1	34	SCBL DET *
35	Add 0	36	Add 2
37	CS 1S	38	CS 3S
39	IDEACTS	40	Gnd

* For ATA/66 and ATA/100 drives, which should be set for Cable Select for proper speed operation. If other drives are detected, pin definition is Gnd.

P12 - Hard Drive LED Connector
4 pin single row header, Amp #640456-4

Pin	Signal
1	LED +
2	LED -
3	LED -
4	LED +

CONNECTORS (CONTINUED)

P13 - SCSI Connector - Channel 0
68 pin "D" right angle connector, Amp/Tyco #3-174682-7

Pin	Signal	Pin	Signal
1	SCD12	35	SCD#12
2	SCD13	36	SCD#13
3	SCD14	37	SCD#14
4	SCD15	38	SCD#15
5	SCDPH	39	SCDPH#
6	SCD0	40	SCD#0
7	SCD1	41	SCD#1
8	SCD2	42	SCD#2
9	SCD3	43	SCD#3
10	SCD4	44	SCD#4
11	SCD5	45	SCD#5
12	SCD6	46	SCD#6
13	SCD7	47	SCD#7
14	SCDPL	48	SCDPL#
15	Gnd	49	Gnd
16	DIFSENSE	50	Gnd
17	TERMPWR	51	TERMPWR
18	TERMPWR	52	TERMPWR
19	NC	53	NC
20	Gnd	54	Gnd
21	SCATN	55	SCATN#
22	Gnd	56	Gnd
23	SCBSY	57	SCBSY#
24	SCACK	58	SCACK#
25	SCRST	59	SCRST#
26	SCMSG	60	SCMSG#
27	SCSEL	61	SCSEL#
28	SCCD	62	SCCD#
29	SCREQ	63	SCREQ#
30	SCIO	64	SCIO#
31	SCD8	65	SCD#8
32	SCD9	66	SCD#9
33	SCD10	67	SCD#10
34	SCD11	68	SCD#11

P14 - SCSI Connector - Channel 1
68 pin "D" right angle connector, Amp/Tyco #3-174682-7

Pin	Signal	Pin	Signal
1	SCD12	35	SCD#12
2	SCD13	36	SCD#13
3	SCD14	37	SCD#14
4	SCD15	38	SCD#15
5	SCDPH	39	SCDPH#
6	SCD0	40	SCD#0
7	SCD1	41	SCD#1

CONNECTORS (CONTINUED)

P14 - SCSI Connector - Channel 1 (continued)

Pin	Signal	Pin	Signal
8	SCD2	42	SCD#2
9	SCD3	43	SCD#3
10	SCD4	44	SCD#4
11	SCD5	45	SCD#5
12	SCD6	46	SCD#6
13	SCD7	47	SCD#7
14	SCDPL	48	SCDPL#
15	Gnd	49	Gnd
16	DIFSENSE	50	Gnd
17	TERMPWR	51	TERMPWR
18	TERMPWR	52	TERMPWR
19	NC	53	NC
20	Gnd	54	Gnd
21	SCATN	55	SCATN#
22	Gnd	56	Gnd
23	SCBSY	57	SCBSY#
24	SCACK	58	SCACK#
25	SCRST	59	SCRST#
26	SCMSG	60	SCMSG#
27	SCSEL	61	SCSEL#
28	SCCD	62	SCCD#
29	SCREQ	63	SCREQ#
30	SCIO	64	SCIO#
31	SCD8	65	SCD#8
32	SCD9	66	SCD#9
33	SCD10	67	SCD#10
34	SCD11	68	SCD#11

P15 - Video Interface Connector

15 pin connector, Amp #1-1470250-3

Pin	Signal	Pin	Signal	Pin	Signal
		6	Gnd		
1	Red			11	NC
		7	Gnd		
2	Green			12	EEDI
		8	Gnd		
3	Blue			13	HSYNC
		9	+5V		
4	NC			14	VSYNC
		10	Gnd		
5	Gnd			15	EECS

CONNECTORS (CONTINUED)

P17 - Universal Serial Bus (USB) Connector
8 pin dual row header, Molex #702-46-0821
(+5V fused with self-resetting fuses)

Pin	Signal	Pin	Signal
1	+5V-USB0	2	+5V-USB1
3	USB0-	4	USB1-
5	USB0+	6	USB1+
7	Gnd-USB0	8	Gnd-USB1

P17A - Universal Serial Bus (USB) Connector
USB vertical connector, Molex #67-329-0000
(+5V fused with self-resetting fuse)

Pin	Signal
1	+5V-USB1
2	USB1-
3	USB1+
4	Gnd-USB1

P17B - Universal Serial Bus (USB) Connector
USB vertical connector, Molex #67-329-0000
(+5V fused with self-resetting fuse)

Pin	Signal
1	+5V-USB0
2	USB0-
3	USB0+
4	Gnd-USB0

P21 - Power Good LED
2 pin single row header, Amp #640456-2

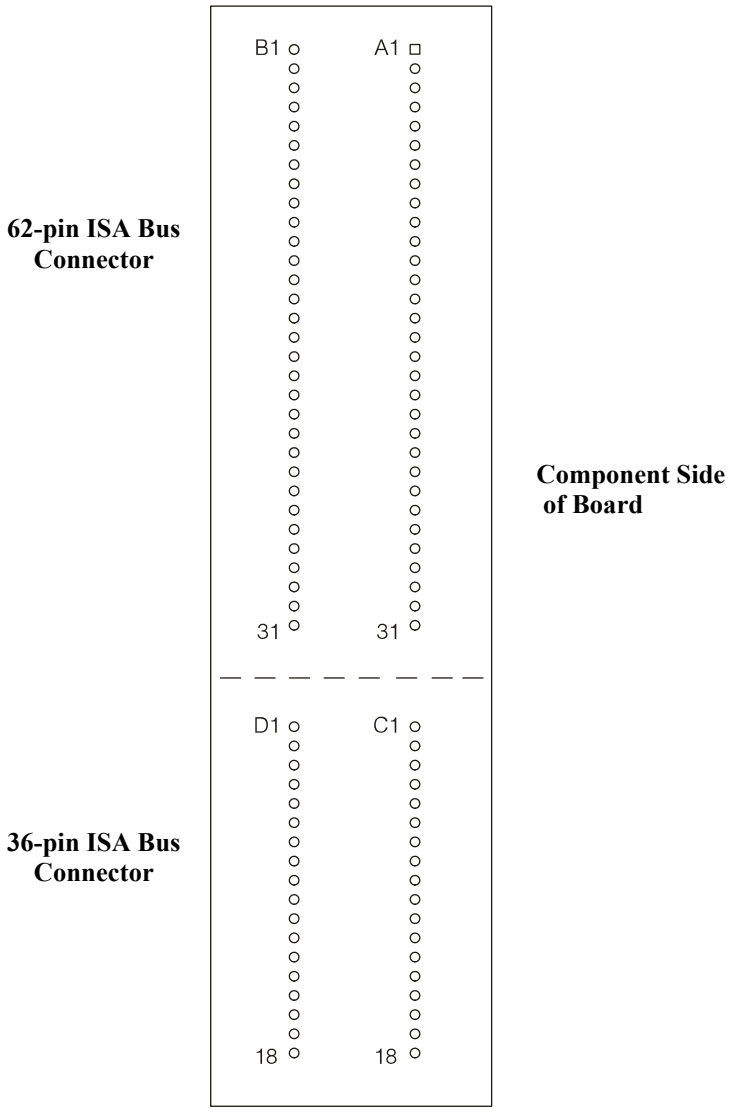
Pin	Signal
1	LED -
2	LED +

P22 - System Management Bus Connector
2 pin single row header, Amp #640456-2

Pin	Signal
1	SMB Clock
2	SMB Data

Chapter 2 ISA/PCI Reference

ISA BUS PIN NUMBERING



ISA Bus Pin Assignments

The following tables summarize pin assignments for the Industry Standard Architecture (ISA) Bus connectors.

I/O Pin	Signal Name	I/O	I/O Pin	Signal Name	I/O
A1	IOCHK#	I	B1	Gnd	Ground
A2	D7	I/O	B2	RESDRV	O
A3	D6	I/O	B3	+5V	Power
A4	D5	I/O	B4	IRQ9	I
A5	D4	I/O	B5	-5V	Power
A6	D3	I/O	B6	DRQ2	I
A7	D2	I/O	B7	-12V	Power
A8	D1	I/O	B8	NOWS#	I
A9	D0	I/O	B9	+12V	Power
A10	CHRDY	I	B10	Gnd	Ground
A11	AEN	O	B11	SMWTC#	O
A12	SA19	I/O	B12	SMRDC#	O
A13	SA18	I/O	B13	IOWC#	I/O
A14	SA17	I/O	B14	IORC#	I/O
A15	SA16	I/O	B15	DAK3#	O
A16	SA15	I/O	B16	DRQ3	I
A17	SA14	I/O	B17	DAK1#	O
A18	SA13	I/O	B18	DRQ1	I
A19	SA12	I/O	B19	REFRESH#	I/O
A20	SA11	I/O	B20	BCLK	O
A21	SA10	I/O	B21	IRQ7	I
A22	SA9	I/O	B22	IRQ6	I
A23	SA8	I/O	B23	IRQ5	I
A24	SA7	I/O	B24	IRQ4	I
A25	SA6	I/O	B25	IRQ3	I
A26	SA5	I/O	B26	DAK2#	O
A27	SA4	I/O	B27	T-C	O
A28	SA3	I/O	B28	BALE	O
A29	SA2	I/O	B29	+5V	Power
A30	SA1	I/O	B30	OSC	O
A31	SA0	I/O	B31	Gnd	Ground

I/O Pin	Signal Name	I/O	I/O Pin	Signal Name	I/O
C1	SBHE#	I/O	D1	M16#	I
C2	LA23	I/O	D2	IO16#	I
C3	LA22	I/O	D3	IRQ10	I
C4	LA21	I/O	D4	IRQ11	I
C5	LA20	I/O	D5	IRQ12	I
C6	LA19	I/O	D6	IRQ15	I
C7	LA18	I/O	D7	IRQ14	I
C8	LA17	I/O	D8	DAK0#	O
C9	MRDC#	I/O	D9	DRQ0	I
C10	MWTC#	I/O	D10	DAK5#	O
C11	D8	I/O	D11	DRQ5	I
C12	D9	I/O	D12	DAK6#	O
C13	D10	I/O	D13	DRQ6	I
C14	D11	I/O	D14	DAK7#	O
C15	D12	I/O	D15	DRQ7	I
C16	D13	I/O	D16	+5V	Power
C17	D14	I/O	D17	Master16#	I
C18	D15	I/O	D18	Gnd	Ground

ISA BUS SIGNAL DESCRIPTIONS

The following is a description of the ISA Bus signals. All signal lines are TTL-compatible.

AEN (O)

Address Enable (AEN) is used to degate the microprocessor and other devices from the I/O channel to allow DMA transfers to take place. When this line is active, the DMA controller has control of the address bus, the data-bus Read command lines (memory and I/O), and the Write command lines (memory and I/O).

BALE (O) (Buffered)

Address Latch Enable (BALE) is provided by the bus controller and is used on the system board to latch valid addresses and memory decodes from the microprocessor. It is available to the I/O channel as an indicator of a valid microprocessor or DMA address (when used with AEN). Microprocessor addresses SA[19::0] are latched with the falling edge of BALE. BALE is forced high during DMA cycles.

BCLK (O)

BCLK is the system clock. The clock has a 50% duty cycle. This signal should only be used for synchronization. It is not intended for uses requiring a fixed frequency.

CHRDY (I)

I/O Channel Ready (CHRDY) is pulled low (not ready) by a memory or I/O device to lengthen I/O or memory cycles. Any slow device using this line should drive it low immediately upon detecting its valid address and a Read or Write command. Machine cycles are extended by an integral number of clock cycles. This signal should be held low for no more than 2.5 micro-seconds.

D[15::0] (I/O)

Data signals D[15::0] provide bus bits 15 through 0 for the microprocessor, memory, and I/O devices. D15 is the most-significant bit and D0 is the least-significant bit. All 8-bit devices on the I/O channel should use D[7::0] for communications to the microprocessor. The 16-bit devices will use D[15::0]. To support 8-bit devices, the data on D[15::8] will be gated to D[7::0] during 8-bit transfers to these devices. 16-bit microprocessor transfers to 8-bit devices will be converted to two 8-bit transfers.

DAK[7::5]#, DAK[3::0]# (O)

DMA Acknowledge DAK[7::5]# and DAK[3::0]# are used to acknowledge DMA requests DRQ[7::5] and DRQ[3::0]. They are active low.

DRQ[7::5], DRQ[3::0] (I)

DMA Requests DRQ[7::5] and DRQ[3::0] are asynchronous channel requests used by peripheral devices and the I/O channel microprocessors to gain DMA service (or control of the system). They are prioritized, with DRQ0 having the highest priority and DRQ7 having the lowest. A request is generated by bringing a DRQ line to an active level. A DRQ line must be held high until the corresponding DMA Request Acknowledge (DAK) line goes active. DRQ[3::0] will perform 8-bit DMA transfers; DRQ[7::5] will perform 16-bit transfers.

IO16# (I)

I/O 16-bit Chip Select (IO16#) signals the system board that the present data transfer is a 16-bit, 1 wait-state, I/O cycle. It is derived from an address decode. IO16# is active low and should be driven with an open collector or tri-state driver capable of sinking 20 mAmps.

IOCHK# (I)

I/O Channel Check (IOCHK#) provides the system board with parity (error) information about memory or devices on the I/O channel. When this signal is active, it indicates an uncorrectable system error.

IORC# (I/O)

I/O Read (IORC#) instructs an I/O device to drive its data onto the data bus. It may be driven by the system microprocessor or DMA controller, or by a microprocessor or DMA controller resident on the I/O channel. This signal is active low.

IOWC# (I/O)

I/O Write (IOWC#) instructs an I/O device to read the data on the data bus. It may be driven by any microprocessor or DMA controller in the system. This signal is active low.

IRQ[15::14], IRQ[12::9], IRQ[7::3] (I)

Interrupt Requests IRQ[15::14], IRQ[12::9] and IRQ[7::3] are used to signal the microprocessor that an I/O device needs attention. The interrupt requests are prioritized, with IRQ[15::14] and IRQ[12::9] having the highest priority (IRQ9 is the highest) and IRQ[7::3] having the lowest priority (IRQ7 is the lowest). An interrupt request is generated when an IRQ line is raised from low to high. The line must be held high until the microprocessor acknowledges the interrupt request (Interrupt Service routine).

LA[23::17] (I/O)

These signals (unlatched) are used to address memory and I/O devices within the system. They give the system up to 16MB of addressability. These signals are valid when BALE is high. LA[23::17] are not latched during microprocessor cycles and therefore do not stay valid for the whole cycle. Their purpose is to generate memory decodes for 1 wait-state memory cycles. These decodes should be latched by I/O adapters on the falling edge of BALE. These signals also may be driven by other microprocessors or DMA controllers that reside on the I/O channel.

M16# (I)

M16# Chip Select signals the system board if the present data transfer is a 1<N>wait-state, 16-bit, memory cycle. It must be derived from the decode of LA[23::17]. M16# should be driven with an open collector or tri-state driver capable of sinking 20 mAmps.

Master16# (I)

Master16# is used with a DRQ line to gain control of the system. A processor or DMA controller on the I/O channel may issue a DRQ to a DMA channel in cascade mode and receive a DAK#. Upon receiving the DAK#, an I/O microprocessor may pull Master16# low, which will allow it to control the system address, data, and control lines (a condition known as tri-state). After Master16# is low, the I/O microprocessor must wait one system clock period before driving the address and data lines, and two clock periods before issuing a Read or Write command. If this signal is held low for more than 15<N>microseconds, system memory may be lost because of a lack of refresh.

NOWS# (I)

The No Wait State (NOWS#) signal tells the microprocessor that it can complete the present bus cycle without inserting any additional wait cycles. In order to run a memory cycle to a 16-bit device without wait cycles, NOWS# is derived from an address decode gated with a Read or Write command. In order to run a memory cycle to an 8-bit device with a minimum of two wait states, NOWS# should be driven active on system clock after the Read or Write command is active gated with the address decode for the device. Memory Read and Write commands to a 8-bit device are active on the falling edge of the system clock. NOWS# is active low and should be driven with an open collector or tri-state driver capable of sinking 20 mAmps.

OSC (O)

Oscillator (OSC) is a high-speed clock with a 70-nanosecond period (14.31818 MHz). This signal is not synchronous with the system clock. It has a 50% duty cycle.

REFRESH# (I/O)

The REFRESH# signal is used to indicate a refresh cycle and can be driven by a microprocessor on the I/O channel.

RESDRV (O)

Reset Drive (RESDRV) is used to reset or initialize system logic at power-up time or during a low line-voltage outage. This signal is active high.

SA[19::0] (I/O)

Address bits SA[19::0] are used to address memory and I/O devices within the system. These twenty address lines, in addition to LA[23::17], allow access of up to 16MB of memory. SA[19::0] are gated on the system bus when BALE is high and are latched on the falling edge of BALE. These signals are generated by the microprocessor or DMA Controller. They also may be driven by other microprocessors or DMA controllers that reside on the I/O channel.

SBHE# (I/O)

System Bus High Enable (SBHE#) indicates a transfer of data on the upper byte of the data bus, D[15::8]. 16-bit devices use SBHE# to condition data bus buffers tied to D[15::8].

SMRDC# (O), MRDC# (I/O)

These signals instruct the memory devices to drive data onto the data bus. SMRDC# is active only when the memory decode is within the low 1MB of memory space. MRDC# is active on all memory read cycles. MRDC# may be driven by any microprocessor or DMA controller in the system. SMRDC is derived from MRDC# and the decode of the low 1MB of memory. When a microprocessor on the I/O channel wishes to drive MRDC#, it must have the address lines valid on the bus for one system clock period before driving MRDC# active. Both signals are active low.

SMWTC# (O), MWTC# (I/O)

These signals instruct the memory devices to store the data present on the data bus. SMWTC# is active only when the memory decode is within the low 1MB of the memory space. MWTC# is active on all memory write cycles. MWTC# may be driven by any microprocessor or DMA controller in the system. SMWTC# is derived from MWTC# and the decode of the low 1MB of memory. When a microprocessor on the I/O channel wishes to drive MWTC#, it must have the address lines valid on the bus for one system clock period before driving MWTC# active. Both signals are active low.

T-C (O)

Terminal Count (T-C) provides a pulse when the terminal count for any DMA channel is reached.

I/O ADDRESS MAP*

Hex Range	Device
000-01F	DMA Controller 1
020-03F	Interrupt Controller 1, Master
040-05F	Timer
060-06F	8042 (Keyboard)
070-07F	Realtime Clock, NMI (non-maskable interrupt) Mask
080-09F	DMA Page Register
0A0-0BF	Interrupt Controller 2
0C0-0DF	DMA Controller 2
0F0	Clear Math Coprocessor Busy
0F1	Reset Math Coprocessor
0F8-0FF	Math Coprocessor
1F0-1F8	Fixed Disk
200-207	Game I/O
278-27F	Parallel Printer Port 2
2F8-2FF	Serial Port 2
300-31F	Prototype Card
360-36F	Reserved
378-37F	Parallel Printer Port 1
380-38F	SDLC, Bisynchronous 2
3A0-3AF	Bisynchronous 1
3B0-3BF	Monochrome Display and Printer Adapter
3C0-3CF	Reserved
3D0-3DF	Color/Graphics Monitor Adapter
3F0-3F7	Diskette Controller
3F8-3FF	Serial Port 1

INTERRUPT ASSIGNMENTS*

Interrupt	Description
IRQ0	Timer Output 0
IRQ1	Keyboard (Output Buffer Full)
IRQ2	Interrupt 8 through 15
IRQ3	erial Port 2
IRQ4	Serial Port 1
IRQ5	Parallel Port 2
IRQ6	Diskette Controller
IRQ7	Parallel Port 1
IRQ8	Realtime Clock Interrupt
IRQ9	Software Redirected to INT 0AH (IRQ2)
IRQ10	Unassigned
IRQ11	Unassigned
IRQ12	PS/2 Mouse
IRQ13	Coprocessor
IRQ14	Fixed Disk Controller
IRQ15	Unassigned (may be assigned by the system to the secondary IDE)

* These are typical parameters, which may not reflect your current system.

PCI LOCAL BUS OVERVIEW

The PCI (Peripheral Component Interconnect) Local Bus is a high performance, 32-bit or 64-bit bus with multiplexed address and data lines. It is intended for use as an interconnect mechanism between highly integrated peripheral controller components, peripheral add-in boards and processor/memory systems.

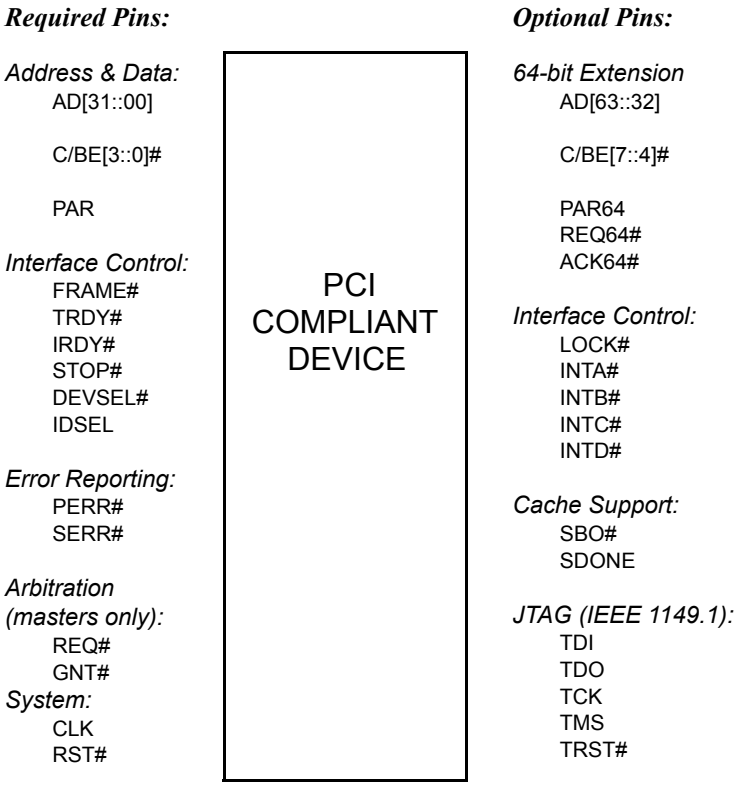
The "local bus" moves peripheral functions with high bandwidth requirements closer to the system's processor bus and can produce substantial performance gains with graphical user interfaces (GUI's) and other high bandwidth functions (i.e., full motion video, SCSI, LAN's, etc.).

The PCI Local Bus accommodates future system requirements and is applicable across multiple platforms and architectures.

The PCI component and add-in card interface is processor independent, enabling an efficient transition to future processor generations, by bridges or by direct integration, and use with multiple processor architectures. Processor independence allows the PCI Local Bus to be optimized for I/O functions, enables concurrent operation of the local bus with the processor/memory subsystem, and accommodates multiple high performance peripherals in addition to graphics. Movement to enhanced video and multimedia displays and other high bandwidth I/O will continue to increase local bus bandwidth requirements. A transparent 64-bit extension of the 32-bit data and address buses is defined, doubling the bus bandwidth and offering forward and backward compatibility of 32-bit (132MB/s peak) and 64-bit (264MB/s peak) PCI Local Bus peripherals.

PCI LOCAL BUS SIGNAL DEFINITION

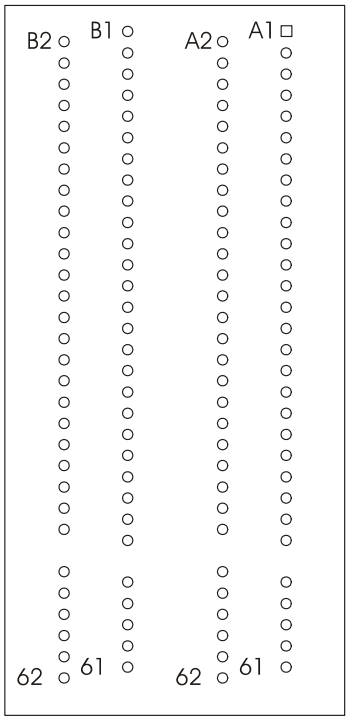
The PCI interface requires a minimum of 47 pins for a target-only device and 49 pins for a master to handle data and addressing, interface control, arbitration and system functions. The diagram below shows the pins in functional groups, with required pins on the left side and optional pins on the right side.



PCI Pin List

PCI LOCAL BUS PIN NUMBERING

Component Side of Board



5-volt/32-bit PCI Connector

PCI Local Bus Pin Assignments

The PCI Local Bus pin assignments shown below are for the PCI option slots on the backplane.

The PCI Local Bus specifies both 5-volt and 3.3-volt signaling environments. The following bus pin assignments are for the 5-volt connector. The 3.3-volt connector bus pin assignments are the same with the following exceptions:

* The pins noted as +V (I/O) are +5 volts or +3.3 volts, depending on which connector is being used.

† Pins B12, B13, A12 and A13 are Gnd (ground) on the 5-volt connector, but are Connector Keys on the 3.3-volt connector.

†† Pin B49 is Gnd (ground) on the 5-volt connector, but is M66EN on the 3.3-volt connector.

††† Pins B50, B51, A50 and A51 are Connectors Keys on the 5-volt connector, but are Gnd (ground) on the 3.3-volt connector.

I/O Pin	Signal Name	I/O Pin	Signal Name	
B1	-12V	A1	TRST#	32-bit connector
B2	TCK	A2	+12V	
B3	Gnd	A3	TMS	
B4	TDO	A4	TDI	
B5	+5V	A5	+5V	
B6	+5V	A6	INTA#	
B7	INTB#	A7	INTC#	
B8	INTD#	A8	+5V	
B9	PRSNT1#	A9	Reserved	
B10	Reserved	A10	+V (I/O) *	
B11	PRSNT2#	A11	Reserved	
B12	Gnd †	A12	Gnd †	
B13	Gnd †	A13	Gnd †	
B14	Reserved	A14	Reserved	
B15	Gnd	A15	RST#	
B16	CLK	A16	+V (I/O) *	
B17	Gnd	A17	GNT#	
B18	REQ#	A18	Gnd	
B19	+V (I/O) *	A19	Reserved	
B20	AD31	A20	AD30	
B21	AD29	A21	+3.3V	
B22	Gnd	A22	AD28	
B23	AD27	A23	AD26	
B24	AD25	A24	Gnd	
B25	+3.3V	A25	AD24	
B26	C/BE3#	A26	IDSEL	
B27	AD23	A27	+3.3V	
B28	Gnd	A28	AD22	
B29	AD21	A29	AD20	
B30	AD19	A30	Gnd	
B31	+3.3V	A31	AD18	
B32	AD17	A32	AD16	
B33	C/BE2#	A33	+3.3V	
B34	Gnd	A34	FRAME#	
B35	IRDY#	A35	Gnd	

PCI LOCAL BUS PIN ASSIGNMENTS (CONTINUED)

I/O Pin	Signal Name	I/O Pin	Signal Name	
B36	+3.3V	A36	TRDY#	
B37	DEVSEL#	A37	Gnd	
B38	Gnd	A38	STOP#	
B39	LOCK#	A39	+3.3V	
B40	PERR#	A40	SDONE	
B41	+3.3V	A41	SBO#	
B42	SERR#	A42	Gnd	
B43	+3.3V	A43	PAR	
B44	C/BE1#	A44	AD15	
B45	AD14	A45	+3.3V	
B46	Gnd	A46	AD13	
B47	AD12	A47	AD11	
B48	AD10	A48	Gnd	
B49	Gnd ††	A49	AD9	
B50	Connector Key †††	A50	Connector Key †††	5-volt key
B51	Connector Key †††	A51	Connector Key †††	5-volt key
B52	AD8	A52	C/BE0#	
B53	AD7	A53	+3.3V	
B54	+3.3V	A54	AD6	
B55	AD5	A55	AD4	
B56	AD3	A56	Gnd	
B57	Gnd	A57	AD2	
B58	AD1	A58	AD0	
B59	+V (I/O) *	A59	+V (I/O) *	
B60	ACK64#	A60	REQ64#	
B61	+5V	A61	+5V	
B62	+5V	A62	+5V	32-bit connector end

PCI LOCAL BUS PIN ASSIGNMENTS (CONTINUED)

The following pin assignments apply only to backplanes with 64-bit PCI option slots.

I/O Pin	Signal Name	I/O Pin	Signal Name	
	Connector Key		Connector Key	64-bit spacer
	Connector Key		Connector Key	64-bit spacer
B63	Reserved	A63	Gnd	64-bit connector start
B64	Gnd	A64	C/BE7#	
B65	C/BE6#	A65	C/BE5#	
B66	C/BE4#	A66	+V (I/O) *	
B67	Gnd	A67	PAR64	
B68	AD63	A68	AD62	
B69	AD61	A69	Gnd	
B70	+V (I/O) *	A70	AD60	
B71	AD59	A71	AD58	
B72	AD57	A72	Gnd	
B73	Gnd	A73	AD56	
B74	AD55	A74	AD54	
B75	AD53	A75	+V (I/O) *	
B76	Gnd	A76	AD52	
B77	AD51	A77	AD50	
B78	AD49	A78	Gnd	
B79	+V (I/O) *	A79	AD48	
B80	AD47	A80	AD46	
B81	AD45	A81	Gnd	
B82	Gnd	A82	AD44	
B83	AD43	A83	AD42	
B84	AD41	A84	+V (I/O) *	
B85	Gnd	A85	AD40	
B86	AD39	A86	AD38	
B87	AD37	A87	Gnd	
B88	+V (I/O) *	A88	AD36	
B89	AD35	A89	AD34	
B90	AD33	A90	Gnd	
B91	Gnd	A91	AD32	
B92	Reserved	A92	Reserved	
B93	Reserved	A93	Gnd	64-bit connector end
B94	Gnd	A94	Reserved	

PCI LOCAL BUS SIGNAL DESCRIPTIONS

The PCI Local Bus signals are described below and may be categorized into the following functional groups:

- System Pins
- Address and Data Pins
- Interface Control Pins
- Arbitration Pins (Bus Masters Only)
- Error Reporting Pins
- Interrupt Pins (Optional)
- Cache Support Pins (Optional)
- 64-Bit Bus Extension Pins (Optional)
- JTAG/Boundary Scan Pins (Optional)

A # symbol at the end of a signal name indicates that the active state occurs when the signal is at a low voltage. When the # symbol is absent, the signal is active at a high voltage.

The following are descriptions of the PCI Local Bus signals.

ACK64# (optional)

Acknowledge 64-bit Transfer, when actively driven by the device that has positively decoded its address as the target of the current access, indicates the target is willing to transfer data using 64bits. ACK64# has the same timing as DEVSEL#.

AD[31::00]

Address and Data are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. During the address phase, AD[31::00] contain a physical address (32 bits). During data phases, AD[07::00] contain the least significant byte (lsb) and AD[31::24] contain the most signficant byte (msb).

AD[63::32] (optional)

Address and Data are multiplexed on the same pins and provide 32additional bits. During an address phase (when using the DAC command and when REQ64# is asserted), the upper 32bits of a 64-bit address are transferred; otherwise, these bits are reserved but are stable and indeterminate. During a data phase, an additional 32bits of data are transferred when REQ64# and ACK64# are both asserted.

C/BE[3::0]#

Bus Command and Byte Enables are multiplexed on the same PCI pins. During the address phase of a transaction, these pins define the bus command; during the data phase they are used as byte enables. The byte enables are valid for the entire data phase and determine which byte lanes carry meaningful data. C/BE0# applies to byte0 (lsb) and C/BE3# applies to byte 3 (msb).

C/BE[7::4]# (optional)

Bus Command and Byte Enables are multiplexed on the same pins. During an address phase (when using the DAC command and when REQ64# is asserted), the actual bus command is transferred on C/BE[7::4]#; otherwise, these bits are reserved and indeterminate. During a data phase, C/BE[7::4]# are byte enables indicating which byte lanes carry meaningful data when REQ64# and ACK64# are both asserted. C/BE4# applies to byte4 and C/BE7# applies to byte7.

CLK

Clock provides timing for all transactions on PCI and is an input to every PCI device.

DEVSEL#

Device Select, when actively driven, indicates that the driving device has decoded its address as the target of the current access. As an input, DEVSEL# indicates whether any device on the bus has been selected.

FRAME#

Cycle Frame is an interface control pin which is driven by the current master to indicate the beginning and duration of an access. When FRAME# is asserted, data transfers continue; when it is deasserted, the transaction is in the final data phase.

GNT#

Grant indicates to the agent that access to the bus has been granted. This is a point to point signal. Every master has its own GNT#.

IDSEL

Initialization Device Select is used as a chip select during configuration read and write transactions.

INTA#, INTB#, INTC#, INTD# (optional)

Interrupts on PCI are optional and defined as "level sensitive," asserted low (negative true), using open drain output drivers. PCI defines one interrupt for a single function and up to four interrupt lines for a multi-function device or connector.

Interrupt A is used to request an interrupt. For a single function device, only INTA# may be used, while the other three interrupt lines have no meaning.

Interrupt B, Interrupt C and Interrupt D are used to request additional interrupts and only have meaning on a multi-function device.

IRDY#

Initiator Ready indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#. During a write, IRDY# indicates that valid data is present on AD[31::0]. During a read, it indicates that the master is prepared to accept data.

LOCK#

Lock indicates an operation that may require multiple transactions to complete. When LOCK# is asserted, non-exclusive transactions may proceed to an address that is not currently locked.

PAR

Parity is even parity across AD[31::00] and C/BE[3::0]#. Parity generation is required by all PCI agents. The master drives PAR for address and write data phases; the target drives PAR for read data phases.

PAR64 (optional)

Parity Upper DWORD is the even parity bit that protects AD[63::32] and C/BE[7::4]#. The master drives PAR64 for address and write data phases; the target drives PAR64 for read data phases.

PERR#

Parity Error is for the reporting of data parity errors during all PCI transactions except a Special Cycle. There are no special conditions when a data parity error may be lost or when reporting of an error may be delayed.

PRSNT1# and PRSNT2#

PRSNT1# and PRSNT2# are related to the connector only, not to other PCI components. They are used for two purposes: indicating that a board is physically present in the slot and providing information about the total power requirements of the board.

REQ#

Request indicates to the arbiter that this agent desires use of the bus. This is a point to point signal. Every master has its own REQ#.

REQ64# (optional)

Request 64-bit Transfer, when actively driven by the current bus master, indicates it desires to transfer data using 64 bits. REQ64# has the same timing as FRAME#. REQ64# has meaning at the end of reset.

RST#

Reset is used to bring PCI-specific registers, sequencers and signals to a consistent state.

SBO# (optional)

Snoop Backoff is an optional cache support pin which indicates a hit to a modified line when asserted. When SBO# is deasserted and SDONE is asserted, it indicates a "clean" snoop result.

SDONE (optional)

Snoop Done is an optional cache support pin which indicates the status of the snoop for the current access. When deasserted, it indicates the result of the snoop is still pending. When asserted, it indicates the snoop is complete.

SERR#

System Error is for reporting address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic. If an agent does not want a non-maskable interrupt (NMI) to be generated, a different reporting mechanism is required.

STOP#

Stop indicates that the current target is requesting the master to stop the current transaction.

TCK (optional)

Test Clock is used to clock state information and test data into and out of the device during operation of the TAP (Test Access Port).

TDI (optional)

Test Data Input is used to serially shift test data and test instructions into the device during TAP (Test Access Port) operation.

TDO (optional)

Test Data Output is used to serially shift test data and test instructions out of the device during TAP (Test Access Port) operation.

TMS (optional)

Test Mode Select is used to control the state of the TAP (Test Access Port) controller in the device.

TRDY#

Target Ready indicates the target agent's (selected device's) ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. During a read, TRDY# indicates that valid data is present on AD[31::00]. During a write, it indicates that the target is prepared to accept data.

TRST# (optional)

Test Reset provides an asynchronous initialization of the TAP controller. This signal is optional in the IEEE Standard Test Access Port and Boundary Scan Architecture.

PICMG Edge Connector Pin Assignments

The pin assignments shown below are for the PICMG portion of the edge connector on the processor board. These pin assignments match those of the PICMG connector of the processor slot on the backplane.

I/O Pin	Signal Name	I/O Pin	Signal Name	
B1	-12V	A1	NC	32-bit connector start
B2	NC	A2	+12V	
B3	Gnd	A3	NC	
B4	NC	A4	NC	
B5	+5V	A5	+5V	
B6	+5V	A6	INTA#	
B7	INTB#	A7	INTC#	
B8	INTD#	A8	+5V	
B9	REQ3#	A9	CLKS2	
B10	REQ1#	A10	+5V	
B11	GNT3#	A11	CLKS3	
B12	Gnd	A12	Gnd	
B13	Gnd	A13	Gnd	
B14	CLKS0	A14	GNT1#	
B15	Gnd	A15	RST#	
B16	CLKS1	A16	+5V	
B17	Gnd	A17	GNT0#	
B18	REQ0#	A18	Gnd	
B19	+5V	A19	REQ2#	
B20	AD31	A20	AD30	
B21	AD29	A21	NC	
B22	Gnd	A22	AD28	
B23	AD27	A23	AD26	
B24	AD25	A24	Gnd	
B25	BKPL3.3V	A25	AD24	
B26	C/BE3#	A26	GNT2#	
B27	AD23	A27	NC	
B28	Gnd	A28	AD22	
B29	AD21	A29	AD20	
B30	AD19	A30	Gnd	
B31	NC	A31	AD18	
B32	AD17	A32	AD16	
B33	C/BE2#	A33	NC	
B34	Gnd	A34	FRAME#	
B35	IRDY#	A35	Gnd	
B36	NC	A36	TRDY#	
B37	DEVSEL#	A37	Gnd	
B38	Gnd	A38	STOP#	
B39	LOCK#	A39	NC	
B40	PERR#	A40	SDONE	
B41	NC	A41	SBO#	
B42	SERR#	A42	Gnd	
B43	NC	A43	PAR	
B44	C/BE1#	A44	AD15	
B45	AD14	A45	NC	
B46	Gnd	A46	AD13	
B47	AD12	A47	AD11	
B48	AD10	A48	Gnd	
B49	M66EN	A49	AD9	

PICMG EDGE CONNECTOR PIN ASSIGNMENTS (CONTINUED)

I/O Pin	Signal Name	I/O Pin	Signal Name
B50	Connector Key	A50	Connector Key
B51	Connector Key	A51	Connector Key
B52	AD8	A52	C/BE0#
B53	AD7	A53	NC
B54	NC	A54	AD6
B55	AD5	A55	AD4
B56	AD3	A56	Gnd
B57	Gnd	A57	AD2
B58	AD1	A58	AD0
B59	+5V	A59	+5V
B60	ACK64#	A60	REQ64#
B61	+5V	A61	+5V
B62	+5V	A62	+5V

32-bit connector end

PICMG EDGE CONNECTOR PIN ASSIGNMENTS (CONTINUED)

The following pin assignments apply only to SBCs with 64-bit PICMG connectors.

I/O Pin	Signal Name	I/O Pin	Signal Name	
	Connector Key		Connector Key	64-bit spacer
	Connector Key		Connector Key	64-bit spacer
B63	NC	A63	Gnd	64-bit connector start
B64	Gnd	A64	C/BE7#	
B65	C/BE6#	A65	C/BE5#	
B66	C/BE4#	A66	+5V	
B67	Gnd	A67	PAR64	
B68	AD63	A68	AD62	
B69	AD61	A69	Gnd	
B70	+5V	A70	AD60	
B71	AD59	A71	AD58	
B72	AD57	A72	Gnd	
B73	Gnd	A73	AD56	
B74	AD55	A74	AD54	
B75	AD53	A75	+5V	
B76	Gnd	A76	AD52	
B77	AD51	A77	AD50	
B78	AD49	A78	Gnd	
B79	+5V	A79	AD48	
B80	AD47	A80	AD46	
B81	AD45	A81	Gnd	
B82	Gnd	A82	AD44	
B83	AD43	A83	AD42	
B84	AD41	A84	+5V	
B85	Gnd	A85	AD40	
B86	AD39	A86	AD38	
B87	AD37	A87	Gnd	
B88	+5V	A88	AD36	
B89	AD35	A89	AD34	
B90	AD33	A90	Gnd	
B91	Gnd	A91	AD32	
B92	NC	A92	NC	
B93	NC	A93	Gnd	
B94	Gnd	A94	NC	64-bit connector end

Chapter 3 System BIOS

BIOS OPERATION

Sections 3 through 7 of this manual describe the operation of the American Megatrends AMIBIOS and the BIOS Setup Utility. Refer to *Running AMIBIOS Setup* later in this chapter for standard Setup screens, options and defaults. The available Setup screens, options and defaults may vary if you have a custom BIOS.

When the system is powered on, AMIBIOS performs the Power-On Self Test (POST) routines. These routines are divided into two phases:

1) **System Test and Initialization**. Test and initialize system boards for normal operations.
2) **System Configuration Verification**. Compare defined configuration with hardware actually installed.

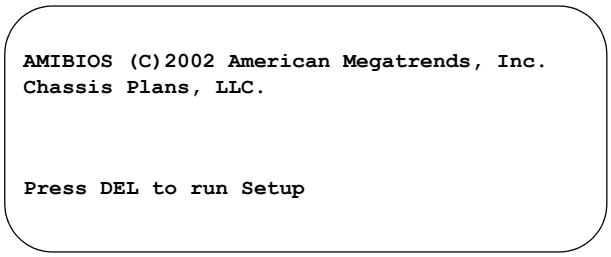
If an error is encountered during the diagnostic tests, the error is reported in one of two different ways. If the error occurs before the display device is initialized, a series of beeps is transmitted. If the error occurs after the display device is initialized, the error message is displayed on the screen. See *BIOS Errors* later in this section for more information on error handling.

The following are some of the Power-On Self Tests (POST's) which are performed when the system is powered on:

- CMOS Checksum Calculation
- Keyboard Controller Test
- CMOS Shutdown Register Test
- 8254 Timer Test
- Memory Refresh Test
- Display Memory Read/Write Test
- Display Type Verification
- Entering Protected Mode
- Memory Size Calculation
- Conventional and Extended Memory Test
- DMA Controller Tests
- Keyboard Test
- System Configuration Verification and Setup

AMIBIOS checks system memory and reports it on both the initial AMIBIOS screen and the AMIBIOS System Configuration screen which appears after POST is completed. AMIBIOS attempts to initialize the peripheral devices and if it detects a fault, the screen displays the error condition(s) which has/have been detected. If no errors are detected, AMIBIOS attempts to load the system from a bootable device, such as a floppy disk or hard disk. Boot order may be specified by the **Boot Device Priority** option on the Boot Setup Menu as described in the *Boot Setup* chapter later in this manual.

Normally, the only POST routine visible on the screen is the memory test. The following screen displays when the system is powered on:



Initial Power-On Screen

You have two options:

- Press **<Del>** to access the BIOS Setup Utility.

  This option allows you to change various system parameters such as date and time, disk drives, etc. The *Running AMIBIOS Setup* section of this manual describes the options available.

  You may be requested to enter a password before gaining access to the BIOS Setup Utility. (See *Password Entry* later in this section.)

  If you enter the correct password or no password is required, the BIOS Setup Utility Main Menu displays. (See *Running AMIBIOS Setup* later in this section.)

- Allow the bootup process to continue without invoking the BIOS Setup Utility.

  In this case, after AMIBIOS loads the system, you may be requested to enter a password. (See *Password Entry* later in this section.)

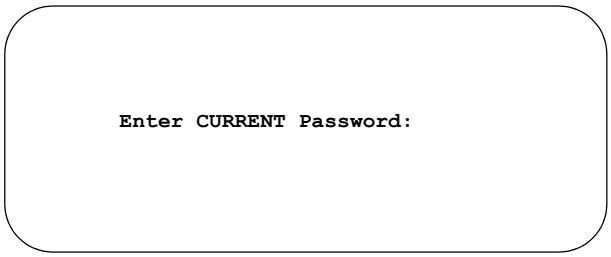
Once the POST routines complete successfully, a screen displays showing the current configuration of your system, including processor type, base and extended memory amounts, floppy and hard drive types, display type and peripheral ports.

Password Entry

The system may be configured so that the user is required to enter a password each time the system boots or whenever an attempt is made to enter the BIOS Setup Utility. The password function may also be disabled so that the password prompt does not appear under any circumstances.

The **Password Check** option in the Security Menu allows you to specify when the password prompt displays: **Always** or only when **Setup** is attempted. This option is available only if the supervisor and/or user password(s) have been established. The supervisor and user passwords may be changed using the **Change Supervisor Password** and **Change User Password** options on the Security Menu. If the passwords are null, the password prompt does not display at any time. See the *Security Setup* section of this chapter for details on setting up passwords.

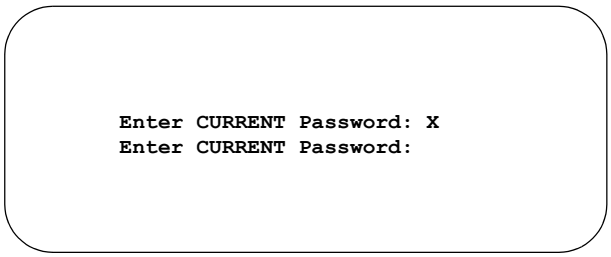
When password checking is enabled, the following password prompt displays:



Type the password and press **<Enter>**.

NOTE: The null password is the system default and is in effect if a password has not been assigned or if the CMOS has been corrupted. In this case, the password prompt does not display. To set up passwords, you may use the **Change Supervisor Password** and **Change User Password** options on the Security Menu of the BIOS Setup Utility. (See the *Security Setup* section later in this chapter.)

If an incorrect password is entered, the following screen displays:



You may try again to enter the correct password. If you enter the password incorrectly three times, the system responds in one of two different ways, depending on the value specified in the **Password Check** option on the *Security* Menu:

1) If the **Password Check** option is set to **Setup**, the system does not let you enter Setup, but does continue the booting process. You must reboot the system manually to retry entering the password.

2) If the **Password Check** option is set to **Always**, the system locks and you must reboot. After rebooting, you will be requested to enter the password.

Once the password has been entered correctly, you are allowed to continue.

BIOS Errors

If an error is encountered during the diagnostic checks performed when the system is powered on, the error is reported in one of two different ways:

1) If the error occurs before the display device is initialized, a series of beeps is transmitted.

2) If the error occurs after the display device is initialized, the screen displays the error message. In the case of a non-fatal error, a prompt to press the **<F1>** key may also appear on the screen.

Explanations of the beep codes and BIOS error messages may be found in *Appendix A - BIOS Messages*.

As the POST routines are performed, test codes are presented on Port 80H. These codes may be helpful as a diagnostic tool and are listed in *Appendix A - BIOS Messages*.

If certain non-fatal error conditions occur, you are requested to run the BIOS Setup Utility. The error messages are followed by this screen:

```
AMIBIOS (C)2002 American Megatrends, Inc.
Chassis Plans, LLC.



Press F1 to Run SETUP
Press F2 to load default values and continue
```

Press **<F1>**. You may be requested to enter a password before gaining access to the BIOS Setup Utility. (See *Password Entry* earlier in this section.)

If you enter the correct password or no password is required, the BIOS Setup Utility Main Menu displays.

RUNNING AMIBIOS SETUP

AMIBIOS Setup keeps a record of system parameters, such as date and time, disk drives, display type and other user-defined parameters. The Setup parameters reside in the Read Only Memory Basic Input/Output System (ROM BIOS) so that they are available each time the system is turned on. The BIOS Setup Utility stores the information in the complementary metal oxide semiconductor (CMOS) memory. When the system is turned off, a backup battery retains system parameters in the CMOS memory.

Each time the system is powered on, it is configured with these values, unless the CMOS has been corrupted or is faulty. The BIOS Setup Utility is resident in the ROM BIOS so that it is available each time the computer is turned on. If, for some reason, the CMOS becomes corrupted, the system is configured with the default values stored in this ROM file.

As soon as the system is turned on, the power-on diagnostic routines check memory, attempt to prepare peripheral devices for action, and offer you the option of pressing **<Del>** to run the BIOS Setup Utility.

If certain non-fatal errors occur during the Power-On Self Test (POST) routines which are run when the system is turned on, you may be prompted to run the BIOS Setup Utility by pressing **<F1>**.

BIOS SETUP UTILITY MAIN MENU

When you press **<F1>** in response to an error message received during the POST routines or when you press the **<Del>** key to enter the BIOS Setup Utility, the following screen displays:

```
                              BIOS SETUP UTILITY
 Main    Advanced    PCIPnP    Chipset    Boot   Security   Exit
System Overview                                  Use [ENTER], {TAB}
_____________________________________________    or [SHIFT-TAB] to
                                                 select a field.
AMIBIOS Version: 08.00.xx
BIOS Build Date: 06/20/02                        Use [+] or [-] to
BIOS ID        : 0ABAF013                        configure System Time.

Processor
Type           : Intel(R) Xeon(TM) CPU 2.80GHz
Speed          : 2000MHz
Count          : 4

System Memory                                    ←→   Select Screen
Size           : 1024MB                          ↑↓   Select Item
                                                 +-   Change Field
System Time                  [00:00:00]          Tab  Select Field
System Date                  [Mon 01/01/2001]    F1   General Help
                                                 F10  Save and Exit
                                                 ESC  Exit
      vxx.xx (C)Copyright 1985-2002, American Megatrends, Inc.
```

BIOS Setup Utility Main Menu

When you display the BIOS Setup Utility Main Menu, the format is similar to the sample shown above. The data displayed on the top portion of the screen details parameters detected by AMIBIOS for your processor board and may not be modified. The system time and date displayed on the bottom portion of the screen may be modified.

BIOS SETUP UTILITY MAIN MENU OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not changed them yet. Once values have been defined, they display each time the BIOS Setup Utility is run.

System Time/System Date

These options allow you to set the correct system time and date. If you do not set these parameters the first time you enter the BIOS Setup Utility, you will receive a "Run SETUP" error message when you boot the system until you set the correct parameters.

The Setup screen displays the system options:

System Time	**[00:00:00]**
System Date	**[Mon 01/01/2001]**

There are three fields for entering the time or date. Use the **<Tab>** key or the **<Enter>** key to move from one field to another and type in the correct value for the field.

If you enter an invalid value in any field, the screen will revert to the previous value when you move to the next field. When you change the value for the month, day or year field, the day of the week changes automatically when you move to the next field.

BIOS SETUP UTILITY OPTIONS

The BIOS Setup Utility allows you to change system parameters to tailor your system to your requirements. Various options which may be changed are listed below. Further explanations of these options and available values may be found in later chapters of this manual, as noted below.

NOTE: Do *not* change the values for any option unless you understand the impact on system operation. Depending on your system configuration, selection of other values may cause unreliable system operation.

Use the **Right Arrow** key to display the desired menu. The following menus are available:

- Select **Advanced** to make changes to Advanced Setup parameters as described in the *Advanced Setup* chapter of this manual. The following options may be modified:
    - CPU Configuration
        - Ratio CMOS Setting
        - HyperThreading
    - IDE Configuration
        - OnBoard PCI IDE Controller
        - Primary IDE Master/Primary IDE Slave
          Secondary IDE Master/Secondary IDE Slave
            - Type
            - LBA/Large Mode
            - Block (Multi-Sector Transfer)
            - PIO Mode
            - DMA Mode
            - S.M.A.R.T.
            - 32Bit Data Transfer
            - ARMD Emulation Type
        - Hard Disk Write Protect
        - IDE Detect Time Out (Sec)
        - ATA(PI) 80Pin Cable Detection

- Floppy Configuration
    - Floppy A/Floppy B
- SuperIO Configuration
    - OnBoard Floppy Controller
    - Serial Port1 Address/Serial Port2 Address
        - Serial Port2 IRQ
        - Serial Port2 Mode
    - Parallel Port Address
        - Parallel Port Mode
        - Parallel Port IRQ
- Event Log Control
    - View Event Log
    - Mark All Events as Read
    - Clear Event Log
    - Event Log Statistics
- Remote Access Configuration
    - Remote Access
    - Serial Port Number
    - Serial Port Mode
    - Post-Boot Support
- USB Configuration
    - USB Function
    - Legacy USB Support
    - USB ZIP Emulation Type
    - USB Beep Message

- Select **PCIPnP** to make changes to PCI Plug and Play Setup parameters as described in the *PCI Plug and Play Setup* chapter of this manual. The following options may be modified:
    - On Board (1GB) Lan
    - On Board SCSI
    - On Board VGA
    - Plug & Play O/S
    - PCI Latency Timer
    - Allocate IRQ to PCI VGA

- Palette Snooping
- PCI IDE BusMaster
- OffBoard PCI/ISA IDE Card
    - OffBoard PCI IDE Primary IRQ
    - OffBoard PCI IDE Secondary
- IRQs 3, 4, 5, 7, 9, 10, 11, 12, 14 and 15
- DMA Channels 0, 1, 3 5, 6 and 7
- Reserved Memory Size
- Reserved Memory Address

- Select **Chipset** to make changes to Chipset Setup parameters as described in the *Chipset Setup* chapter of this manual. The following options may be modified:
    - Intel E7500/E7501 NorthBridge Configuration
        - Chipset Memory Remap Feature
    - Intel ICH3 SouthBridge Configuration
        - ICH3 Dev31 Func1, IDE
        - ICH3 Dev31 Func3, SMBUS
        - ICH3 Dev29 Func0, USB#1
        - LPC 4Eh-4Fh Decode/LPC 2Eh/2Fh Decode
        - ISA BUS
        - IOAPIC
        - Extended IOAPIC
        - CPU B.I.S.T.
        - ICH3 DMA Collection
        - DMA Types 0, 1, 2, 3, 5, 6 and 7
    - Intel PCI-64 Hub 2 Configuration
        - PCI Bus Frequency

- Select **Boot** to make changes to Boot Setup parameters as described in the *Boot Setup* chapter of this manual. The following options may be modified:
    - Boot Settings Configuration
        - Quick Boot
        - Quiet Boot
        - AddOn ROM Display Mode
        - Bootup Num-Lock

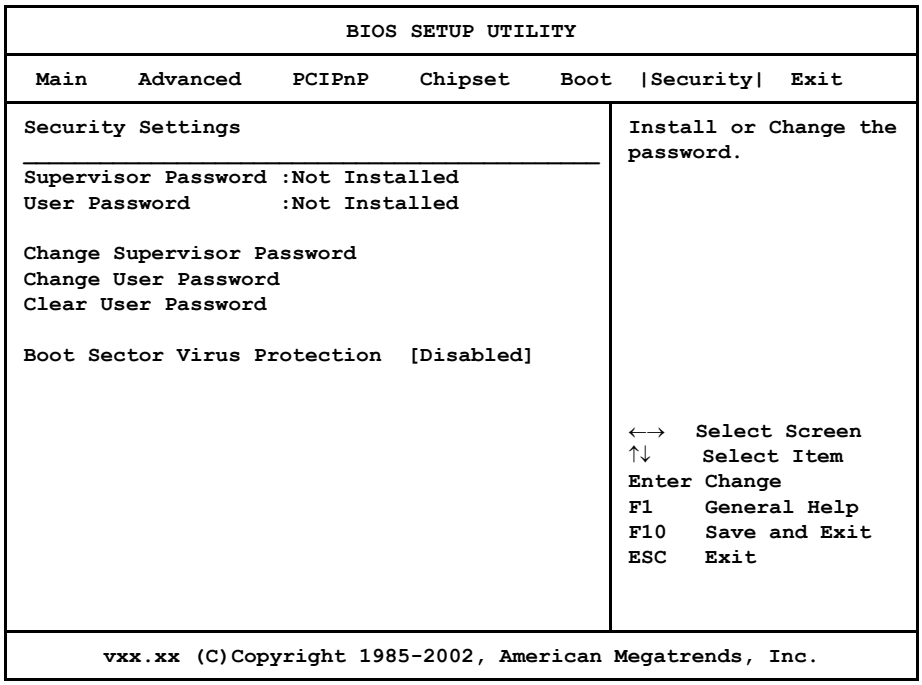
        - PS/2 Mouse Support
        - System Keyboard
        - Boot To OS/2
        - Wait For ‘F1’ If Error
        - Hit ‘DEL’ Message Display
    - Boot Device Priority
    - Hard Disk Drives
    - Removable Devices
    - ATAPI CDROM Drives
    - Interrupt 19 Capture

- Select **Security** to establish or change the supervisor or user password or to enable boot sector virus protection. These functions are described later in this chapter. The following options may be modified:
    - Change Supervisor Password
        - User Access Level
        - Password Check
    - Change User Password
        - Unattended Start
        - Password Check
    - Clear User Password
    - Boot Sector Virus Protection

- Select **Exit** to save or discard changes you have made to AMIBIOS parameters or to load the Optimal or Failsafe default settings. These functions are described later in this chapter. The following options are available:
    - Save Changes and Exit
    - Discard Changes and Exit
    - Discard Changes
    - Load Optimal Defaults
    - Load Failsafe Defaults

SECURITY SETUP

When you select **Security** from the BIOS Setup Utility Main Menu, the following Setup screen displays:



Security Setup Screen

When you display the Security Setup screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>**.

NOTE: The values on this screen do not necessarily reflect the values appropriate for your SBC. Refer to the explanations below for specific instructions about entering correct information.

SECURITY SETUP OPTIONS

The Security Setup options allow you to establish, change or clear the supervisor or user password and to enable boot sector virus protection.

The descriptions for the system options listed below show the values as they appear if you have not changed them yet. Once values have been defined, they display each time the BIOS Setup Utility is run.

CHANGE SUPERVISOR PASSWORD

This option allows you to establish a supervisor password, change the current password or disable the password prompt by entering a null password. The password is stored in CMOS RAM.

If you have signed on under the user password, this option is *not* available.

The **Change Supervisor Password** feature can be configured so that a password must be entered each time the system boots or just when a user attempts to enter the BIOS Setup Utility.

NOTE: The null password is the system default and is in effect if a password has not been assigned or if the CMOS has been corrupted. In this case, the "Enter CURRENT Password" prompt is bypassed when you boot the system, and you must establish a new password.

If you select the **Change Supervisor Password** option, the following window displays:



This is the message which displays before you have established a password, or if the last password entered was the null password. If a password has already been established, you are asked to enter the *current* password before being prompted to enter the *new* password.

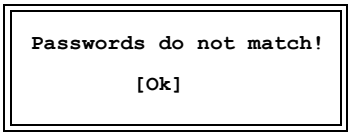
Type the new password and press **<Enter>**. The password cannot exceed six (6) characters in length. The screen displays an asterisk (*) for each character you type.

After you have entered the new password, the following window displays:



Re-key the new password as described above.

If the password confirmation is miskeyed, AMIBIOS Setup displays the following message:



No retries are permitted; you must restart the procedure.

If the password confirmation is entered correctly, the following message displays:



Press the **<Enter>** key to return to the Security screen. **Installed** displays on the screen next to the **Supervisor Password** option, indicating the password has been accepted. This setting will remain in effect until the supervisor password is either disabled or discarded upon exiting the BIOS Setup Utility.

If you have created a new password, be sure to select **Exit**, then **Save Changes and Exit** to save the password. The password is then stored in CMOS RAM. The next time the system boots, you are prompted for the password.

NOTE: Be sure to keep a record of the new password each time it is changed. If you forget it, use the Password Clear jumper to reset it to the default (null password). See the *Specifications* chapter of this manual for details.

If a password has been established, the following options and their default values are added to the screen:

```
User Access Level          [Full Access]
Password Check             [Setup]
```

User Access Level

This option allows you to define the level of access the user will have to the system.

The Setup screen displays the system option:

User Access Level **[Full Access]**

Four options are available:

- Select **No Access** to prevent user access to the BIOS Setup Utility.
- Select **View Only** to allow access to the BIOS Setup Utility for viewing, but to prevent the user from changing any of the fields.
- Select **Limited** to allow the user to change only a limited number of options, such as Date and Time.
- Select **Full Access** to allow the user full access to change any option in the BIOS Setup Utility.

Password Check

This option determines when a password is required for access to the system.

The Setup screen displays the system option:

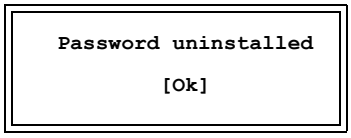
Password Check **[Setup]**

Two options are available:

- Select **Setup** to have the password prompt appear only when an attempt is made to enter the BIOS Setup Utility program.
- Select **Always** to have the password prompt appear each time the system is powered on.

DISABLING THE SUPERVISOR PASSWORD

To *disable* password checking so that the password prompt does not appear, you may create a null password selecting the **Change Supervisor Password** function and pressing **<Enter>** without typing in a new password. You will be asked to enter the current password before being allowed to enter the null password. After you press **<Enter>** at the **Enter New Password** prompt, the following message displays:



CHANGE USER PASSWORD

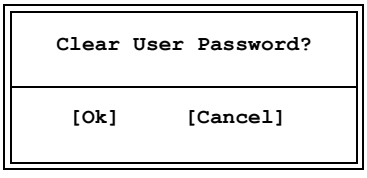
The **Change User Password** option is similar in functionality to the **Change Supervisor Password** and displays the same messages. If you have signed on under the user password, the **Change Supervisor Password** function is not available for modification.

If a user password has been established, the **Password Check** option and its default value is added to the screen. This option determines when a user password is required for access to the system. For details, refer to the description for **Password Check** under the **Change Supervisor Password** heading earlier in this section.

CLEAR USER PASSWORD

This option allows you to clear the user password. It disables the user password by entering a null password.

If you select the **Clear User Password** option, the following window displays:



You have two options:

- Select **Ok** to clear the user password.
- Select **Cancel** to leave the current user password in effect.

BOOT SECTOR VIRUS PROTECTION

This option allows you to request AMIBIOS to issue a warning when any program or virus issues a Disk Format command or attempts to write to the boot sector of the hard disk drive.

The Setup screen displays the system option:

Boot Sector Virus Protection [Disabled]

Available options are:

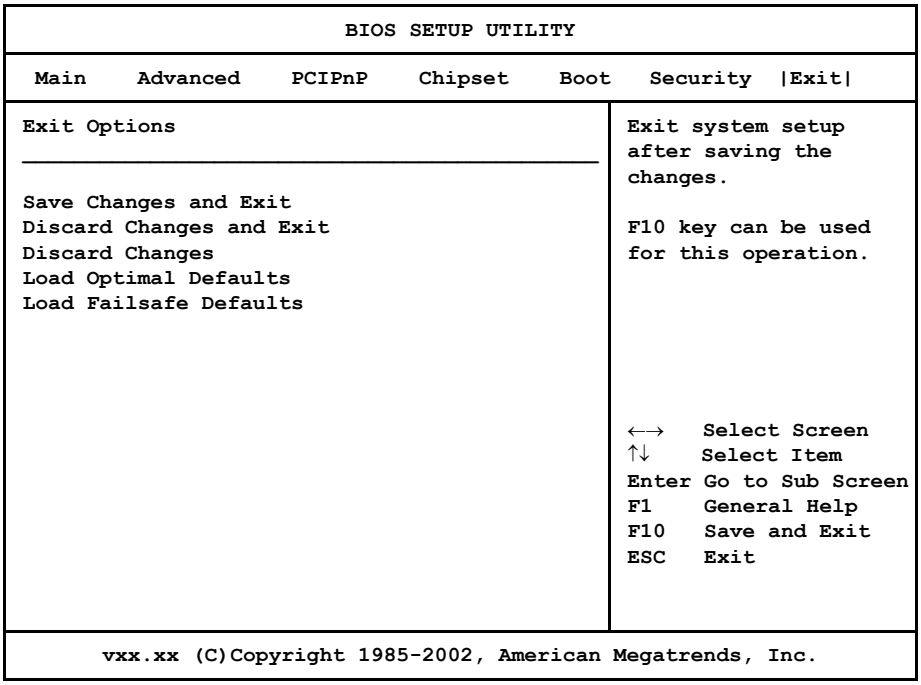
Disabled
Enabled

NOTE: You should *not* enable boot sector virus protection when formatting a hard drive.

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EXIT MENU

When you select **Exit** from the BIOS Setup Utility Main Menu, the following screen displays:



Exit Menu Screen

When you display the Exit Menu screen, the format is similar to the sample shown above. Highlight the option you wish to select and press **<Enter>**.

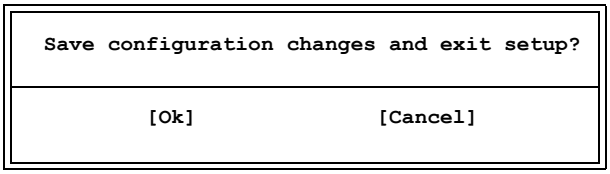
EXIT MENU OPTIONS

When you are running the BIOS Setup Utility program, you may either save or discard changes you have made to AMIBIOS parameters, or you may load the Optimal or Failsafe default settings.

Save Changes and Exit

The features selected and configured in the Setup screens are stored in the CMOS when this option is selected. The CMOS checksum is calculated and written to the CMOS. Control is then passed back to the AMIBIOS and the booting process continues, using the new CMOS values.

If you select the **Save Changes and Exit** option, the following window displays:



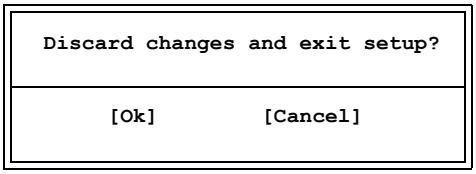
You have two options:

- Select **Ok** to save the system parameters and continue with the booting process.
- Select **Cancel** to return to the BIOS Setup Utility screen.

Discard Changes and Exit

When the **Discard Changes and Exit** option is selected, the BIOS Setup Utility exits *without* saving the changes in the CMOS. Control is then passed back to AMIBIOS and the booting process continues, using the previous CMOS values.

If you select the **Discard Changes and Exit** option, the following window displays:



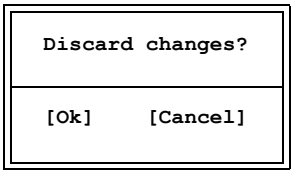
You have two options:

- Select **Ok** to continue the booting process without writing any changes to the CMOS.
- Select **Cancel** to return to the BIOS Setup Utility screen.

Discard Changes

When the **Discard Changes** option is selected, the BIOS Setup Utility resets any parameters you have changed back to the values at which they were set when you entered the Setup Utility. Control is then passed back to the BIOS Setup Utility screen.

If you select the **Discard Changes** option, the following window displays:



You have two options:

- Select **Ok** to reset any parameters you have changed back to the values at which they were set when you entered the BIOS Setup Utility. This option then returns you to the BIOS Setup Utility screen.
- Select **Cancel** to return to the BIOS Setup Utility screen *without* discarding any changes you have made.

Load Optimal or Failsafe Defaults

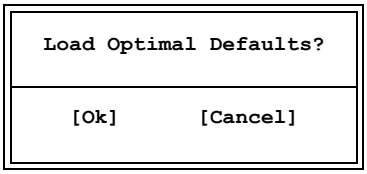
Each AMIBIOS Setup option has two default settings (Optimal and Failsafe). These settings can be applied to all AMIBIOS Setup options when you select the appropriate configuration option from the BIOS Setup Utility Main Menu.

You can use these configuration options to quickly set the system configuration parameters which should provide the best performance characteristics, or you can select a group of settings which have a better chance of working when the system is having configuration-related problems.

Load Optimal Defaults

This option allows you to load the Optimal default settings. These settings are best-case values which should provide the best performance characteristics. If CMOS RAM is corrupted, the Optimal settings are loaded automatically.

If you select the **Load Optimal Defaults** option, the following window displays:



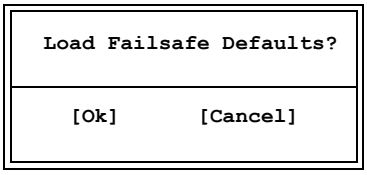
You have two options:

- Select **Ok** to load the Optimal default settings.
- Select **Cancel** to leave the current values in effect.

Load Failsafe Defaults

This option allows you to load the Failsafe default settings when you cannot boot your computer successfully. These settings are more likely to configure a workable computer. They may not provide optimal performance, but are the most stable settings. You may use this option as a diagnostic aid if your system is behaving erratically. Select the Failsafe settings and then try to diagnose the problem after the computer boots.

If you select the **Load Failsafe Defaults** option, the following window displays:



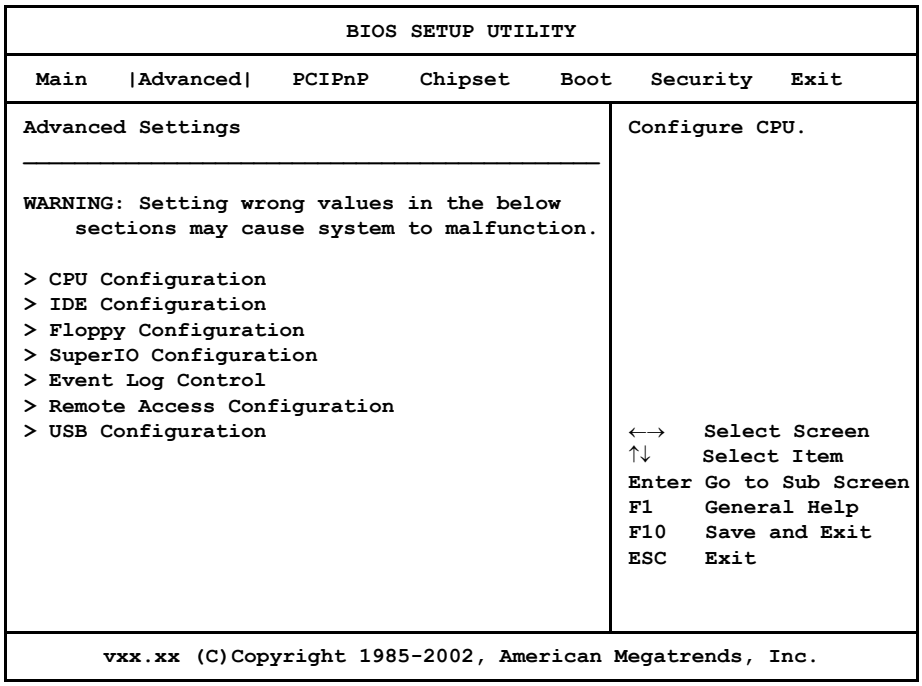
You have two options:

- Select **Ok** to load the Failsafe default settings.
- Select **Cancel** to leave the current values in effect.

Chapter 4 Advanced Setup

ADVANCED SETUP

When you select **Advanced** from the BIOS Setup Utility Main Menu, the following Setup screen displays:



Advanced Setup Screen

When you display the Advanced Setup screen, the format is similar to the sample shown above, allowing you to continue to subscreens designed to change parameters for each of the Advanced Setup options. Highlight the option you wish to change and press **<Enter>** to proceed to the appropriate subscreen.

NOTE: The values on the Advanced Setup subscreens do not necessarily reflect the values appropriate for your SBC. Refer to the explanations following each screen for specific instructions about entering correct information.

ADVANCED SETUP OPTIONS

NOTE: Do not change the values for any Advanced Setup option unless you understand the impact on system operation. Depending on your system configuration, selection of other values may cause unreliable system operation.

CPU Configuration

The **CPU Configuration** subscreen provides you with information about the processor in your system and allows you to modify the following option:

- Ratio CMOS Setting
- HyperThreading

IDE Configuration

The options on the **IDE Configuration** subscreens allow you to set up or modify parameters for your IDE controller and hard disk drive(s). The following options may be modified:

- OnBoard PCI IDE Controller
- Primary IDE Master/Primary IDE Slave
    - Type
    - LBA/Large Mode
    - Block (Multi-Sector Transfer)
    - PIO Mode
    - DMA Mode
    - S.M.A.R.T.
    - 32Bit Data Transfer
    - ARMD Emulation Type
- Secondary IDE Master/Secondary IDE Slave
    - (see options above)
- Hard Disk Write Protect
- IDE Detect Time Out (Sec)
- ATA(PI) 80Pin Cable Detection

Floppy Configuration

The options on the **Floppy Configuration** subscreen allow you to set up or modify parameters for your floppy disk drive(s). The following options may be modified:

- Floppy A/Floppy B

SuperIO Configuration

The options on the **SuperIO Configuration** subscreen allow you to set up or modify parameters for your on-board peripherals. The following options may be modified:

- OnBoard Floppy Controller

- Serial Port1 Address/Serial Port2 Address
    - Serial Port2 IRQ
    - Serial Port2 Mode
- Parallel Port Address
    - Parallel Port Mode
    - Parallel Port IRQ

Event Log Control

The options on the **Event Log Control** subscreen allow you to set up or modify parameters for using the event log, which allows you to log errors and other events which occur in the system. The following options may be modified:

- View Event Log
- Mark All Events as Read
- Clear Event Log
- Event Log Statistics

Remote Access Configuration

The options on the **Remote Access Configuration** subscreen allow you to set up or modify parameters for configuring remote access type and parameters. The following options may be modified:

- Remote Access
- Serial Port Number
- Serial Port Mode
- Post-Boot Support

USB Configuration

The options on the **USB Configuration** subscreen allow you to set up or modify parameters for your on-board peripherals. The following options may be modified:

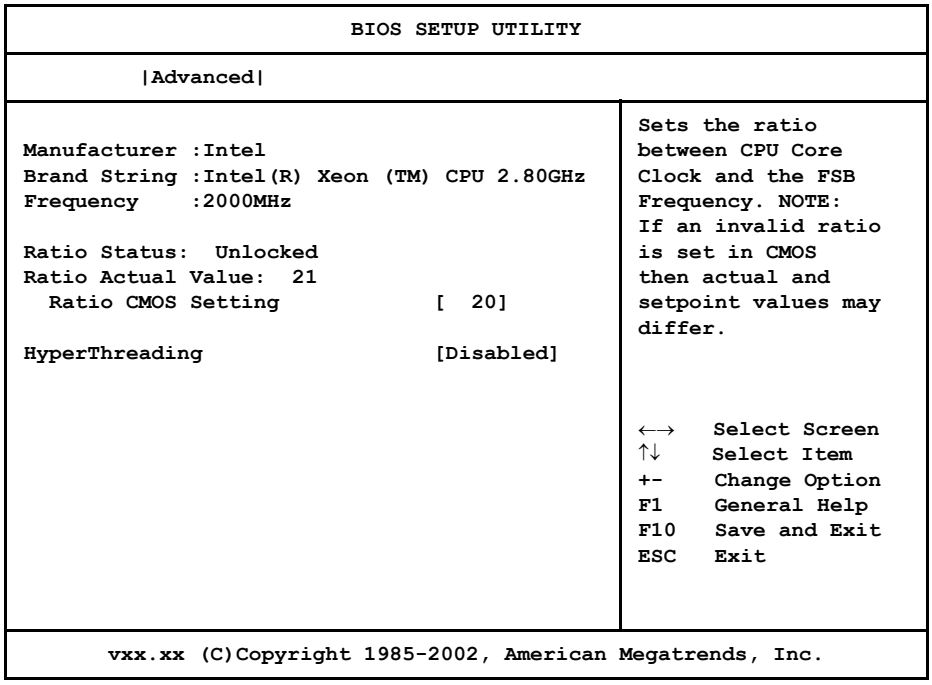
- USB Configuration
    - USB Function
    - Legacy USB Support
    - USB ZIP Emulation Type
    - USB Beep Message

Saving and Exiting

When you have made all desired changes to **Advanced Setup**, you may make changes to other Setup options by using the right and left arrow keys to access other menus. When you have made all of your changes, you may save them by selecting the **Exit** menu, or you may press **<Esc>** at any time to exit the BIOS Setup Utility without saving the changes.

CPU CONFIGURATION

When you select **CPU Configuration** from the Advanced Setup Screen, the following Setup screen displays:



CPU Configuration Screen

When you display the CPU Configuration screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

CPU CONFIGURATION OPTIONS

The description for the system options listed below show the values as they appear if you have not yet run Advanced Setup. Once you change the settings, the new settings display each time Advanced Setup is run.

Ratio CMOS Setting

Xeon processors are shipped from the vendor as "fuse limited," indicating that they run up to the designated speed (e.g., 2.0GHz), but also have the ability to reset to a "safe mode" of 800MHz. The XPT SBC is set at the Chassis Plans factory to the correct processor speed before shipment, but if the CMOS settings have been corrupted or if you have used the JU12 jumper to clear CMOS, the Xeon processor may reset to the safe mode. The result is a reduction in execution speed which affects overall system performance. After clearing CMOS, you should always check the operating speed and reset it if necessary.

This option allows you to reset the operating speed of the SBC to its correct value. You must manually type in the value. When the system reboots, you can verify that the boot-up screen displays the correct processor speed.
The Setup screen displays the system option:

Ratio CMOS Setting [##]

where ## is the CPU ratio setting for the processor speed (e.g., 8 indicates 800MHz, 20 indicates 2.0GHz, etc.)

HyperThreading

Hyper-Threading is a feature which can be used to maximize the Xeon processor's efficiency and execution speed by using the single processor as two logical processors. The two logical processors have separate architectural and local APIC states, but unlike separate physical processors, these logical processors share common execution resources.

Hyper-Threading improves overall performance in many systems designed for multi-processing, high-demand multi-tasking and multi-threaded applications. If you are using a system which can take advantage of Hyper-Threading technology, you may change the setting of the **HyperThreading** option to **Enabled**.

Intel® recommends enabling Hyper-Threading on systems that use Microsoft® Windows® XP® or Linux® 2.4.x operating systems.

The factory setting of the **HyperThreading** option in the system BIOS is **Disabled**. For systems which use applications and operating systems which cannot take advantage of Hyper-Threading technology, the **HyperThreading** option should remain **Disabled**. Intel recommends disabling Hyper-Threading when using the following operating systems: Microsoft Windows 98®, Windows NT®, Windows 2000®, Windows ME®, IBM® OS/2® and any version of Linux before revision 2.4.x. These operating systems are not optimized for Hyper-Threading technology and some applications may actually experience some performance degradation.

The Setup screen displays the system option:

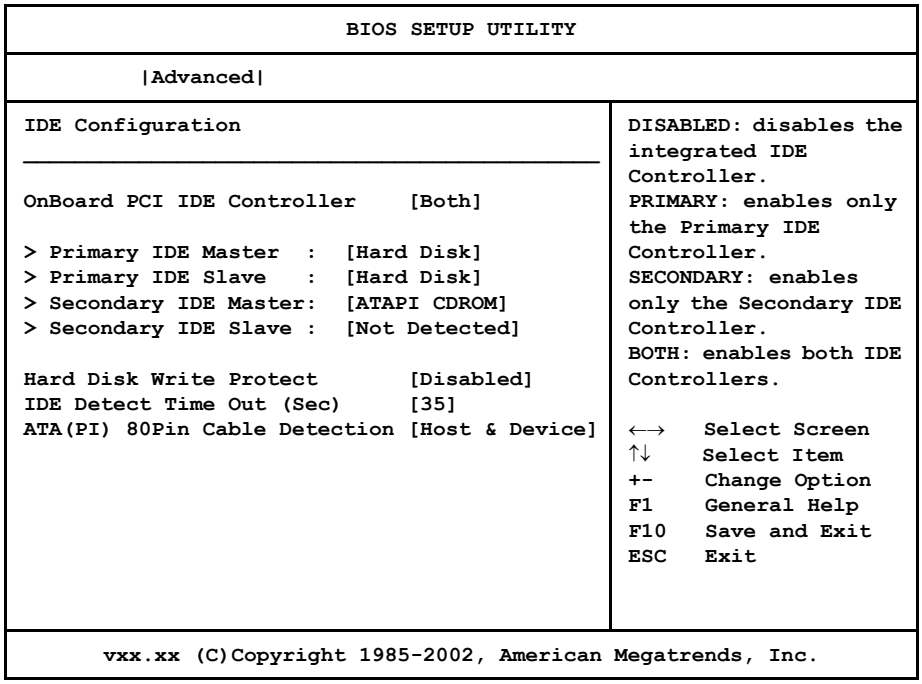
HyperThreading [Disabled]

Available options are:

Disabled
Enabled

IDE CONFIGURATION

When you select **IDE Configuration** from the Advanced Setup Menu, the following Setup screen displays:



IDE Configuration Screen

When you display the IDE Configuration screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

Some of the options on this screen allow you to continue to subscreens designed to change parameters for that particular option. Highlight the option you wish to change and press **<Enter>** to proceed to the appropriate subscreen.

IDE CONFIGURATION OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not run the BIOS Setup Utility program yet. Once values have been defined, they display each time the BIOS Setup Utility is run.

OnBoard PCI IDE Controller

This option specifies whether or not the on-board integrated drive electronics (IDE) controllers are to be used.

The Setup screen displays the system option:

OnBoard PCI IDE Controller [Both]

Available options are:

Disabled
Primary
Secondary
Both

Primary IDE Master/Primary IDE Slave
Secondary IDE Master/Secondary IDE Slave

The SBC has an enhanced IDE (EIDE) interface which can support up to four IDE disk drives through a primary and secondary controller in a master/slave configuration. This EIDE interface allows disk drives greater than 528MB to be used. Each of the four drives may be a different type.

Devices attached to the primary and secondary controllers are detected automatically by AMIBIOS and displayed on the IDE Configuration screen.

The Setup screen displays the system options:

Primary IDE Master [Hard Disk]
Primary IDE Slave [Hard Disk]

Secondary IDE Master [ATAPI CDROM]
Secondary IDE Slave [Not Detected]

To view and/or change parameters for any IDE device, press **<Enter>** to proceed to the IDE Device Setup screen, which is described later in this section.

Hard Disk Write Protect

This option allows you to disable or enable device write protection. Write protection will be effective only if the device is accessed through the BIOS.

The Setup screen displays the system option:

Hard Disk Write Protect [Disabled]

Available options are:

Disabled
Enabled

IDE Detect Time Out (Sec)

This option allows you to select the time-out value (in seconds) for detecting an ATA/ ATAPI device.

The Setup screen displays the system option:

IDE Detect Time Out (Sec) [35]

Available options are:

0
5
10
15
20
25
30
35

ATA(PI) 80Pin Cable Detection

This option allows you to select the mechanism for detecting an 80-pin ATA(PI) cable.

The Setup screen displays the system option:

ATA(PI) 80Pin Cable Detection [Host & Device]

Available options are:

Host & Device
Host
Device

This page intentionally left blank.

IDE DEVICE SETUP

When you select one of the IDE devices from the **IDE Configuration** screen, a Setup screen similar to the following displays:

```
                        BIOS SETUP UTILITY
          |Advanced|
Primary IDE Master                                  Select the type
_____________________________________________       of device connected
Device    :Hard Disk                                to the system.
Vendor    :ST38418A
Size      :8.6GB
LBA Mode  :Supported
Block Mode:32Sectors
PIO Mode  :4
Async DMA :MultiWord DMA-2
Ultra DMA :Ultra DMA-2
S.M.A.R.T.:Supported
_____________________________________________
Type                            [Auto}          ←→   Select Screen
LBA/Large Mode                  [Auto]          ↑↓   Select Item
Block (Multi-Sector Transfer)   [Auto]          +-   Change Option
PIO Mode                        [Auto]          F1   General Help
DMA Mode                        [Auto]          F10  Save and Exit
S.M.A.R.T.                      [Auto]          ESC  Exit
32Bit Data Transfer             [Disabled]
ARMD Emulation Type             [Auto]
      vxx.xx (C)Copyright 1985-2002, American Megatrends, Inc.
```

IDE Device Screen

When you display the IDE Device subscreen, the format is similar to the sample shown above. The data displayed on the top portion of the screen details the parameters detected by AMIBIOS for the specified device and may not be modified. The data displayed on the bottom portion of the screen may be modified.

The drive information which displays the first time the BIOS Setup Utility is run indicates the drive(s) on your system which were detected by AMIBIOS upon initial bootup.

IDE DEVICE SETUP OPTIONS

The following options are available for each of the four IDE devices on the primary and secondary IDE controllers:

Type

This option allows you to specify what type of device is on the IDE controller.

The Setup screen displays the system option:

Type **[Auto]**

Available options are:

Not Installed
Auto
CDROM
ARMD

If **Not Installed** is selected, the other options on the bottom portion of this screen do not display. If **CDROM** is selected, the **ARMD Emulation Type** option is not available.

LBA/Large Mode

This option allows you to enable IDE LBA (Logical Block Addressing) Mode for the specified IDE drive. Data is accessed by block addresses rather than by the traditional cylinder-head-sector format. This allows you to use drives larger than 528MB.

The Setup screen displays the system option:

LBA/Large Mode [Auto]

Two options are available:

- Select **Disabled** to have AMIBIOS use the physical parameters of the hard disk and do no translation to logical parameters. The operating system which uses the parameter table will then see only 528MB of hard disk space even if the drive contains more than 528MB.
- Select **Auto** to enable LBA mode and translate the physical parameters of the drive to logical parameters. LBA Mode must be supported by the drive and the drive must have been formatted with LBA Mode enabled.

Block (Multi-Sector Transfer) Mode

This option supports transfer of multiple sectors to and from the specified IDE drive. Block mode boosts IDE drive performance by increasing the amount of data transferred during an interrupt.

If **Block Mode** is set to **Disabled**, data transfers to and from the device occur one sector at a time.

The Setup screen displays the system option:

Block (Multi-Sector Transfer) [Auto]

Available options are:

Disabled
Auto

PIO Mode

IDE Programmed I/O (PIO) Mode programs timing cycles between the IDE drive and the programmable IDE controller. As the PIO mode increases, the cycle time decreases.

Set the **PIO Mode** option to **Auto** to have AMIBIOS select the PIO mode used by the IDE drive being configured. If you select a specific value for the PIO mode, you must make absolutely certain that you are selecting the PIO mode supported by the IDE drive being configured.

The Setup screen displays the system option:

PIO Mode [Auto]

Available options are:

Auto
0
1
2
3
4

DMA Mode

This option allows you to select DMA Mode for the device.

The Setup screen displays the system option:

DMA Mode [Auto]

Available options are:

Auto	
SWDMA0	(SingleWord DMA 0 - 2)
SWDMA1	
SWDMA2	
MWDMA0	(MultiWord DMA 0 - 2)
MWDMA1	
MWDMA2	
UDMA0	(UltraDMA 0 - 4)
UDMA1	
UDMA2	
UDMA3	
UDMA4	

S.M.A.R.T.

This option allows AMIBIOS to use the SMART (Self-Monitoring Analysis and Reporting Technology) protocol for reporting server system information over a network.

The Setup screen displays the system option:

S.M.A.R.T. [Auto]

Available options are:

Auto
Disabled
Enabled

32Bit Data Transfer

Hard disk drives connected to the SBC via the ISA Bus transfer data 16 bits at a time. An IDE drive on the PCI Local Bus can use a 32-bit data path.

If the **32Bit Data Transfer** parameter is set to **Enabled**, AMIBIOS enables 32-bit data transfers. If the host controller does not support 32-bit transfer, this feature must be set to **Disabled**.

The Setup screen displays the system option:

32Bit Data Transfer [Disabled]

Available options are:

Disabled
Enabled

ARMD Emulation Type

This option specifies the type of ARMD (ATAPI Removable Media Device) emulation used for a non-disk device attached to the specified IDE device.

If the option is set to **Auto**, AMIBIOS automatically determines the proper emulation type and will support particular storage devices with ATAPI interface.

If **CDROM** is selected in the **Type** field, this option is not available for modification.

The Setup screen displays the system options:

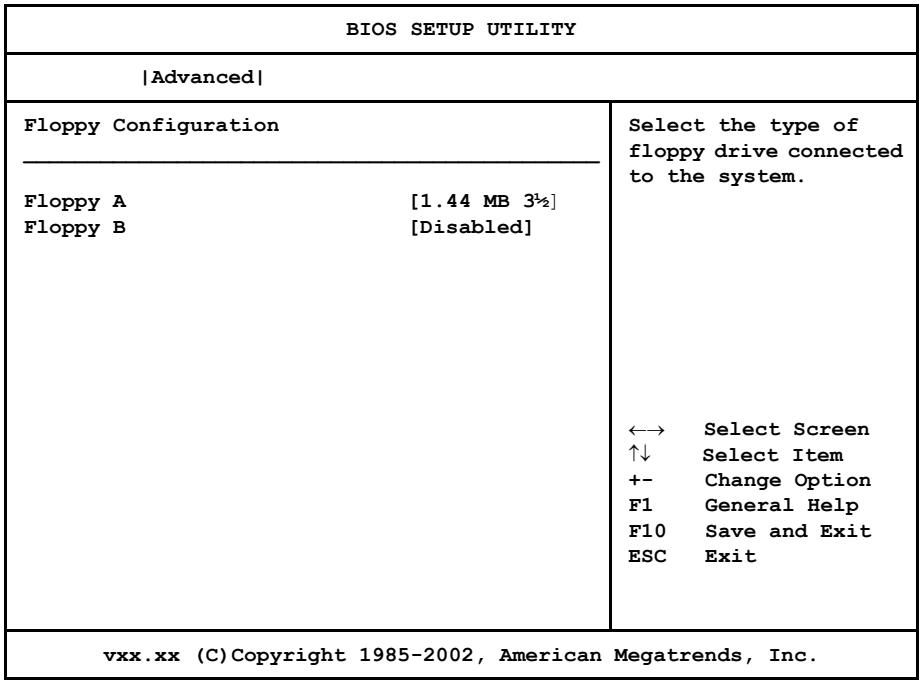
ARMD Emulation Type [Auto]

Available options are:

Auto
Floppy
Hard Disk

FLOPPY CONFIGURATION

When you select **Floppy Configuration** from the Advanced Setup Menu, the following Setup screen displays:



Floppy Configuration Screen

When you display the Floppy Configuration screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

The drive information which displays the first time the BIOS Setup Utility is run indicates the drive(s) on your system which were detected by AMIBIOS upon initial bootup.

FLOPPY CONFIGURATION OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not run the BIOS Setup Utility program yet. Once values have been defined, they display each time the BIOS Setup Utility is run.

Floppy A/Floppy B

The floppy drive(s) in your system can be configured using these options. The **Disabled** option can be used for diskless workstations.

The Setup screen displays the system options:

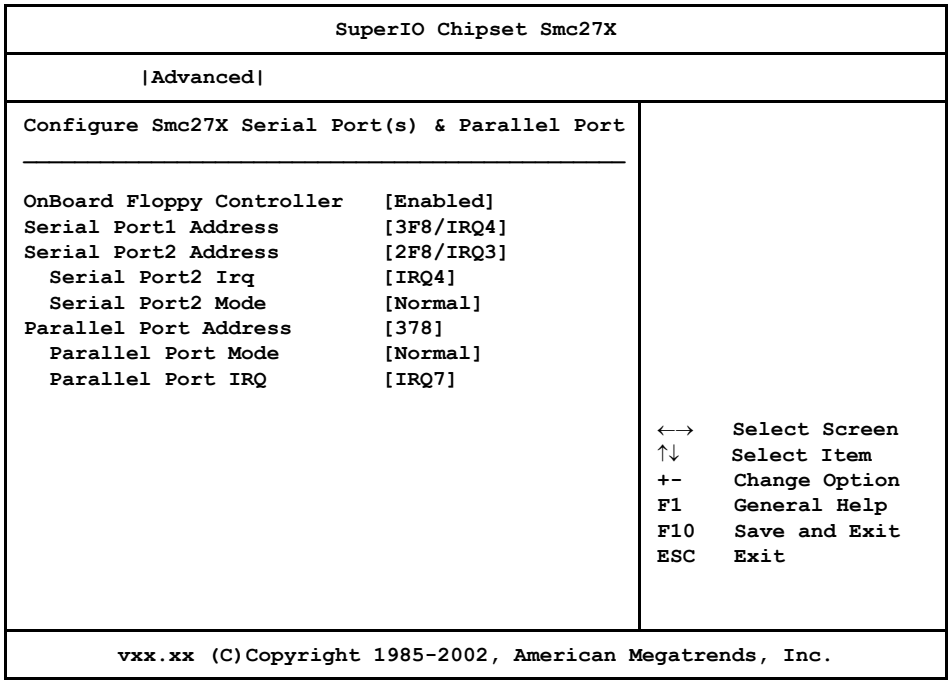
Floppy A	**[1.44 MB 3½"]**
Floppy B	**[Disabled]**

Available options are:

Disabled
360 KB 5¼"
1.2 MB 5¼"
720 KB 3½"
1.44MB 3½"
2.88MB 3½"

SUPERIO CONFIGURATION

When you select **SuperIO Configuration** from the Advanced Setup Menu, the following Setup screen displays:



SuperIO Configuration Screen

When you display the SuperIO Configuration screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

SUPERIO CONFIGURATION OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not run the BIOS Setup Utility program yet. Once values have been defined, they display each time the BIOS Setup Utility is run.

OnBoard Floppy Controller

The on-board floppy drive controller may be enabled or disabled using this option.

The Setup screen displays the system option:

OnBoard Floppy Controller [Enabled]

Available options are:

Disabled
Enabled

Serial Port1 Address/Serial Port2 Address

Each of these options enables the specified serial port on the SBC and establishes the base I/O address and the number of the interrupt request for the port.

The Setup screen displays the system option:

Serial Port1 Address	**[3F8/IRQ4]**
Serial Port2 Address	**[2F8/IRQ3]**

Available options are:

Disabled
3F8/IRQ4
3E8/IRQ4
2F8/IRQ3
2E8/IRQ3

NOTE: The values available for each on-board serial port may vary, depending on the setting previously selected for the other on-board serial port and any off-board serial ports. If an I/O address is assigned to another serial port, AMIBIOS automatically omits that address from the values available.

If the system has off-board serial ports which are configured to specific starting I/O ports via jumper settings, AMIBIOS configures the on-board serial ports to avoid conflicts.

AMIBIOS checks the ISA Bus for serial ports. Any off-board serial ports found on the ISA Bus are left at their assigned addresses. Serial Port1, the first on-board serial port, is configured with the first available address and Serial Port2, the second on-board serial port, is configured with the next available address. The default address assignment order is 3F8H, 2F8H, 3E8H, 2E8H. Note that this same assignment order is used by AMIBIOS to place the active serial port addresses in lower memory (BIOS data area) for configuration as logical COM devices.

For example, if there is one off-board serial port on the ISA Bus and its address is set to 2F8H, Serial Port1 is assigned address 3F8H and Serial Port2 is assigned address 3E8H. Configuration is then as follows:

COM1 - Serial Port1 (at 3F8H)
COM2 - off-board serial port (at 2F8H)
COM3 - Serial Port2 (at 3E8H)

If **Serial Port2 Address** is set to **Disabled**, the **Serial Port2 IRQ** and **Serial Port2 Mode** options are not available.

Serial Port2 IRQ

If the **Serial Port2 Address** option is set to **Disabled**, this option is not available for modification.

The Setup screen displays the system option:

Serial Port2 IRQ [IRQ4]

Available options are:

Disabled
IRQ3
IRQ4

Serial Port2 Mode

If the **Serial Port2 Address** option is set to **Disabled**, this option is not available for modification.

The Setup screen displays the system option:

Serial Port2 Mode [Normal]

Available options are:

Normal
IrDA Sir-A
ASK IR
IrDA Sir-B
IrDA HDLC
IrDA 4PPM
Consumer
Raw Ir

Parallel Port Address

This option enables the parallel port on the SBC and establishes the base I/O address for the port.

The Setup screen displays the system option:

Parallel Port Address [378]

Available options are:

Disabled
378
278
3BC

AMIBIOS checks the ISA Bus for off-board parallel ports. Any parallel ports found on the ISA Bus are left at their assigned addresses. The on-board Parallel Port is automatically configured with the first available address not used by an off-board parallel port.

If this option is set to **Disabled**, the **Parallel Port Mode** and **Parallel Port IRQ** options are not available.

Parallel Port Mode

This option specifies the parallel port mode. ECP and EPP are both bidirectional data transfer schemes which adhere to the IEEE P1284 specifications.

If the **Parallel Port Address** option is set to **Disabled**, this option is not available for modification.

The Setup screen displays the system option:

Parallel Port Mode **[Normal]**

Four options are available:

- Select **Normal** to use normal parallel port mode.
- Select **Bi-Directional** to use bi-directional parallel port mode.
- Select **EPP** to allow the parallel port to be used with devices which adhere to the Enhanced Parallel Port (EPP) specification. EPP uses the existing parallel port signals to provide asymmetric bidirectional data transfer driven by the host device.
- Select **ECP** to allow the parallel port to be used with devices which adhere to the Extended Capabilities Port (ECP) specification. ECP uses the DMA protocol to achieve transfer rates of approximately 2.5MB/second. ECP provides symmetric bidirectional communication.

Parallel Port IRQ

This option specifies the interrupt request (IRQ) which is used by the parallel port.

If the **Parallel Port Address** option is set to **Disabled**, this option is not available for modification.

The Setup screen displays the system option:

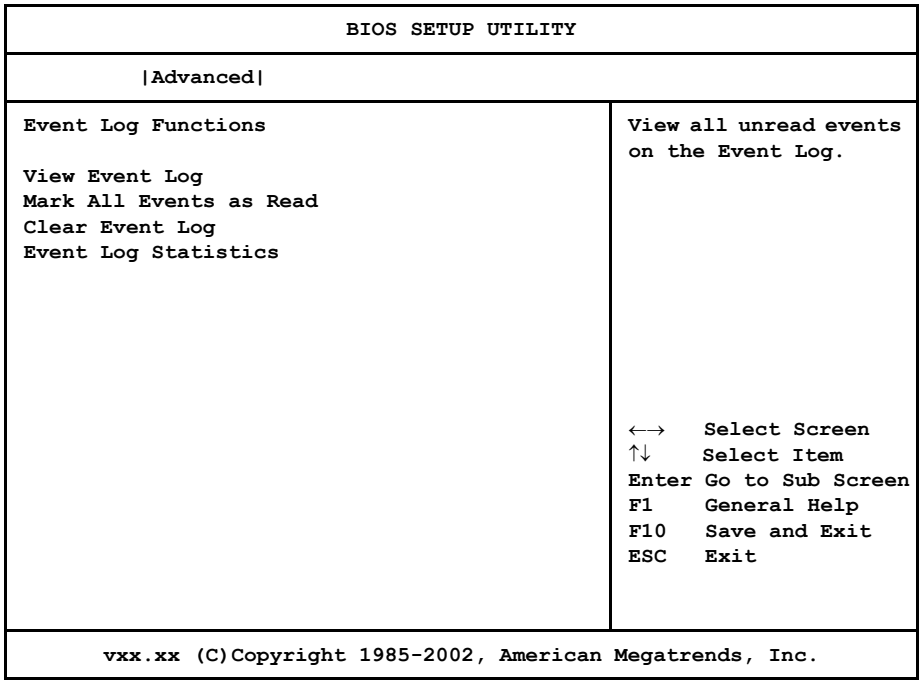
Parallel Port IRQ **[IRQ7]**

Available options are:

IRQ5
IRQ7

EVENT LOG CONTROL

When you select **Event Log Control** from the Advanced Setup Menu, the following Setup screen displays:



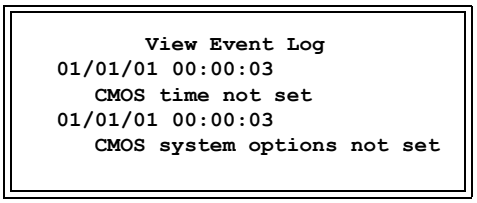
Event Log Control Screen

When you display the Event Log Control screen, the format is similar to the sample shown above. Highlight the option you wish to access and press **<Enter>**. After you have finished, select the appropriate response.

EVENT LOG CONTROL OPTIONS

View Event Log

When you select this option, a window similar to the following displays showing unread events in the Event Log:

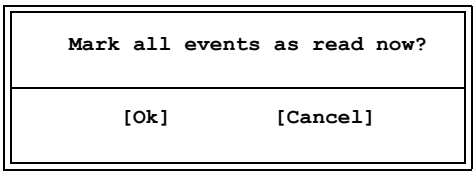


When you have finished viewing the Event Log, press **<Esc>** to continue.

Mark All Events As Read

After you have reviewed the events in the event log, you may select this option, which allows you to mark all unread event log entries as having been read.

The following window displays:

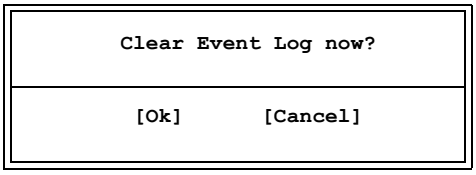


Selecting **Ok** marks all unread entries currently in the event log file as having been read. The next time you select the **View Event Log** option, only the new, unmarked events are displayed.

Clear Event Log

This option specifies whether or not the event log should be cleared.

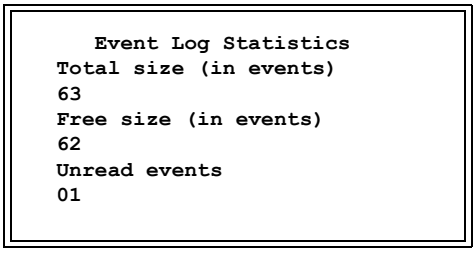
The following window displays:



Selecting **Ok** discards all entries in the Event Log. The next time you select the **View Event Log** option, only new entries will display.

Event Log Statistics

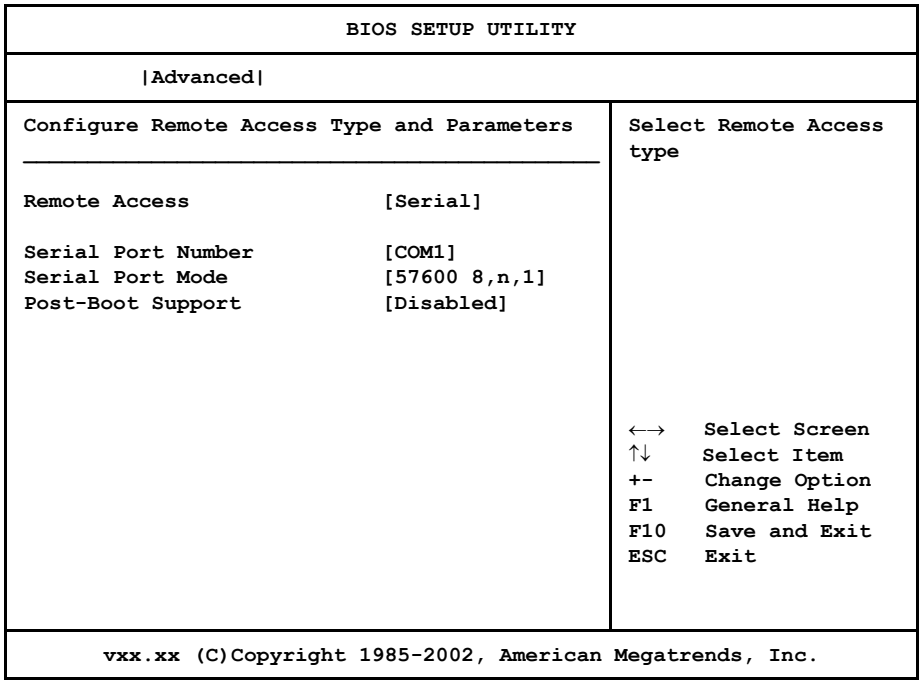
When you select this option, a window similar to the following displays showing statistics for events which have been logged:



When you have finished viewing the Event Log statistics, press **<Esc>** to continue.

REMOTE ACCESS CONFIGURATION

When you select **Remote Access Configuration** from the Advanced Setup Menu, the following Setup screen displays:



Remote Access Configuration Screen

When you display the Remote Access Configuration screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

REMOTE ACCESS CONFIGURATION OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not run the BIOS Setup Utility program yet. Once values have been defined, they display each time the BIOS Setup Utility is run.

Remote Access

This option allows you to use a terminal connected to the serial port of the SBC to control changes to the BIOS settings.

The Setup screen displays the system option:

Remote Access [Disabled]

Available options are:

Disabled
Serial

If this option is set to **Disabled**, the **Serial Port Number**, **Serial Port Mode** and **Post-Boot Support** options are not available.

Serial Port Number

This option specifies the serial port on which remote access is to be enabled.

If the **Remote Access** option is set to **Disabled**, this option is not available.

The Setup screen displays the system option:

Serial Port Number [COM1]

Available options are:

COM1
COM2

Serial Port Mode

This option specifies settings for the serial port on which remote access is enabled. The settings indicate baud rate, eight bits per character, no parity and one stop bit.

If the **Remote Access** option is set to **Disabled**, this option is not available.

The Setup screen displays the system option:

Serial Port Mode [57600 8,n,1]

Available options are:

115200 8,n,1
57600 8,n,1
19200 8,n,1

Post-Boot Support

This option specifies whether or not to keep redirection active after booting to DOS.

If the **Remote Access** option is set to **Disabled**, this option is not available.

The Setup screen displays the system option:

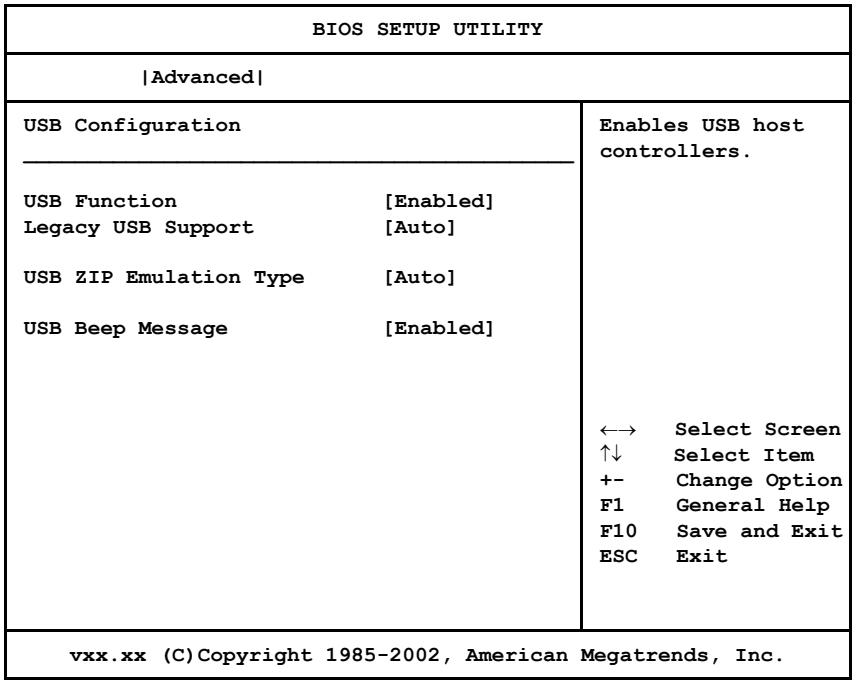
Post-Boot Support [Disabled]

Two options are available:

- Select **Disabled** to deactivate redirection.
- Select **Enabled** to keep redirection active.

USB CONFIGURATION

When you select **USB Configuration** from the Advanced Setup Menu, the following Setup screen displays:



USB Configuration Screen

When you display the USB Configuration screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

USB CONFIGURATION OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not run the BIOS Setup Utility program yet. Once values have been defined, they display each time the BIOS Setup Utility is run.

USB Function

This option allows you to enable the Universal Serial Bus (USB).

If this option is set to **Disabled**, the **Legacy USB Support**, **USB ZIP Emulation Type** and **USB Beep Message** options are not available.

The Setup screen displays the system option:

USB Function [Enabled]

Available options are:

Disabled
Enabled

Legacy USB Support

This option allows you to enable support for older USB devices.

If the **USB Function** option is set to **Disabled**, this option is not available.

The Setup screen displays the system option:

Legacy USB Support [Auto]

Available options are:

Disabled
Enabled
Auto

USB ZIP Emulation Type

This option allows you to set the emulation type for USB Zip drives.

If the **USB Function** option is set to **Disabled**, this option is not available.

The Setup screen displays the system option:

USB ZIP Emulation Type [Auto]

Available options are:

Auto
Floppy
Hard Disk

USB Beep Message

This option allows you to enable the beep during USB device enumeration.

If the **USB Function** option is set to **Disabled**, this option is not available.

The Setup screen displays the system option:

USB Beep Message [Enabled]

Available options are:

Disabled
Enabled

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Chapter 5 PCI Plug and Play Setup

PCI PLUG AND PLAY SETUP

When you select **PCIPnP** from the BIOS Setup Utility Main Menu, the following Setup screen displays:

```
                        BIOS SETUP UTILITY
 Main    Advanced   |PCIPnP|   Chipset    Boot   Security   Exit
Advanced PCI/PnP Settings
_____________________________________________

WARNING: Setting wrong values in below sections
         may cause system to malfunction.

On board (1GB) Lan              [Enabled]
On board SCSI                   [Enabled]
On board VGA                    [Enabled]
Plug & Play O/S                 [No]
PCI Latency Timer               [64]
Allocate IRQ to PCI VGA         [Yes]
Palette Snooping                [Disabled]
PCI IDE BusMaster               [Disabled]
OffBoard PCI/ISA IDE Card       [Auto]

IRQ3                            [Available]
IRQ4                            [Available]
IRQ5                            [Available]
IRQ7                            [Available]
IRQ9                            [Available]
IRQ10                           [Available]
IRQ11                           [Available]
IRQ12                           [Available]
IRQ14                           [Available]
IRQ15                           [Available]

DMA Channel 0                   [Available]
DMA Channel 1                   [Available]      ←→   Select Screen
DMA Channel 3                   [Available]      ↑↓   Select Item
DMA Channel 5                   [Available]      +-   Change Option
DMA Channel 6                   [Available]      F1   General Help
DMA Channel 7                   [Available]      F10  Save and Exit
                                                 ESC  Exit
Reserved Memory Size            [Disabled]
Reserved Memory Address         [C8000]

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```

PCIPnP Setup Screen

When you display the PCIPnP Setup screen, the format is similar to the sample shown above, except the screen does not display all of the options at one time. If you need to change other options, use the down arrow key to locate the appropriate option. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

NOTE: The values on the PCIPnP Setup screen do not necessarily reflect the values appropriate for your SBC. Refer to the explanations below for specific instructions about entering correct information.

PCIPnP Setup Options

The descriptions for the system options listed below show the values as they appear if you have not yet run PCIPnP Setup. Once values have been defined, they display each time PCIPnP Setup is run.

NOTE: Do not change the values for any PCIPnP Setup option unless you understand the impact on system operation. Depending on your system configuration, selection of other values may cause unreliable system operation.

On Board (1GB) LAN

This option specifies whether there is an on-board 10/100/1000Base-T (1GB) Ethernet device on your system.

The Setup screen displays the system option:

On board (1GB) Lan [Enabled]

Available options are:

Disabled
Enabled

On Board SCSI

This option specifies whether there is an on-board SCSI device on your system.

The Setup screen displays the system option:

On board SCSI [Enabled]

Available options are:

Disabled
Enabled

On Board VGA

This option specifies whether there is an on-board video device on your system.

The Setup screen displays the system option:

On board VGA [Enabled]

Available options are:

Disabled
Enabled

Plug & Play O/S

This option indicates whether or not the operating system installed in the computer is Plug and Play-aware. AMIBIOS only detects and enables PnP ISA adapter cards which are required for system boot. An operating system which is PnP-aware detects and enables all other PnP-aware adapter cards. Set this option to **No** if the operating system (such as DOS, OS/2, Windows 3.x) does *not* use PnP.

NOTE: You must set this option correctly or PnP-aware adapter cards installed in your computer will not be configured properly.

The Setup screen displays the system option:

Plug & Play O/S [No]

Two options are available:

- Select **No** to allow AMIBIOS to configure the devices in the system.
- Select **Yes** if your system has a Plug and Play operating system and you want to allow the operating system to configure all Plug and Play (PnP) devices which are not required for bootup.

PCI Latency Timer

This option specifies the latency of all PCI devices on the PCI Local Bus. The settings are in units equal to PCI clocks.

The Setup screen displays the system option:

PCI Latency Timer [64]

Available options are:

32	160
64	192
96	224
128	248

Allocate IRQ to PCI VGA

This option allows you to assign an IRQ to a PCI VGA card if the card requests an IRQ.

The Setup screen displays the system option:

Allocate IRQ to PCI VGA [Yes]

Available options are:

Yes
No

Palette Snooping

This option, when set to **Enabled**, indicates to the PCI devices that an ISA graphics device is installed in the system so the card will function correctly.

The Setup screen displays the system option:

Palette Snooping [Disabled]

Available options are:

Disabled
Enabled

PCI IDE BusMaster

This option specifies whether the IDE controller on the PCI Local Bus has bus mastering capability for reading and writing to IDE drives. The IDE drive(s) must support PCI bus mastering.

The Setup screen displays the system option:

PCI IDE BusMaster [Disabled]

Available options are:

Disabled
Enabled

OffBoard PCI/ISA IDE Card

This option specifies the PCI expansion slot on the SBC where the off-board PCI IDE controller is installed, if any.

The Setup screen displays the system option:

OffBoard PCI/ISA IDE Card [Auto]

Available options are:

Auto
PCI Slot1
PCI Slot2
PCI Slot3
PCI Slot4
PCI Slot5
PCI Slot6

If you select any value other than **Auto**, the following options and their default values are added to the screen:

OffBoard PCI IDE Primary IRQ/OffBoard PCI IDE Secondary

These options specify the PCI interrupts used by the primary and secondary IDE channels on the off-board PCI IDE controller. You may use the **INTA**, **INTB**, **INTC** and **INTD** options to assign IRQs to the Int Pin used by the specified channel.

If the **OffBoard PCI/ISA IDE Card** option is set to **Auto**, these options are not available.

The Setup screen displays the system options:

OffBoard PCI IDE Primary IRQ [Disabled]
OffBoard PCI IDE Secondary [Disabled]

Available options are:

Disabled
INTA
INTB
INTC
INTD
Hardwired

IRQ3/IRQ4/IRQ5/IRQ7/IRQ9/IRQ10/IRQ11/IRQ12/IRQ14/IRQ15

These options indicate whether or not the specified interrupt request (IRQ) is available for use by the system for PCI/Plug and Play devices or is reserved for use by legacy devices. This allows you to specify IRQs for use by legacy ISA adapter cards.

The IRQ setup options indicate whether AMIBIOS should remove an IRQ from the pool of available IRQs passed to BIOS configurable devices.

The Setup screen displays the system option:

IRQ# [Available]

where # is the number of the interrupt request (IRQ)

Two options are available:

- Select **Available** to make the specified IRQ available for use by PCI/PnP devices.
- Select **Reserved** to reserve the specified IRQ for use by legacy ISA devices.

DMA Channels 0, 1, 3, 5, 6 and 7

These options indicate whether or not the specified DMA channel is available for use by the system for PCI/Plug and Play devices or is reserved for use by legacy ISA devices.

The Setup screen displays the system option:

DMA Channel # [Available]

where # is the DMA Channel number

Two options are available:

- **Available** indicates that the specified DMA channel is available for use by PCI/PnP devices.
- **Reserved** indicates the specified DMA channel is reserved for use by legacy ISA devices.

Reserved Memory Size

This option specifies the size of the memory area reserved for legacy ISA devices.

If this option is set to **Disabled**, the **Reserved Memory Address** option is not available.

The Setup screen displays the system option:

Reserved Memory Size [Disabled]

Available options are:

Disabled
16k
32k
64k

Reserved Memory Address

This option specifies the beginning address (in hexadecimal) of the ROM memory area reserved for use by legacy ISA adapter cards.

If the **Reserved Memory Size** option is set to **Disabled**, this option is not available.

The Setup screen displays the system option:

Reserved Memory Address [C8000]

Available options are:

C0000	D0000
C4000	D4000
C8000	D8000
CC000	DC000

Saving and Exiting

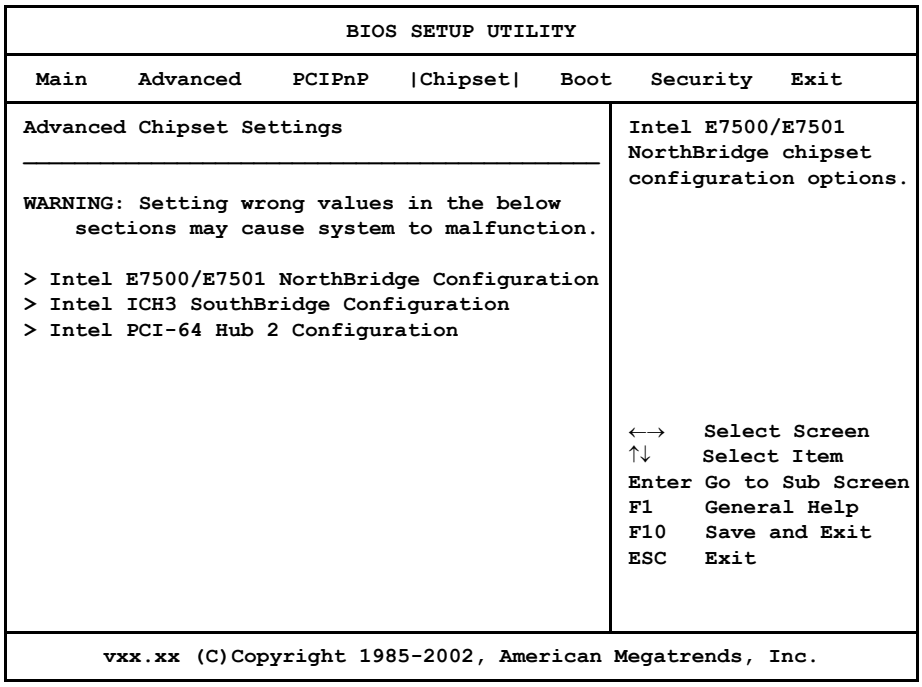
When you have made all desired changes to PCIPnP Setup, you may make changes to other Setup options by using the right and left arrow keys to access other menus. When you have made all of your changes, you may save them by selecting the Exit menu, or you may press **<Esc>** at any time to exit the BIOS Setup Utility without saving the changes.

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Chapter 6 Chipset Setup

CHIPSET SETUP

When you select **Chipset** from the BIOS Setup Utility Main Menu, the following Setup screen displays:



Chipset Setup Screen

When you display the Chipset Setup screen, the format is similar to the sample shown above, allowing you to continue to subscreens designed to change parameters for each of the Chipset Setup options. Highlight the option you wish to change and press **<Enter>** to proceed to the appropriate subscreen.

NOTE: The values on the Chipset Setup subscreens do not necessarily reflect the values appropriate for your SBC. Refer to the explanations following each screen for specific instructions about entering correct information.

CHIPSET SETUP OPTIONS

NOTE: Do not change the values for any Chipset Setup option unless you understand the impact on system operation. Depending on your system configuration, selection of other values may cause unreliable system operation.

Intel E7500/E7501 NorthBridge Configuration

The **Intel E7500/E7501 NorthBridge Configuration** subscreen allows you to change the setting of the following option:

- Chipset Memory Remap Feature

Intel ICH3 SouthBridge Configuration

The options on the **ICH3 SouthBridge Configuration** subscreen allow you to set up or modify parameters to configure the Intel ICH3 SouthBridge chip. The following options may be modified:

- ICH3 Dev31 Func1, IDE
- ICH3 Dev31 Func3, SMBUS
- ICH3 Dev29 Func0, USB#1
- LPC 4Eh-4Fh Decode
- LPC 2Eh-2Fh Decode
- ISA Bus
- IOAPIC
- Extended IOAPIC
- CPU B.I.S.T.
- ICH3 DMA Collection
- DMA Types 0 through 7

The **Intel PCI-64 Hub 2 Configuration** subscreen allows you to change the setting of the following option:

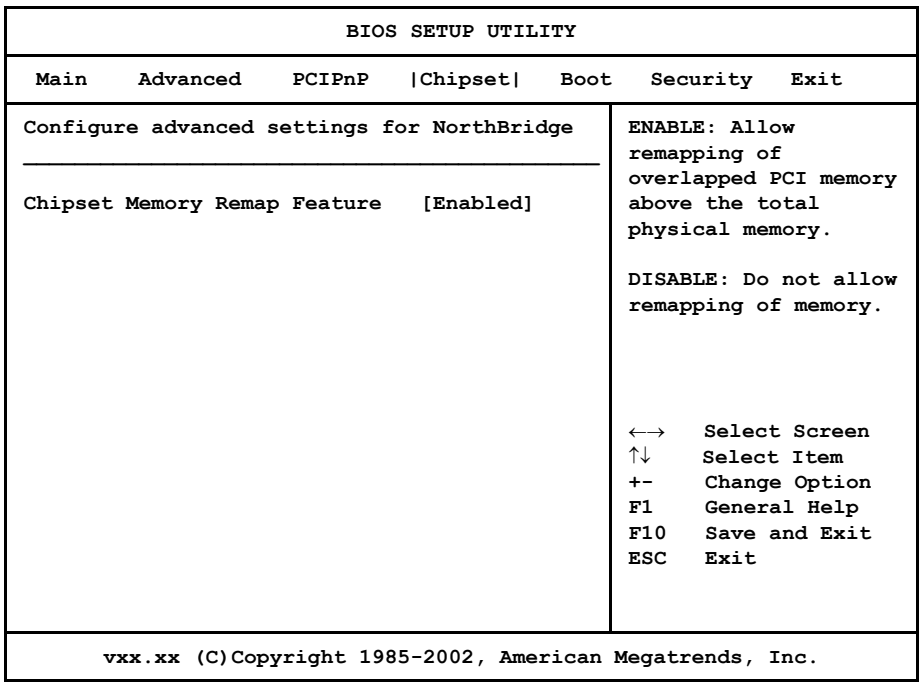
- PCI Bus Frequency

Saving and Exiting

When you have made all desired changes to **Chipset Setup**, you may make changes to other Setup options by using the right and left arrow keys to access other menus. When you have made all of your changes, you may save them by selecting the **Exit** menu, or you may press **<Esc>** at any time to exit the BIOS Setup Utility without saving the changes.

INTEL E7500/ E7501 NORTHBRIDGE CONFIGURATION

When you select **Intel E7500/E7501 NorthBridge Configuration** from the Chipset Setup Screen, the following Setup screen displays:



Intel E7500/E7501 NorthBridge Configuration Screen

When you display the Intel E7500/E7501 NorthBridge Configuration screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

E7500/E7501 NORTHBRIDGE CONFIGURATION OPTIONS

The description for the system option listed below shows the value as it appears if you have not yet run Chipset Setup. Once you change the setting, the new setting displays each time Chipset Setup is run.

Chipset Memory Remap Feature

This option allows the remapping of overlapped PCI memory above the total physical memory.

The Setup screen displays the system option:

Chipset Memory Remap Feature [Enabled]

Available options are:

Disabled
Enabled

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INTEL ICH3 SOUTHBRIDGE CONFIGURATION

When you select **Intel ICH3 SouthBridge Configuration** from the Chipset Setup Screen, the following Setup screen displays:

```
                        BIOS SETUP UTILITY
 Main    Advanced    PCIPnP   |Chipset|   Boot   Security   Exit
Configure advanced settings for SouthBridge   Enable/Disable ICH3
_____________________________________________ IDE Controller
ICH3 Dev31 Func1, IDE          [Enabled]      function.
ICH3 Dev31 Func3, SMBUS        [Enabled]
ICH3 Dev29 Func0, USB#1        [Enabled]

LPC 4Eh-4Fh Decode             [Enabled]
LPC 2Eh-2Fh Decode             [Enabled]

ISA BUS                        [Enabled]
IOAPIC                         [Enabled]
Extended IOAPIC                [Enabled]
CPU B.I.S.T.                   [Enabled]
ICH3 DMA Collection            [Enabled]

DMA-0 Type                     [PC/PCI]
DMA-1 Type                     [PC/PCI]      ←→   Select Screen
DMA-2 Type                     [LPC DMA]     ↑↓   Select Item
DMA-3 Type                     [PC/PCI]      +-   Change Option
DMA-5 Type                     [PC/PCI]      F1   General Help
DMA-6 Type                     [PC/PCI]      F10  Save and Exit
DMA-7 Type                     [PC/PCI]      ESC  Exit

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```

Intel ICH3 SouthBridge Configuration Screen

When you display the Intel ICH3 SouthBridge Configuration screen, the format is similar to the sample shown above, except the screen does not display all of the options at one time. If you need to change other options, use the down arrow key to locate the appropriate option. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

INTEL ICH3 SOUTHBRIDGE CONFIGURATION OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not yet run Chipset Setup. Once values have been defined, they display each time Chipset Setup is run.

ICH3 Dev31 Func1, IDE

This option allows you to enable or disable ICH3 IDE Controller function.

The Setup screen displays the system option:

ICH3 Dev31 Func1, IDE [Enabled]

Available options are:

Disabled
Enabled

ICH3 Dev31 Func3, SMBUS

This option allows you to enable or disable ICH3 SMBUS Controller function.

The Setup screen displays the system option:

ICH3 Dev31 Func3, SMBUS [Enabled]

Available options are:

Disabled
Enabled

ICH3 Dev31 Func0, USB#1

This option allows you to enable or disable USB Host Controller #1 function.

The Setup screen displays the system option:

ICH3 Dev31 Func0, USB#1 [Enabled]

Available options are:

Disabled
Enabled

LPC 4Eh-4Fh Decode/LPC 2Eh-2Fh Decode

The **LPC 4Eh-4Fh Decode** option allows you to enable or disable decoding of I/O locations 4Eh and 4Fh to the LPC interface. The **LPC 2Eh-2Fh Decode** option cannot be modified.

The Setup screen displays the system options:

LPC 4Eh-4Fh Decode [Enabled]
LPC 2Eh-2Fh Decode [Enabled]

Available options are:

Disabled
Enabled

ISA BUS

This option allows you to enable or disable the PCI/ISA on-board bridge.

If this option is set to **Enabled**, the **ICH3 Positive Decode** option is not available.

The Setup screen displays the system option:

ISA BUS [Enabled]

Available options are:

Disabled
Enabled

ICH3 Positive Decode

This option allows you to enable or disable positive decode in ICH3. Set this option to **Enabled** if the on-board PCI/1SA bridge is present.

If the **ISA BUS** option is set to **Disabled**, this option is not available.

The Setup screen displays the system option:

ICH3 Positive Decode [Enabled]

Available options are:

Disabled
Enabled

IOAPIC

This option allows you to enable or disable the ICH3 IOAPIC function.

The Setup screen displays the system option:

IOAPIC [Enabled]

Available options are:

Disabled
Enabled

Extended IOAPIC

This option allows you to enable or disable the extended mode of the ICH3 IOAPIC function.

The Setup screen displays the system option:

Extended IOAPIC [Enabled]

Available options are:

Disabled
Enabled

CPU B.I.S.T.

This option allows you to enable or disable the CPU Built-In Self Test.

The Setup screen displays the system option:

CPU B.I.S.T. [Enabled]

Available options are:

Disabled
Enabled

ICH3 DMA Collection

This option allows you to enable or disable the DMA collection buffer.

The Setup screen displays the system option:

ICH3 DMA Collection [Enabled]

Available options are:

Disabled
Enabled

DMA Types 0, 1, 2, 3, 5, 6 and 7

This option allows you to select the type of DMA performed on the specified channel.

The Setup screen displays the system option:

DMA-# Type [PC/PCI]

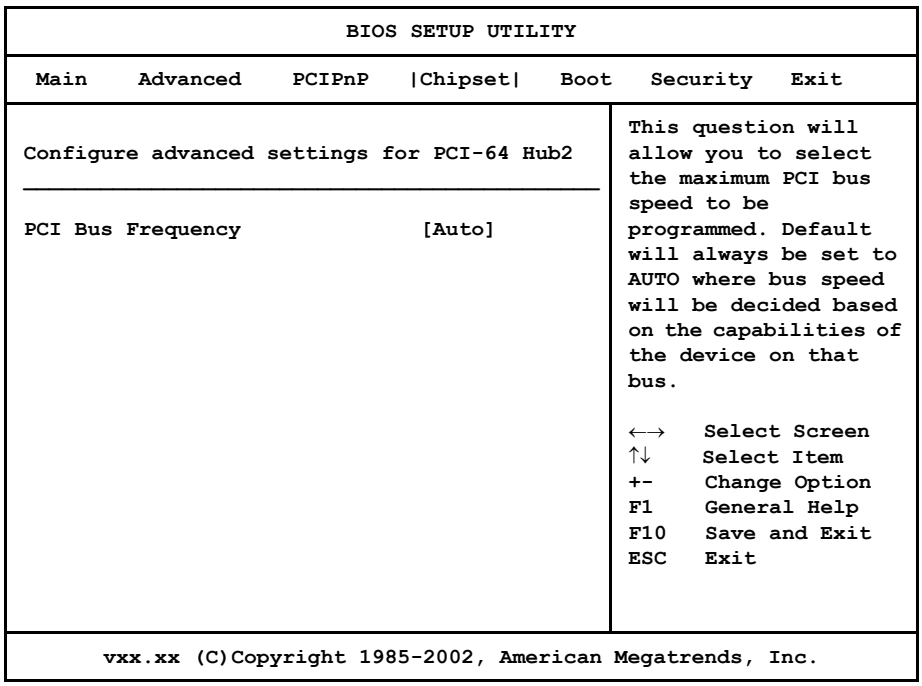
where # is the DMA number

Available options are:

PC/PCI
LPC DMA

INTEL PCI-64 HUB 2 CONFIGURATION

When you select **Intel PCI-64 Hub 2 Configuration** from the Chipset Setup Screen, the following Setup screen displays:



Intel PCI-64 Hub 2 Configuration Screen

When you display the Intel PCI-64 Hub 2 Configuration screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

INTEL PCI-64 HUB 2 CONFIGURATION OPTIONS

The description for the system option listed below shows the value as it appears if you have not yet run Chipset Setup. Once you change the setting, the new setting displays each time Chipset Setup is run.

PCI Bus Frequency

This option allows you to select the maximum bus speed to be programmed. If this option is set to **Auto**, bus speed is decided based on the capabilities of the device on the bus.

The Setup screen displays the system option:

PCI Bus Frequency [Auto]

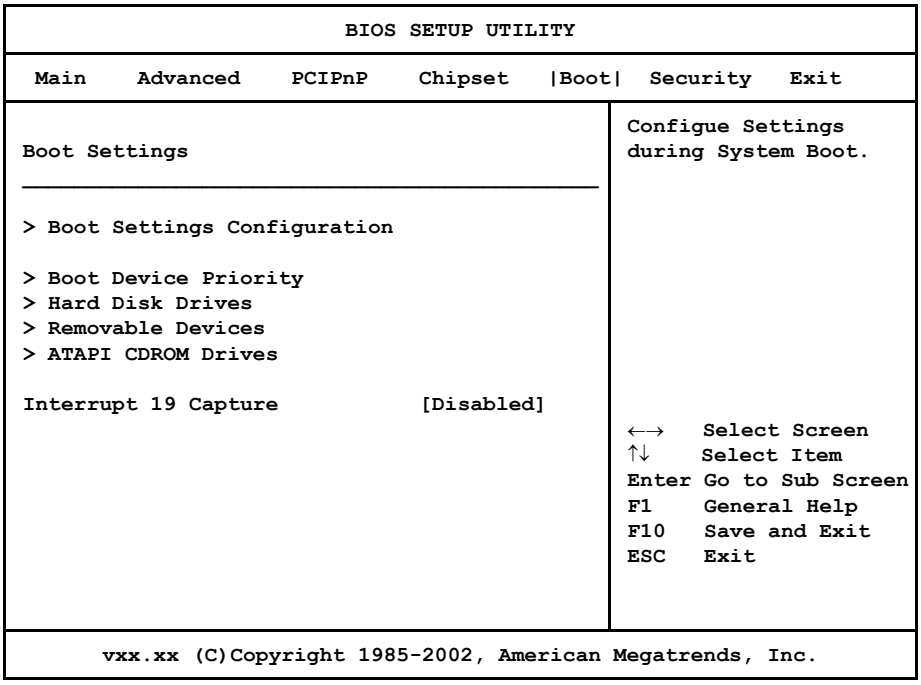
Available options are:

33 MHz
66 MHz
100 MHz
133 MHz
Auto

Chapter 7 Boot Setup

BOOT SETUP

When you select **Boot** from the BIOS Setup Utility Main Menu, the following Setup screen displays:



Boot Setup Screen

When you display the Boot Setup screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

Some of the options on this screen allow you to continue to subscreens designed to change parameters for that particular option. Highlight the option you wish to change and press **<Enter>** to proceed to the appropriate subscreen.

NOTE: If no device is found for one of the device types, the line item for that device type does not display.

BOOT SETUP OPTIONS

The descriptions for the system option listed below show the values as they appear if you have not yet run Boot Setup. Once values have been changed, they display each time Boot Setup is run. You may also continue to subscreens to specify boot parameters and the boot sequence of bootable devices in your system.

Boot Settings Configuration

The options on the **Boot Settings Configuration** subscreen allow you to set up or modify parameters for boot procedures. The following options may be modified:

- Quick Boot
- Quiet Boot
- AddOn ROM Display Mode
- Bootup Num-Lock
- PS/2 Mouse Support
- System Keyboard
- Boot To OS/2
- Wait For 'F1' If Error
- Hit 'DEL' Message Display

Boot Device Priority

The options on the **Boot Device Priority** subscreen specify the order in which AMIBIOS attempts to boot devices available in the system. It allows you to select the type of drive which will be booted first, second, third, etc. If there are multiple drives of a particular type, you may specify the order in which each drive of that type will be selected by using the other options on the Boot Setup Menu.

Hard Disk Drives

The **Hard Disk Drives** subscreen specifies the boot sequence of the hard drives available in the system.

Removable Devices

The **Removable Devices** subscreen specifies the boot sequence of the removable devices available in the system.

ATAPI CDROM Drives

The **ATAPI CDROM Drives** subscreen specifies the boot sequence of the ATAPI CDROM devices available in the system.

Interrupt 19 Capture

The Setup screen displays the system option:

Interrupt 19 Capture [Disabled]

Available options are:

Disabled
Enabled

Saving and Exiting

When you have made all desired changes to **Boot Setup**, you may make changes to other Setup options by using the right and left arrow keys to access other menus. When you have made all of your changes, you may save them by selecting the **Exit** menu, or you may press **<Esc>** at any time to exit the BIOS Setup Utility without saving the changes.

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BOOT SETTINGS CONFIGURATION

When you select **Boot Settings Configuration** from the Boot Setup Menu, the following Setup screen displays:

```
                        BIOS SETUP UTILITY
                                |Boot|
Boot Settings Configuration                  Allows BIOS to skip
_____________________________________________certain tests while
                                             booting. This will
Quick Boot                    [Disabled]     decrease the time
Quiet Boot                    [Disabled]     needed to boot the
AddOn ROM Display Mode        [Force BIOS]   system.
Bootup Num-Lock               [On]
PS/2 Mouse Support            [Enabled]
System Keyboard               [Present]
Boot To OS/2                  [No]
Wait For 'F1' If Error        [Enabled]
Hit 'DEL' Message Display     [Enabled]
                                             ←→   Select Screen
                                             ↑↓   Select Item
                                             +-   Change Option
                                             F1   General Help
                                             F10  Save and Exit
                                             ESC  Exit
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```

Boot Settings Configuration Screen

When you display the Boot Settings Configuration screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

BOOT SETTINGS CONFIGURATION OPTIONS

The descriptions for the system options listed below show the values as they appear if you have not run the BIOS Setup Utility program yet. Once values have been defined, they display each time the BIOS Setup Utility is run.

Quick Boot

This option allows you to have the AMIBIOS boot quickly when the computer is powered on or go through more complete testing. If you set the **Quick Boot** option to **Enabled**, the BIOS skips certain tests while booting and decreases the time needed to boot the system.

The Setup screen displays the system option:

Quick Boot **[Disabled]**

Available options are:

Disabled
Enabled

Quiet Boot

This option specifies what will be displayed on the screen while the system is performing the POST routines when the computer is powered on or a soft reboot is performed.

The Setup screen displays the system option:

Quiet Boot [Disabled]

Two options are available:

- Select **Disabled** to display normal POST messages.
- Select **Enabled** to display the OEM logo instead of the POST messages.

AddOn ROM Display Mode

This option specifies the system display mode which is set at the time the AMIBIOS post routines initialize an optional option ROM.

The Setup screen displays the system option:

AddOn ROM Display Mode [Force BIOS]

Two options are available:

- Select **Force BIOS** to use the display mode currently being used by AMIBIOS.
- Select **Keep Current** to use the current display mode.

BootUp Num-Lock

This option enables you to turn off the Num-Lock option on the enhanced keyboard when the system is powered on. If Num-Lock is turned off, the arrow keys on the numeric keypad can be used, as well as the other set of arrow keys on the enhanced keyboard.

The Setup screen displays the system option:

BootUp Num-Lock [On]

Available options are:

Off
On

PS/2 Mouse Support

This option indicates whether or not a PS/2-type mouse is supported.

The Setup screen displays the system option:

PS/2 Mouse Support [Enabled]

Available options are:

Disabled
Enabled

System Keyboard

This option indicates whether or not a keyboard is attached to the computer.

The Setup screen displays the system option:

System Keyboard [Present]

Available options are:

Absent
Present

Boot To OS/2

This option should be set to **Yes** if you are running the IBM OS/2 operating system and using more than 64MB of system memory on the SBC.

The Setup screen displays the system option:

Boot To OS/2 [No]

Available options are:

No
Yes

Wait For 'F1' If Error

Before the system boots up, the AMIBIOS executes the Power-On Self Test (POST) routines, a series of system diagnostic routines. If any of these tests fail but the system can still function, a non-fatal error has occurred. The AMIBIOS responds with an appropriate error message followed by:

Press F1 to RESUME

If this option is set to **Disabled**, a non-fatal error does not generate the "Press F1 to RESUME" message. The AMIBIOS still displays the appropriate message, but

continues the booting process without waiting for the **<F1>** key to be pressed. This eliminates the need for any user response to a non-fatal error condition message. Non-fatal error messages are listed in *Appendix A - BIOS Messages*.

The Setup screen displays the system option:

Wait For 'F1' If Error [Enabled]

Available options are:

Disabled
Enabled

Hit 'DEL' Message Display

The "Hit DEL to run Setup" message displays when the system boots up. Disabling this option prevents the message from displaying.

The Setup screen displays the system option:

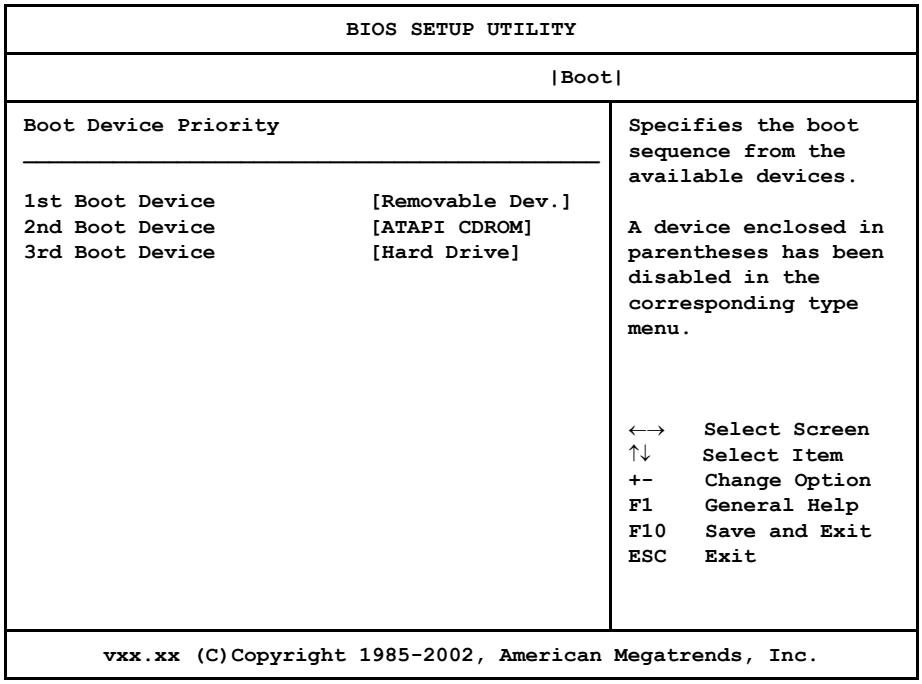
Hit 'DEL' Message Display [Enabled]

Available options are:

Disabled
Enabled

BOOT DEVICE PRIORITY

When you select **Boot Device Priority** from the Boot Setup Menu, the following Setup screen displays:



Boot Device Priority Screen

When you display the Boot Device Priority screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

NOTE: The number of line items on this screen may vary depending on the number of bootable devices available on your system.

BOOT DEVICE PRIORITY OPTIONS

1st Boot Device/2nd Boot Device/3rd Boot Device

This option specifies the device type of each boot drive from which AMIBIOS attempts to boot after the POST routines complete. Available options for each boot device line item are determined by the types of bootable devices available on your system.

The Setup screen displays the system option(s):

1st Boot Device	**[Removable Dev.]**
2nd Boot Device	**[ATAPI CDROM]**
3rd Boot Device	**[Hard Drive]**

Available options are:

Removable Dev.
ATAPI CDROM
Hard Drive
Disabled

HARD DISK DRIVES When you select **Hard Disk Drives** from the Boot Setup Menu, the following Setup screen displays:

```
                        BIOS SETUP UTILITY
                                |Boot|
Hard Disk Drives                          | Specifies the boot
_____________________________________     | sequence from the
1st Hard Disk Drive      [xxxxxxxxx]      | available devices.
2nd Hard Disk Drive      [xxxxxxxxx]      |
3rd Hard Disk Drive      [xxxxxxxxx]      |
                                          |
                                          |
                                          |
                                          |
                                          |
                                          |
                                          |
                                          |
                                          |
                                          | ←→   Select Screen
                                          | ↑↓   Select Item
                                          | +-   Change Option
                                          | F1   General Help
                                          | F10  Save and Exit
                                          | ESC  Exit
      vxx.xx (C)Copyright 1985-2002, American Megatrends, Inc.
```

Hard Disk Drives Screen

When you display the Hard Disk Drives screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

NOTE: This screen is available only if there is at least one hard disk drive on your system. The number of line items is determined by the number of hard disk drives available.

HARD DISK DRIVES OPTIONS The SBC supports up to four hard disk drives through a primary and secondary controller in a master/slave configuration.

1st Hard Drive/2nd Hard Drive/3rd Hard Drive

When the system boots up, it searches for all hard drives and displays the description of each disk drive(s) it has detected.

If you have more than one hard disk drive, you may change the order in which the system will attempt to boot the available hard drives by changing these line items. The number of options displayed for each line item depends on the number of hard disk drives in your system.

Disabled is also available as an option if you do not want a particular drive to be included in the boot sequence.

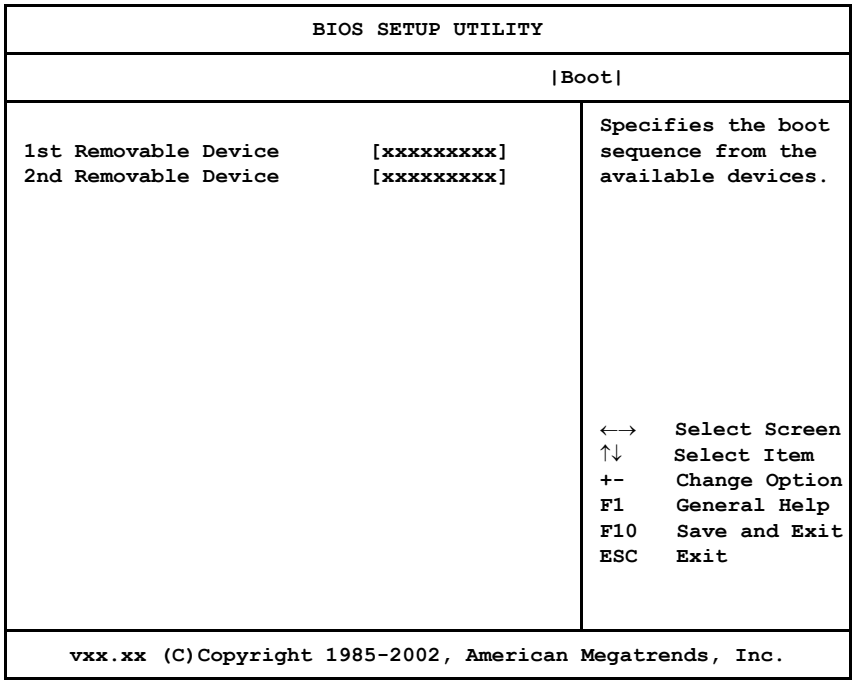
The Setup screen displays the system options:

1st Hard Disk Drive	[xxxxxxxxx]
2nd Hard Disk Drive	[xxxxxxxxx]
3rd Hard Disk Drive	[xxxxxxxxx]

where xxxxxxxxx is the description of the hard drive

REMOVABLE DEVICES

When you select **Removable Devices** from the Boot Setup Menu, the following Setup screen displays:



Removable Devices Screen

When you display the Removable Devices screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

NOTE: This screen is available only if there is at least one removable device on your system. The number of line items is determined by the number of removable devices available.

REMOVABLE DEVICES OPTIONS

The SBC supports multiple removable devices and allows you to change the boot sequence of these devices.

1st Removable Device/2nd Removable Device

When the system boots up, it searches for all removable devices and displays the description of each device it has detected.

If you have more than one removable device, you may change the order in which the system will attempt to boot the available devices by changing these line items. The number of options displayed for each line item depends on the number of removable devices in your system.

Disabled is also available as an option if you do not want a particular device to be included in the boot sequence.

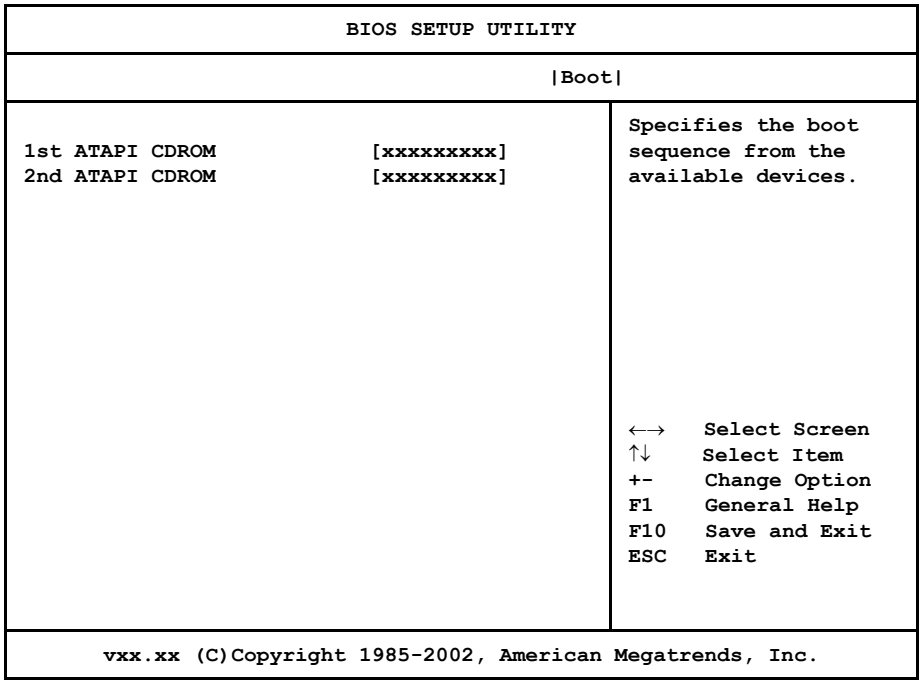
The Setup screen displays the system option:

1st Removable Device [xxxxxxxxx]
2nd Removable Device [xxxxxxxxx]

where xxxxxxxxx is the description of the removable device (e.g., floppy drive, IOMEGA ZIP drive, etc.)

ATAPI CDROM DRIVES

When you select **ATAPI CDROM Drives** from the Boot Setup Menu, the following Setup screen displays:



ATAPI CDROM Drives Screen

When you display the ATAPI CDROM Drives screen, the format is similar to the sample shown above. Highlight the option you wish to change and press **<Enter>** to display the available settings. Select the appropriate setting and press **<Enter>** again to accept the highlighted value.

NOTE: This screen is available only if there is at least one ATAPI CDROM drive on your system. The number of line items is determined by the number of ATAPI CDROM drives available.

ATAPI CDROM DRIVES OPTIONS

The SBC supports multiple ATAPI CD-ROM devices and allows you to change the boot sequence of these devices.

1st ATAPI CDROM/2nd ATAPI CDROM

When the system boots up, it searches for all ATAPI CD-ROM drives and displays the description of each drive it has detected.

If you have more than one ATAPI CD-ROM drive, you may change the order in which the system will attempt to boot the available drives by changing these line items. The number of options displayed for each line item depends on the number of ATAPI CD-ROM devices in your system.

Disabled is also available as an option if you do not want a particular drive to be included in the boot sequence.

The Setup screen displays the system option:

1st ATAPI CDROM [xxxxxxxxx]
2nd ATAPI CDROM [xxxxxxxxx]

where xxxxxxxxx is the description of the ATAPI CD-ROM drive

Appendix A BIOS Messages

BIOS BEEP CODES

Errors may occur during the POST (Power-On Self Test) routines which are performed each time the system is powered on.

Non-fatal errors are those which, in most cases, allow the system to continue the bootup process. The error message normally appears on the screen. See *BIOS Error Messages* later in this section for descriptions of these messages.

Fatal errors are those which will not allow the system to continue the bootup procedure.

These fatal errors are usually communicated through a series of audible beeps. Each error message has its own specific beep code, defined by the number of beeps following the error detection. The following table lists the errors which are communicated audibly.

Beep Count	Description
1	Memory refresh timer error
2	Parity Error
3	Main memory read/write test error
4	Timer not operational
5	Processor error
6	Keyboard controller BAT test error
7	General exception error
8	Display memory error
9	ROM checksum error
10	CMOS shutdown register read/write error
11	Cache memory bad

BIOS BEEP CODE TROUBLESHOOTING

Beep Count	Troubleshooting Action
1, 2 or 3	Reseat the memory or replace with known good modules.
4-7, 9-11	Fatal error. Perform the following steps before calling Technical Support.
	Remove all expansion cards and and try to reboot. If the beep code is still generated, call Technical Support. If the beep code is not generated, one of the add-in cards is causing the malfunction. Insert the cards back into the system one at a time until the problem recurs. This will indicate the malfunctioning card.
8	The board may be faulty. Call Technical Support.

BIOS ERROR MESSAGES

If a non-fatal error occurs during the POST routines performed each time the system is powered on, the error message will appear on the screen in the following format:

ERROR Message Line 1
ERROR Message Line 2
Press F1 to Resume

Note the error message and press the **<F1>** key to continue with the bootup procedure.

NOTE: If the "Wait for 'F1' If Any Error" option in the Advanced Setup portion of the BIOS Setup Program has been set to **Disabled**, the "Press F1 to Resume" prompt will not appear on the last line.

For most of the error messages, there is no ERROR Message Line 2. Generally, for those messages containing an ERROR Message Line 2, the text will be "RUN SETUP UTILITY." Pressing the **<F1>** key will invoke the BIOS Setup Utility.

A description of each error message appears below.

MEMORY ERRORS

Message	Description
Gate20 Error	The BIOS is unable to properly control the SBC's Gate A20 function, which controls access to memory over 1MB. This may indicate a problem with the board.
Multi-Bit ECC Error	This message only occurs on systems using ECC enabled memory modules. ECC memory has the ability to correct single-bit errors that may occur from faulty memory modules. A multiple bit corruption of memory has occurred, and the ECC memory algorithm cannot correct it. This may indicate a defective memory module.
Parity Error	Fatal memory parity error. System halts after displaying this message.

BOOT ERRORS

Message	Description
Boot Failure ...	This is a generic message indicating the BIOS could not boot from a particular device. This message is usually followed by other information concerning the device.
Invalid Boot Diskette	A diskette was found in the drive, but it is not configured as a bootable diskette.
Drive Not Ready	The BIOS was unable to access the drive because it indicated it was not ready for data transfer. This is often reported by drives when no media is present.

BIOS ERROR MESSAGES (CONTINUED)

BOOT ERRORS (continued)

Message	Description
A: Drive Error	The BIOS attempted to configure the A: drive during POST, but was unable to properly configure the device. This may be due to a bad cable or faulty diskette drive.
B: Drive Error	The BIOS attempted to configure the B: drive during POST, but was unable to properly configure the device. This may be due to a bad cable or faulty diskette drive.
Insert BOOT diskette in A:	The BIOS attempted to boot from the A: drive, but could not find a proper boot diskette.
Reboot and Select proper Boot device or Insert Boot Media in selected Boot device	BIOS could not find a bootable device in the system and/or removable media drive does not contain media.
NO ROM BASIC	This message occurs on some systems when no bootable device can be detected.

STORAGE DEVICE ERRORS

Message	Description
The following errors are typically displayed when the BIOS is trying to detect and configure IDE/ ATAPI devices in POST.	
XXXXXX Hard Disk Error XXXXXX - ATAPI Incompatible	Messages in this format indicate that the specified device could not be properly initialized by the BIOS. Possible message are: Primary Master Hard Disk Error Primary Slave Hard Disk Error Secondary Master Hard Disk Error Secondary Slave Hard Disk Error Primary Master Drive - ATAPI Incompatible Primary Slave Drive - ATAPI Incompatible Secondary Master Drive - ATAPI Incompatible Secondary Slave Drive - ATAPI Incompatible
The following messages can be reported by an ATAPI device using the S.M.A.R.T. error reporting standard. The S.M.A.R.T. failure message may indicate the need to replace the hard disk.	
S.M.A.R.T. Capable but Command Failed	The BIOS tried to send a S.M.A.R.T. message to a hard disk, but the command transaction failed.
S.M.A.R.T. Command Failed	The BIOS tried to send a S.M.A.R.T. message to a hard disk, but the command transaction failed.
S.M.A.R.T. Status BAD, Backup and Replace	A S.M.A.R.T. capable hard disk sends this message when it detects an imminent failure.
S.M.A.R.T. Capable and Status BAD	A S.M.A.R.T. capable hard disk sends this message when it detects an imminent failure.

BIOS ERROR MESSAGES (CONTINUED)

VIRUS RELATED ERRORS

Message	Description
The following messages only display if Virus Detection is enabled in the BIOS Setup Utility.	
BootSector Write !!	The BIOS has detected software attempting to write to a drive's boot sector. This is flagged as possible virus activity.
VIRUS: Continue (Y/N)?	The BIOS has detected possible virus activity.

SYSTEM CONFIGURATION ERRORS

Message	Description
DMA-2 Error	Error initializing secondary DMA controller. This is a fatal error, often indicating a problem with system hardware.
DMA Controller Error	POST error while trying to initialize the DMA controller. This is a fatal error, often indicating a problem with system hardware.
Checking NVRAM..Update Failed	BIOS could not write to the NVRAM block. This message appears when the FLASH part is write-protected or if there is no FLASH part (system uses a PROM or EPROM).
Microcode Error	BIOS could not find or load the CPU Microcode Update to the CPU. This message only applies to INTEL CPUs. The message is most likely to appear when a brand new CPU is installed in an SBC with an outdated BIOS. In this case, the BIOS must be updated to include the Microcode Update for the new CPU.
NVRAM Checksum Bad, NVRAM Cleared	There was an error while validating the NVRAM data. This causes POST to clear the NVRAM data.
Resource Conflict	More than one system device is trying to use the same non-shareable resources (memory or I/O).
NVRAM Ignored	The NVRAM data used to store Plug and Play (PnP) data was not used for system configuration in POST.
NVRAM Bad	The NVRAM data used to store Plug and Play (PnP) data was not used for system configuration in POST due to a data error.
Static Resource Conflict	Two or more static devices are trying to use the same resource space (usually memory or I/O).
PCI I/O Conflict	A PCI adapter generated an I/O resource conflict when configured by BIOS POST.
PCI ROM Conflict	A PCI adapter generated an I/O resource conflict when configured by BIOS POST.
PCI IRQ Conflict	A PCI adapter generated an I/O resource conflict when configured by BIOS POST.
PCI IRQ Routing Table Error	BIOS POST (DIM code) found a PCI device in the system but was unable to figure out how to route an IRQ to the device. Usually this error is caused by an incomplete description of the PCI Interrupt Routine of the system.

BIOS ERROR MESSAGES (CONTINUED)

SYSTEM CONFIGURATION ERRORS (continued)

Message	Description
Timer Error	Indicates an error while programming the count register of channel 2 of the 8254 timer. This may indicate a problem with system hardware.
Interrupt Controller-1 Error	BIOS POST could not initialize the Master Interrupt Controller. This may indicate a problem with system hardware.
Interrupt Controller-2 Error	BIOS POST could not initialize the Slave Interrupt Controller. This may indicate a problem with system hardware.

CMOS ERRORS

Message	Description
CMOS Date/Time Not Set	The CMOS Date and/or Time are invalid. This error can be resolved by readjusting the system time in the BIOS Setup Utility.
CMOS Battery Low	CMOS Battery is low. This message usually indicates that the CMOS battery needs to be replaced. It could also appear when the user intentionally discharges the CMOS battery.
CMOS Settings Wrong	CMOS settings are invalid. This error can be resolved by using the BIOS Setup Utility.
CMOS Checksum Bad	CMOS contents failed the Checksum check. Indicates that the CMOS data has been changed by a program other than the BIOS or that the CMOS is not retaining its data due to malfunction. This error can typically be resolved by using the BIOS Setup Utility.

MISCELLANEOUS ERRORS

Message	Description
Keyboard Error	Keyboard is not present or the hardware is not responding when the keyboard controller is initialized.
Keyboard/Interface Error	Keyboard Controller failure. This may indicate a problem with system hardware.
System Halted	The system has been halted. A reset or power cycle is required to reboot the machine. This message appears after a fatal error has been detected.

BOOTBLOCK INITIALIZATION CODE CHECKPOINTS

The Bootblock initialization code sets up the chipset, memory and other components before system memory is available. The following table describes the type of checkpoints that may occur during the Bootblock initialization portion of the BIOS:

Checkpoint	Description
Before D1	Early chipset initialization is done. Early super I/O initialization is done including RTC and keyboard controller. NMI is disabled.
D1	Perform keyboard controller BAT test. Check if waking up from power management suspend state. Save power-on CPUID value in scratch CMOS.
D0	Go to flat mode with 4GB limit and GA20 enabled. Verify the bootblock checksum.
D2	Disable cache before memory detection. Execute full memory sizing module. Verify that flat mode is enabled.
D3	If memory sizing module not executed, start memory refresh and do memory sizing in Bootblock code. Do additional chipset initialization. Reenable cache. Verify that flat mode is enabled.
D4	Test base 512K memory. Adjust policies and cache first 8MB. Set stack.
D5	Bootblock code is copied from ROM to lower system memory and control is given to it. BIOS now executes out of RAM.
D6	Both key sequence and OEM specific method is checked to determine if BIOS recovery is forced. Main BIOS checksum is tested. If BIOS recovery is necessary, control flows to checkpoint E0. See the *Bootblock Recovery Code Checkpoints* section of this appendix for more information.
D7	Restore CPUID value back into register. The Bootblock-Runtime interface module is moved to system memory and control is given to it. Determine whether to execute serial flash.
D8	The Runtime module is uncompressed into memory. CPUID information is stored in memory.
D9	Store the Uncompressed pointer for future use in PMM. Copy Main BIOS into memory. Leave all RAM below 1MB Read/Write including E000 and F000 shadow areas but closing SMRAM.
DA	Restore CPUID value back into register. Give control to BIOS POST (ExecutePOSTKernel). See the *POST Code Checkpoints* section of this appendix for more information.

BOOTBLOCK RECOVERY CODE CHECKPOINTS

The Bootblock recovery code gets control when the BIOS determines that a BIOS recovery needs to occur because the user has forced the update or the BIOS checksum is corrupt. The following table describes the type of checkpoints that may occur during the Bootblock recovery portion of the BIOS:

Check-point	Description
E0	Initialize the floppy controller in the super I/O. Some interrupt vectors are initialized. DMA contoller is initialized. 8259 interrupt controller is initialized. L1 cache is enabled.
E9	Set up floppy controller and data. Attempt to read from floppy.
EA	Enable ATAPI hardware. Attempt to read from ARMD and ATAPI CDROM.
EB	Disable ATAPI hardware. Jump back to checkpoint E9.
EF	Read error occurred on media. Jump back to checkpoint EB.
E9 or EA	Determine information about root directory of recovery media.
F0	Search for pre-defined recovery file name in root directory.
F1	Recovery file not found.
F2	Start reading FAT table and analyze FAT to find the clusters occupied by the recovery file.
F3	Start reading the recovery file cluster by cluster.
F5	Disable L1 cache.
FA	Check the validity of the recovery file configuration to the current configuration of the flash part.
FB	Make flash write enabled through chipset and OEM specific method. Detect proper flash part. Verify that the found flash part size equals the recovery file size.
	The recovery file size does not equal the found flash part size.
F4	Erase the flash part.
FC	Program the flash part.
FD FF	The flash has been updated successfully. Make flash write disabled. Disable ATAPI hardware. Restore CPUID value back into register. Give control to F000 ROM at F000:FFF0h.

POST CODE CHECKPOINTS

The POST code checkpoints are the largest set of checkpoints during the BIOS pre-boot process. The following table describes the type of checkpoints that may occur during the POST portion of the BIOS:

Check-point	Description
03	Disable NMI, parity, video for EGA and DMA controllers. Initialize BIOS, POST, Runtime data area. Also initialize BIOS modules on POST entry and GPNV area. Initialize CMOS as mentioned in the Kernel Variable “wCMOSFlags.”
04	Check CMOS diagnostic byte to determine if battery power is OK and CMOS checksum is OK. Verify CMOS checksum manually by reading storage area. If the CMOS checksum is bad, update CMOS with power-on default values and clear passwords. Initialize status register A. Initialize data variables that are based on CMOS setup questions. Initialize both the 8259 compatible PICs in the system.
05	Initialize the interrupt controlling hardware (generally OPIC) and interrupt vector table.
06	Do read/write test to CH-2 count register. Initialize CH-0 as system timer. Install the POSTINT1Ch handler. Enable IRQ-0 in PIC for system timer interrupt. Traps INT1Ch vector to “POSTINT1ChHandlerBlock.”
08	Initialize the CPU. The BAT test is being done on KBC. Program the keyboard controller command byte is being done after auto detection of keyboard/mouse using AMI KB-5.
0A	Initialize the 8042 compatible keyboard controller.
0B	Detect the presence of PS/2 mouse.
0C	Detect the presence of keyboard in KBC port.
0E	Testing and initialization of different input devices. Also, update the Kernel variables. Traps the INT09h vector, so that the POST INT09h handler gets control for IRQ1. Uncompress all available language, BIOS logo and silent logo modules.
13	Early POST initialization of chipset registers.
24	Uncompress and initialize any platform specific BIOS modules.
30	Initialize System Management Interrupt.
2A	Initialize different devices through DIM. See *DIM Code Checkpoints* section of this appendix for more information.
2C	Initialize different devices. Detects and initializes the video adapter installed in the system.
2E	Initialize all the output devices.
31	Allocate memory for ADM module and uncompress it. Give control to ADM module for initialization. Initialize language and font modules for ADM. Activate ADM module.
33	Initialize the silent boot module. Set the window for displaying text information.
37	Display sign-on message, CPU information, setup key message and any OEM specific information.

POST CODE CHECKPOINTS (CONTINUED)

Check-point	Description
38	Initialize different devices through DIM. See *DIM Code Checkpoints* section of this appendix for more information.
39	Initialize DMAC-1 and DMAC-2.
3A	Initialize RTC date/time.
3B	Test for total memory installed in the system. Also, check for DEL or ESC keys to limit memory test. Display total memory in the system.
3C	Mid POST initialization of chipset registers.
40	Detect different devices (parallel ports, serial ports and coprocessor in CPU, etc.) successfully installed in the system and update the BDA, EBDA, etc.
50	Program the memory hole or any kind of implementation that needs an adjustment in system RAM size if needed.
52	Updates CMOS memory size from memory found in memory test. Allocates memory for Extended BIOS Data Area from base memory.
60	Initialize NUM-LOCK status and program the keyboard Typematic rate.
75	Initialize INT13 and prepare for IPL detection.
78	Initialize IPL devices controlled by BIOS and option ROMs.
7A	Initialize remaining option ROMs.
7C	Generate and write contents of ESCD in NVRAM.
84	Log errors encountered during POST.
85	Display errors to the user and get the user response for error.
87	Execute BIOS setup if needed/requested.
8C	Late POST initialization of chipset registers.
8E	Program the peripheral parameters. Enable/disable NMI as selected.
90	Late POST initialization of system management interrupt.
A0	Check boot password if installed.
A1	Clean-up work needed before booting to OS.
A2	Take care of runtime image preparation for different BIOS modules. Fill the free area in F000h segment with 0FFh.
	Initialize the Microsoft IRQ Routing Table. Prepare the runtime language module. Disable the system configuration display if needed.
A4	Initialize runtime language module.

POST CODE CHECKPOINTS (CONTINUED)

Check-point	Description
A7	Display system configuration screen if enabled. Initialize the CPU before boot, which includes the programming of the MTRRs.
A8	Prepare CPU for OS boot, including final MTRR values.
A9	Wait for user input at configuration display if needed.
AA	Uninstall POST INT1Ch vector and INT09h vector. Deinitialize the ADM module.
AB	Prepare BBS for INT19 boot.
AC	End of POST initialization of chipset registers.
B1	Save system context for ACPI.
00	Pass control to OS Loader (typically INT19h)

DIM CODE CHECKPOINTS

The Device Initialization Manager module gets control at various times during BIOS POST to initialize different buses. The following table describes the main checkpoints where the DIM module is accessed:

Check-point	Description
2A	Initialize different buses and perform the following functions: Reset, Detect and Disable (function 0); Static Device Initialization (function 1); Boot Output Device Initialization (function 2). Function 0 disables all device nodes, PCI devices and PnP ISA cards. It also assigns PCI Bus numbers. Function 1 initializes all static devices, which include manually configured on-board peripherals, memory and I/O decode windows in PCI-to-PCI bridges and non-compliant PCI devices. Static resources are also reserved. Function 2 searches for and initializes any PnP, PCI or AGP video drivers.
38	Initialize different buses and perform the following functions: Boot Input Device Initialization (function 3); IPL Device Initialization (function 4); General Device Initialization (function 5). Function 3 searches for and configures PCI input devices and detects if system has standard keyboard controller. Function 4 searches for and configures all PnP and PCI boot devices. Function 5 configures all on-board peripherals that are set to an automatic configuration and configures all remaining PnP and PCI devices.

ADDITIONAL CHECKPOINTS

While control is in the different functions, additional checkpoints are output to Port 80H as word values to identify the routines being executed.

The low byte value indicates the main POST Code Checkpoint. The high byte is divided into two nibbles and contains two sets of information. The details of the high byte of these checkpoints are detailed in the following table:

HIGH BYTE XY

The upper nibble 'X' indicates the function number that is being executed. 'X' can be from 0 to 7.

0	Function 0. Disable all devices on the bus.
1	Function 1. Initialize static devices on the bus.
2	Function 2. Initialize output devices on the bus.
3	Function 3. Initialize input devices on the bus.
4	Function 4. Initialize IPL devices on the bus.
5	Function 5. Initialize general devices on the bus.
6	Function 6. Error reporting for the bus.
7	Function 7. Initialize add-on ROMs for all buses.
8	Funciton 8. Initialize BBS ROMs for all buses.

The lower nibble 'Y' indicates the bus on which the different routines are being executed. 'Y' can be from 0 to 5.

0	Generic DIM (Device Initialization Manager)
1	On-board system devices
2	ISA devices
3	EISA devices
4	ISA PnP devices
5	PCI devices

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Declaration of Conformity

APPLICATION OF COUNCIL DIRECTIVE(S)

89/336/EEC

Standard(s) to which Conformity is Declared:

EN55024: 1998; EN55022: 1998, CLASS B
EN61000-3-2: 2000; EN61000-3-3: 1995

Manufacturer:	Chassis Plans, LLC. 8295 Aero Place, Suite 200 San Diego, CA 92123 USA Telephone: (858) 571-4330 FAX: (858) 571-6146
Type of Equipment:	PCI CPU Board
Model Name(s):	92-006090 (Also Known As: XPT/2.8E, XPT/2.8, XPT/2.66E, XPT/2.6, XPT/2.4E, XPT/2.4, XPT/2.2, XPT/2.0E, XPT/2.0A and XPT/1.8)

I, the undersigned, hereby declare that the specified equipment conforms to the Directive(s) and Standard(s) listed above.

Name: Charles B. Hinson

Title: Development Quality Assurance Manager

Date: April 2, 2003

Chassis Plans, LLC.
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