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IR104-V4 User Guide

Manufactured by
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Engineered Solutions for Embedded Applications

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PREFACE

This manual is for integrators of applications of embedded systems. It contains information on hardware requirements and interconnection to other embedded electronics.

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CHAPTER 1 Relay Output Control (ROC)

The relays are energized and de-energize through I/O writes and are grouped in two banks of eight and one bank of four. The bank I/O address is an offset from the base decoded address. If an I/O read is executed, then the content of the relay output register is accessed. This feature allows the relay data to be read back. To energize a relay to close the contact, write a logic "1" to the corresponding bit in the bank register. To de-energize (open) a relay, write a logic "0" to the corresponding bit in the bank register.

Relays are grouped as follows:

Bank 1: Outputs DO1 to DO8 I/O address = Base Address (0x00)
Bank 2: Outputs DO9 to DO16 I/O address = Base Address + 1 (0x01)
Bank 3: Outputs DO17 to DO20 I/O address = Base Address + 2 (0x02)

Table 1 : Relay Output Control I/O Map

Relay	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
ROC Bank 1	Relay8	Relay7	Relay6	Relay5	Relay4	Relay3	Relay2	Relay1
ROC Bank 2	Relay16	Relay15	Relay14	Relay13	Relay12	Relay11	Relay10	Relay9
ROC Bank 3	Not used	Not used	Not used	Not used	Relay20	Relay19	Relay18	Relay17

CHAPTER 2 Digital Input Reading (DIR)

The inputs are accessed through I/O reads and are grouped in two banks of eight and one bank of four. The bank I/O address is an offset from the base decoded address. A logic "0" read for an input indicates the corresponding physical input is "powered". A logic "1" read on any input indicates the corresponding physical input is "non-powered".

Bank 1: Inputs DI1 to DI8 I/O address = Base Address + 4 (0x04)
Bank 2: Inputs DI9 to DI16 I/O address = Base Address + 5 (0x05)
Bank 3: Inputs DI17 to DI20 I/O address = Base Address + 6 (0x06)

Table 2 : Digital Input I/O Map

Input	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
DIR Bank 1	Input8	Input7	Input6	Input5	Input4	Input3	Input2	Input1
DIR Bank 2	Input16	Input15	Input14	Input13	Input12	Input11	Input10	Input9
DIR Bank 3	Not used	Not used	Not used	Not used	Input20	Input19	Input18	Input17

CHAPTER 3 Input Change Flags (ICF)

– New with IR104 Version 4

When a change is detected on one of the inputs, the corresponding bit in the Flag register is set to logic "1". The input change flags are accessed through I/O reads and are grouped in two banks of eight and one bank of four. The bank I/O address is an offset from the base decoded address.

NOTE: An input change flag can be cleared by reading the corresponding input bank.

Bank 1: Flag F1 to F8 I/O address = Base Address + 8 (0x08)
Bank 2: Flag F9 to F16 I/O address = Base Address + 9 (0x09)
Bank 3: Flag F17 to F20 I/O address = Base Address + 10 (0x0A)

Table 3 : Input Change Flag I/O Map

Flag	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
ICF Bank 1	Flag8	Flag7	Flag6	Flag5	Flag4	Flag3	Flag2	Flag1
ICF Bank 2	Flag16	Flag15	Flag14	Flag13	Flag12	Flag11	Flag10	Flag9
ICF Bank 3	Not used	Not used	Not used	Not used	Flag20	Flag19	Flag18	Flag17

CHAPTER 4 Interrupts Control Register (ICR)

– New with IR104 Version 4

Interrupts are generated and issued on the PC/104 bus when all of the following conditions are met:

1. A change of input state has occurred as indicated by the Flag registers.
2. The input that changed has its Interrupt Enable set (logic “1”).
3. One of the Interrupt Output Enables is set (logic “1”).

NOTE: An Interrupt will stay asserted until all the Input Change Flags that have their Interrupt Enabled flags enabled are cleared. An input change flag can be cleared by reading the corresponding input bank.

NOTE: The IR104-V4 interrupts cannot be shared with other PC/104 boards. Attempting to share an IRQ may cause damage to the IR104-V4 and the other PC/104 board as well.

The I/O map of the IR104 V4 has one Interrupt Enable per input. The Interrupt Enable register is divided into three banks as below.

The IR104 V4 has four Interrupt Output enables (IRQen4, IRQen5, IRQen6 and IRQen7). Each of the Interrupt Outputs corresponds to a PC/104 interrupt line. Only one Interrupt Output should be enabled. See Table 4.

Bank 1: Enables IE1 to IE8 I/O address = Base Address + 12 (0x0C)
Bank 2: Enables IE9 to IE16 I/O address = Base Address + 13 (0x0D)
Bank 3: Enables IE17 to IE20 & IRQen4 to 7 I/O address = Base Address + 14 (0x0E)

Table 4 : Interrupt Control Register I/O Map

Flag	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
ICR Bank 1	IE8	IE7	IE6	IE5	IE4	IE3	IE2	IE1
ICR Bank 2	IE16	IE15	IE14	IE13	IE12	IE11	IE10	IE9
ICR Bank 3	IRQen7	IRQen6	IRQen5	IRQen4	IE20	IE19	IE18	IE17

CHAPTER 5 Base Address Setting

There are four decode base addresses (0x240, 0x260, 0x280, 0x300) , which are jumper selectable using the address select block JP1 and JP2.

Table 5 : Base Address Map, Hex 240

Base Address	0x240
JP1 (1 to 2)	Jumper Not Installed
JP2 (2 to 3)	Jumper Not Installed

Offset	I/O Address	Description of Register Function	Register Name
0	0x240	Relay 1 to Relay 8	ROC Bank 1
1	0x241	Relay 9 to Relay 16	ROC Bank 2
2	0x242	Relay 17 to Relay 20	ROC Bank 3
3	0x243	Not Used	N/A
4	0x244	Input 1 to Input 8	DIR Bank 1
5	0x245	Input 9 to Input 16	DIR Bank 2
6	0x246	Input 17 to Input 20	DIR Bank 3
7	0x247	Not Used	N/A
8	0x248	Change flag Input 1 to input 8	ICF Bank 1
9	0x249	Change flag Input 9 to input 16	ICF Bank 2
10	0x24A	Change flag Input 17 to input 20	ICF Bank 3
11	0x24B	Not Used	N/A
12	0x24C	Interrupt enables Input 1 to Input 8	ICR Bank 1
13	0x24D	Interrupt enables Input 9 to Input 16	ICR Bank 2
14	0x24E	Interrupt enables Input 17 to Input 30 & IRQ output enables IRQ 4, 5, 6 & 7	ICR Bank 3

Table 6 : Base Address Map, Hex 260

Base Address	0x260
JP1 (1 to 2)	Jumper Not Installed
JP2 (2 to 3)	Jumper Installed

Offset	I/O Address	Description of Register Function	Register Name
0	0x260	Relay 1 to Relay 8	ROC Bank 1
1	0x261	Relay 9 to Relay 16	ROC Bank 2
2	0x262	Relay 17 to Relay 20	ROC Bank 3
3	0x263	Not Used	N/A
4	0x264	Input 1 to Input 8	DIR Bank 1
5	0x265	Input 9 to Input 16	DIR Bank 2
6	0x266	Input 17 to Input 20	DIR Bank 3
7	0x267	Not Used	N/A
8	0x268	Change flag Input 1 to input 8	ICF Bank 1
9	0x269	Change flag Input 9 to input 16	ICF Bank 2
10	0x26A	Change flag Input 17 to input 20	ICF Bank 3
11	0x26B	Not Used	N/A
12	0x26C	Interrupt enables Input 1 to Input 8	ICR Bank 1
13	0x24D	Interrupt enables Input 9 to Input 16	ICR Bank 2
14	0x26E	Interrupt enables Input 17 to Input 30 & IRQ output enables IRQ 4, 5, 6 & 7	ICR Bank 3

Table 7 : Base Address Map, Hex 280

Base Address	0x280
JP1 (1 to 2)	Jumper Installed
JP2 (2 to 3)	Jumper Not Installed

Offset	I/O Address	Description of Register Function	Register Name
0	0x280	Relay 1 to Relay 8	ROC Bank 1
1	0x281	Relay 9 to Relay 16	ROC Bank 2
2	0x282	Relay 17 to Relay 20	ROC Bank 3
3	0x283	Not Used	N/A
4	0x284	Input 1 to Input 8	DIR Bank 1
5	0x285	Input 9 to Input 16	DIR Bank 2
6	0x286	Input 17 to Input 20	DIR Bank 3
7	0x287	Not Used	N/A
8	0x288	Change flag Input 1 to input 8	ICF Bank 1
9	0x289	Change flag Input 9 to input 16	ICF Bank 2
10	0x28A	Change flag Input 17 to input 20	ICF Bank 3
11	0x28B	Not Used	N/A
12	0x28C	Interrupt enables Input 1 to Input 8	ICR Bank 1
13	0x28D	Interrupt enables Input 9 to Input 16	ICR Bank 2
14	0x28E	Interrupt enables Input 17 to Input 30 & IRQ output enables IRQ 4, 5, 6 & 7	ICR Bank 3

Table 8 : Base Address Map, Hex 300

Base Address	0x300
JP1 (1 to 2)	Jumper Installed
JP2 (2 to 3)	Jumper Installed

Offset	I/O Address	Description of Register Function	Register Name
0	0x300	Relay 1 to Relay 8	ROC Bank 1
1	0x301	Relay 9 to Relay 16	ROC Bank 2
2	0x302	Relay 17 to Relay 20	ROC Bank 3
3	0x303	Not Used	N/A
4	0x304	Input 1 to Input 8	DIR Bank 1
5	0x305	Input 9 to Input 16	DIR Bank 2
6	0x306	Input 17 to Input 20	DIR Bank 3
7	0x307	Not Used	N/A
8	0x308	Change flag Input 1 to input 8	ICF Bank 1
9	0x309	Change flag Input 9 to input 16	ICF Bank 2
10	0x30A	Change flag Input 17 to input 20	ICF Bank 3
11	0x30B	Not Used	N/A
12	0x30C	Interrupt enables Input 1 to Input 8	ICR Bank 1
13	0x30D	Interrupt enables Input 9 to Input 16	ICR Bank 2
14	0x30E	Interrupt enables Input 17 to Input 30 & IRQ output enables IRQ 4, 5, 6 & 7	ICR Bank 3

CHAPTER 6 Relay and Input Locations

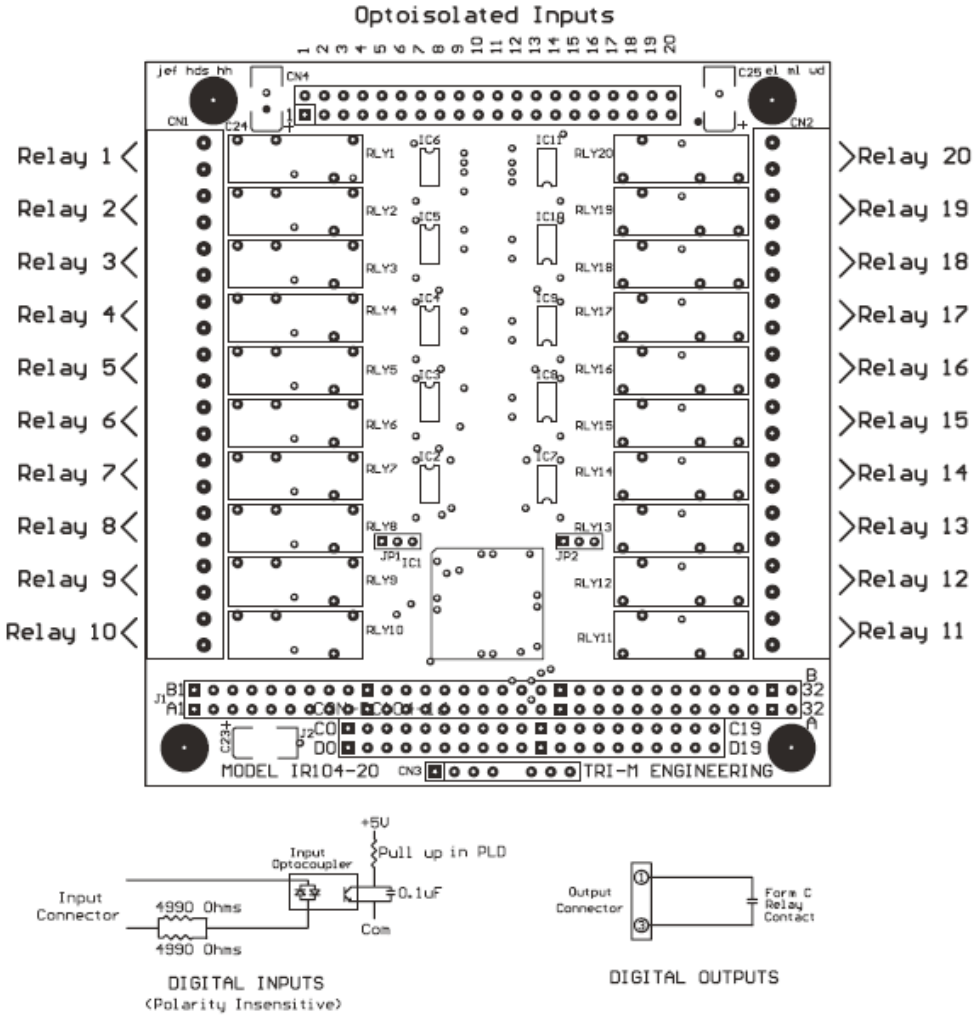


Figure 1 : IR104 Relay Locations

CHAPTER 7 Mechanical Board Dimensions

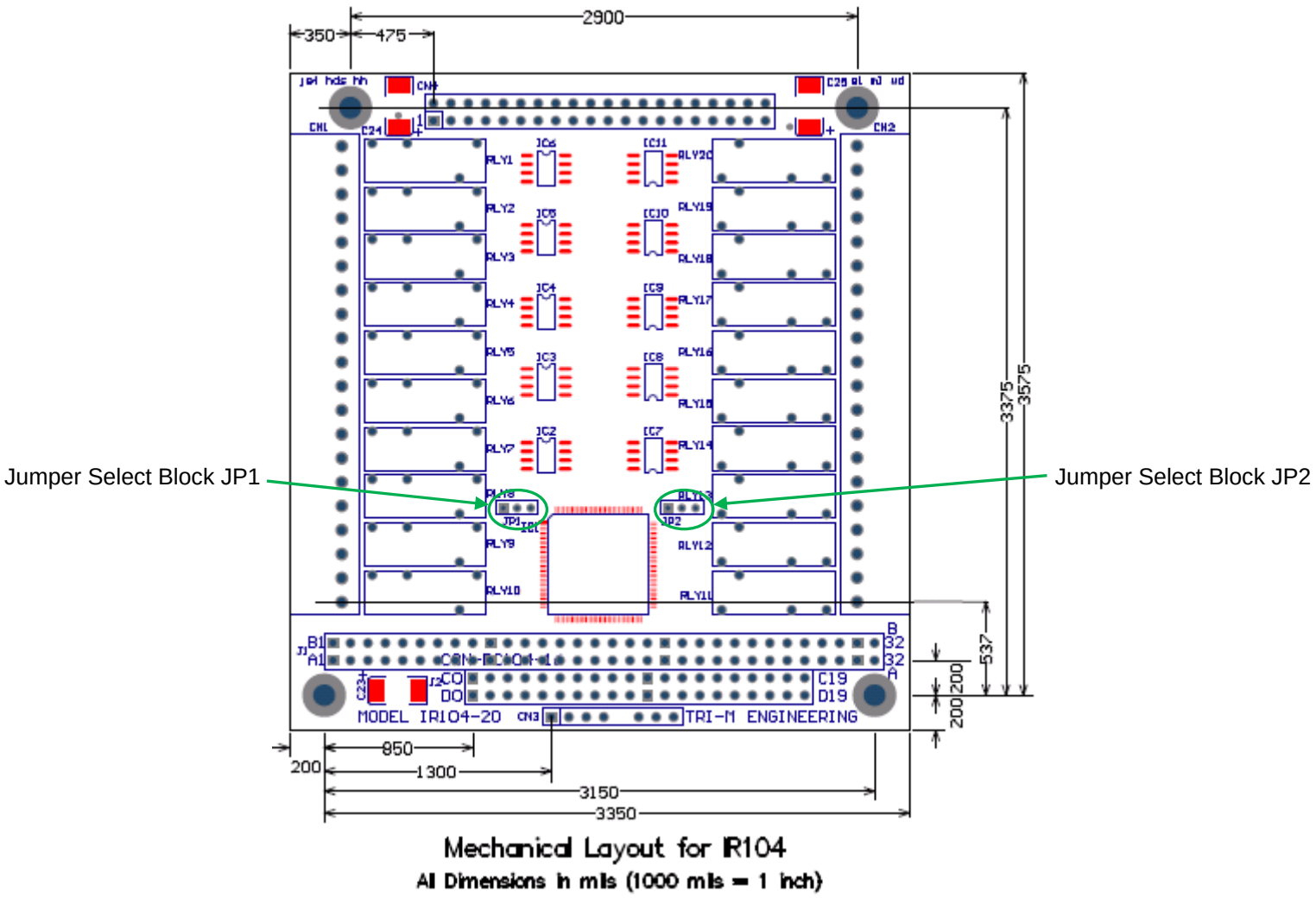


Figure 2 : IR104 Mechanical Dimensions

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