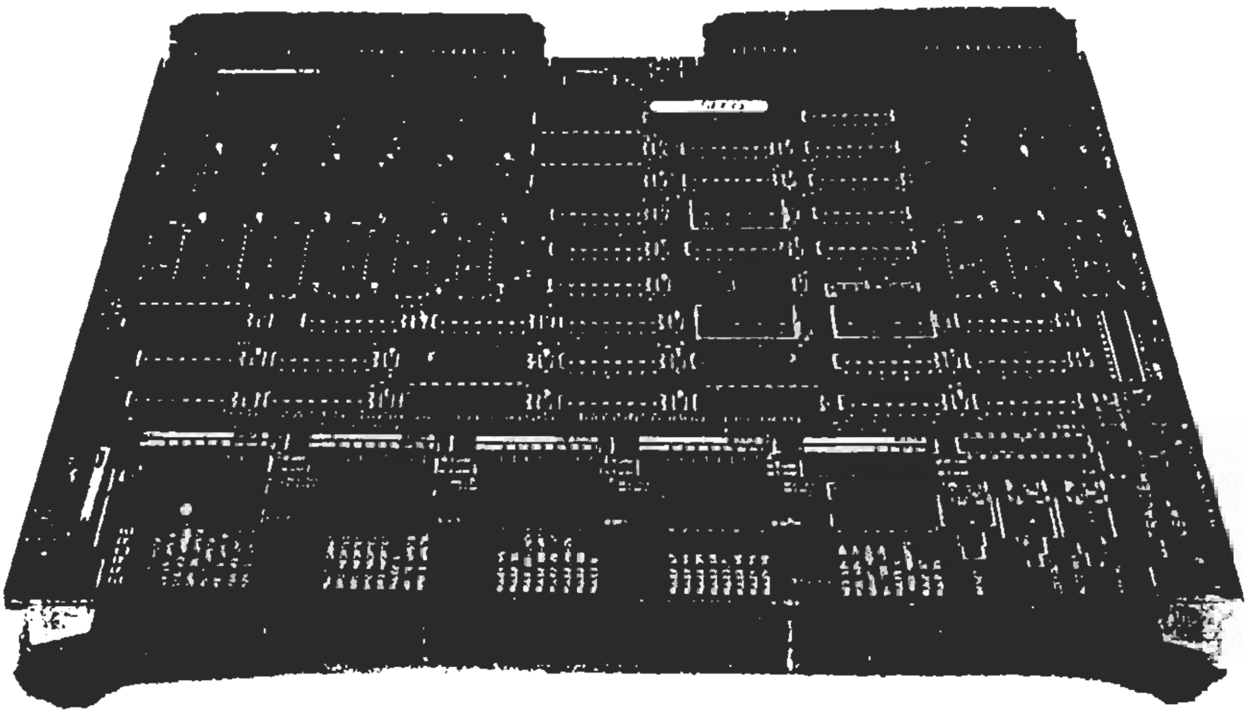
VBAT
VME Bus Anomaly Trigger



Automatically Recognizes Violations of VME Specification

The VME Bus Anomaly Trigger (VBAT) board is simply plugged into a slot in any VME computer system, where it automatically monitors all bus traffic and continuously and concurrently screens for a broad range of common timing violations of the VME bus protocols.

Real-Time Detection

Each violation illuminates an LED and generates a fast trigger output within 20 to 80 nanoseconds, giving you a direct lead to the problem.

Massively Parallel Trigger Board

This powerful broad-coverage trigger can then trigger a conventional logic analyzer for immediate viewing of the problem.

Finds the Real Cause of Incompatibilities Between VME Vendors

The VBAT aids designers and integrators of VME boards and systems by finding serious latent non-compliances in new products, as well as violations that cause all-too-common "incompatibilities" between VME boards from diverse vendors.

Finds Design Errors By Watching Every Bus Cycle in a Machine During Actual Operation

The VBAT's 104 asynchronous rule-based trigger elements continuously and simultaneously screen 98 VMEbus lines, to detect 28 classes of VMEbus timing violations. It detects any and all data, address and strobe lines that are not stable during the required intervals as well as strobes that are shorter than allowed or have improper timing relationships with other signals. Finally, by detecting timing edges that are out-of-sequence, the VBAT finds violations of the important VMEbus arbitration, data transfer and interrupt protocols.

ULTRAVIEW

Features

- Concurrently screens 98 lines for 28 classes of violations.
- Finds serious latent non-compliances in new VME boards.
- Ends finger-pointing by isolating the true cause(s) of "incompatibilities" between boards from different vendors.
- Fully automatic. 104 preset triggers eliminate the need to specify trigger words or attach probes. Just plug it in.
- Triggers on many deep bugs in VME boards that are indirectly visible at the bus, WITHOUT the need to devise a trigger strategy.
- Asynchronous edge-sequence triggers isolate events too short or complex to reasonably trigger conventional analyzers.
- Recognizes complex arbitration, interrupt and data transfer problems.
- 37 individual LEDs and trigger outputs, plus ORed master output.
- Excellent field service tool. May be sent rapidly to troubled customers.
- Detects extra transitions on strobe lines caused by metastability or bus ringing, cross-talk and ground bounce.
- Identifies memory boards (and other slaves) which drive DTACK* before providing valid data.
- Screens ALL types and sizes of VMEbus data transfer cycles.
- Real-world use reveals that a large number of VME systems have violations, most of which are simple to rectify.

Not Just For Emergency Debugging

– Good For Routine Screening of All New Prototypes and Production Boards.

The VBAT can be used as a partial "noncompliance detector", as it uncovers design, manufacturing and field-failure-induced flaws in portions of the bus interface circuitry of both VME masters and slaves.

The VBAT can even detect a wide variety of hardware problems originating in other parts of a VME board, that indirectly cause illegal bus activity. It does this by watching the boards in question during real world use in the actual system configuration of concern. A VBAT installed in a malfunctioning system can, for example, help determine why a customer is having trouble integrating your board into a foreign system, or why another manufacturer's board doesn't function with yours.

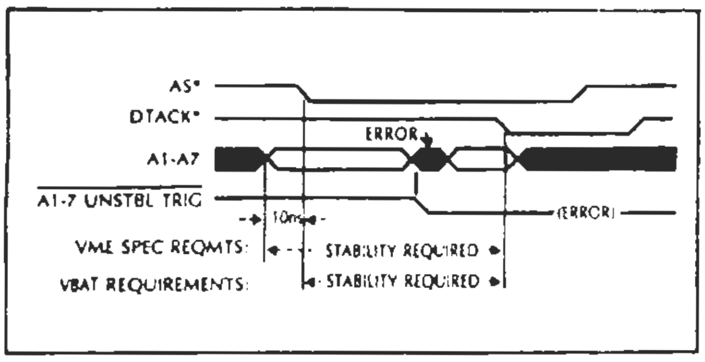
Essential When You Don't Know What To Trigger On

The most difficult part of debugging solely with a logic analyzer is determining what to trigger on. Often the symptom of failure gives no clue as to its cause. The VBAT's 104 parallel triggers continuously comb the bus for illegal activity, and can often establish an immediate trigger on extremely obscure bugs which might otherwise require days to devise a suitable triggering strategy for a conventional logic analyzer. This makes the VBAT ideal for field service/customer support purposes. The VBAT is even fast enough to trigger many oscilloscopes (containing delay lines) on repetitive violations.

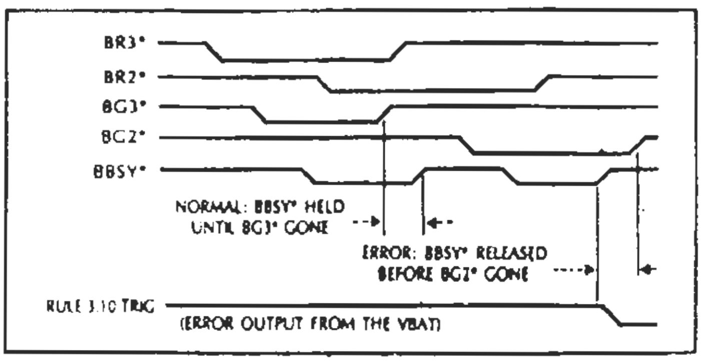
Unique Trigger Can Even Partially Automate The Debugging Process

The VBAT's capabilities are very different than those of existing logic analyzers. Its 104 concurrently active trigger elements give nearly two orders of magnitude more coverage than the one or two simple ORed trigger conditions of a conventional logic analyzer. It is only through such sheer "brute force" fault coverage that the VBAT's automatic triggering becomes practical for debugging. Also, it's asynchronous triggers finds faults of much shorter-duration than are detectable with a logic analyzer's trigger circuitry.

Finally, the VBAT's edge-sequence-rule-based triggering recognizes events that cannot be directly detected using logic analyzers. For example, the VBAT automatically recognizes "instability", (ie. changes on a line) on all address and data lines at once, without the need to be told the correct state of these lines beforehand. This is essential for concurrently screening for all address and data stability violations in all VMEbus cycles. This capability further enables the VBAT to detect extraneous transitions on strobe lines due to metastability, bus ringing and noise.



Example 1. VBAT detecting premature changes in address lines caused by a second board taking over the bus before the first has completed its cycle. "/A1-7 UNSTBL TRIG" is the VBAT's trigger output.



Example 2. "Rule 3.10 Violation" – VBAT recognizes a master (illegally) rescinding BBSY* before the bus grant goes high.

Specifications

VME BUS Specification Compliance:

Revision C.1 October 1985, also IEEE P1014

Board Size:

220 x 233mm – Standard double-height VME board, but with extra length so that LEDs and jumpers are conveniently accessible.

Violations Screened For:

1. Data lines D31-D00 changing when they should be stable. (VMEbus specification rules 2.16, 2.48, 2.54, 2.56, 4.36 & 4.38)
2. Address lines A31-A01 changing when they should be stable. (rules 2.30, 2.40 & 4.18)
3. Multiple bus grants (more than one at a time)
4. Bus request line(s) aborted prior to BBSY* or bus grant active. (part of rule 3.11, also caused by rule 3.13 violation)
5. Illegal combination of DSO*, DSI*, A01, LWORD* (rule 2.1)
6. WRITE* line unstable when it should be stable. (rules 2.38, 2.49, 4.23 & 4.31)
7. Address Modifiers AM5-AMO changing when they should be stable. (rules 2.30 & 2.40)
8. IACKIN asserted while DTACK* is low (rule 4.45)
9. DSO,1* asserted before DTACK* high (rules 2.35 & 4.20)
10. IACK* asserted before bus granted (part of rules 2.28 & 4.16)
11. WRITE* asserted before bus granted (part of rules 2.28)
12. LWORD* asserted before bus granted (part of rules 2.28 & 4.16)
13. DSO,1* asserted before bus granted (part of rules 2.28 & 4.16)
14. AS* asserted before bus granted (rules 2.20 & 4.16)
15. New bus grant generated before BBSY* rescinded (rule 3.6)
16. DSO,1* rescinded before DTACK asserted (rules 2.17 & 4.30)
17. AS* removed before last falling edge on DTACK* (rules 2.44 & 4.27) Also detects noise on ending edge of DTACK*.
18. Excessive skew between DSA*, DSB* assertion (rules 2.39 & 4.24)
19. BBSY* rescinded before bus grant goes high (rule 3.10)
20. Insufficient duration of BBSY* — <90ns (rule 3.7)
21. Insufficient duration of AS* (rules 2.45, 4.28)
22. IACKOUT* lingers more than 30ns after AS* ends (rules 4.41 & 4.47)
23. IACKOUT* driven low less than 40ns after DSA* (rule 4.46)
24. +5 Volt power dips below 4.85 Volts
25. SYSRESET* high before +5V power reaches 4.85V (part of rule 5.1)
26. Interrupt request line(s) aborted prior to interrupt acknowledge cycle (rules 4.5 & 4.6)
27. Insufficient DS* de-assertion time (rules 2.37 & 4.22)
28. Insufficient AS* de-assertion time (rules 2.31 & 4.17). Also detects noise on AS*.

Note: All above rules are defined in detail in the user manual, and also in the Rev. C1 VMEbus Spec. (and IEEE P1014 document).

Non Violations Indicated:

1. +12 Volt and -12 Volt Power Present.
2. Daisy-chained bus grant(s) hidden from VBAT during error – unable to fully examine bus arbitration functionality.

Warranty: Two years parts and labor.

Trigger Characteristics:

1. Master active-low trigger, as well as individual active-low TTL outputs for each type of violation.
2. Trigger speed:
   Individual Triggers: Asserted 20 to 80ns after fault.
   Master Trigger: Asserted within 100ns of fault.
3. Any or all violation triggers may be used individually.
4. Trigger reset modes:
   A. Manual – error LED and trigger latched until reset via push button.
   B. Automatic – LED and trigger reset approximately 90ns after occurrence.

Specifications subject to change without notice. Ultraview Corporation does not asssume any liability arising out of the application or use of any product described herein.

What the VBAT Cannot Do

The VBAT cannot be used as a completely "definitive bus compliance validator", since it does not check for all possible bus specification violations. Also, the VBAT triggers on significant violations of bus timing; a signal only out of spec by several nanoseconds may not trigger the VBAT.

Recommended Ancillary Equipment

While the VBAT's trigger outputs may be used to trigger any logic timing analyzer, best results in viewing bus anomalies will be obtained by using a logic analyzer with 100 MHz or faster sampling rate. For studying certain errors, a sampling rate of up to 400 MHz may be desirable.