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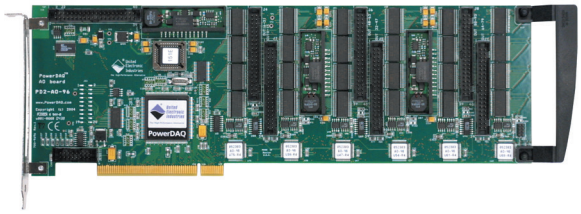
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PD2-AO-96/16

96-Channel PCI Card for Analog Output Data Acquisition

- 96 analog outputs (16-bit resolution)
- 8 digital inputs; 8 digital outputs
- Three 24-bit counters/timers; three clock/interrupt lines
- User-defined power-on state
- Simultaneous channel update; update on external event
- 2k samples onboard buffer size (upgradable to 64K samples)



Supports **UEIDaq Framework** Data Acquisition Software Library for Windows. Linux and QNX drivers available. Visit our website for more details.

General Description:

Analog outputs are no afterthought at UEI! In fact, we offer some of the highest-density cards in the industry. For instance, our PD2-AO-96/16 packs 96 analog outputs, each at 16-bit resolution. Even though the maximum per-channel update rate across all channels is 100k samples/sec, you can drive 32 of the outputs at an aggregate update rate of 1.5M samples/sec. In addition to that, it's possible to update multiple channels simultaneously and use multiple boards in one system.

The card calibrates each analog output individually without using trimpots. Instead relies on a special D/A-based scheme that stores calibration coefficients in EEPROM and loads them automatically upon power up. This method also keeps board outputs in a predefined user-programmable state upon system startup. The PD2-AO-96/16 is pin-compatiable with 16-channel analog-output cards from Keithley and Measurement Computing (formerly ComputerBoards).

Technical Specifications:

Analog Outputs	
Number of channels	96
Resolution	16 bits
Update rate	100 kS/s per channel; 450kS/s aggregate in non-DMA mode; up to 1100 kS/s aggregate in DMA mode
DSP buffer size	2k samples (2 buffers x 1k sample)
Type of D/A	double-buffered
Data transfer modes	DMA, interrupt, software
Accuracy	±3 LSB max
DNL	±3 LSB max
Monotonicity over temp.	15 bits, -40 to 85°C
Calibrated gain error	3mV typ, 6mV max @ ±9.8V
Calibrated offset error	1mV typ, 2mV max @ 0.0V
Ranges	±10V
Output coupling	DC
Output impedance	0.15Ω max
Current drive	±5 mA min
Capacitive loads	180 pF min
Settling time	10µs to 0.003%
Slew rate	10V/µs
Gain bandwidth	1 MHz
Noise	less than 2 LSB RMS, 0-10000 Hz
Output protection	short to ground, ±15V
Power-on state	0.0000V ±5mV (default), user programmable
Gain drift	25 ppm/°C

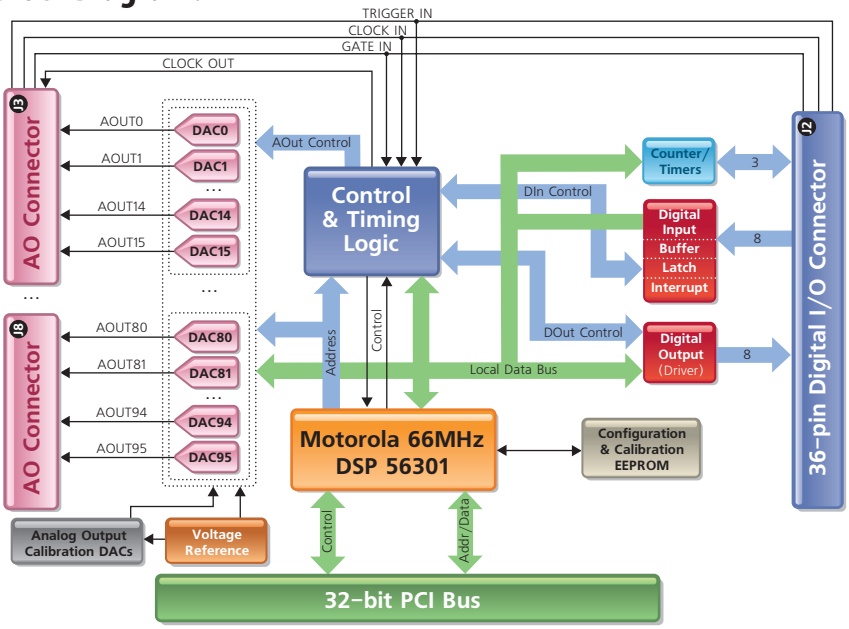
Digital I/O	
Number of channels	8 inputs, 8 outputs
Compatibility	CMOS/TTL, 2kV ESD protected
Power-on state	logic zero (default), user programmable
Data transfer modes	DMA, interrupt, software
Input termination	4.7kΩ pull-up to 5V
Output high level	3.0V typ @ -32mA, 3.4V typ @ -16mA, 4.2V @ -2mA
Output low level	0.55V max @ 64mA
Input low voltage	0.0 - 0.8V
Input high voltage	2.0 - 5.0V
Counter/Timer	
Number of channels	3
Resolution	24 bits
Max frequency	16.5 MS/s for external clock, 33 MS/s for internal DSP clock
Min frequency	0.00002 Hz for internal clock, no low limit for external clock
Min pulse width	20 ns
Output high level	2.9V typ @ -4 mA
Output low level	0.5V min @ 4 mA
Protection	7 kV ESD, ±30V over/undershoot
Input low voltage	0.0 - 0.8V
Input high voltage	2.0 - 5.0V

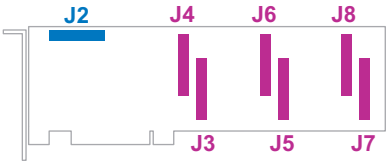
Connection Schemes:

Connector On The Board	Cable Required	Target Panel	Description
J3 - J8	PD-CBL-40	PD-STP-40	Carries 16 analog output lines to 16-channel terminal panel
J3 - J8	PD-CBL-4037	PD-STP-3716	Carries 16 analog output lines to 16-channel terminal panel*
J2	PD-CBL-37	PD-STP-3716	Carries 8 digital input and 8 output lines to 16-channel terminal panel
J3 - J8	PD-CBL-4037-INV	PD-AO-AMP-100	Carries 16 analog output lines to ±100V amplifier
J3 - J8	PD-CBL-4037-INV	PD-AO-AMP-115	Carries 16 analog output lines to ±115V amplifier
J2	PD-CBL-3650-8/8	PD2-DIO-BPLANE16	Carries digital lines to digital isolation panel for adding relays to the DIO lines

* Legacy connection scheme. Use PD-CBL-40 / PD-STP-40 combination instead.

Block Diagram:





Pinout Diagrams:

J2 — IDC-36 (male) 36-pin header:

DGND	1	2	DGND
TMR0	3	4	TMR2
DGND	5	6	DGND
DGND	7	8	DGND
TMR1	9	10	+5V 200mA max
DIN0	11	12	DGND
DIN1	13	14	DOUT0
DIN2	15	16	DOUT1
DIN3	17	18	DOUT2
DIN4	19	20	DOUT3
DIN5	21	22	DOUT4
DIN6	23	24	DOUT5
DIN7	25	26	DOUT6
GATE IN	27	28	DOUT7
CLOCK IN	29	30	DGND
TRIGGER IN	31	32	DGND
DGND	33	34	DGND
DGND	35	36	DGND

J3 — IDC-40 (male) 40-pin connector:

CLOCK IN	1	2	CLOCK OUT
TRIGGER IN	3	4	GATE IN
DGND	5	6	AGND
AOUT0	7	8	AGND
AOUT1	9	10	AGND
AOUT2	11	12	AGND
AOUT3	13	14	AGND
AOUT4	15	16	AGND
AOUT5	17	18	AGND
AOUT6	19	20	AGND
AOUT7	21	22	AGND
AOUT8	23	24	AGND
AOUT9	25	26	AGND
AOUT10	27	28	AGND
AOUT11	29	30	AGND
AOUT12	31	32	AGND
AOUT13	33	34	AGND
AOUT14	35	36	AGND
AOUT15	37	38	AGND

J4 — IDC-40 (male) 40-pin connector:

NC	1	2	NC
NC	3	4	NC
DGND	5	6	AGND
AOUT16	7	8	AGND
AOUT17	9	10	AGND
AOUT18	11	12	AGND
AOUT19	13	14	AGND
AOUT20	15	16	AGND
AOUT21	17	18	AGND
AOUT22	19	20	AGND
AOUT23	21	22	AGND
AOUT24	23	24	AGND
AOUT25	25	26	AGND
AOUT26	27	28	AGND
AOUT27	29	30	AGND
AOUT28	31	32	AGND
AOUT29	33	34	AGND
AOUT30	35	36	AGND
AOUT31	37	38	AGND

J5 — IDC-40 (male) 40-pin connector:

NC	1	2	NC
NC	3	4	NC
DGND	5	6	AGND
AOUT32	7	8	AGND
AOUT33	9	10	AGND
AOUT34	11	12	AGND
AOUT35	13	14	AGND
AOUT36	15	16	AGND
AOUT37	17	18	AGND
AOUT38	19	20	AGND
AOUT39	21	22	AGND
AOUT40	23	24	AGND
AOUT41	25	26	AGND
AOUT42	27	28	AGND
AOUT43	29	30	AGND
AOUT44	31	32	AGND
AOUT45	33	34	AGND
AOUT46	35	36	AGND
AOUT47	37	38	AGND

J6 — IDC-40 (male) 40-pin connector:

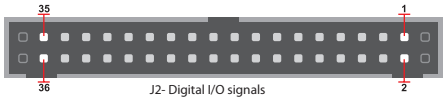
NC	1	2	NC
NC	3	4	NC
DGND	5	6	AGND
AOUT48	7	8	AGND
AOUT49	9	10	AGND
AOUT50	11	12	AGND
AOUT51	13	14	AGND
AOUT52	15	16	AGND
AOUT53	17	18	AGND
AOUT54	19	20	AGND
AOUT55	21	22	AGND
AOUT56	23	24	AGND
AOUT57	25	26	AGND
AOUT58	27	28	AGND
AOUT59	29	30	AGND
AOUT60	31	32	AGND
AOUT61	33	34	AGND
AOUT62	35	36	AGND
AOUT63	37	38	AGND

J7 — IDC-40 (male) 40-pin connector:

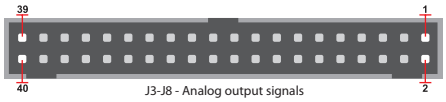
NC	1	2	NC
NC	3	4	NC
DGND	5	6	AGND
AOUT64	7	8	AGND
AOUT65	9	10	AGND
AOUT66	11	12	AGND
AOUT67	13	14	AGND
AOUT68	15	16	AGND
AOUT69	17	18	AGND
AOUT70	19	20	AGND
AOUT71	21	22	AGND
AOUT72	23	24	AGND
AOUT73	25	26	AGND
AOUT74	27	28	AGND
AOUT75	29	30	AGND
AOUT76	31	32	AGND
AOUT77	33	34	AGND
AOUT78	35	36	AGND
AOUT79	37	38	AGND

J8 — IDC-40 (male) 40-pin connector:

NC	1	2	NC
NC	3	4	NC
DGND	5	6	AGND
AOUT80	7	8	AGND
AOUT81	9	10	AGND
AOUT82	11	12	AGND
AOUT83	13	14	AGND
AOUT84	15	16	AGND
AOUT85	17	18	AGND
AOUT86	19	20	AGND
AOUT87	21	22	AGND
AOUT88	23	24	AGND
AOUT89	25	26	AGND
AOUT90	27	28	AGND
AOUT91	29	30	AGND
AOUT92	31	32	AGND
AOUT93	33	34	AGND
AOUT94	35	36	AGND
AOUT95	37	38	AGND



J2- Digital I/O signals



J3-J8 - Analog output signals

Pin-to-Pin Mapping Diagrams:

Depending on the cable used to connect the board to different terminal panels, pins of J2, J3-J8 connectors may be remapped. Please refer to the diagrams below for detailed information about pin-to-pin mapping for PD-CBL-4037, PD-CBL-4037-INV and PD-CBL-37 cables.

PD-CBL-4037

Pin		Pin

PD-CBL-4037-INV

Pin		Pin

PD-CBL-37

Pin		Pin
1	>	1
2	>	20
3	>	2
4	>	21
5	>	3
6	>	22
7	>	4
8	>	23
9	>	5
10	>	24
11	>	6
12	>	25
13	>	7
14	>	26
15	>	8
16	>	27
17	>	9
18	>	28
19	>	10
20	>	29
21	>	11
22	>	30
23	>	12
24	>	31
25	>	13
26	>	32
27	>	14
28	>	33
29	>	15
30	>	34
31	>	16
32	>	35
33	>	17
34	>	36
35	>	18
36	>	37
		19

Board-Mating Side — 36-pin IDC Header (female) — 37-pin D-Sub Connector (female) — Panel-Mating Side

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