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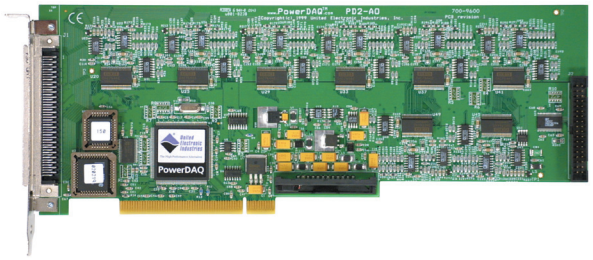
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Find the *United Electronic Industries PD2-AO-32/16* at our website: *Click HERE*

PD2-AO-32/16

32-Channel PCI Card for Analog Output Data Acquisition

- 32 analog outputs (16-bit resolution)
- 8 digital inputs; 8 digital outputs
- Three 24-bit counters/timers
- Three clock/interrupt lines
- Channel list (64 locations)
- Independent waveform on each channel
- Simultaneous channel update; update on external event
- 2k samples onboard buffer size



Supports **UEIDaq Framework** Data Acquisition Software Library for Windows. Linux and QNX drivers available. Visit our website for more details.

General Description:

Offering 32 analog outputs with 16-bit resolution, the PD2-AO-32/16 PCI-bus data acquisition board expands on the dual 12-bit calibration DAC-based output supplied on PD2-MF multifunction boards. Here you not only significantly increase the number of analog outputs, you also keep 16 digital I/O lines and three counter/timers. With these functions, the PD2-AO-32/16 is well suited to implement complex closed-loop systems as well as handle motor control and many other industrial-automation tasks.

The card calibrates each analog output individually without using trimpots. Instead relies on a special D/A based scheme that stores calibration coefficients in EEPROM and loads them automatically upon power up. This method also keeps board outputs in a predefined user-programmable state upon system startup.

Technical Specifications:

Analog Outputs	
Number of channels	32
Resolution	16 bits
Update rate	100 kS/s per channel; 450kS/s aggregate in non-DMA mode; up to 1100 kS/s aggregate in DMA mode
DSP buffer size	2k samples (2 buffers x 1k sample)
Type of D/A	double-buffered
Data transfer modes	DMA, interrupt, software
Accuracy	±3 LSB max
DNL	±3 LSB max
Monotonicity over temp.	15 bits, -40 to 85°C
Calibrated gain error	3mV typ, 6mV max @ ±9.8V
Calibrated offset error	1mV typ, 2mV max @ 0.0V
Output range	±10V (custom ranges available)
Output coupling	DC
Output impedance	0.15Ω max
Current drive	±20mA min, ±320mA max for all channels
Capacitive loads	180 pF min
Settling time	10µs to 0.003%
Slew rate	10V/µs
Gain bandwidth	1 MHz
Noise	2 LSB RMS, 0-10000 Hz
Output protection	short to ground, ±15V
Power-on state	0.0000V ±5mV (default), user programmable
Gain drift	25 ppm/°C

Digital I/O	
Number of channels	8 inputs, 8 outputs
Compatibility	CMOS/TTL, 2kV ESD protected
Power-on state	logic zero (default), user programmable
Data transfer modes	DMA, interrupt, software
Input termination	4.7kΩ pull-up to 5V
Output high level	3.0V typ @ -32mA, 3.4V typ @ -16mA, 4.2V @ -2mA
Output low level	0.55V max @ 64mA
Input low voltage	0.0 - 0.8V
Input high voltage	2.0 - 5.0V
Counter/Timer	
Number of channels	3
Resolution	24 bits
Max frequency	16.5 MS/s for external clock, 33 MS/s for internal DSP clock
Min frequency	0.00002 Hz for internal clock, no low limit for external clock
Min pulse width	20 ns
Output high level	2.9V typ @ -4 mA
Output low level	0.5V min @ 4 mA
Protection	7 kV ESD, ±30V over/undershoot
Input low voltage	0.0 - 0.8V
Input high voltage	2.0 - 5.0V

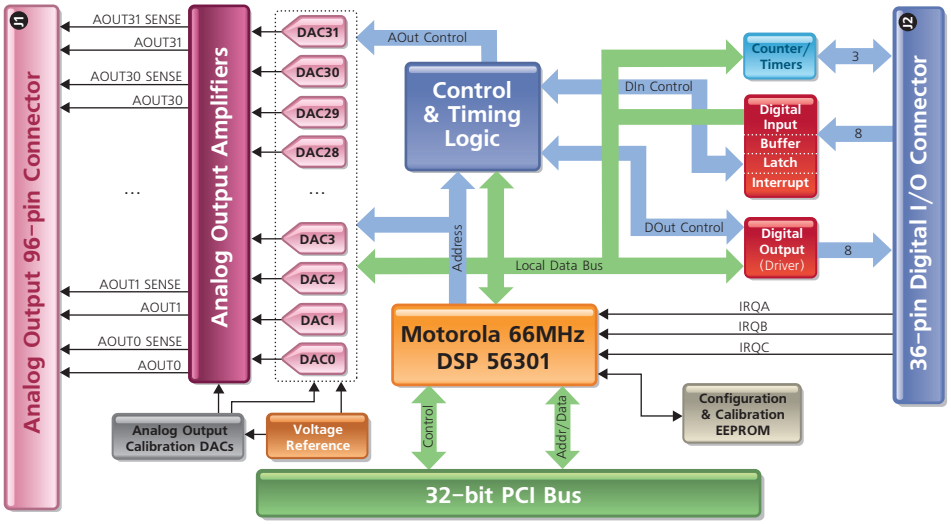
Connection Schemes:

Connector On The Board	Cable Required	Target Panel	Description
J1	PD-CBL-96	PD2-AO-STP-32	Carries analog output lines to 32-channel terminal panel
J2	PD-CBL-37	PD2-AO-STP-32	Carries 8 digital input and 8 digital output lines to 32-channel terminal panel
J1	PD-CBL-96	PD-BNC-64*	Carries analog output lines to 64-channel BNC terminal panel
J2	PD-CBL-37	PD-BNC-64	Carries 8 digital input and 8 digital output lines to 64-channel BNC terminal panel
J2	PD-CBL-3650-8/8	PD2-DIO-BPLANE16	Carries digital lines to digital isolation panel for adding relays to the DIO lines
J1	PD-CBL-96	PD-AO-AMP-100	Amplifies 16 analog outputs to ±100V per channel
J1	PD-CBL-96	PD-AO-AMP-115	Amplifies 16 analog outputs to ±115V per channel

* PD-BNC-64 was initially designed for analog input subsytem of UEI's multifunction boards. Thus the analog output signals transfered via PD-CBL-96 will not match the signal designations on PD-BNC-64's J1 connector. See PowerDAQ Analog Output Manual for more details and remapping diagram.

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Block Diagram:

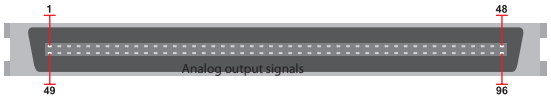


Note: AOUT**X** on PD2-AO-32/16 board is internally connected to the corresponding AOUT**X** SENSE line. If you need remote sensing option, please use PD2-AO-32/16HC board.

Pinout Diagrams:

J1 — pinless SCSI (male)
96-pin connector:

AGND	49	1	AGND
AGND	50	2	AGND
AGND	51	3	AGND
AGND	52	4	AGND
AGND	53	5	AGND
AGND	54	6	AGND
AOUT30	55	7	AOUT31
AOUT28	56	8	AOUT29
AOUT26	57	9	AOUT27
AOUT24	58	10	AOUT25
AOUT23	59	11	AGND
AOUT21	60	12	AOUT22
AOUT19	61	13	AOUT20
AGND	62	14	AOUT18
AOUT16	63	15	AOUT17
AOUT14	64	16	AOUT15
AOUT12	65	17	AOUT13
AOUT11	66	18	AGND
AOUT9	67	19	AOUT10
AOUT7	68	20	AOUT8
AGND	69	21	AOUT6
AOUT4	70	22	AOUT5
AOUT2	71	23	AOUT3
AOUT0	72	24	AOUT1
AGND	73	25	AGND
AGND	74	26	AGND
AGND	75	27	AGND
AGND	76	28	AGND
AGND	77	29	AGND
AOUT31 SENSE	78	30	AGND
AOUT29 SENSE	79	31	AOUT30 SENSE
AGND	80	32	AOUT28 SENSE
AOUT26 SENSE	81	33	AOUT27 SENSE
AOUT24 SENSE	82	34	AOUT25 SENSE
AOUT22 SENSE	83	35	AOUT23 SENSE
AOUT21 SENSE	84	36	AGND
AOUT19 SENSE	85	37	AOUT20 SENSE
AOUT17 SENSE	86	38	AOUT18 SENSE
AOUT15 SENSE	87	39	AOUT16 SENSE
AOUT14 SENSE	88	40	AGND
AOUT12 SENSE	89	41	AOUT13 SENSE
AOUT10 SENSE	90	42	AOUT11 SENSE
AGND	91	43	AOUT9 SENSE
AOUT7 SENSE	92	44	AOUT8 SENSE
AOUT5 SENSE	93	45	AOUT6 SENSE
AOUT3 SENSE	94	46	AOUT4 SENSE
AOUT2 SENSE	95	47	AGND
AOUT0 SENSE	96	48	AOUT1 SENSE





J2 — IDC-36 (male)
36-pin header:

DGND	1	2	DGND
TMR0	3	4	TMR2
DGND	5	6	DGND
DGND	7	8	DGND
TMR1	9	10	+5V 200mA max
DIN0	11	12	DGND
DIN1	13	14	DOUT0
DIN2	15	16	DOUT1
DIN3	17	18	DOUT2
DIN4	19	20	DOUT3
DIN5	21	22	DOUT4
DIN6	23	24	DOUT5
DIN7	25	26	DOUT6
IRQA	27	28	DOUT7
IRQB	29	30	DGND
IRQC	31	32	DGND
DGND	33	34	DGND
DGND	35	36	DGND



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