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Model V253

16-Channel Programmable Gain/Filter

INSTRUCTION MANUAL

August 30, 2002

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UNPACKING AND INSTALLATION

The Model V253 is shipped in an anti-static bag within a styrofoam packing container. Carefully remove the module from its static-proof bag and prepare to set the various options to conform to the desired operating environment. Although there are covers on this module, care should be taken to avoid ESD (Electro-static Discharge) damage.

Logical Address Switches

The V253 represents one of the 255 devices permitted in a VXIbus system. (Logical Address 0 is reserved for the Slot 0 device). The module is shipped from the factory with its address set for Logical Address 255. This address can be shared by multiple devices in a system that supports dynamic configuration. If the V253 is to be used in a system that does not support dynamic configuration, or in a system where static configuration of the module is desired, the Logical Address must be manually established. This is accomplished by manipulating eight rocker switches located under the access hole in the module's right-side ground shield.

1 - V253 Switch Locations

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The eight switches represent a binary combination of numbers that range from zero to 255. Use an appropriate instrument to set the Logical Address to the desired value.

The bit pattern for the base address is shown below:

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	1	LA128	LA64	LA32	LA16	LA8	LA4	LA2	LA1	0	0	0	0	0	0

Bits 15 and 14 are set to a default value of "1" (VXI defined).

Bits 13 thru 6 are user-selectable via the address switches LA128-LA1. See Note 1 below.

Bits 5 thru 0 are set to "0" to provide the rest of the base address in A16 address space.

Module Insertion

The V253 is a C-sized, single width VXIbus module. Except for Slot 0, it can be mounted in any unoccupied slot in a C-size VXIbus main frame. For MUX-bus operation, the module must be to the right of an ADC module.

CAUTION: TURN MAINFRAME POWER OFF WHEN INSERTING OR REMOVING MODULE

WARNING: REMEMBER TO REMOVE INTERRUPT ACKNOWLEDGE DAISY-CHAIN JUMPERS PRIOR TO INSERTING MODULE IN BACKPLANE

To insure proper interrupt acknowledge cycles from the V253 module, the daisy-chain Interrupt Acknowledge jumper must be removed before the module is installed in a slot. Conversely, daisy-chain jumpers must be installed in any empty slot between the V253 and the Slot 0 Controller.

Note 1: Setting these address switches to all "1" allows the module to be dynamically addressed.

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FRONT PANEL INFORMATION

LEDs

The "ADD_REC" (Addressed Received) LED is illuminated when the registers are being accessed.

The "FAILED" LED is illuminated when the V253 has failed its self-test.

The "OVR LAP DET" (Overlap Detect) LED is illuminated when a timing violation is detected on the MUX-bus. Specifically, more than one channel is attempting to drive a MUX-bus line simultaneously. If the Overlap LED is on, The V253 will not output any voltages out on the MUX-bus.

Connectors

There are two high density 68 pin connectors (J3 AMP 749831-7, J4 AMP 2-174341-5) mounted on the front panel. For a definition of the pins on these connectors, see Figure 4 and Table 5.

Reference Monitor

The internal 10 volt reference may be monitored by connecting a high impedance (100 MOhm minimum, 6 ½ digit) digital voltmeter across the +/- terminals. Adjustment is made via the Ref Adj potentiometer through the front panel.

External Sample/Hold

The External Sample/Hold SMB Connector allows external control of the sample/hold amplifiers. A low TTL level holds the data in the sample/hold amplifiers.

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Figure 2 - V253 Block Diagram 16-Channel Programmable Gain/Filter

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GENERAL DESCRIPTION

This single width module conforms both electrically and mechanically to the VXI specification.

Input and Output connections are made to this card via a removable Termination Assembly which interfaces to the card via two front panel connectors, or through cable connectors plugged directly into the Front panel connectors.

This module contains sixteen (16) channels of signal conditioning (Refer to Figure 2), each channel capable of amplifying and filtering the signal coming from the users' unit under test. The signal input circuitry consists of a high impedance, differential input stage that is capable of withstanding up to 20 volts, continuously applied without damage and also provides protection against ESD.

A seventeenth channel allows cold junction temperatures to be measured. This channel is designed to be used with the KineticSystems' Terminal Panel Model 1992-V1D or Isothermal Housing Model V752-ZB11, which provides an isothermal block and temperature sensor. This channel may be accessed in place of the normal sixteenth channel during pretest.

The transfer function of this cold junction channel is given by:

$$\text{Temp}(^0\text{C}) = (\text{Output Volts}) * 10$$

Two stages of gain selection are provided. The Programmable Instrumentation Amplifier provides gains of 1, 10 and 100, as well as providing a very high input impedance and common mode rejection. The second gain stage is provided by the Programmable Gain Amplifier, with available gains of 1, 2, 5 and 10. Care should always be taken to select the highest gain in the Instrumentation Amplifier stage. For example, if an overall gain of 100 is desired, better performance will be achieved by selecting a gain of 100 for the first stage and a gain of 1 for the second stage, rather than gains of 10 on both stages.

Filtering is implemented on each channel using a plug-in module (8 channels per module). The standard filter is either a Bessel or Chebyshev 6 pole with four programmable bandedges of 20Hz, 200Hz, 1kHz and 2kHz. If the V253 is in the by-pass mode, the bandwidth will be greater than 20KHz.

This module is designed to be used in conjunction with our family of A/D converter modules using the analog MUX-bus (on the P2 connector) to pass the channel output to the A/D module. This module contains all circuitry necessary to interface to this bus.

Additionally, it is possible to take the output signal (non-multiplexed) via the termination assembly or from connector J3 to another A/D converter.

Optional sample and hold module is available for reading data from the sixteen channels to the ADC at one time frame. Without the option, data is read from the sixteen channels sequentially to the ADC.

The Instrumentation Amplifiers used at the front end of the V253 Sixteen Channel Programmable Gain/Filter Module utilize a custom hybrid design to provide the high performance achieved by these modules. In particular, the amplifiers exhibit

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low values of input bias current and offset current.

For most applications, these currents will not be of concern. However, these input currents must have a return path to ground, otherwise the inputs to the amplifier will saturate. In general, the signal source will be ground referenced and no problem will arise. If, on the other hand, the source is floating, then a return path must be provided. Refer to Figure 3.

Voltage inputs should be limited to less than + and - 10 volts.

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Figure 3 - Providing Ground Path For Return Currents

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CALIBRATION

A high degree of flexibility has been provided in this module to allow for ease of calibration. A multiplexer at the front end of each channel allows one of four sources to be selected:

1) Line (input signal)

2) Front panel calibration (allows user to input a known voltage) via the terminator housing or connector J3.

3) Internal programmable calibrator (a precision voltage calibrator that allows any voltage from +/-2 millivolts to +/-10 volts in 1,2,5,10 progression to be applied to the channel input. This precision voltage may be referenced either to the on-board 10 volt reference or to the 10 volt reference provided by the ADC module via the MUX-bus. Table 1 contains the necessary programming information.

4) Zero (provides a ground reference to measure channel offsets).

The internal calibrator error can be measured by a NIST traceable DVM and stored in the on-board EEPROM. This error term is available to the user for software error correction. Table 2 shows the locations in EEPROM used to store the calibrator correction terms. These terms are stored as a single 16 bit integer value representing the calibrator span error in parts per million. To apply this correction term to the gain calibration of a channel, multiply by 10^6 and add one. Then multiply the channel gain (M) by this value.

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TABLE 1 - Calibration Register Values

Cal Voltage	On Board Source	MUX-bus Source
+10.0	0x8091	0x0091
+5.0	0x80A1	0x00A1
+2.0	0x80C1	0x00C1
+1.0	0x8092	0x0092
+0.5	0x80A2	0x00A2
+0.2	0x80C2	0x00C2
+0.1	0x8094	0x0094
+0.05	0x80A4	0x00A4
+0.2	0x80C4	0x00C4
+0.01	0x8098	0x0098
+0.005	0x80A8	0x00A8
+0.002	0x80C8	0x00C8
-0.002	0x8148	0x0148
-0.005	0x8128	0x0128
-0.01	0x8118	0x0118
-0.02	0x8144	0x0144
-0.05	0x8124	0x0124
-0.1	0x8114	0x0114
-0.2	0x8142	0x0142
-0.5	0x8122	0x0122
-1.0	0x8112	0x0112
-2.0	0x8141	0x0141
-5.0	0x8121	0x0121
-10.0	0x8111	0x0111

TABLE 2 - Calibrator Correction Terms

CAL Range	EEPROM Location
+/- 10.0	0x2010
+/- 5.0	0x2012
+/- 2.0	0x2014
+/- 1.0	0x2016
+/- 0.5	0x2018
+/- 0.2	0x201A

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+/- 0.1	0x201C
+/- 0.05	0x201E
+/- 0.02	0x2020
+/- 0.01	0x2022
+/- 0.005	0x2024
+/- 0.002	0x2026

TABLE 3 - Zero Correction Terms

Channel 1	0x2040
Channel 2	0x2042
Channel 3	0x2044
Channel 4	0x2046
Channel 5	0x2048
Channel 6	0x204A
Channel 7	0x204C
Channel 8	0x204E
Channel 9	0x2050
Channel 10	0x2052
Channel 11	0x2054
Channel 12	0x2056
Channel 13	0x2058
Channel 14	0x205A
Channel 15	0x205C
Channel 16	0x205E

CALIBRATOR CALIBRATION

In order to achieve the high degree of accuracy for the V253, error coefficients for both gain and offset are stored in the Correction Table (non-volatile RAM) on the V253. Coefficients are stored for the Calibrator to compensate for any gain error. These coefficients are applied in software during channel calibration to compute the true voltage applied to a channel during gain calibration. These coefficients are stored in the "Correction Table" (Table 2) starting at A24 offset 0x2010. Coefficients are also stored to compensate for channel to channel offsets errors. These coefficients are applied during software channel offset calibration and are stored starting at A24 offset 0x2040.

It is recommended that this calibration procedure be performed approximately every six months. The calibration date is also stored in the "Correction Table" to help track the last calibration date. The date is stored at the beginning of the "Correction Table" starting at A24 offset 0x2000. The following is a list of steps to follow in performing the V253 module calibration.

Note- Install jumper at STP1 (next to Address switches) before attempting to write to EEPROM, remove jumper when calibration is complete.

1.) The V253 should have a minimum of 30 minute warmup period.

2.) Connect "+" and "-" front panel test points to a precision voltage meter.

3.) Adjust the "Ref Adj" potentiometer on the front panel for +10.0000 Volts DC.

4.) Connect "Cal Ref Out" (J3 pin 33 is Hi, J3 pin 67 is Lo) to a precession

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voltage meter. All channel input pins must be connected to ground (use the "-" front panel test point for ground).

5.) In software set each channel of the V253 to "input MUX to line", "gain x1000", "filter to by-pass".

6.) Gain Calibration - repeat steps 6a to 6c for all 12 differential calibrator voltages. In the following equation, these expected calibrator voltages are referred to as "CALIBRATOR", ranging from 10 volts to 2 millivolts. The calibrator voltages are set by writing to the calibration Registers (Operational register in A24 space at offset 0x0002). Make sure to wait for the calibrator voltage to settle before any measurements are taken.

6a.) Use a precession meter to measure the positive calibration voltages (average 10 points). The measured positive calibration voltage is referred to as PCAL in the following equation.

6b.) Use a precession meter to measure the negative calibration voltages (average 10 points). The measured negative calibration voltage is referred to as NCAL in the following equation.

6c.) Store the gain error coefficient into the Correction Table (Table 2) as a 16 bit signed integer according to the following equation:

BOLD GAIN~ COEFFICIENT~ =~ (~ { PCAL~-~NCAL } over { CALIBRATOR ~times~ 2 }~-~1~) ~times~ 10 SUP 6

Please note: Must wait a minimum of 3 mS after writing coefficient before writing again.

7.) If offset calibration is not needed, then skip to step # 9.

8.) Offset calibration - for every channel repeat steps 8a through 8f.

8a.) See Step # 5 for V253 setup. Install V207 (or other ADC to left of V253).

8b.) Measure front panel offset voltage (RTO) and use this equation to convert the COUNTS read from the V207 into RTO voltage.

VOLTAGE~~(RTO)~=~(~COUNTS~~-~32768~)~times~312.5~µVolts

This front panel ground measurement is referred to as FP OFFSET in the following equation.

8c.) On the V253 in software connect all the channels input MUX to "zero", all other settings are the same as Step # 5.

8d.) Measure zero offset voltage (RTO), using equation in Step 8b. The zero ground measurement is referred to as CAL OFFSET in the following equation.

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8d.) Store the zero error coefficient into the Correction Table (Table 3) as a 16 bit signed integer according to the following equation:

OFFSET~COEFFICIENT~=~{(~FP~OFFSET~-~CAL~ OFFSET~)}over{1000}~times~10^9

9.) Store calibration date into the Coefficient Table (Table 2).

Please note: Must wait a minimum of 3 mS after writing coefficient before writing again.

10.) Remove jumper at STP1.

MUX-bus

The MUX-bus makes use of the VXI P2 connector lines LBUSC00 - LBUSC11 on this module. Signal conditioning modules supporting the MUX-bus may be plugged into the crate only to the right of the V207 (or any other ADC module using MUX-bus).

The MUX-bus pin definition (P2) is:

LBUSC00 MUX path A signal hi
LBUSC01 MUX path A signal lo
LBUSC02 MUX path B signal hi
LBUSC03 MUX path B signal lo
LBUSC04 MUX path C signal hi
LBUSC05 MUX path C signal lo
LBUSC06 MUX path D signal hi
LBUSC07 MUX path D signal lo
LBUSC08 Reference Hi
LBUSC09 Reference Lo
LBUSC10 Overlap Detect
LBUSC11 MUX-bus CLOCK

Reference Hi and Reference Lo provide a +10 volt differential signal to adjacent signal conditioning modules, allowing all channels to be referenced to a common standard. This greatly simplifies system calibration.

Overlap Detect is used by the signal conditioning modules to detect if two or more modules are attempting to output their voltages at the same time. This helps prevent conflicts caused by an incorrectly programmed Scan RAM.

The MUX-bus clock generates the control signal that causes the output multiplexers on the signal conditioning modules to access the bus at the appropriate time.

Scan RAM

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NOTE: As a general rule, the V207 or any other receiving MUX-bus module, should be the FIRST to be put in "setup" mode and the LAST to be put in "run" mode.

The Scan RAM contains the Scan Table which must be setup properly on all MUX-bus modules. The Scan RAM is 2048 words long, and the Scan Table is a subset of the Scan RAM. Each module scans through their Scan Table sequentially at the ADC clock rate. At any time, the current data on the list dictates which module is to connect a channel to the MUX-bus.

Before the Scan Table can be written into Scan RAM, the V253 and the V207 must be put in "setup" mode by resetting the ADSEL bit in the Configuration Register. As a general rule, the V207 or any other receiving MUX-bus module, should be the FIRST to be put in "setup" mode, and the LAST to be put in "run" mode. The Scan RAM is organized the same on all modules (except for Bit 14) whether it sources or receives voltages on the MUX-bus. Bit 14 is the enable bit which connects the specified channel to MUX-bus. The enable bit must be set on only one sourcing module at any one time in the Scan Table (only one voltage may be output on the MUX-bus at one time). The Enable bit is ignored on all MUX-bus receiving modules because all channels listed in the Scan Table are active channels. The channel is specified by the first 14 bits of Scan RAM. The MUX-bus is four channels wide and is distributed evenly across all 16 channels of the V253. For instance, channels 1, 5, 9, and 13 of V253 are connected to Path A of the MUX-bus. Bit 15 is the end of list bit. This bit must be set in the last active location of the Scan Table on all MUX-bus modules. Finally, all modules using MUX-bus should be put in "run" mode starting with the sourcing (V253, V246, etc.) modules first.

NOTE: Physical channels 1-16 of the V253 are mapped as channels 0-15 in the Scan RAM.

OVERLAP DETECT CHECKLIST

Should overlap condition occur on a MUX-bus module, this detailed list may help in finding the specific cause of the overlap condition.

Cause 1 If an overlap occurred on only 1 MUX-bus module, then that module was programmed to output a channel at an inappropriate time. To increase the bandwidth of MUX-bus and improve accuracy, MUX-bus has 4 distinct paths (A through D). However, any given channel, on any given module, is available only on one path. MUX-bus must run in order from Path A through to Path D. The following Table 4 gives an example of a properly programmed Scan Table.

A24 Offset	MUX-bus Path	Available Chan	Data (7-0)	Chan Enabled
0x200	Path A	1,5,9,13...	xxxxxx00	V253 chan 1
0x202	Path B	2,6,10,14...	xxxxxx01	V253 Chan 2
0x204	Path C	3,7,11,15...	xxxxxx10	V253 Chan 3
0x206	Path D	4,8,12,16...	xxxxxx11	V253 Chan 4

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0x208	Path A	1,5,9,13...	xxxxx100	V253 Chan 5
0x20A	Path B	2,6,10,14...	xxxxx101	V253 Chan 6
0x20C	Path C	3,7,11,15...	xxxxx110	V253 Chan 7
0x20E	Path D	4,8,12,16...	xxxxx111	V253 Chan 8
. . .	. . .	. . .	. . .	. . .

TABLE 4 - V253 Scan Table, MUX-bus Path

Cause 2 If an overlap occurred on two MUX-bus modules, the one of two possibilities can cause the overlap. One possibility is that both modules were programmed to output a channel at an inappropriate time (see Cause 1). The other possibility is that two MUX-bus modules tried to output voltages at the same time. This would occur if the enable bit in the Scan Table was set at the same location on both modules.

/Cause 3 If an overlap occurred on multiple, but not all MUX-bus modules, then most likely a combination of Causes 1 and Causes 2 had occurred.

Cause 4 If an overlap occurred on all MUX-bus modules, then one of two possibilities caused the overlap. One possibility is that the ADC (V207) was not the last to be put in the "run" mode. The other possibility is that the "End of List" bit was not set at the same location in each of their Scan Tables.

TROUBLE SHOOTING GUIDE

Problem	Solutions
Output at + or - 12 Volts	· Input MUX open or no input connection. · Input signal saturating amplifier, gain to high.
Output always at zero	· Input MUX set to Zero. · Gain set to low for input signal. · Filter set to wrong bandedge.
Signal is clipped	· Gain set to high.
Output not changing with input signal	· Input MUX set to other than "Line", set to "zero" or "Cal". · Gain set to low.
ADC module not receiving data from V253	· MUX-bus not setup correctly (check Scan Ram). · V253 not to right of ADC module.
V253 calibrating wrong	· Input MUX set to wrong Calibrator source.
Fail LED is on always	· V253 failed self test. One or more channels are

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	bad.
Overlap LED is on	· Scan Ram setup improperly.

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FIGURE 4 - 68 Pin Connectors, J3 and P4

TABLE 5 - 68 Pin High Density Connectors, J3 and P4 Pinout

Pin #	V253 J3 Description	Pin #	V253 P4 Description
1	Channel 1 Out +	1	Channel 1 In +
35	Channel 1 Out –	35	Channel 1 In –
2	Channel 2 Out +	2	Channel 1 Shield

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Pin #	V253 J3 Description	Pin #	V253 P4 Description
36	Channel 2 Out –	36	Channel 2 Shield
3	Channel 3 Out +	3	Channel 2 In +
37	Channel 3 Out –	37	Channel 2 In –
4	Channel 4 Out +	4	Channel 3 In +
38	Channel 4 Out –	38	Channel 3 In –
5	Channel 5 Out +	5	Channel 3 Shield
39	Channel 5 Out –	39	Channel 4 Shield
6	Channel 6 Out +	6	Channel 4 In +
40	Channel 6 Out –	40	Channel 4 In –
7	Channel 7 Out +	7	Channel 5 In +
41	Channel 7 Out –	41	Channel 5 In –
8	Channel 8 Out +	8	Channel 5 Shield
42	Channel 8 Out –	42	Channel 6 Shield
9	Channel 9 Out +	9	Channel 6 In +
43	Channel 9 Out –	43	Channel 6 In –
10	Channel 10 Out +	10	Channel 7 In +
44	Channel 10 Out –	44	Channel 7 In –
11	Channel 11 Out +	11	Channel 7 Shield
45	Channel 11 Out –	45	Channel 8 Shield
12	Channel 12 Out +	12	Channel 8 In +
46	Channel 12 Out –	46	Channel 8 In –
13	Channel 13 Out +	13	Channel 9 In +
47	Channel 13 Out –	47	Channel 9 In –
14	Channel 14 Out +	14	Channel 9 Shield
48	Channel 14 Out –	48	Channel 10 Shield
15	Channel 15 Out +	15	Channel 10 In +
49	Channel 15 Out –	49	Channel 10 In –
16	Channel 16 Out +	16	Channel 11 In +
50	Channel 16 Out –	50	Channel 11 In –
17		17	Channel 11 Shield
51		51	Channel 12 Shield

Pin #	V253 J3 Description	Pin #	V253 P4 Description
18		18	Channel 12 In +
52		52	Channel 12 In –
19		19	Channel 13 In +
53		53	Channel 13 In –
20		20	Channel 13 Shield
54		54	Channel 14 Shield
21		21	Channel 14 In +
55		55	Channel 14 In –
22		22	Channel 15 In +
56		56	Channel 15 In –
23		23	Channel 15 Shield
57		57	Channel 16 Shield
24		24	Channel 16 In +
58		58	Channel 16 In –
25		25	
59		59	
26		26	
60		60	
27		27	
61		61	
28		28	
62		62	
29		29	
63		63	
30		30	
64		64	
31		31	F P Calib In +
65		65	F P Calib In -
32		32	External Trig S/H
66		66	Digital Ground
33	Calibrator Out +	33	Channel 17 In -

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Pin #	V253 J3 Description	Pin #	V253 P4 Description
67	Calibrator Out -	67	Channel 17 In +
34	Constat 0	34	Constat 2
68	Constat 1	68	Digital Ground

J3 Front Panel Connector is AMP 749831-7 68 Sockets

P4 Front Panel Connector is AMP 2-174341-5 68 Pins

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V752 TERMINATION HOUSING ASSEMBLY

Description

The V752 16 Channel VXI Termination Housing contains 16 input and output channels for connecting inputs to a VXI signal conditioning card. An Isothermal version (V752-ZC11) of this termination housing is intended to be used with the V253, when connecting to thermocouples. The V752-ZC11 contains an isothermal block with compensating reference connected to channel 17 of the V253.

The termination housing contains terminal blocks with screw terminals capable of accepting wire sizes of 26 AWG to 12 AWG. Terminals are available for connection of the customer's external calibration voltage. This input is controlled by software selection of either internal or external "reference Input".

When the V253 is used for Voltage inputs, it is recommended that a shielded cable be used, with the shield connected to Shield at the termination housing and connected to ground at the signal source end.

V765 RACK MOUNT TERMINATION PANEL

Description

The V765 Rack Mount Termination Panel contains a convenient method for connecting inputs or outputs to a VXI signal conditioning card. One panel is needed for inputs and one panel is needed for outputs. The panels are connected to the V253 by means of a cable (Model 5868. An Isothermal version (V792-ZA11) of this termination panel is intended to be used with the V253, when connecting to thermocouples. The V792 contains an isothermal block with compensating reference connected to channel 17 of the V253.

The termination panel contains terminal blocks with screw terminals capable of accepting wire sizes of 22 AWG to 14 AWG. Terminals are available for connection of the customer's external calibration voltage.

When the V253 is used for Voltage inputs, it is recommended that a shielded cable be used, with the shield connected to Shield terminal at the Termination Panel and connected to ground at the signal source end.

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PROGRAMMING INFORMATION

Address Map

A16 Space -- VXI Configuration Registers

$ 0x00 - ID Register (R)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
0	1	0	0	1	1	1	1	0	0	1	0	1	0	0	1

[15:14] (R) Class = Extended
[13:12] (R) Mode = A16/A24
[11:0] (R) ID = F29

$ 0x00 - ID Register (W)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
								LAR 7	LAR 6	LAR 5	LAR 4	LAR 3	LAR 2	LAR 1	LAR 0
X	X	X	X	X	X	X	X								

LAR[7:0] (W) Logical Address Register

$ 0x02 - Device Type Register (R)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	0	0	1	0	0	1	0	0	1	0	1	0	0	1	1

[15:12] (R) Memory = 16 KBytes
[11:0] (R) Model = 253

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$ 0x04 - Status Control Register (Mixed)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
A24	MODID										READY	PASSD	INHBT	RESET	
			1	1	1	1	1	1	1	1	1				

A24 (RW) A24 Enable
Modid (R) Active low Modid line to V253
Ready (R) V253 is ready for VXI access
Passd (R) V253 passed all of the self tests
Inhbt (RW) Inhibits assertion of *Sysfail on VXI bus
Reset (RW) Soft reset, run self test after Reset is deserted

$ 0x06 - Offset Register (RW)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
OFF 15	OFF 14	OFF 13	OFF 12	OFF 11	OFF 10	OFF 9	OFF 8	OFF 7	OFF 6	OFF 5	OFF 4	OFF 3	OFF 2	OFF 1	OFF 0

OFF[15:0] (RW) Offset Register which points to base address of module in A24 space

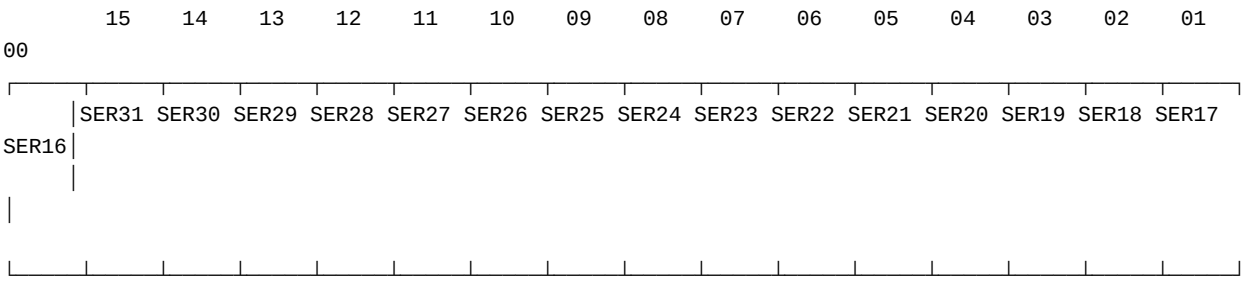
$ 0x08 - Attribute Register (R)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	1	1	1	1	1	1	1	1	1	1	1	0	1	0	

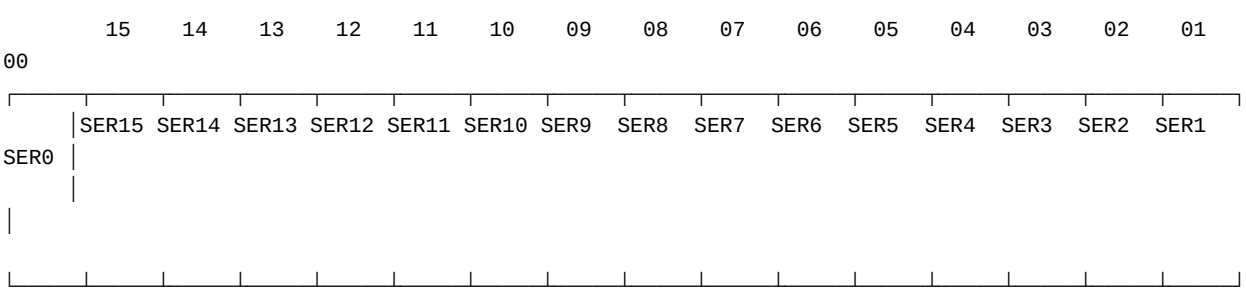
[2] (R) Interrupt Control Capability
[1] (R) No Interrupt Handler Capability
[0] (R) Interrupt Status Capability

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$ 0x0A - Serial Number High (R)

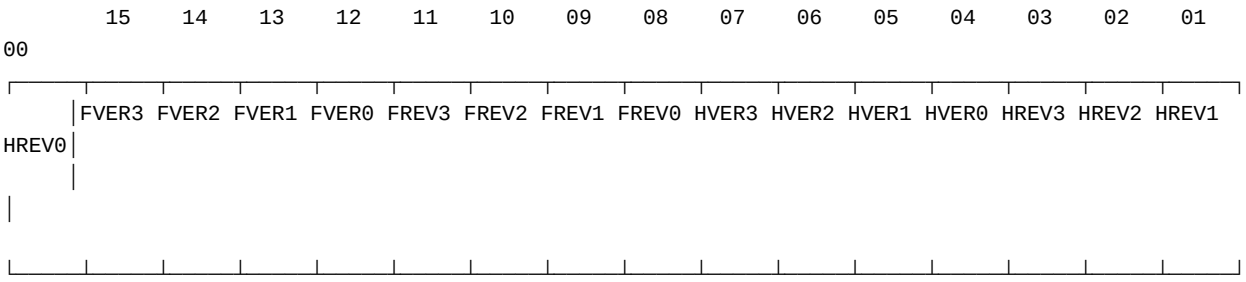


$ 0x0C - Serial Number Low (R)



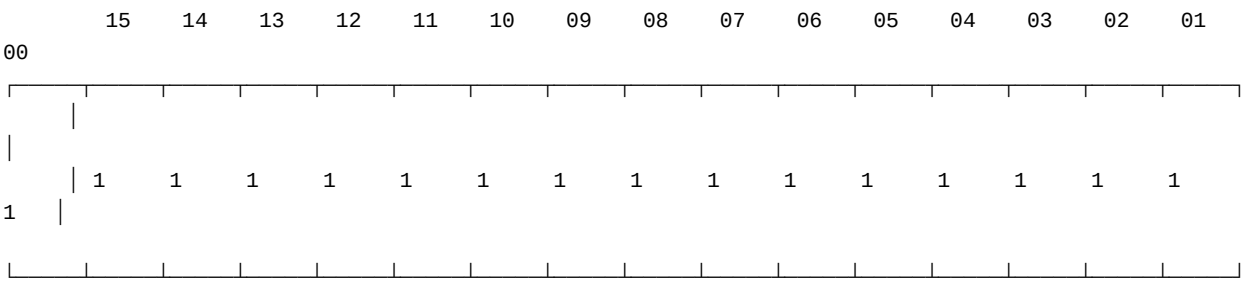
SER[31:0] (R)KSC's unique serial number for every module

$ 0x0E - Version Number Register (R)

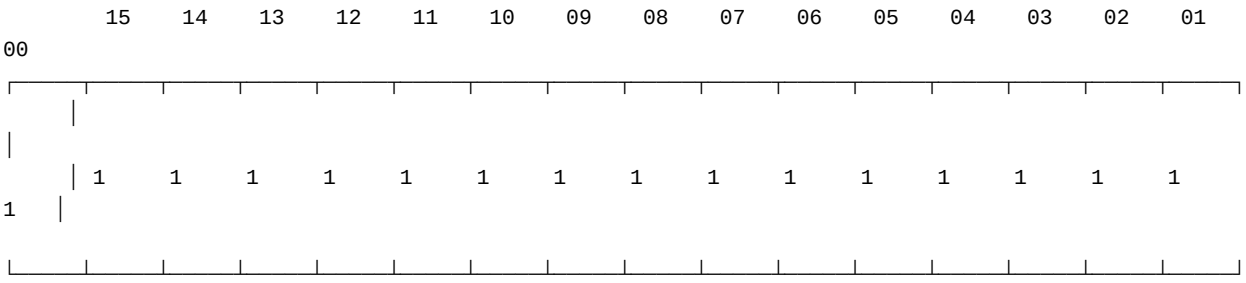


FVER[3:0] (R) ..... Firmware Main Version #
FREV[3:0] (R) ..... Firmware Revision #
HVER[3:0] (R) ..... Hardware Main Version #
HREV[3:0] (R) ..... Hardware Revision #

$ 0x10 to 0x18 - Reserved (R)

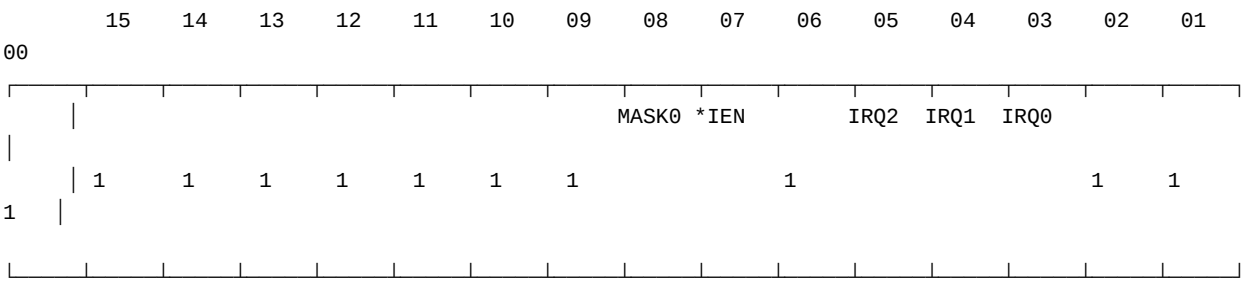


$ 0x1A - Interrupt Status Register (R)



[15:8] (R) ..... Status ID = FF
[7:0] (R) ..... Reserved

$ 0x1C - Interrupt Control Register (RW)



MASK0 (RW) ..... Interrupt Mask Bit for Interrupt Source

*IEN #0 .....

IRQ[2:0] (RW) ..... Interrupt Enable
(RW) ..... Interrupt Request Level
000 ..... IRQ7 001 IRQ6
010 ..... IRQ5
011 ..... IRQ4
100 ..... IRQ3

101 ..... IRQ2
110 ..... IRQ1
111 ..... Disconnected

$ 0x1E - Subclass Register (R)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

[15] (R) ..... VXI Extended Device
[14:0] (R)7FFE = Extended Register Based Device

$ 0x20 - Suffix High Register (R)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SUF31	SUF30	SUF29	SUF28	SUF27	SUF26	SUF25	SUF24	SUF23	SUF22	SUF21	SUF20	SUF19	SUF18	SUF17	SUF16

$ 0x22 - Suffix Low Register (R)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SUF15	SUF14	SUF13	SUF12	SUF11	SUF10	SUF9	SUF8	SUF7	SUF6	SUF5	SUF4	SUF3	SUF2	SUF1	SUF0

SUF[31:0] (R) 4 Character string representing the model's suffix.

$ 0x24 to 0x3F - User Defined Register (RW)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
USE15	USE14	USE13	USE12	USE11	USE10	USE9	USE8	USE7	USE6	USE5	USE4	USE3	USE2	USE1	USE0

USE[15:0] (RW) User defined register stored in EEPROM (non-volatile RAM).

A24 Space -- V253 Operational Registers

Note: Setting a bit in the following registers corresponds to programming a "1" and resetting a bit corresponds to programming a "0". NU = Bit not used.

$ 0x00 - Configuration Register (RW)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
EXTRG	CH17	NU	NU	CON3	CON2	CON1	CON0	NU	OVRLP	ADSEL	NU	TRIG3	TRIG2	TRIG1	TRIG0
(0)	(0)	(0)	(0)	(?)	(?)	(?)	(?)	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

() Power up value

EXTRG (RW) When set, the Front Panel Sample/Hold Signal is enabled.

CH16 (RW) When set, (Cold Junction Reference) is enabled in the CH16 slot. When reset, CH16 is enabled.

OVRLP (R) Overlap detected by V253 on MUX-bus.

CON[3:0] (R) Connector Type

1111 No Termination Housing (V752)

1101 V253 Termination Housing

ADSEL (RW) Address select bit for MUX-bus.

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```
              0             Setup Mode
              1             Run Mode

TRIG[3:0]     (RW)          TTL Trigger select for sample hold option.


1000    TTL Trig 0
1001    TTL Trig 1
1010    TTL Trig 2
1011    TTL Trig 3
1100    TTL Trig 4
1101    TTL Trig 5
1110    TTL Trig 6
1111    TTL Trig 7
0000    Disable
 .       .
 .       .
0111    Disable
```

$ 0x02 - Calibration Register (RW)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
REF	NU	NU	NU	NU	NU	NU	CAL9	CAL8	CAL7	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1
(0)	(0)	(0)	(0)	(0)	(0)	(0)	(1)	(0)	(0)	(1)	(0)	(0)	(0)	(0)	(1)

() Power up value

The on-board calibrator is a precision active attenuator that has as an input a 10 volt reference voltage, either on-board or from the MUX-bus. Use bit 15 to select this reference source.

Reference bit 15

1 - On-board reference
0 - MUX-bus reference

Bits 0 - 8 program the on-board calibrator as shown:

```
        bit 8 = Cal. polarity -                                  | Polarity stage
        bit 7 = Cal. polarity +                                  |

        bit 6 = stage one multiplier x 0.2                  |
        bit 5 = stage one multiplier x 0.5                  | stage one
        bit 4 = stage one multiplier x 1.0                  |

        bit 3 = stage two multiplier x 0.001                |
        bit 2 = stage two multiplier x 0.01                 | stage two
```

bit 1 = stage two multiplier x 0.1 |
bit 0 = stage two multiplier x 1.0 |

Select one ("1" = true) for each of the three stages. The output voltage from the calibrator will be the composite of the three stages multiplied by 10 volts (the value of the reference).

$ 0x04 - Selftest Register (R)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1
(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)	(?)

() Power up value

Bits 0-15 contain selftest results for each of the channels. A "0" designates a failed channel, a "1" designates the associated channel has passed selftest.

Setup Registers

$ 0x10 - CH 1 Setup (W)
$ 0x18 - CH 2 Setup (W)
$ 0x20 - CH 3 Setup (W)
$ 0x28 - CH 4 Setup (W)
$ 0x30 - CH 5 Setup (W)
$ 0x38 - CH 6 Setup (W)
$ 0x40 - CH 7 Setup (W)
$ 0x48 - CH 8 Setup (W)
$ 0x50 - CH 9 Setup (W)
$ 0x58 - CH 10 Setup (W)
$ 0x60 - CH 11 Setup (W)
$ 0x68 - CH 12 Setup (W)
$ 0x70 - CH 13 Setup (W)
$ 0x78 - CH 14 Setup (W)
$ 0x80 - CH 15 Setup (W)
$ 0x88 - CH 16 Setup (W)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
IMX1	IMX1	NU	FILBP	2KHZ	1KHZ	200HZ	20HZ	2G10	2G5	2G2	2G1	NU	1G100	1G10	1G1
(0)	(1)	(0)	(0)	(1)	(0)	(0)	(0)	(0)	(0)	(0)	(1)	(0)	(0)		



( ) Power up value

Bits [2:0]
- 001 - Stage 1 Gain = 1
- 010 - Stage 1 Gain = 10
- 100 - Stage 1 Gain = 100
- 000, 011, 101, 110, 111 = Invalid

Bits [7:4]
- 0001 - Stage 2 Gain = 1
- 0010 - Stage 2 Gain = 2
- 0100 - Stage 2 Gain = 5
- 1000 - Stage 2 Gain = 10
- 0000, 0011, 0101, 0111, 1001, 1010, 1011, 1100, 1101, 1110, 1111 = Invalid

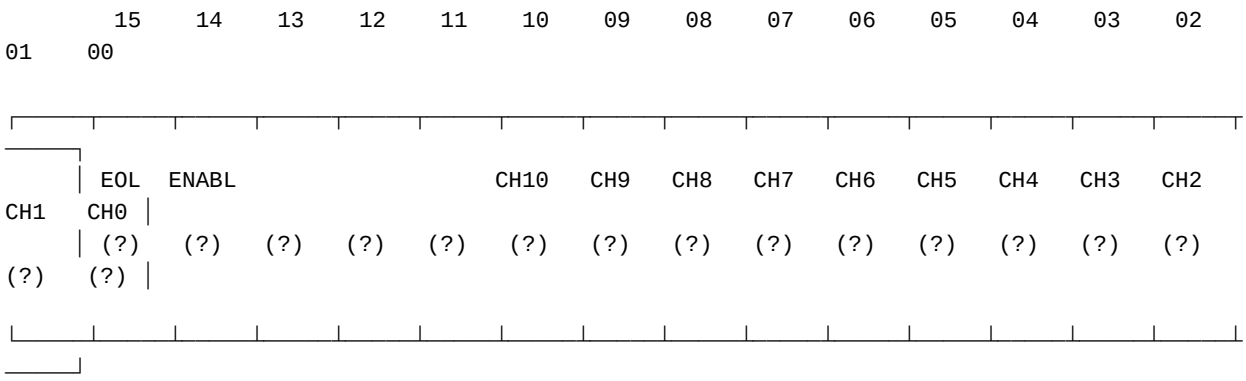
Bits [11:8]
- 0001 - Filter Bandedge = 20 Hz
- 0010 - Filter Bandedge = 200 Hz
- 0100 - Filter Bandedge = 1 KHz
- 1000 - Filter Bandedge = 2 KHz
- 0000, 0011, 0101, 0111, 1001, 1010, 1011, 1100, 1101, 1110, 1111 = Invalid

Bit [12]
- 0 - Filter Bypass Mode
- 1 - Filter Mode

Bits [15:14]
- 00 - Input MUX = Line
- 01 - Input MUX = Cal
- 10 - Input MUX = FPCal
- 11 - Input MUX = Zero

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Scan Ram 0x200 - 0x11FE



() power up value

EOL	(RW)	End of list.
ENABL	(RW)	Enables channel specified in CH [10:0].
CH [10:0]	(RW)	Selects channel number on the V253 to be placed out on the MUX-bus.

Note: A bus error will occur if a write is attempted while in 'run mode'.

Scan RAM is to be programmed to reflect a list of the active channels for a given application. There can be up to 2048 ADC Time Slots per frame dependent upon the Sample Clock frequency that has been selected. The channels, each representing an ADC time slot, are multiplexed into four paths with the channels being assigned to the paths as follows:

MUX Path A -- Channels 1,5,9,13
MUX Path B -- Channels 2,6,10,14
MUX Path C -- Channels 3,7,11,15
MUX Path D -- Channels 4,8,12,16

NOTE: Physical channels 1-16 are mapped as channels 0-15 in the Scan Ram.

This physical mapping of the channels causes certain restrictions on the loading of the Scan RAM in order to attain maximum system performance.
The Scan RAM must be loaded to allow acquiring consecutive samples from Path A, Path B, Path C, Path D respectively. For example, consecutive entries in the Scan RAM might appear as follows:

Address	Data(10-0)
0x200	xxxxxxxxx00 -- Corresponds to a Channel assigned to MUX Path A
0x202	xxxxxxxxx01 -- Corresponds to a Channel assigned to MUX Path B
0x204	xxxxxxxxx10 -- Corresponds to a Channel assigned to MUX Path C
0x206	xxxxxxxxx11 -- Corresponds to a Channel assigned to MUX Path D

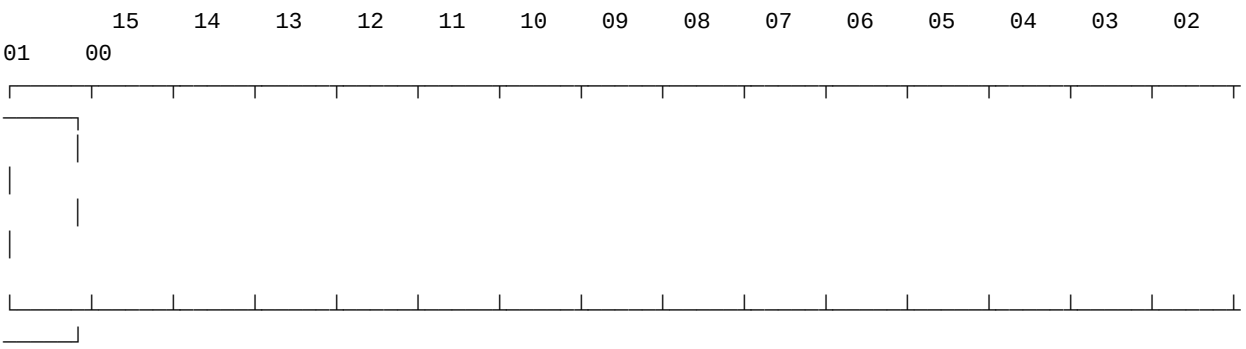
Bit 14 is a Channel by Channel Enable and should be set for all active channels that are to be converted.

Bit 15 is the End-of-List Bit and should be set for the last channel to be converted.

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NOTE: This Scan RAM should be programmed to the same values as the ADC Scan RAM except for the Enable Bit (Bit 14).

EEPROM 0x2000 - 0x21FE



The EEPROM space listed above is reserved for storing the calibrator correction terms as stated in Table 2.

APPENDIX A

The sample code supplied in this appendix shows an example configuring all 16 channels of the V253 with the first 16 channels of a V207.

```
#include <stdio.h>

typedef unsigned short uint16;
typedef unsigned long uint32;
typedef short int16;

uint16 const A24SuperData = 0x6;
uint16 const A32SuperData = 0x7;
uint32 const V253_serial = 1234;
uint32 const V207_serial = 3456;
uint16 const V253_sufhi = (('Z' << 8) | 'D');
uint16 const V253_suflo = (('1' << 8) | '1');
uint16 const V207_sufhi = (('Z' << 8) | 'B');
uint16 const V207_suflo = (('1' << 8) | '1');

void reportError() {
   printf("Error: closing VXIlibrary\n");
   CloseVXIlibrary();
   exit(1);
   }

uint16 find_la (
uint16 model,
uint32 serial_numb,
uint16 suf_high_numb,
uint16 suf_low_numb
) {
   int16  i,error;
   uint16 data,id,dev_type,la;
   uint16 serial,sufhi,suflo;

   la = 0xFF;
   for (I=0; i<0xFF; I++) {
      error = VXIinReg(i,0x0,&id);
      id &= 0xFFF;


      if (error ==0) {
         /* get device type value */
         error = VXIinReg(i,0x2,&dev_type);
         dev_type &= 0xFFF;
```

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```
        if (error != 0)
           reportError();

        /* get serial number */
        error = VXIinReg(i,0xA,&(uint16)serial);
        if (error != 0)
           reportError();
        error = VXIinReg(i,0xC,&data);
        if (error != 0)
           reportError();
        serial = (serial << 16) + (uint32)data;

        /* get suffix number */
        error = VXIinReg(i,0x20,&sufhi);
        if (error != 0)
           reportError();
        error = VXIinReg(i,0x22,&suflo);
        if (error != 0)
           reportError();

        if (id==0xF29 && dev_type==model && serial==serial_numb
        && sufhi==suf_high_numb && suflo==suf_low_numb) {
           la = I;
           printf("V%x found at logical address 0x%x\n",model,la);
           }
        }
     }
   if (la == 0xFF) {
      printf("V%x not found, search parameters incorrect\n",model);
      reportError();
      }

   return la;
   }
```

```
/*      The main program will assign all 16 channels of the V253 to      */
/* the first 16 channels of V207.  MUXbus will be enabled after both     */
/* Scan Tables have been written.                                        */
main () {
  uint16 V253,V207,data,i;
  uint32 address,A24_V253,A32_V207;
  int16 error;

  error = InitVXIlibrary();
  if (error != 0) {
    printf("Error: opening InitVXIlibrary()\n");
    exit(1);
    }
```

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Model V253

```
 V253 = find_la ( 0x253, V253_serial, V253_sufhi, V253_suflo);
 error = GetDevInfo(V253,12,&A24_V253);
 if (error != 0)
   reportError();

 V207 = find_la ( 0x207, V207_serial, V207_sufhi, V207_suflo);
 error = GetDevInfo(V207,12,&A32_V207);
 if (error != 0)
   reportError();

 address =  A32_V207 + 0x6;   /* V207 in setup mode   */
 data = 0;
 error = VXIout(A32SuperData,address,2,data);
 if (error != 0)
   reportError();

 address =  A24_V253;        /* V253 in setup mode   */
 data = 0;
 error = VXIout(A24SuperData,address,2,data);
 if (error != 0)
   reportError();









 address = A32_V207 + 0x200;         /* set V207 for 16 channels   */
 for (I=0; i<15; I++) {
   data = 0x4000 | I;
   error = VXIout(A32SuperData,address,2,data);
   if (error != 0)
     reportError();
   address += 2;
   }
 data = 0xC00F;
 error = VXIout(A32SuperData,address,2,data);
 if (error != 0)
   reportError();

 address = A24_V253 + 0x200;         /* set V253 for 16 channels   */
 for (I=0; i<15; I++) {
   data = 0x4000 | I;
   error = VXIout(A24SuperData,address,2,data);
   if (error != 0)
     reportError();
   address += 2;
   }
 data = 0xC00F;
```

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Model V253

```
 error = VXIout(A24SuperData,address,2,data);
 if (error != 0)
   reportError();

 for (I=1; I<=16; I++) { /* set all channels to unity gain */
   address = A24_V253 + (0x8*(I+1));
   data = 0x11;
   error = VXIout(A24SuperData,address,2,data);
   if (error != 0)
     reportError();
   }

 address = A32_V207;  /* V207 Internal Clk = 10 KHz */
 data = 0x45;
 error = VXIout(A32SuperData,address,2,data);
 if (error != 0)
   reportError();
 address =  A24_V253;        /* V253 in run mode */
 data = 0x20;
 error = VXIout(A24SuperData,address,2,data);
 if (error != 0)
   reportError();

 address =  A32_V207 + 0x6;    /* V207 in run mode */
 data = 0x01;
 error = VXIout(A32SuperData,address,2,data);
 if (error != 0)
   reportError();

 CloseVXIlibrary();
 }
```

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APPENDIX B

SAMPLE VOLTAGE CALIBRATION CODE

```
/* ---------------------------------------------------------------------
 * Function: v253VCal (Voltage Cal)
 *
 * Description:
 *     Given the channel name (from function getName), write the m and b
 *     values calculated based on the current values of the V253 stage gains
 *     into a data file to be retrieved by the getCalFile function (RETbcf)
 *     during load time.
 *
 * Inputs:
 *
 *       chan = V207 channel calibrated
 *       LocalID = local channel id
 *       LA of card to be calibrated
 *
 *
 * ---------------------------------------------------------------------*/
int v253VCal (uint8 LA, uint16 LocalID, uint16 chan, float *pm1, float *pb1)
{
uint16 I, wait, value, *prval;
int16          gain1, gain2, filter;
float          m, b, fullScale;
float          plusCal = 0.0;
float          minusCal = 0.0;
float          zeroCal = 0.0;
char           name[db_name_dim], fileName[16];

               /* put V253 into filter mode */
               KscV253SetupMode (V253SETUPMODE);
               KscV253SetFilterBypass (LA, FILTER);
               KscV253SetupMode (V253RUNMODE);

        /* calibrate channel */
        /* obtain stage 1, 2 gains */
        gain1 = KscV253GetStage1Gain(LA, LocalID);
               if (gain1 < 0)
                       printf("v253VCal: error obtaining gain1\n");
               switch (gain1) {
                       case V253S1X1: gain1= 1; break;
                       case V253S1X10: gain1= 10; break;
                       case V253S1X100: gain1= 100; break;
                       default: gain1 = 1; break;
               }
               gain2 = KscV253GetStage2Gain(LA, LocalID);
               if (gain2<0)
                       printf("v253VCal: error obtaining gain2\n");
               switch (gain2) {
                       case V253S2X1: gain2= 1; break;
```

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```
                case V253S2X2: gain2= 2; break;
                case V253S2X5: gain2= 5; break;
                case V253S2X10: gain2= 10; break;
                default: gain2 = 1; break;
        }
fullScale = (float) (10.0/gain1/gain2);
KscV253SetInputMUX (LA, V253CAL, LocalID);

        /* obtain filter setting and set the appropriate settling time */
        filter = KscV253GetFilter(LA, LocalID);
        wait = getWait (filter);
        plusCal = 0.0;
KscV253SetCalibration (LA, convert(fullScale), MUXBUS);
        taskDelay(wait);
for (I=1; i<NUM_ITER+1; I++) {
                KscV207ReadChan (v207LA, chan, &value);
                plusCal = plusCal + (float)(value);
                taskDelay(1);
}
        plusCal = plusCal / NUM_ITER;

/* repeat for minus full scale */
fullScale = -fullScale;

KscV253SetCalibration (LA, convert(fullScale), MUXBUS);
        filter = KscV253GetFilter(LA, LocalID);
        wait = getWait (filter);
        minusCal = 0.0;
        taskDelay(wait);
        for (I=1; i<NUM_ITER+1; I++) {
                KscV207ReadChan (v207LA, chan, &value);
                minusCal = minusCal + (float)(value);
                taskDelay(1);
        }
        minusCal = minusCal / NUM_ITER;
        /* zero pt cal */
        KscV253SetInputMUX (LA, V253ZERO, LocalID);
        filter = KscV253GetFilter(LA, LocalID);
        wait = getWait (filter);
        zeroCal = 0.0;
        taskDelay(wait);
        for (I=1; i<NUM_ITER+1; I++) {
                KscV207ReadChan (v207LA, chan, &value);
                zeroCal = zeroCal + (float) (value);
                taskDelay(1);
        }
        zeroCal= (float) (zeroCal / NUM_ITER);

        /* calc m and b and write to cal file */
        m = - (plusCal - minusCal)/(2*fullScale);
        *pm1 = m;
        b = zeroCal;
        *pb1 = b;
```

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```
        /* return V253 channel to in-line mode */
        KscV253SetInputMUX(LA, V253INLINE, LocalID);
        return 0;
}
```

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