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SYNCHRONOUS DRAM MODULE

MT2LSDT432U – 16MB
MT4LSDT832UD – 32MB
MT4LSDT1632UD – 64MB
MT4LSDT3232UD – 128MB

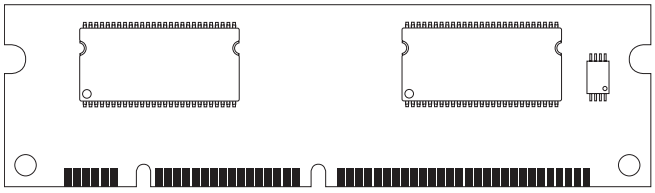
For the latest data sheet, please refer to the Micron® Web site: www.micron.com/products/modules

Features

- 100-pin, dual in-line memory module (DIMM)
- PC 100- and PC133-compliant
- 16MB (4 Meg x 32) , 32MB (8 Meg x 32), 64MB (16 Meg x 32), and 128MB (32 Meg x 32)
- Utilizes 125 MHz and 133 MHz SDRAM components
- Single +3.3V power supply
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8, or full page
- Auto Precharge and Auto Refresh Modes
  16MB, 32MB, and 64MB modules; 64ms, 4,096-cycle refresh (15.625µs refresh interval); 128MB modules; 64ms, 8,192-cycle refresh (7.81µs refresh interval)
- LVTTL-compatible inputs and outputs
- Serial Presence-Detect (SPD)
- Gold edge contacts

Figure 1: 100-Pin DIMM (MO–161)

Standard 1.00in. (25.40mm)



Options

Options	Marking
• Package	
100-pin DIMM (standard)	G
100-pin DIMM (lead-free)	Y
• Timing (Cycle Timing)	
7.5ns (133 MHz)	-75
8ns (125 MHz)	-8
10ns (100 MHz)	-10
• PCB	
Standard 1.00in. (25.40mm)	

Table 1: Timing Parameters

CL = CAS (READ) Latency

SPEED GRADE	CLOCK FREQUENCY	ACCESS TIME		SETUP TIME	HOLD TIME
		CL = 2	CL = 3		
-75	133 MHz	5.4ns	5.4ns	1.5ns	0.8ns
-8	125 MHz	6ns	6ns	2ns	1ns
-10	100 MHz	9ns	7.5ns	2ns	1ns

Table 2: Address Table

MODULE DENSITY	16MB	32MB	64MB	128MB
Refresh Count	4K	4K	4K	8K
Device Banks	4 (BA0–BA1)	4 (BA0–BA1)	4 (BA0–BA1)	4 (BA0–BA1)
Device Configuration	64Mb (4 Meg x 16)	64Mb (4 Meg x 16)	128Mb (8 Meg x 16)	256Mb (16 Meg x 16)
Device Row Addressing	4K (A0–A11)	4K (A0–A11)	4K (A0–A11)	8K (A0–A12)
Device Column Addressing	256 (A0–A7)	256 (A0–A7)	512 (A0–A8)	512 (A0–A8)
Module Ranks	1 (S0#, S2#)	2 (S0#, S2#, S1#, S3#)	2 (S0#, S2#, S1#, S3#)	2 (S0#, S2#, S1#, S3#)

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Table 3: Part Numbers

PART NUMBER[1]	DENSITY	CONFIGURATION	SYSTEM BUS SPEED
MT2LSDT432UG-75__	16MB	4 Meg x 32	133 MHz
MT2LSDT432UY-75__	16MB	4 Meg x 32	133 MHz
MT2LSDT432UG-8__	16MB	4 Meg x 32	125 MHz
MT2LSDT432UY-8__	16MB	4 Meg x 32	125 MHz
MT2LSDT432UG-10__	16MB	4 Meg x 32	100 MHz
MT2LSDT432UY-10__	16MB	4 Meg x 32	100 MHz
MT4LSDT832UDG-75__	32MB	8 Meg x 32	133 MHz
MT4LSDT832UDY-75__	32MB	8 Meg x 32	133 MHz
MT4LSDT832UDG-8__	32MB	8 Meg x 32	125 MHz
MT4LSDT832UDY-8__	32MB	8 Meg x 32	125 MHz
MT4LSDT832UDG-10__	32MB	8 Meg x 32	100 MHz
MT4LSDT832UDY-10__	32MB	8 Meg x 32	100 MHz
MT4LSDT1632UDG-75__	64MB	16 Meg x 32	133 MHz
MT4LSDT1632UDY-75__	64MB	16 Meg x 32	133 MHz
MT4LSDT1632UDG-8__	64MB	16 Meg x 32	125 MHz
MT4LSDT1632UDY-8__	64MB	16 Meg x 32	125 MHz
MT4LSDT1632UDG-10__	64MB	16 Meg x 32	100 MHz
MT4LSDT1632UDY-10__	64MB	16 Meg x 32	100 MHz
MT4LSDT3232UDG-75__	128MB	32 Meg x 32	133 MHz
MT4LSDT3232UDY-75__	128MB	32 Meg x 32	133 MHz
MT4LSDT3232UDG-8__	128MB	32 Meg x 32	125 MHz
MT4LSDT3232UDY-8__	128MB	32 Meg x 32	125 MHz
MT4LSDT3232UDG-10__	128MB	32 Meg x 32	100 MHz
MT4LSDT3232UDY-10__	128MB	32 Meg x 32	100 MHz

NOTE:

1. All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT2LSDT432UG-8B1.

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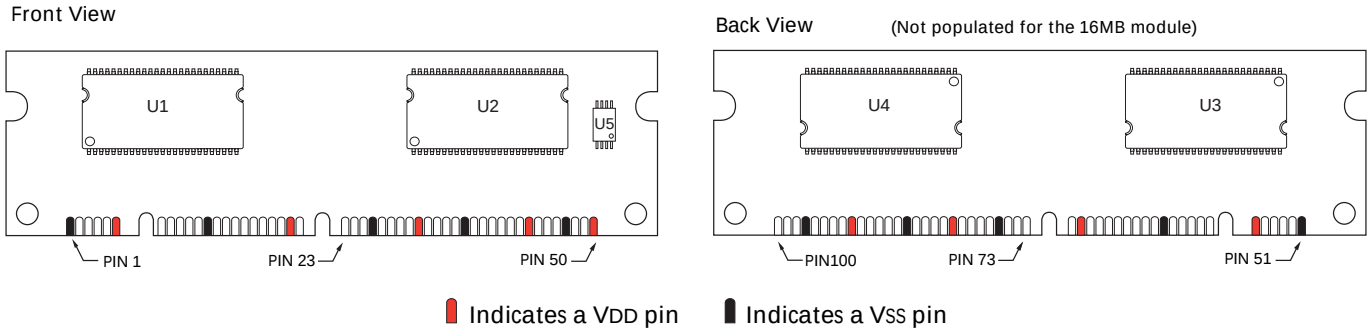
Table 4: Pin Assignment (100-Pin DIMM Front)

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	VSS	13	A0	26	VSS	38	DQ16
2	DQ0	14	A2	27	CKE0	39	DQ17
3	DQ1	15	A4	28	WE#	40	DQ18
4	DQ2	16	A6	29	S0#	41	DQ19
5	DQ3	17	A8	30	S2#	42	VDD
6	VDD	18	A10	31	VDD	43	DQ20
7	DQ4	19	BA1	32	NC	44	DQ21
8	DQ5	20	A12	33	NC	45	DQ22
9	DQ6	21	VDD	34	NC	46	DQ23
10	DQ7	22	DNU	35	NC	47	VSS
11	DQMB0	23	RFU	36	VSS	48	SDA
12	VSS	24	RFU	37	DQMB2	49	SCL
		25	CK0			50	VDD

Table 5: Pin Assignment (100-Pin DIMM Back)

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
51	VSS	63	A1	76	VSS	88	DQ24
52	DQ8	64	A3	77	CKE1	89	DQ25
53	DQ9	65	A5	78	DNU	90	DQ26
54	DQ10	66	A7	79	S1#	91	DQ27
55	DQ11	67	A9	80	S3#	92	VDD
56	VDD	68	BA0	81	VDD	93	DQ28
57	DQ12	69	A11	82	NC	94	DQ29
58	DQ13	70	NC	83	NC	95	DQ30
59	DQ14	71	VDD	84	NC	96	DQ31
60	DQ15	72	RAS#	85	NC	97	VSS
61	DQMB1	73	CAS#	86	VSS	98	SA0
62	VSS	74	RFU	87	DQMB3	99	SA1
		75	CK1			100	SA2

Figure 2: Module Layout



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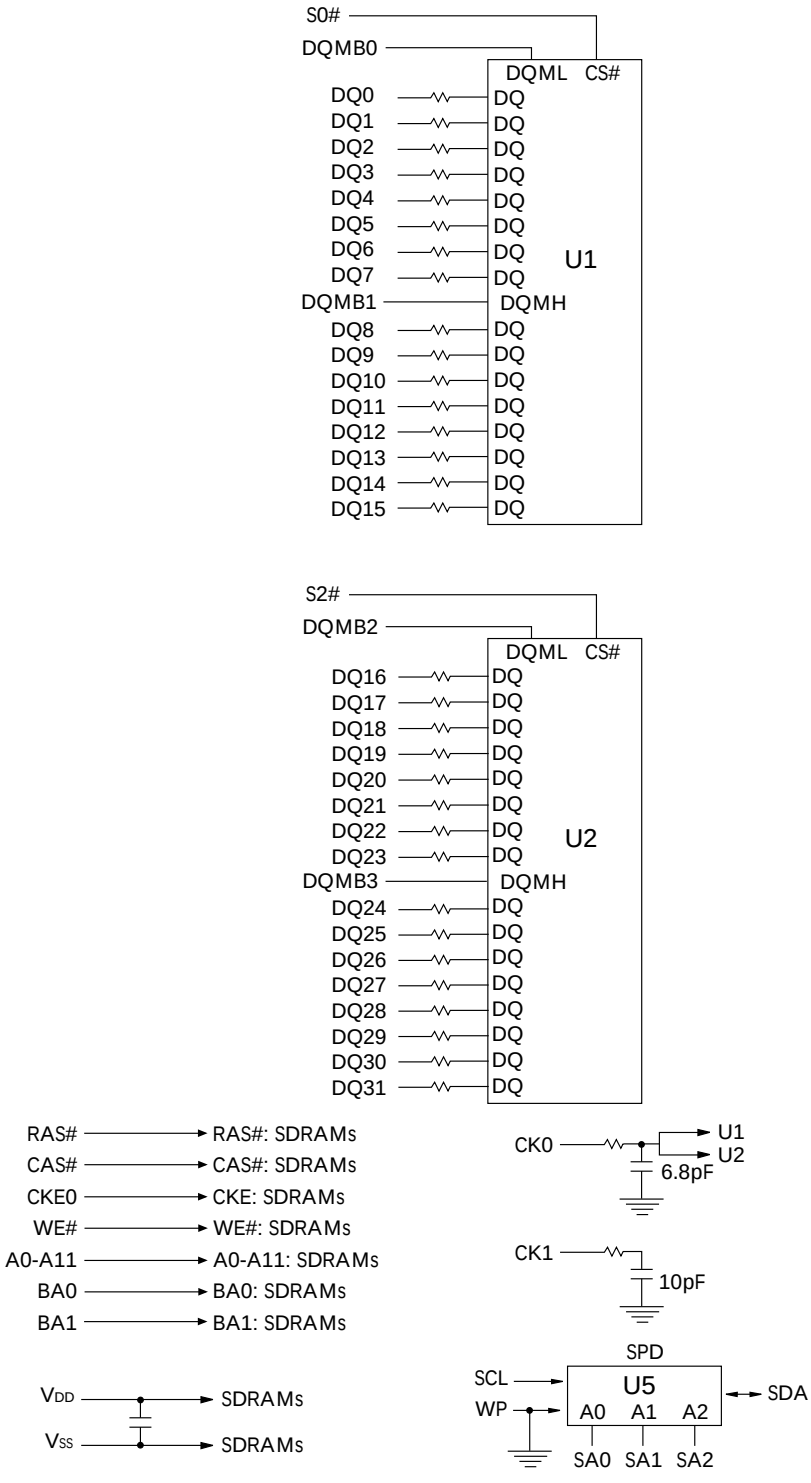
Table 6: Pin Descriptions

Pin numbers may not correlate with symbols; for more information refer to the Pin Assignment tables on page 3

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
28, 72, 73	RAS#, CAS#, WE#	Input	Command Inputs: RAS#, CAS# and WE# (along with S#) define the command being entered.
25, 75	CK0, CK1	Input	Clock: CK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CK. CK also increments the internal burst counter and controls the output registers.
27, 77	CKE0, CKE1	Input	Clock Enable: CKE activates (HIGH) and deactivates (LOW) the CK signal. Deactivating the clock provides POWER-DOWN and SELF REFRESH operation (all banks idle), or CLOCK SUSPEND operation (burst access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CK is disabled during power-down and self refresh modes, providing low standby power.
29, 30, 79, 80	S0#–S3#	Input	Chip Select: S# enables (registered LOW) and disablse (registered HIGH) the command decoder. All commands are masked when S# is registered HIGH. S# is considered part of the command code.
11, 37, 61, 87	DQMB0–DQMB3	Input	Input/Output Mask: DQMB is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQMB is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (after a two-clock latency) when DQMB is sampled HIGH during a READ cycle.
19, 68	BA0, BA1	Input	Bank Address: BA0 and BA1 define to which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied.
13-18, 63-67, 69–70	A0–A12	Input	Address Inputs: A0-A12 are sampled during the ACTIVE command (row-address A0-A12) and READ/WRITE command (column-address A0-A8, with A10 defining AUTO PRECHARGE) to select one location out of the memory array in the respective bank. A10 is sampled during a PRE-CHARGE command to determine if both banks are to be precharged (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
2–5, 7–10, 38–41, 43–46, 52–55, 57–60, 88–91, 93–96	DQ0–DQ31	Input/ Output	Data I/Os: Data bus.
6, 21, 31, 42, 50, 56, 71, 81, 92	V_{DD}	Supply	Power Supply: +3.3V ±0.3V.
1, 12, 26, 36, 47, 51, 62, 76, 86, 97	V_{SS}	Supply	Ground.
48	SDA	Input/ Output	Serial Presence-Detect Data: SDA is a bidirectional pin used to transfer addresses and data into and data out of the presence-detect portion of the module.
49	SCL	Input	Serial Clock for Presence-Detect: SCL is used to synchronize the presence-detect data transfer to and from the module.
98-100	SA0–SA2	Input	Presence-Detect Address Inputs: These pins are used to configure the presence-detect device.
23, 24, 74	RFU	–	Reserved for Future Use: These pins should be left unconnected.
22, 78	DNU	–	Do Not Use: These pins are not connected on this module but are assigned pins on the compatible DRAM version.
32–35, 70, 82–85	NC	–	Not connected.

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Figure 3: Functional Block Diagram – 16MB



NOTE:

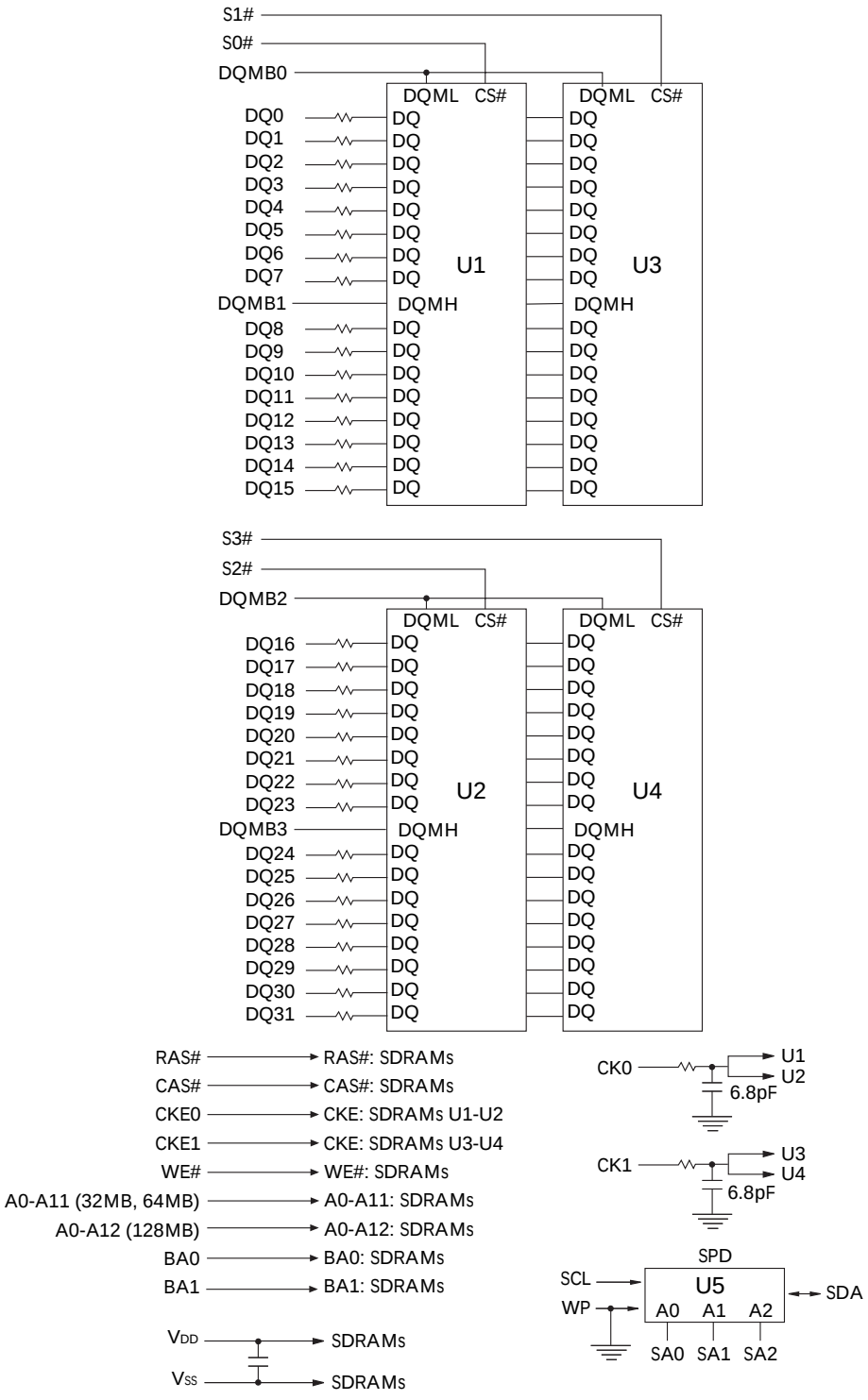
1. All resistor values are 10Ω.
2. Per industry standard, Micron utilizes various component speed grades as referenced in the Module Part Numbering Guide at www.micron.com/numberguide.

Standard modules use the following SDRAM devices:
MT48LC8M16A2TG

Lead-free modules use the following SDRAM devices:
MT48LC8M16A2P

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Figure 4: Functional Block Diagram – 32MB, 64MB, 128MB



NOTE:

1. All resistor values are 10Ω.
2. Per industry standard, Micron utilizes various component speed grades as referenced in the Module Part Numbering Guide at www.micron.com/numberguide.

Standard modules use the following SDRAM devices:
MT48LC8M16A2TG (32MB); MT48LC16M16A2TG (64MB);
MT48LC32M16A2TG (128MB)

Lead-free modules use the following SDRAM devices:
MT48LC8M16A2P (32MB); MT48LC16M16A2TG (64MB);
MT48LC32M16A2TG (128MB)

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General Description

The MT2LSDT432U, MT4LSDT832UD, MT4LSDT1632UD, and MT4LSDT3232UD are high-speed CMOS, dynamic random-access, 16MB, 32MB, 64MB, and 128MB memory modules organized in a x32 configuration. These modules use SDRAM devices which are internally configured as quad-bank DRAMs with a synchronous interface (all signals are registered on the positive edge of the clock signal CK).

Read and write accesses to the SDRAM module are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the device bank and row to be accessed. BA0, BA1 select the device bank; A0–A11 (16MB, 32MB, and 64MB) or A0–A12 (128MB). The address bits registered coincident with the READ or WRITE command (A0–A7 for 16MB and 32MB; A0–A8 for 64MB and 128MB) are used to select the starting device column location for the burst access.

These modules provide for programmable READ or WRITE burst lengths of 1, 2, 4, or 8 locations, or the full page, with a burst terminate option. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence. These modules use an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one device bank while accessing one of the other three device banks will hide the PRECHARGE cycles and provide seamless, high-speed, random access operation.

These modules are designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs, outputs, and clocks are LVTTL-compatible.

SDRAM modules offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal device banks in order to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access. For more information regarding SDRAM operation, refer to the 64Mb, 128Mb, or 256Mb SDRAM component data sheets.

Serial Presence-Detect Operation

These modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard I^2C bus using the DIMM's SCL (clock) and SDA (data) signals. Write protect (WP) is tied to ground on the module, permanently disabling hardware write protect.

Initialization

SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Once power is applied to V_{DD} and the clock is stable (stable clock is defined as a signal cycling within timing constraints specified for the clock pin), the SDRAM requires a 100µs delay prior to issuing any command other than a COMMAND INHIBIT or NOP. Starting at some point during this 100µs period and continuing at least through the end of this period, COMMAND INHIBIT or NOP commands should be applied.

Once the 100µs delay has been satisfied with at least one COMMAND INHIBIT or NOP command having been applied, a PRECHARGE command should be applied. All device banks must then be precharged, thereby placing the device in the all banks idle state.

Once in the idle state, two AUTO REFRESH cycles must be performed. After the AUTO REFRESH cycles are complete, the SDRAM is ready for mode register programming. Because the mode register will power up in an unknown state, it should be loaded prior to applying any operational command.

Mode Register Definition

The mode register is used to define the specific mode of operation of the SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency, an operating mode and a write burst mode, as shown in Figure 5, Mode Register Definition Diagram, on page 8. The mode register is programmed via the LOAD MODE REGISTER command and will retain the stored information until it is programmed again or the device loses power.

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Mode register bits M0–M2 specify the burst length, M3 specifies the type of burst (sequential or interleaved), M4–M6 specify the CAS latency, M7 and M8 specify the operating mode, M9 specifies the write burst mode, and M10 and M11 are reserved for future use. For the 128MB module, address A12 (M12) is undefined but should be driven LOW during loading of the mode register.

The mode register must be loaded when all device banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Burst Length

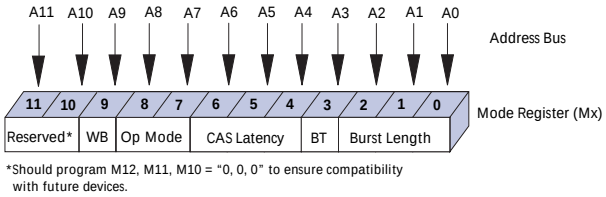
Read and write accesses to the SDRAM are burst oriented, with the burst length being programmable, as shown in Figure 5, Mode Register Definition Diagram. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 1, 2, 4, or 8 locations are available for both the sequential and the interleaved burst types, and a full-page burst is available for the sequential type. The full-page burst is used in conjunction with the BURST TERMINATE command to generate arbitrary burst lengths.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached, as shown in Table 7, Burst Definition, on page 9. The block is uniquely selected by A1–A*i* when the burst length is set to two; by A2–A*i* when the burst length is set to four; and by A3–A*i* when the burst length is set to eight. The remaining (least significant) address bit(s) is (are) used to select the starting location within the block See note 7 of Table 7, Burst Definition, on page 9 for values of A*i*. Full-page bursts wrap within the page if the boundary is reached, as shown in Table 7, Burst Definition, on page 9.

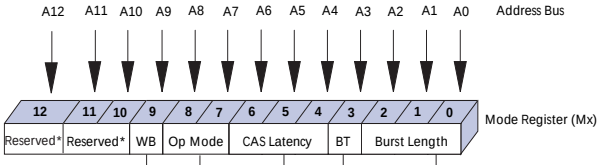
Figure 5: Mode Register Definition Diagram

16MB, 32MB, and 64MB Modules



*Should program M12, M11, M10 = "0, 0, 0" to ensure compatibility with future devices.

128MB Module



*Should program M11, M10 = "0, 0" to ensure compatibility with future devices.

	Burst Length	
M2 M1 M0	M3 = 0	M3 = 1
0 0 0	1	1
0 0 1	2	2
0 1 0	4	4
0 1 1	8	8
1 0 0	Reserved	Reserved
1 0 1	Reserved	Reserved
1 1 0	Reserved	Reserved
1 1 1	Full Page	Reserved

M3	Burst Type
0	Sequential
1	Interleaved

M6 M5 M4	CAS Latency
0 0 0	Reserved
0 0 1	Reserved
0 1 0	2
0 1 1	3
1 0 0	Reserved
1 0 1	Reserved
1 1 0	Reserved
1 1 1	Reserved

M8	M7	M6-M0	Operating Mode
0	0	Defined	Standard Operation
-	-	-	All other states reserved

M9	Write Burst Mode
0	Programmed Burst Length
1	Single Location Access

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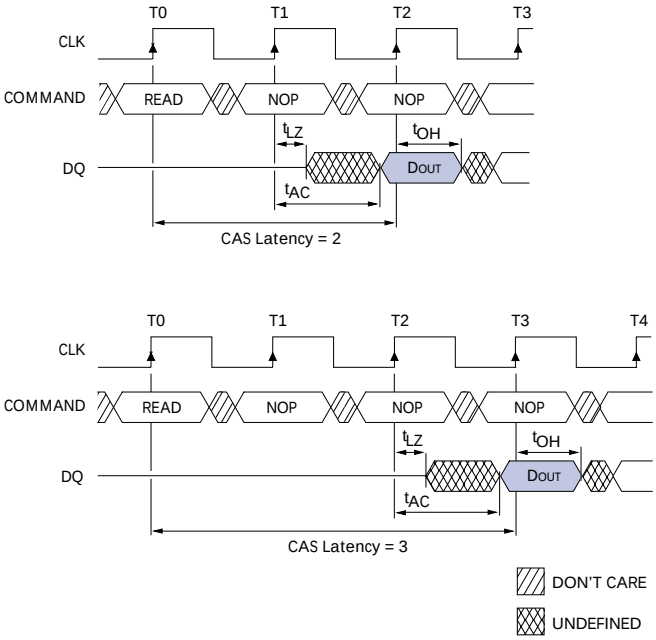
Table 7: Burst Definition

BURST LENGTH	STARTING COLUMN ADDRESS	ORDER OF ACCESSES WITHIN A BURST	
		TYPE = SEQUENTIAL	TYPE = INTERLEAVED
2	A0		
	0	0-1	0-1
	1	1-0	1-0
4	A1 A0		
	0 0	0-1-2-3	0-1-2-3
	0 1	1-2-3-0	1-0-3-2
	1 0	2-3-0-1	2-3-0-1
	1 1	3-0-1-2	3-2-1-0
8	A2 A1 A0		
	0 0 0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0 0 1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0 1 0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0 1 1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1 0 0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1 0 1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1 1 0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1 1 1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full Page (512)	n = A0–A8 (location 0–y)	Cn, Cn+1, Cn+2, Cn+3, Cn+4..., ...Cn-1, Cn...	Not Supported

NOTE:

1. For a burst length of two, A1–A*i* select the block-of-two burst; A0 selects the starting column within the block.
2. For a burst length of four, A2–A*i* select the block-of-four burst; A0-A1 select the starting column within the block.
3. For a burst length of eight, A3–A*i* select the block-of-eight burst; A0-A2 select the starting column within the block.
4. For a full-page burst, the full row is selected, and A0–A*i* select the starting column.
5. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
6. For a burst length of one, A0–A*i* select the unique column to be accessed, and Mode Register bit M3 is ignored.
7. A*i* = A7 for 16MB and 32MB;
   A*i* = A8 for 64MB and 128MB

Figure 6: CAS Latency Diagram



CAS Latency

The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to two or three clocks.

If a READ command is registered at clock edge *n*, and the latency is *m* clocks, the data will be available by clock edge *n* + *m*. The DQs will start driving as a result of the clock edge one cycle earlier (*n* + *m* - 1), and provided that the relevant access times are met, the data will be valid by clock edge *n* + *m*.

For example, assuming that the clock cycle time is such that all relevant access times are met, if a READ command is registered at T0 and the latency is programmed to two clocks, the DQ will start driving after T1 and the data will be valid by T2, as shown in Figure 6, CAS Latency Diagram.

Table 8, CAS Latency Table, indicates the operating frequencies at which each CAS latency setting can be used.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

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Operating Mode

The normal operating mode is selected by setting M7 and M8 to zero; the other combinations of values for M7 and M8 are reserved for future use and/or test modes. The programmed burst length applies to both READ and WRITE bursts.

Write Burst Mode

When M9 = 0, the burst length programmed via M0–M2 applies to both READ and WRITE bursts; when M9 = 1, the programmed burst length applies to READ bursts, but write accesses are single-location (non-burst) accesses.

Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

Table 8: CAS Latency Table

SPEED	ALLOWABLE OPERATING CLOCK FREQUENCY (MHz)	
	CAS LATENCY = 2	CAS LATENCY = 3
-75	≤ 100	≤ 133
-8	≤ 100	≤ 133
-10	≤ 100	≤ 100

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Commands

Table 9, Commands and DQMB Operation Truth Table provides a general reference of available commands. For a more detailed description of commands and operations, refer to the 64Mb, 128Mb, or 256Mb SDRAM component data sheet.

Table 9: Commands and DQMB Operation Truth Table

CKE is HIGH for all commands shown except SELF REFRESH

NAME (FUNCTION)	S#	RAS#	CAS#	WE#	DQMB	ADDR	DQS	NOTES
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	
NO OPERATION (NOP)	L	H	H	H	X	X	X	
ACTIVE (Select bank and activate row)	L	L	H	H	X	Bank/Row	X	1
READ (Select bank and column, and start READ burst)	L	H	L	H	L/H[7]	Bank/Col	X	2
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	L/H[7]	Bank/Col	Valid	4
BURST TERMINATE	L	H	H	L	X	X	Active	
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	X	Code	X	3
AUTO REFRESH or	L	L	L	H	X	X	X	4, 5
SELF REFRESH (Enter self refresh mode)								
LOAD MODE REGISTER	L	L	L	L	X	Op-Code	X	6
Write Enable/Output Enable	–	–	–	–	L	–	Active	7
Write Inhibit/Output High-Z	–	–	–	–	H	–	High-Z	7

NOTE:

1. A0–A11(32MB) or A0–A12 (64MB, 128MB, and 128MB) provide row address and BA0 and BA1 determine which bank is made active.
2. A0–A8 (16MB and 32MB) or A0–A8 (64MB and 128MB) provide column address; A10 HIGH enables the auto precharge feature (nonpersistent), while A10 LOW disables the auto precharge feature; BA0 and BA1 determine which bank is being read from or written to.
3. A10 LOW: BA0 and BA1 determine which bank is being precharged. A10 HIGH: both banks are precharged and BA0 and BA1 are "Don't Care."
4. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
5. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.
6. A0–A11 (32MB) or A0–A12 (64MB, 128MB, and 128MB) define the op-code written to the Mode Register.
7. Activates or deactivates the DQs during WRITEs (zero-clock delay) and READs (two-clock delay).

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Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Voltage on V_{DD} Supply
Relative to V_{SS} . . . . . -1V to +4.6V
Voltage on Inputs, NC or I/O Pins
Relative to V_{SS} . . . . . -1V to +4.6V

Operating Temperature
T_{OPR} (Commercial - ambient) . . . . . 0°C to +65°C
Storage Temperature (plastic) . . . . . -55°C to +150°C

Table 10: DC Electrical Characteristics and Operating Conditions – 16MB

Notes: 1, 6; V_{DD} = +3.3V ±0.3V

PARAMETER/CONDITION		SYM	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE		V_{DD}	3	3.6	V	
INPUT HIGH VOLTAGE: Logic 1; All inputs		V_{IH}	2	V_{DD} + 0.3	V	22
INPUT LOW VOLTAGE: Logic 0; All inputs		V_{IL}	-0.3	0.4	V	22
INPUT LEAKAGE CURRENT: Any input 0V ≤ V_{IN} ≤ V_{DD} (All other pins not under test = 0V)	Command and Address	I_{I1}	-10	10	µA	33
	CK, DQMB	I_{I2}	-10	10	µA	
	S#	I_{I3}	-5	5	µA	
OUTPUT LEAKAGE CURRENT: DQs are disabled; 0V ≤ V_{OUT} ≤ V_{DD}	DQ	I_{OZ}	-5	5	µA	33
OUTPUT LEVELS: Output High Voltage (I_{OUT} = -4mA) Output Low Voltage (I_{OUT} = 4mA)		V_{OH}	2.4	–	V	
		V_{OL}	–	0.4	V	

Table 11: DC Electrical Characteristics and Operating Conditions – 32MB, 64MB, 128MB

Notes: 1, 6; notes appear on page 18; V_{DD} = +3.3V ±0.3V

PARAMETER/CONDITION		SYM	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE		V_{DD}	3	3.6	V	
INPUT HIGH VOLTAGE: Logic 1; All inputs		V_{IH}	2	V_{DD} + 0.3	V	22
INPUT LOW VOLTAGE: Logic 0; All inputs		V_{IL}	-0.3	0.8	V	22
INPUT LEAKAGE CURRENT: Any input 0V ≤ V_{IN} ≤ V_{DD} (All other pins not under test = 0V)	Command and Address	I_{I1}	-20	20	µA	33
	CK, DQMB	I_{I2}	-10	10	µA	
	S#	I_{I3}	-5	5	µA	
OUTPUT LEAKAGE CURRENT: DQs are disabled; 0V ≤ V_{OUT} ≤ V_{DD}	DQ	I_{OZ}	-10	10	µA	33
OUTPUT LEVELS: Output High Voltage (I_{OUT} = -4mA) Output Low Voltage (I_{OUT} = 4mA)		V_{OH}	2.4	–	V	
		V_{OL}	–	0.4	V	

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Table 12: IDD Specifications and Conditions – 16MB

Notes: 1, 6, 11, 13; notes appear on page 18; VDD = +3.3V ±0.3V

			MAX				
PARAMETER/CONDITION		SYM	-75	-8	-10	UNITS	NOTES
OPERATING CURRENT: Active Mode; Burst = 2; READ or WRITE; RC = tRC (MIN); CAS latency = 3		IDD1	230	190	180	mA	3, 18, 19, 29
STANDBY CURRENT: Power-Down Mode; CKE = LOW; All banks idle		IDD2	4	4	6	mA	29
STANDBY CURRENT: Active Mode; CKE = HIGH; S3# = HIGH; All banks active after tRCD met; No accesses in progress		IDD3	90	70	60	mA	3, 12, 19, 29
OPERATING CURRENT: Burst Mode; Continuous burst; READ or WRITE; All banks active; CAS latency = 3		IDD4	280	240	210	mA	3, 18, 19, 29
AUTO REFRESH CURRENT: CKE = HIGH; S# = HIGH	tRC = tRC (MIN); CL = 3	IDD5	420	380	340	mA	3, 12, 18, 19, 29, 30
	tRC = 15.625µs; CL = 3	IDD6	6	80	70	mA	
SELF REFRESH CURRENT: CKE ≤ 0.2V		IDD7	2	2	4	mA	4

Table 13: IDD Specifications and Conditions – 32MB

Notes: 1, 6, 11, 13; notes appear on page 18; VDD = +3.3V ±0.3V

			MAX				
PARAMETER/CONDITION		SYM	-75	-8	-10	UNITS	NOTES
OPERATING CURRENT: Active Mode; Burst = 2; READ or WRITE; RC = tRC (MIN); CAS latency = 3		IDD1[a]	234	260	240	mA	3, 18, 19, 29
STANDBY CURRENT: Power-Down Mode; CKE = LOW; All banks idle		IDD2[b]	8	8	12	mA	29
STANDBY CURRENT: Active Mode; CKE = HIGH; S# = HIGH; All banks active after tRCD met; No accesses in progress		IDD3[a]	104	140	120	mA	3, 12, 19, 29
OPERATING CURRENT: Burst Mode; Continuous burst; READ or WRITE; All banks active; CAS latency = 3		IDD4[a]	304	310	270	mA	3, 18, 19, 29
AUTO REFRESH CURRENT: CKE = HIGH; S# = HIGH	tRC = tRC (MIN); CL = 3	IDD5[b]	1,240	760	680	mA	3, 12, 18, 19, 29, 30
	tRC = 15.625µs; CL = 3	IDD6[b]	12	160	140	mA	
SELF REFRESH CURRENT: CKE ≤ 0.2V		IDD7[b]	8	4	8	mA	4

a - Value calculated as one module rank in this operating condition, and all other ranks in Power-Down Mode.
b - Value calculated reflects all module ranks in this operating condition.

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Table 14: IDD Specifications and Conditions – 64MB

Notes: 1, 6, 11, 13; notes appear on page 18; VDD = +3.3V ±0.3V

			MAX				
PARAMETER/CONDITION		SYM	-75	-8	-10	UNITS	NOTES
OPERATING CURRENT: Active Mode; Burst = 2; READ or WRITE; RC = tRC (MIN); CAS latency = 3		IDD1[a]	304	360	360	mA	3, 18, 19, 29
STANDBY CURRENT: Power-Down Mode; CKE = LOW; All banks idle		IDD2[b]	8	8	8	mA	29
STANDBY CURRENT: Active Mode; CKE = HIGH; S# = HIGH; All banks active after tRCD met; No accesses in progress		IDD3[a]	104	160	160	mA	3, 12, 19, 29
OPERATING CURRENT: Burst Mode; Continuous burst; READ or WRITE; All banks active; CAS latency = 3		IDD4[a]	304	360	360	mA	3, 18, 19, 29
AUTO REFRESH CURRENT: CKE = HIGH; S# = HIGH	tRC = tRC (MIN); CL = 3	IDD5[b]	1,240	800	800	mA	3, 12, 18, 19, 29, 30
	tRC = 15.625µs; CL = 3	IDD6[b]	12	180	180	mA	
SELF REFRESH CURRENT: CKE ≤ 0.2V		IDD7[b]	8	6	6	mA	4

a - Value calculated as one module rank in this operating condition, and all other ranks in Power-Down Mode.
b - Value calculated reflects all module ranks in this operating condition.

Table 15: IDD Specifications and Conditions – 128MB

Notes: 1, 6, 11, 13; notes appear on page 18; VDD = +3.3V ±0.3V

			MAX				
PARAMETER/CONDITION		SYM	-75	-8	-10	UNITS	NOTES
OPERATING CURRENT: Active Mode; Burst = 2; READ or WRITE; RC = tRC (MIN); CAS latency = 3		IDD1	254	254	254	mA	3, 18, 19, 29
STANDBY CURRENT: Power-Down Mode; CKE = LOW; All banks idle		IDD2	8	8	8	mA	29
STANDBY CURRENT: Active Mode; CKE = HIGH; S# = HIGH; All banks active after tRCD met; No accesses in progress		IDD3	84	84	84	mA	3, 12, 19, 29
OPERATING CURRENT: Burst Mode; Continuous burst; READ or WRITE; All banks active; CAS latency = 3		IDD4	274	274	274	mA	3, 18, 19, 29
AUTO REFRESH CURRENT: CKE = HIGH; S# = HIGH	tRC = tRC (MIN); CL = 3	IDD5	1,080	1,080	1,080	mA	3, 12, 18, 19, 29, 30
	tRC = 7.8125µs; CL = 3	IDD6	14	14	14	mA	
SELF REFRESH CURRENT: CKE ≤ 0.2V		IDD7	10	10	10	mA	4

a - Value calculated as one module rank in this operating condition, and all other ranks in Power-Down Mode.
b - Value calculated reflects all module ranks in this operating condition.

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Table 16: Capacitance – 16MB

Note: 2; notes appear on page 18

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Capacitance: Address and Command	C_{I1}	5	7.6	pF
Input Capacitance: CKE	C_{I2}	5	7.6	pF
Input Capacitance: CK	C_{I3}	11.8	13.8	pF
Input Capacitance: S#	C_{I4}	5	7.6	pF
Input Capacitance: DQMB	C_{I5}	5	7.6	pF
Input/Output Capacitance: DQ	C_{IO}	4	6	pF

Table 17: Capacitance – 32MB, 64MB, and 128MB

Note: 2; notes appear on page 18

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Capacitance: Address and Command	C_{I1}	10	15.2	pF
Input Capacitance: CKE	C_{I2}	5	7.6	pF
Input Capacitance: CK	C_{I3}	11.8	13.8	pF
Input Capacitance: S#	C_{I4}	5	7.6	pF
Input Capacitance: DQMB	C_{I5}	10	15.2	pF
Input/Output Capacitance: DQ	C_{IO}	8	12	pF

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Table 18: SDRAM Component AC Electrical Characteristics

Notes: 5, 6, 8, 9, 11, 31; notes appear on page 18

AC CHARACTERISTICS			-75		-8		-10			
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from CLK (positive edge)	CL = 3	^tAC		5.4		6		7.5	ns	27
	CL = 2	^tAC		6		6		9	ns	
Address hold time		^tAH	0.8		1		1		ns	
Address setup time		^tAS	1.5		2		2		ns	
CLK high-level width		^tCH	2.5		3		3		ns	
CLK low-level width		^tCL	2.5		3		3		ns	
Clock cycle time	CL = 3	^tCK	7.5		8		10		ns	22
	CL = 2	^tCK	10		10		15		ns	22
CKE hold time		^tCKH	0.8		1		1		ns	
CKE setup time		^tCKS	1.5		2		2		ns	
CS#, RAS#, CAS#, WE#, DQM hold time		^tCMH	0.8		1		1		ns	
CS#, RAS#, CAS#, WE#, DQM setup time		^tCMS	1.5		2		2		ns	
Data-in hold time		^tDH	0.8		1		1		ns	
Data-in setup time		^tDS	1.5		2		2		ns	
Data-out high-impedance time	CL=3	^tHZ		5.4		5.4		6	ns	10
	CL = 2	^tHZ		5.4		6		6	ns	10
Data-out low-impedance time		^tLZ	1		1		2		ns	
Data-out hold time (load)		^tOH	3		3		3		ns	
Data-out hold time (no load)		^tOH_N	1.8		1.8		n/a		ns	28
ACTIVE to PRECHARGE command period		^tRAS	44	120,000	50	120,000	60	120,000	ns	32
ACTIVEto ACTIVE command period		^tRC	66		70		90		ns	
AUTO REFRESH period		^tRCAR	66		70		90		ns	
ACTIVE to READ or WRITE delay		^tRCD	20		20		30		ns	
Refresh period (8,192 cycles)		^tREF		64		64		64	ms	
PRECHARGE command period		^tRP	20		20		30		ns	
ACTIVE bank A to ACTIVE bank B command period		^tRRD	15		20		20		ns	
Transition time		^tT	0.3		1		1	1.2	ns	7
WRITE recovery time		^tWR	1 CLK + 7ns		1 CLK + 7ns		1 CLK + 7ns		–	23
			15		15		15		ns	24
Exit SELF REFRESH to ACTIVE command		^tXSR	75		90		90		ns	20

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Table 19: AC Functional Characteristics

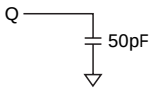
Notes: 5, 6, 8, 9, 11, 31; notes appear on page 18

PARAMETER		SYMBOL	-75	-8	-10	UNITS	NOTES
READ/WRITE command to READ/WRITE command		^tCCD	1	1	1	^tCK	17
CKE to clock disable or power-down entry mode		^tCKED	1	1	1	^tCK	14
CKE to clock enable or power-down exit setup mode		^tPED	1	1	1	^tCK	14
DQM to input data delay		^tDQD	0	0	0	^tCK	17
DQM to data mask during WRITEs		^tDQM	0	0	0	^tCK	17
DQM to data high-impedance during READs		^tDQZ	2	2	2	^tCK	17
WRITE command to input data delay		^tDWD	0	0	0	^tCK	17
Data-in to ACTIVATE command		^tDAL	5	4	4	^tCK	15, 21
Data-in to precharge		^tDPL	2	2	2	^tCK	16, 21
Last data-in to BURST STOP command		^tBDL	1	1	1	^tCK	17
Last data-in to new READ/WRITE command		^tCDL	1	1	1	^tCK	17
Lastdata-intoPRECHARGEcommand		^tRDL	2	2	2	^tCK	16, 21
LOAD MODE REGISTER command to ACTIVE or REFRESH command		^tMRD	2	2	2	^tCK	25
Data-out to high-impedance from PRECHARGE command	CL = 3	^tROH	3	3	3	^tCK	17
	CL = 2	^tROH	2	2	2	^tCK	17

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Notes

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. $V_{DD} = V_{DD}Q = +3.3V$; f = 1 MHz, $T_A = 25°C$; pin under test biased at 1.4V..
3. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is ensured.
6. An initial pause of 100µs is required after power-up, followed by two Auto Refresh commands, before proper device operation is ensured. The two Auto Refresh command wake-ups should be repeated any time the tREF refresh requirement is exceeded.
7. AC characteristics assume ^tT = 1ns.
8. In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
9. Outputs measured at 1.5V with equivalent load:



10. ^tHZ defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}. The last valid data element will meet ^tOH before going High-Z.
11. AC timing and I_{DD} tests have V_{IL} = 0V and V_{IH} = 3V, with timing referenced to 1.5V crossover point. If the input transition time is longer than 1ns, then the timing is referenced at V_{IL} (MAX) and V_{IH} (MIN) and no longer at the 1.5V crossover point.
12. Other input signals are allowed to transition no more than once every two clocks and are otherwise at valid V_{IH} or V_{IL} levels.
13. I_{DD} specifications are tested after the device is properly initialized.
14. Timing actually specified by ^tCKS; clock(s) specified as a reference only at minimum cycle rate.
15. Timing actually specified by ^tWR plus ^tRP; clock(s) specified as a reference only at minimum cycle rate.
16. Timing actually specified by ^tWR.
17. Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.
18. The I_{DD} current will decrease or decrease in a proportional amount by the amount the frequency is altered for th etest condition.
19. Address transitions average one transition every two clocks.
20. CLK must be toggled a minimum of two times during this period.
21. Based on ^tCK = 133 MHz for -75, ^tCK = 125 MHz for -8, and ^tCK = 100 MHz for -10.
22. V_{IH} overshoot: V_{IH} (MAX) = V_{DD} + 2V for a pulse width ≤ 3ns, and the pulse width cannot be greater than one third of the cycle rate. V_{IL} undershoot: V_{IL} (MIN) = -2V for a pulse width ≤ 3ns, and the pulse width cannot be greater than one third of the cycle rate.
23. The clock frequency must remain constant (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) during access or precharge states (READ, WRITE, including ^tWR, and PRECHARGE commands). CKE may be used to reduce the data rate.
24. Auto precharge mode only. The precharge timing budget (^tRP) begins 7ns after the first clock delay, after the last WRITE is executed.
25. Precharge mode only.
26. JEDEC specifies three clocks.
27. ^tAC for -75 at CL = 3 with no load is 4.6ns and is guaranteed by design.
28. Parameter guaranteed by design.
29. ^tCK = 7.5ns for -75, ^tCK = 8ns for -8, and ^tCK = 15ns for -10.
30. CKE is HIGH during refresh command period ^tRFC(MIN), else CKE is LOW. The I_{DD6} limit is actually a nominal value and does not result in a fail value.
31. Refer to device data sheet for timing waveforms.
32. The value of ^tRAS used in -13E speed grade modules is calculated from $^tRC - ^tRP$.
33. Leakage number reflects the worst-case leakage possible through the module pin, not what each memory device contributes.

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SPD Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (as shown in Figure 7, Data Validity, and Figure 8, Definition of Start and Stop).

SPD Start Condition

All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

SPD Stop Condition

All communications are terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the SPD device into standby power mode.

SPD Acknowledge

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data (as shown in Figure 9, Acknowledge Response from Receiver).

The SPD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the SPD device will respond with an acknowledge after the receipt of each subsequent eight-bit word. In the read mode the SPD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

Figure 7: Data Validity

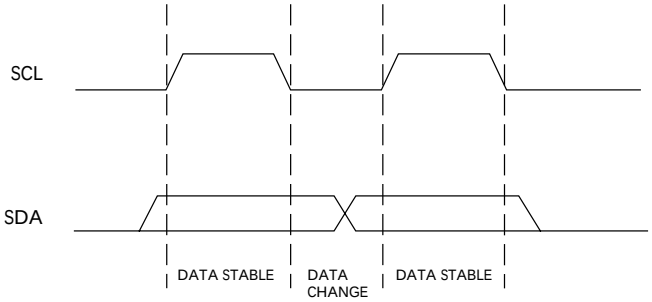


Figure 8: Definition of Start and Stop

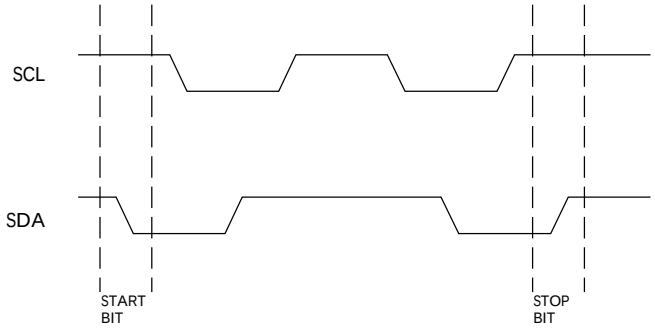
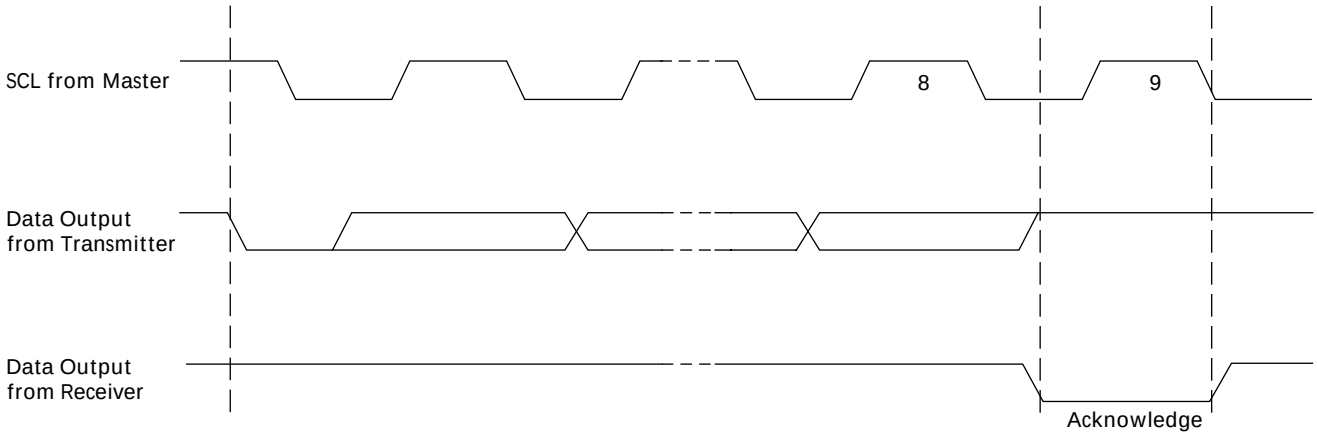


Figure 9: Acknowledge Response from Receiver



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Table 20: EEPROM Device Select Code

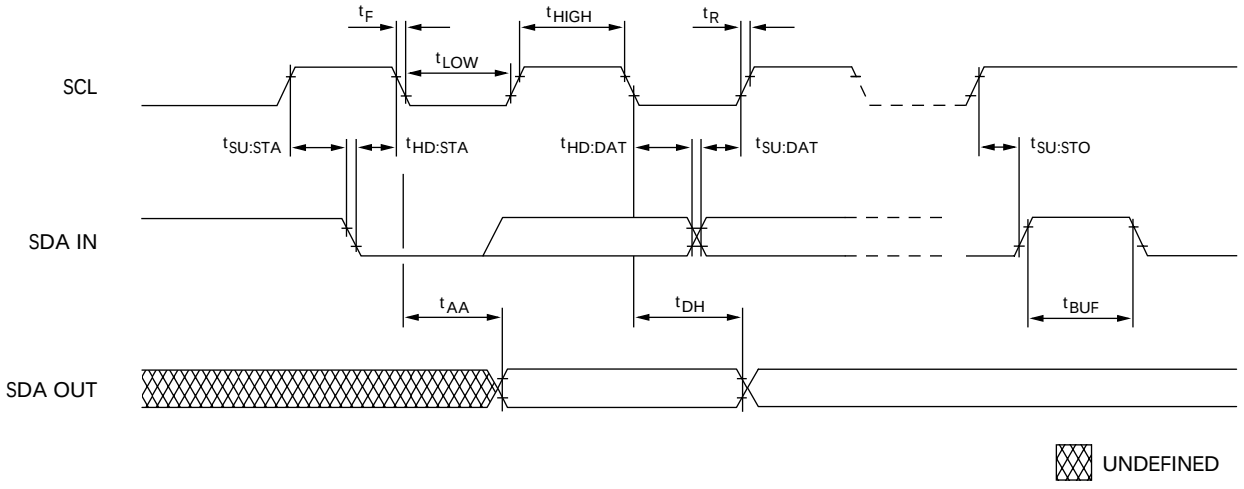
Most significant bit (b7) is sent first

SELECT CODE	DEVICE TYPE IDENTIFIER				CHIP ENABLE			RW
	b7	b6	b5	b4	b3	b2	b1	b0
Memory Area Select Code (two arrays)	1	0	1	0	SA2	SA1	SA0	RW
Protection Register Select Code	0	1	1	0	SA2	SA1	SA0	RW

Table 21: EEPROM Operating Modes

MODE	RW BIT	WC	BYTES	INITIAL SEQUENCE
Current Address Read	1	VIH or VIL	1	Start, Device Select, RW = 1
RandomAddressRead	0	VIH or VIL	1	Start, Device Select, RW= 0, Address
	1	VIH or VIL		RESTART, Device Select, RW= 1
Sequential Read	1	VIH or VIL	≥ 1	Similar to Current or Random Address Read
Byte Write	0	VIL	1	START, Device Select, RW = 0
Page Write	0	VIL	≤ 16	START, Device Select, RW = 0

Figure 10: SPD EEPROM



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Table 22: Serial Presence-Detect EEPROM DC Operating Conditions

All voltages referenced to V_{SS}; V_{DDSPD} = +2.3V to +3.6V

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS
SUPPLY VOLTAGE	V_{DD}	3	3.6	V
INPUT HIGH VOLTAGE: Logic 1; All inputs	V_{IH}	V_{DD} x 0.7	V_{DD} + 0.5	V
INPUT LOW VOLTAGE: Logic 0; All inputs	V_{IL}	-1	V_{DD} x 0.3	V
OUTPUT LOW VOLTAGE: I_{OUT} = 3mA	V_{OL}	–	0.4	V
INPUT LEAKAGE CURRENT: V_{IN} = GND to V_{DD}	I_{LI}	–	10	µA
OUTPUT LEAKAGE CURRENT: V_{OUT} = GND to V_{DD}	I_{LO}	–	10	µA
STANDBY CURRENT: SCL = SDA = V_{DD} - 0.3V; All other inputs = V_{SS} or V_{DD}	I_{SB}	–	30	µA
POWER SUPPLY CURRENT: SCL clock frequency = 100 KHz	I_{DD}	–	2	mA

Table 23: Serial Presence-Detect EEPROM AC Operating Conditions

All voltages referenced to V_{SS}; V_{DDSPD} = +2.3V to +3.6V

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SCL LOW to SDA data-out valid	^{t}AA	0.2	0.9	µs	1
Time the bus must be free before a new transition can start	^{t}BUF	1.3		µs	
Data-out hold time	^{t}DH	200		ns	
SDA and SCL fall time	^{t}F		300	ns	2
Data-in hold time	$^{t}HD:DAT$	0		µs	
Start condition hold time	$^{t}HD:STA$	0.6		µs	
Clock HIGH period	$^{t}HIGH$	0.6		µs	
Noise suppression time constant at SCL, SDA inputs	^{t}I		50	ns	
Clock LOW period	^{t}LOW	1.3		µs	
SDA and SCL rise time	^{t}R		0.3	µs	2
SCL clock frequency	^{f}SCL		400	KHz	
Data-in setup time	$^{t}SU:DAT$	100		ns	
Start condition setup time	$^{t}SU:STA$	0.6		µs	3
Stop condition setup time	$^{t}SU:STO$	0.6		µs	
WRITE cycle time	^{t}WRC		10	ms	4

NOTE:

1. To avoid spurious START and STOP conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a reSTART condition, or following a WRITE cycle.
4. The SPD EEPROM WRITE cycle time (^{t}WRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.

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Table 24: Serial Presence-Detect Matrix – 16MB, 32MB

"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"

BYTE	DESCRIPTION	ENTRY (VERSION)	MT2LSDT432U	MT4LSDT832UD
0	Number of Bytes Used by Micron	128	80	80
1	Total Number of SPD Memory Bytes	256	08	08
2	Memory Type	SDRAM	04	04
3	Number of Row Addresses	12	0C	0C
4	Number of Column Addresses	8	08	08
5	Number of Module Ranks	1 or 2	01	02
6	Module Data Width	32	20	20
7	Module Data Width (continued)	0	00	00
8	Module Voltage Interface Levels	LVTTL	01	01
9	SDRAM Cycle Time, ^{t}CK (CAS Latency = 3)	7.5ns (-75) 8ns (-8) 10ns (-10)	75 80 A0	75 80 A0
10	SDRAM Access From Clock, ^{t}AC (CAS Latency = 3)	5.4ns (-75) 6ns (-8) 7.5ns (-10)	54 60 75	54 60 75
11	Module Configuration Type	None	00	00
12	Refresh Rate/Type	15.625µs/Self	80	80
13	SDRAM Width (Primary SDRAM)	8	10	10
14	Error-Checking SDRAM Data Width	0	00	00
15	Minimum Clock Delay, ^{t}CCD	1 ^{t}CK	01	01
16	Burst Lengths Supported	1, 2, 4, 8, Page	8F	8F
17	Number of Banks on SDRAM Device	4	04	04
18	CAS Latencies Supported	2, 3	06	06
19	CS Latency	0	01	01
20	WE Latency	0	01	01
21	SDRAM Module Attributes	Unbuffered	00	00
22	SDRAM Device Attributes: General	Attributes	0E	0E
23	SDRAM Cycle Time, ^{t}CK (CAS Latency = 2)	10ns (-75/-8) 15ns (-10)	A0 F0	A0 F0
24	SDRAM Access From Clock, ^{t}AC, (CAS Latency = 2)	6ns (-75/-8) 9ns (-10)	60 90	60 90
25	SDRAM Cycle Time, ^{t}CK (CAS Latency = 1)	Not Supported	00	00
26	SDRAM Access From Clock, ^{t}AC, (CAS Latency = 1)	Not Supported	00	00
27	Minimum Row Precharge Time, ^{t}RP	20ns (-75/-8) 30ns (-10)	14 1E	14 1E
28	Minimum Row Active to Row Active, ^{t}RRD	15ns (-75) 20ns (-8/-10)	0F 14	0F 14
29	Minimum RAS# to CAS# Delay, ^{t}RCD	20ns (-75/-8) 30ns (-10)	14 1E	14 1E
30	Minimum RAS# Pulse Width, ^{t}RAS	44ns (-75) 50ns (-8) 60ns (-10)	2C 32 3C	2C 32 3C
31	Module Rank Density	16MB	04	04
32	Command Address Setup, ^{t}AS	1.5ns (-75) 2ns (-8/-10)	15 20	15 20
33	Command Address Hold, ^{t}AH	0.8ns (-75) 1ns (-8/-10)	08 10	08 10

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Table 24: Serial Presence-Detect Matrix – 16MB, 32MB (Continued)

"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"

BYTE	DESCRIPTION	ENTRY (VERSION)	MT2LSDT432U	MT4LSDT832UD
34	Data Signal Input Setup, ^{t}DS	1.5ns (-75) 2ns (-8/-10)	15 20	15 20
35	Data Signal Input Hold, ^{t}DH	0.8ns (-75) 1ns (-8/-10)	08 10	08 10
36-40	Reserved Bytes	–	00	00
41	Device Minimum Active/Auto-Refresh Time, ^{t}RC	66ns (-75) 71ns (-8) 66ns (-10)	42 46 5A	42 46 5A
42–61	Reserved Bytes	–	00	00
62	SPD Revision	REV. 2.0	02	02
63	Checksum for Bytes 0-62	(-75) (-8) (-10)	A5 F6 DD	A6 F7 DE
64	Manufacturer's JEDEC ID Code	MICRON	2C	2C
65-71	Manufacturer's JEDEC Code (Cont.)		FF	FF
72	Manufacturing Location	1-12	01-0C	01-0C
73-90	Module Part Number (ASCII)		Variable Data	Variable Data
91	PCB Identification Code	1-9	01-09	01-09
92	Identification Code (Continuted)	0	00	00
93	Year of Manufacture in BCD		Variable Data	Variable Data
94	Week of Manufacture in BCD		Variable Data	Variable Data
95-98	Module Serial Number		Variable Data	Variable Data
99-127	Manufacturer-Specific Data (RSVD)		–	–

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Table 25: Serial Presence-Detect Matrix – 64MB, 128MB

"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"

BYTE	DESCRIPTION	ENTRY (VERSION)	MT4LSDT1632UD	MT4LSDT3232UD
0	Number of Bytes Used by Micron	128	80	80
1	Total Number of SPD Memory Bytes	256	08	08
2	Memory Type	SDRAM	04	04
3	Number of Row Addresses	12 or 13	0C	0D
4	Number of Column Addresses	9	09	09
5	Number of Module Ranks	2	02	02
6	Module Data Width	32	20	20
7	Module Data Width (continued)	0	00	00
8	Module Voltage Interface Levels	LVTTL	01	01
9	SDRAM Cycle Time, ^{t}CK (CAS Latency = 3)	7.5ns(-75) 8ns (-8) 10ns(-10)	75 80 A0	75 80 A0
10	SDRAM Access From Clock, ^{t}AC (CAS Latency = 3)	5.4(-75) 6ns (-8) 7.5ns (-10)	54 60 75	54 60 75
11	Module Configuration Type	None	00	00
12	Refresh Rate/Type	15.625µs, 7.81µs/ Self	80	82
13	SDRAM Width (Primary SDRAM)	8	10	10
14	Error-Checking SDRAM Data Width	0	00	00
15	Minimum Clock Delay, ^{t}CCD	1 ^{t}CK	01	01
16	Burst Lengths Supported	1, 2, 4, 8, Page	8F	8F
17	Number of Banks on SDRAM Device	4	04	04
18	CAS Latencies Supported	2, 3	06	06
19	CS Latency	0	01	01
20	WE Latency	0	01	01
21	SDRAM Module Attributes	Unbuffered	00	00
22	SDRAM Device Attributes: General	Attributes	0E	0E
23	SDRAM Cycle Time, ^{t}CK (CAS Latency = 2)	10ns (-75/-8) 15ns (-10)	A0 F0	A0 F0
24	SDRAM Access From Clock, ^{t}AC, (CAS Latency = 2)	6ns (-75/-8) 9ns (-10)	60 90	60 90
25	SDRAM Cycle Time, ^{t}CK (CAS Latency = 1)	Not Supported	00	00
26	SDRAM Access From Clock, ^{t}AC, (CAS Latency = 1)	Not Supported	00	00
27	Minimum Row Precharge Time, ^{t}RP	20ns (-75/-8) 30ns (-10)	14 1E	14 1E
28	Minimum Row Active to Row Active, ^{t}RRD	15ns (-75) 20ns (-10/-8)	0F 14	0F 14
29	Minimum RAS# to CAS# Delay, ^{t}RCD	20ns (-75/-8) 30ns (-10)	14 1E	14 1E
30	Minimum RAS# Pulse Width, ^{t}RAS	44ns (-75) 50ns (-8) 60ns (-10)	2C 32 3C	2C 32 3C
31	Module Rank Density	32MB or 64MB	08	10
32	Command Address Setup, ^{t}AS	1.5ns (-75) 2ns (-8/-10)	15 20	15 20
33	Command Address Hold, ^{t}AH	0.8ns (-75) 1ns (-8/-10)	08 10	08 10

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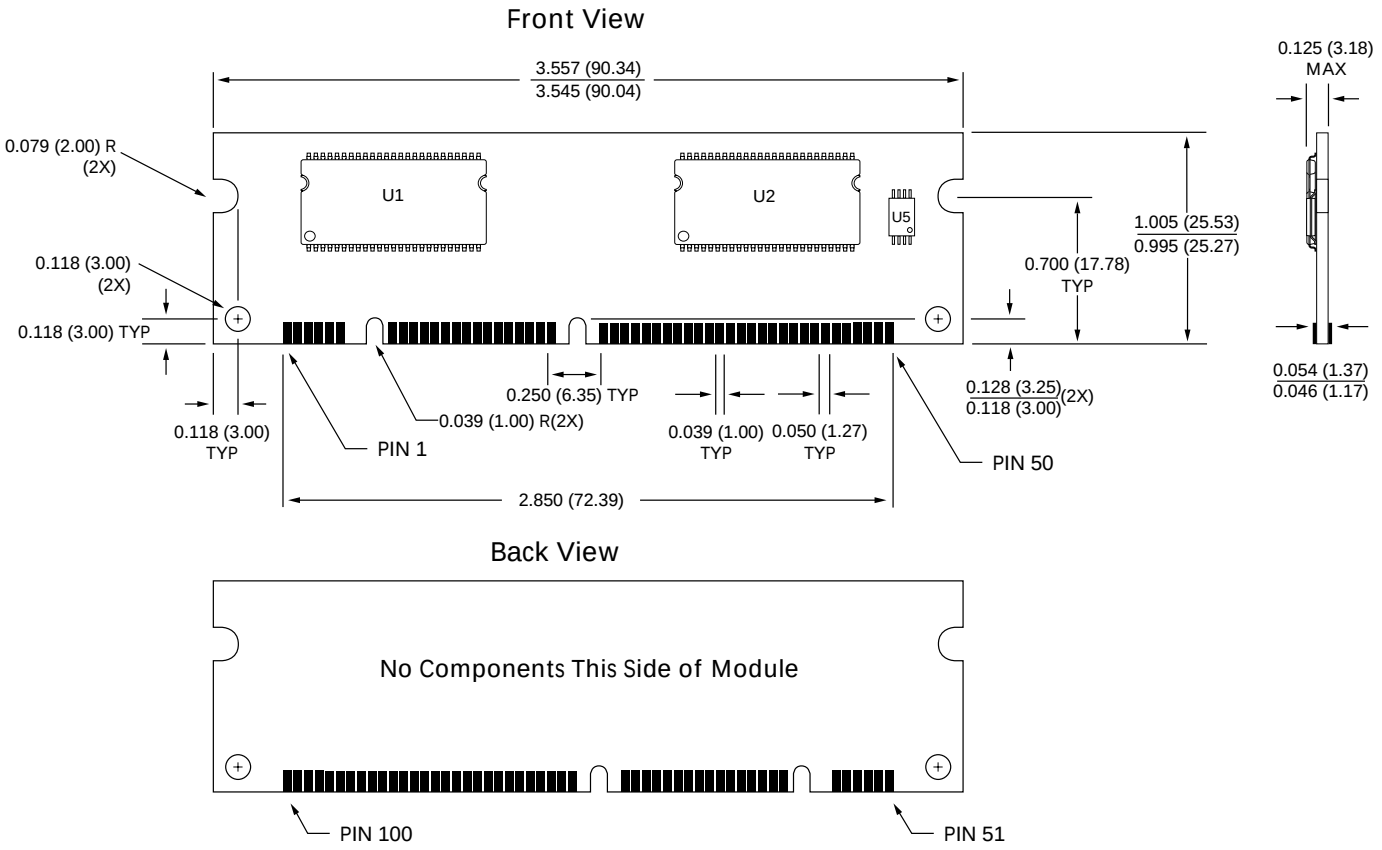
Table 25: Serial Presence-Detect Matrix – 64MB, 128MB (Continued)

"1"/"0": Serial Data, "driven to HIGH"/"driven to LOW"

BYTE	DESCRIPTION	ENTRY (VERSION)	MT4LSDT1632UD	MT4LSDT3232UD
34	Data Signal Input Setup, ^{t}DS	1.5ns (-75) 2ns (-8/-10)	15 20	15 20
35	Data Signal Input Hold, ^{t}DH	0.8ns (-75) 1ns (-8/-10)	08 10	08 10
36-40	Reserved Bytes	–	00	00
41	Device Minimum Active/Auto-Refresh Time, ^{t}RC	66ns (-75) 71ns (-8) 66ns (-10)	42 46 5A	42 46 5A
42–61	Reserved Bytes	–	00	00
62	SPD Revision	REV. 2 or 2	02	02
63	Checksum For Bytes 0-62	(-75) (-8) (-10)	AB FC E3	B6 02 EE
64	Manufacturer's JEDEC ID Code	MICRON	2C	2C
65-71	Manufacturer's JEDEC Code (Cont.)		FF	FF
72	Manufacturing Location	1-12	01-0C	01-0C
73-90	Module Part Number (ASCII)		Variable Data	Variable Data
91	PCB Identification Code	1-9	01-09	01-09
92	Identification Code (Continuted)	0	00	00
93	Year of Manufacture in BCD		Variable Data	Variable Data
94	Week of Manufacture in BCD		Variable Data	Variable Data
95-98	Module Serial Number		Variable Data	Variable Data
99-127	Manufacturer-Specific Data (Rsvd)		–	–

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Figure 11: 100-Pin DIMM Dimensions – 16MB

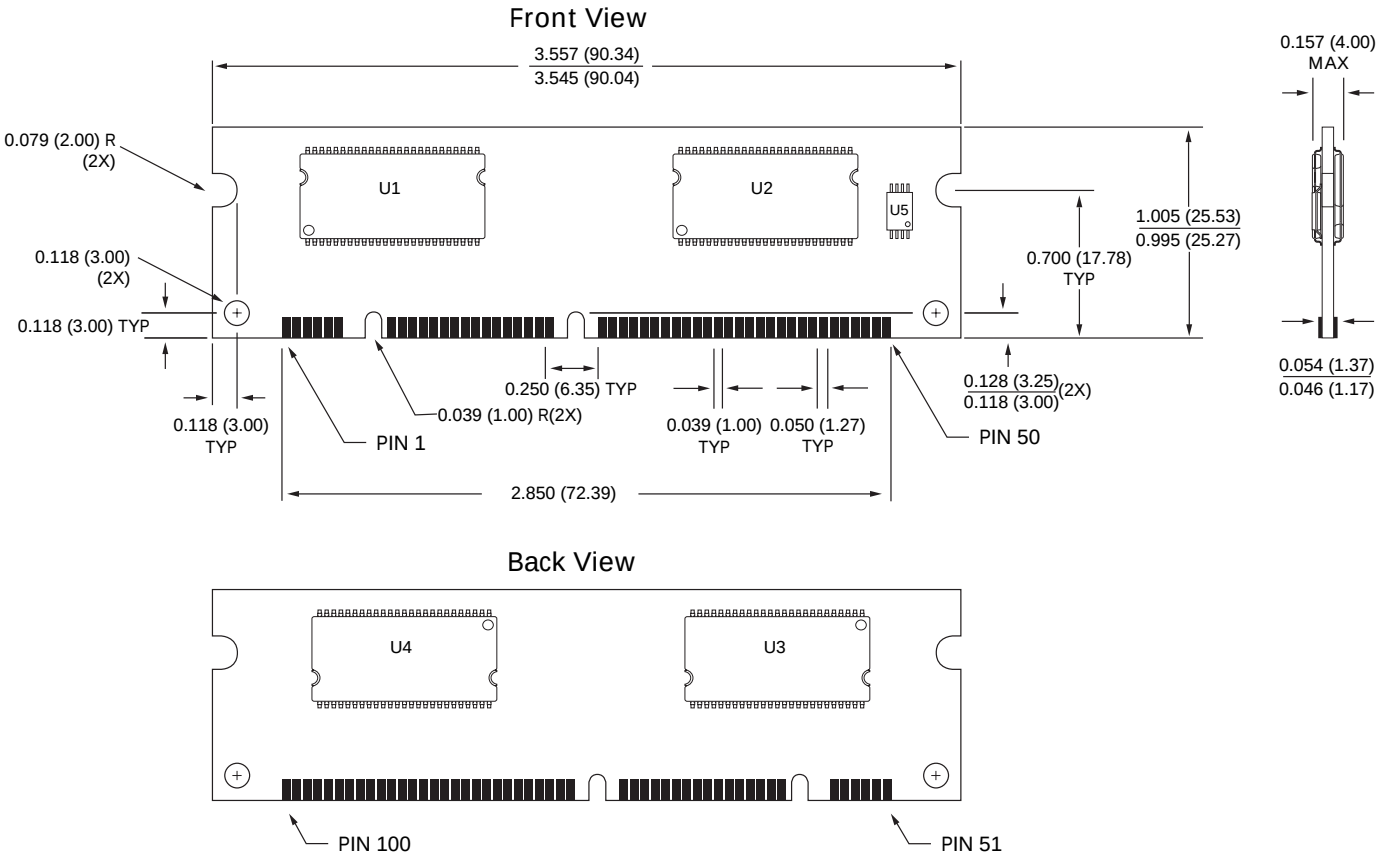


NOTE:

All dimensions in inches (millimeters); $\frac{MAX}{MIN}$ or typical where noted.

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Figure 12: 100-Pin DIMM Dimensions – 32MB, 64MB, and 128MB



NOTE:

All dimensions in inches (millimeters); MAX/MIN or typical where noted.

Data Sheet Designation

Released (No Mark): This data sheet contains minimum and maximum limits specified over the complete power supply and temperature range for production devices. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.

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