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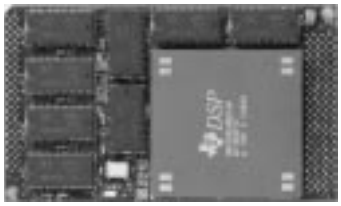
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Find the *Vecima / Spectrum Signal Processing MDC40SS* at our website: *Click HERE*



TIM-DSP1

`C40 SRAM DSP Module

- 50/60 MHz TMS320C40 processor
- 50 MFLOPS, 275 MOPS (or 60 MFLOPS, 330 MOPS) single-width TIM-40 module
- Up to 2 MBytes of 0ws SRAM with a 60 MHz `C40
- Up to 8 MBytes of 0ws SRAM with a 50 MHz `C40
- Six 20 MBytes/s comm ports brought off module
- Global expansion connector for carrier board access
- EEPROM for bootstrapping and operating system identification

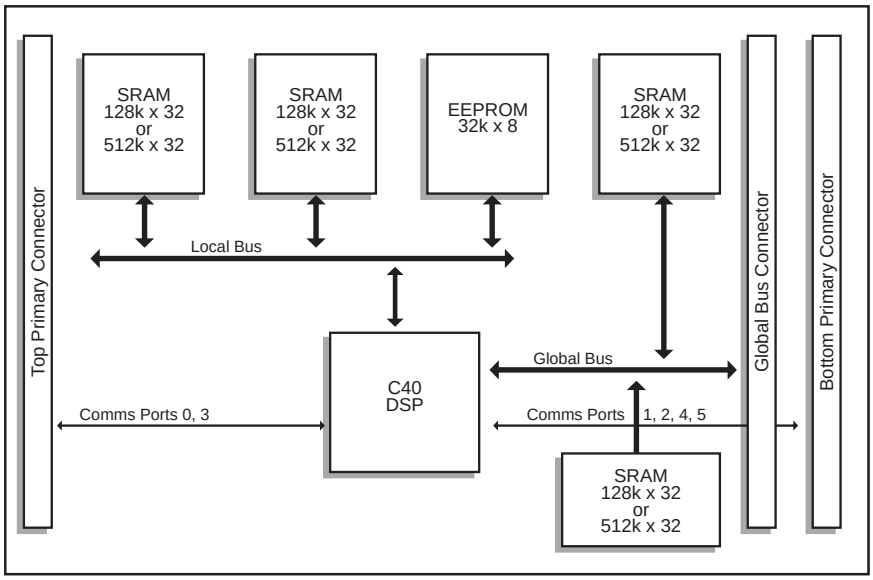
The TIM-DSP1 features a TMS320C40 parallel digital signal processor. It has been designed to comply with the Texas Instruments TIM-40 module standard.

The TIM-DSP1 architecture delivers the full performance and capability of the TMS320C40 in both single processor and multi-processor systems. The `C40's six-channel DMA controller supports true concurrent I/O, independent of and in parallel with the CPU, allowing efficient interprocessor communications and minimizing data-flow bottlenecks.

On module memory consists of up to four separate banks of zero wait-state SRAM, up to two on the local memory port and up to two on the global memory port. The 1.5MB version has one empty global memory bank, and the 4MB version has one empty global memory bank and one empty local bank.

The module incorporates an 80-pin global TIM-40 connector which accepts the `C40's 31 lines of the global address bus as well as the 32-bit global data bus and all the global control signals.

One of the key features of the module is the ability to run independently from a host by booting from the on module 32 kByte EEPROM. The ROM also allows multi-processing operating systems to identify the module and its processing or memory capabilities for dynamic load sharing.



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