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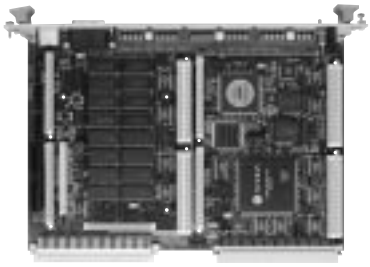
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Find the *Vecima / Spectrum Signal Processing MDC40SS* at our website: *Click HERE*



Maranello

TMS320C4x-Based VME64bus Master B

NEW

- Octal configuration using Twin TIM modules (eight 60 MHz TMS320C44S)
- Up to 480 MFLOPS VME64 Master/Slave DSP board with TIM-40 modules
- Four TIM-40 module sites offer wide range of memory and I/O options
- Shared bus memory architecture (Up to 8MB)
- 10 comm ports available at front panel
- DSP~LINK3 interface for connection to IndustryPack® carriers and modules
- I/O board site for Spectrum's I/O board or custom I/O
- A serial port (full duplex UART)
- Real-time multiprocessor C Source debugging using JTAG
- Comprehensive software support

Maranello offers a complete set of solutions for DSP-based applications on the TMS320C4x processor. The Maranello features four TIM-40 module sites, 10 external communication ports, a JTAG emulation port, application specific ports, a shared memory architecture, a VME64 Master/Slave interface, a UART, and an optimized de-coupled I/O interface.

Scalable and Modular Architecture

Maranello's scalable, modular architecture enables the use of high-performance, industry standard options providing flexibility through different I/O expansion and TIM modules. A range of system building blocks conforming to the TIM-40 industry standard are available including digital radio, DSP acceleration, memory and multi-processor modules. It can be configured with up to eight `C4x DSPs capable of up to 480 MFLOPS of processing power.

Modules can run independently from the host processor by booting from their own 32 kByte PEROM. This also allows multi-processing operating systems to identify each module and its processing and memory capabilities when dynamically determining system configurations.

Memory Architecture

Maranello supports a shared bus architecture which allows the TIM-40 module sites and the VME64 interface to access a bank of on-board global, shared SRAM. The on-board memory options offer a choice of three available configurations to allow for optimum application performance.

Interface Architecture

Maranello incorporates a Master/Slave VME64 interface (SCV64 with an A16/A24/A32 - D64/D32/D16/D08 Master & A24/A32 - D64/D32/D16/D08 Slave interface) with Slot 1 controller capabilities. The shared memory on the board can be accessed by the VME64 interface which operates at up to 60 MByte/s offering a high bandwidth data transfer mechanism. This interface is also connected to the Test Bus Controller to facilitate on-board JTAG emulation and debug.

Input/Output

Inter-processor data transfers are supported by 20 MBytes/s communication ports with up to a maximum of ten available at the front panel.

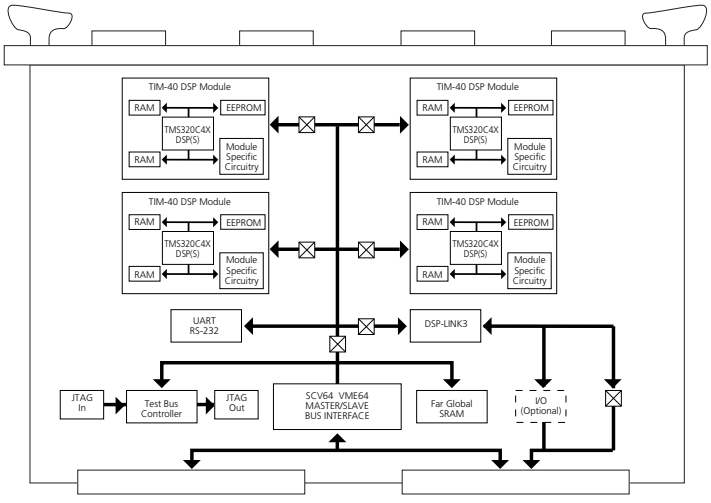
DSP~LINK3 System Expansion Interface

Maranello offers Spectrum's open standard DSP~LINK3, which is a 32-bit, 40 MBytes/s I/O interface with low interrupt latency. All processors have direct access to this I/O expansion interface via an arbitrated shared bus. Spectrum has a complete range of multi-channel analog and digital I/O boards and the full DSP~LINK3 specifications are published. The DSP~LINK3 interface has also been specially designed for optimal performance when used with Spectrum's line of IndustryPack™ I/O products.

Software Development Tools

Spectrum offers an integrated High Level Language Interface Library with Device Drivers for a range of operating systems including Windows NT, Solaris and VxWorks.

A wide range of software tools are available including real-time operating systems and debugger utilities. An on-board JTAG Test Bus Controller (TBC) provides comprehensive debug capability.



`C4x-based carrier boards Do Not include TIM modules

Spectrum Signal Processing Inc.
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