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Find the *Vecima / Spectrum Signal Processing XCM-3321* at our website: ***Click HERE***

SPECTRUM SIGNAL PROCESSING

XMC-3321

Dual Transceiver XMC Module

XMC

Preliminary

flexComm

Benefits

- Rugged design for deployment in harsh environments
- Supports conversion and processing of intermediate frequency (IF) signals including industry standard 10.7, 21.4 and 70 MHz
- Supports multi-channel coherent operation necessary in many Multiple-Input, Multiple-Output (MIMO) and Smart Antenna applications
- Increase communications range and improve payload data throughput with ultra low additive jitter clock circuitry design that is essential to maximize energy per bit/noise spectral density (Eb/No)
- Provides independent data and control signal paths necessary for real-time transceiver operation
- *quic*Comm™ software architecture accelerates application development, simplifies the programming model and ensures code portability
- Dual converter design supports I/Q sampling necessary in Zero IF architectures or operating two independent channels
- Modified COTS - designed for optimization of size, weight, power and cost to meet fielded application or program requirements

Applications

Typical applications include:

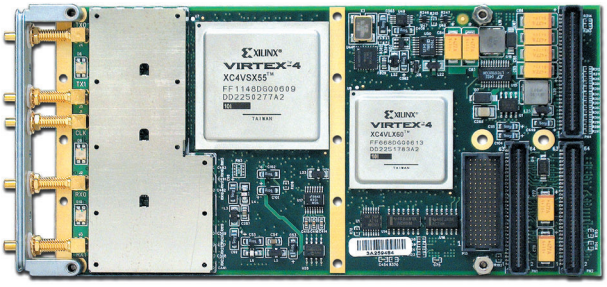
- Tactical Military Communications (MILCOM) - ground vehicular, airborne, unmanned aerial vehicles (UAV) and shipborne
- Electronic Warfare (EW) including Electronic Attack - jamming
- Military Satellite Communications (MILSATCOM) gateways, terminals and hubs

Features

- Available in conduction-cooled and air-cooled versions with (optional) conformal coating. Rugged conduction-cooled PMC module versions follow the industry standard ANSI VITA 20 specification and operate with IEEE 1101.2 compliant XMC carriers.
- IF to digital conversion via two 14-bit A/D converters sampling at 96.0 MSPS (alternate sampling rates 36 to 105 MSPS optional)
- Digital to IF conversion via two 14-bit D/A converters sampling at 192.0 MSPS (alternate sampling rates up to 300 MSPS optional)
- Two 12 bit D/A converters up to 100 KSPS suitable for driving AGC input of an RF front-end
- Four 12 bit A/D converters up to 100 KSPS suitable for reading RSSI output of an RF front-end
- XMC interface (ANSI VITA 42.0) provides high-speed, low latency, deterministic data flow to an industry standard carrier. Compatible with PMC and ePMC (Solano®) carriers.
- User programmable Xilinx® Virtex-4™ FPGA for wideband processing and low power consumption
- PCI 32-bit/33 MHz host bus for control
- High-speed analog inputs are AC coupled, DC coupled input is optional
- JTAG interface compatible with Xilinx's ChipScope™ debugger
- General Purpose I/O (GPIO) lines via PN4 connect the user programmable FPGA to the carrier board
- Internal or external 10 MHz reference oscillator drives on-board sample clock

Description

The XMC-3321 is a key component in Spectrum's series of software defined digital radio modules from the *flex*Comm™ wireless communications product line. The XMC-3321 supports industry standard IF frequencies including 10.7, 21.4 and 70 MHz through the use of dual 14-bit A/D converters sampling at up to 105 MSPS and dual 14-bit D/A converters sampling at up to 300 MSPS in a single-width XMC form factor. The XMC (ANSI VITA 42.0) standard is fully compatible with IEEE P1386.1 PMC standard but offers the additional benefit of dedicated high-speed links between an XMC-compliant carrier and its mezzanine modules. The XMC-3321 is capable of supporting either the Solano Communication Technology or Parallel RapidIO (ANSI VITA 42.1) via the high-speed XMC interface. The module also features a single user programmable Xilinx Virtex-4 FPGA device for wide bandwidth signal processing and filtering in the digital domain.



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Block Diagram

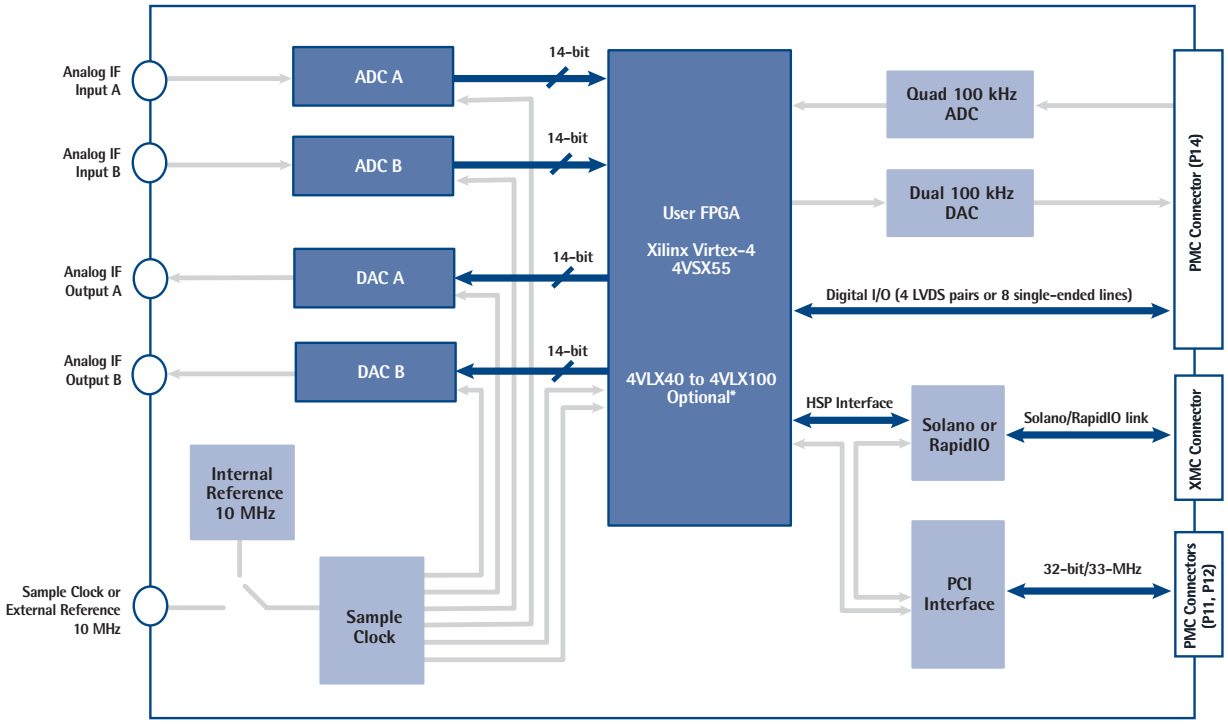


Figure 1. XMC-3321 Block Diagram. *See future options section of this datasheet.

Architecture

[XMC ANSI VITA 42.0 Compliant]

The XMC-3321 is an ANSI VITA 42.0 XMC compliant module which is capable of supporting either Spectrum's high-speed Solano Communications Technology or industry standard ANSI VITA 42.1 Parallel RapidIO. The ANSI VITA 42.0 XMC base standard defines physical features that enable switched communications between a standard mezzanine card and its carrier.

[Solano Communications Technology]

The XMC-3321 supports two Solano Enhanced PMC (ePMC) links via the XMC interface. The Solano Communications Technology used in the ePMC specification provides high bandwidth deterministic data paths between ePMC mezzanine modules and ePMC carriers. Each Solano high-speed link is capable of greater than 200 MB/s full-duplex communications and requires much less power than RapidIO. Two Solano links are electrically equivalent to one RapidIO link.

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[Parallel RapidIO Compatibility*]

The ANSI VITA 42.1 Parallel RapidIO standard uses a point-to-point scalable switched-fabric for its transport layer. Using LVDS signaling with a double-data-rate clocking methodology, data rates of up to 500 MB/s full-duplex are supported. The XMC-3321 supports a single Parallel RapidIO link. RapidIO benefits the designer who requires an industry standard high-speed fabric and interface.

[Xilinx Virtex-4 FPGA]

The Xilinx Virtex-4 FPGA platform is ideally suited for high-performance IF and baseband signal processing tasks inherent in tactical MILCOM applications such as channelization, network synchronization, carrier and baud recovery and resampling. On the XMC-3321, a Xilinx Virtex-4 (LX100, LX60, LX40 or SX55) is available for user programming. Power consumption of the Xilinx Virtex-4 is reduced by up to 50% over comparable Virtex-II Pro™ FPGAs using Xilinx's Triple-Oxide Technology. The Virtex-4 SX55 user programmable FPGA is a standard feature with the XMC-3321.

[A/D Converters and D/A Converters]

The XMC-3321 uses two AD6645 14-bit ADCs, sampling at 96.0 MSPS and supports a range of sampling rates of 36 MSPS up to 105 MSPS. The input includes an AC (transformer) coupled circuit that has a passband of 0.5 MHz to 105 MHz. A DC-coupled analog input, necessary to perform I/Q sampling for Zero IF based systems, is availabe as an option.

The XMC-3321 uses two AD9755 14-bit DACs sampling at 192.0 MSPS and supports sampling rates of up to 210 MSPS. DAC sampling rates of up to 300 MSPS is a future option*.

[Ultra Low Additive Jitter]

The XMC-3321 clock circuitry design incorporates techniques to minimize "additive" jitter (phase noise) which is essential to maximize energy per bit/noise spectral density ratio (Eb/No), improving the overall performance of a digital communications system. Radios designed to maximize Eb/No provide significant benefits to the end-user. These include increasing communications range and improving payload data throughput. The XMC-3321 "additive" jitter is less than 800 femtoseconds (800×10^{-15} seconds) "additive" to the jitter spec of other system components such as an external reference clock.

[Analog Channel Balance]

Engineered to minimize phase and amplitude imbalance between ADC channels - this is a prime characteristic of the XMC-3321 design that is essential to maximize SFDR and image rejection performance for radios that employ I/Q sampling. Phase imbalance, commonly known as "skew" is minimized between the I/Q clocks. Further to this, the XMC-3321 analog design minimizes phase and amplitude imbalance in the analog path across the entire range of the XMC-3321 high-speed ADC sample rates (36 to 105 MSPS).

*See future options section of this datasheet.

[High-speed ADC/DAC Reference Clock Options]

The XMC-3321 high-speed ADC/DAC sampling clock supports input from an industry standard 10 MHz internal or external reference clock. In addition to this, an XMC-3321 optional feature allows input of an external sampling clock which may range from 36 MHz to 210 MHz. The standard product XMC-3321 clocks the DAC at 192.0 MHz, twice the ADC rate of 96.0 MHz. Alternate sampling rates are supported as an optional feature.

[Additional Interfaces]

Four 100 KSPS 12-bit ADCs and two 100 KSPS 12-bit DACs are available to provide control of an RF front-end. For example, an analog signal generated from the RF front-end may be digitized in the ADC for the purpose of received signal strength indication (RSSI) or a DAC may be used to output an AGC signal. These converters can alternatively be used to support other off-board peripherals.

GPIO provides a direct connection to the user FPGA and is interfaced to the PMC PN4 connector. The GPIO lines are organized as 4 differential input/output LVDS pairs or 8 single-ended lines (inputs/outputs). Access to the GPIO is via the backplane or carrier board.

[Built-In Test*]

The XMC-3321 supports built-in-test (BIT) that is executed by the carrier board processor (carrier board must support BIT). Facilities are available for Power-up BIT (PBIT) that automatically initiaties a hardware self-test whenever it is powered on or reset, and provides an indication to the user that the test has passed. In addition to this, user-initiated BIT (IBIT) is available for testing the hardware under the control of a technician.

[Operation in Rugged Environment]

To address tactical military needs for operation in harsh environments, the XMC-3321 is designed to support conduction cooling, extended temperature range, and increased shock and vibration immunity by using industrial grade components, embedded stiffening and thermal mechanical structures. For protection against high levels of humidity and other environmental contaminants, the XMC-3321 can be conformally coated with a protective sealant. Software readable temperature sensors are included to monitor temperature on hot components.

[Modified COTS Optimization]

The XMC-3321 hardware and software architecture is based on Spectrum's Tactical MILCOM reference designs resulting in a quick turn-around to optimize the product to meet the size, weight, power, cost and/or ruggedization characteristics of fielded applications. In addition to this, the XMC-3321 supports independent hard and soft real-time communications fabrics that allows rapid re-spin through the use of custom data-routing techniques. Using our Modified COTS (MCOTS) process, Spectrum works with our customers to provide an MCOTS solution while substantially minimizing the time-to-deployment. For more information on the benefits of Spectrum's MCOTS process, please contact Spectrum Sales.

*See ordering options section of this datasheet.

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Software

[*quic*Comm Software Development Kit (SDK)]

The XMC-3321 software interface is via a *quic*Comm SDK that is available on all supported platforms. *quic*Comm software abstracts the underlying hardware providing users with basic transport level access and control of Spectrum's *flex*Comm products. This significantly accelerates user application development. *quic*Comm is standard across all *flex*Comm products, allowing code portability. This software includes a board support package for control and data handling which allows configuration and control of the data links between processors and mezzanine cards, initiates and manages data transfers, manages interrupt, and is used to load applications onto the user programmable FPGA.

As a part of Spectrum's *quic*Comm package, an FPGA wrapper is provided to abstract all board level interfaces on the Virtex-4 FPGA, including the interfaces to the analog converters, communication fabrics, etc. The wrapper is designed so users can expedite the integration of third party or custom FPGA IP cores into the XMC-3321 module.

Resources available to the user on the SX55 user programmable FPGA are estimated in Figure 2.

Device	4VSX55	Estimated Resources
Logic cells	55,296	45,400
Block RAM (Kbits)	5,760	5,380
DSP Slices	512	512
Digital Clock Management Blocks	8	3

Figure 2. User programmable FPGA attributes and estimated resources available to user

Spectrum provides software examples with the XMC-3321 SDK that illustrate data flow between major devices on the module. The examples provide application developers with a starting point for their own application software. The developer can obtain quick familiarity with data flow details resulting in substantial time savings with their application development.

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[FPGA Cores]

Virtex-4 compatible cores can be used on the XMC-3321. In order to accelerate FPGA development, high-quality cores can be obtained via a variety of means.

Spectrum's Application Engineering Services (AES) organization routinely develops custom IP cores for clients when these are otherwise unavailable. For more information on custom cores, please contact Spectrum Sales.

The Xilinx IP center contains a wide range of free cores including digital upconverters, downconverters, FFTs and filters. The Xilinx AllianceCORE program is a cooperative effort between Xilinx and independent third-party core developers, resulting in a broad selection of industry-standard solutions.

RF Engines Ltd. (www.rfel.com) provides individual IP cores and integrated turn-key designs for digital RF signal processing that are highly optimized in terms of speed, power and size compared to cores available from the major FPGA vendors. These include pipelined FFT, tunable PFT, half-band filters, FIR filters, windowing functions and CORDICS. Spectrum can integrate these off-the-shelf cores into your system. Contact Spectrum Sales for more information.

[FPGA Tool Flow]

Although other tools can be used, the XMC-3321 is designed to support the Xilinx ISE Foundation™ tool flow. ISE is an integrated programmable logic design environment that includes schematic capture, power analysis tools, physical synthesis for FPGAs, advanced Place and Route Algorithms, and COREgenerator, a graphical interactive design entry tool that is used to create high-level modules. Xilinx's System Generator tool can also be used to graphically design and simulate FPGA-based algorithms within the Simulink environment from The MathWorks.

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Services

[Customer Training]

Spectrum's training workshops are designed to get your team up and running in the shortest time possible by using a combination of lectures and at least 60% hands-on experience with your system. Experience thus far has shown this service to be an invaluable tool that generates significant cost savings and reduces risk for Spectrum customers.

The standard SDR-4000 training consists of two days with a Spectrum Applications Engineer working with actual hardware. An additional two day course that covers the SCA Core Framework and SCA BSP is available. Alternatively a four day course is offered covering both SDR-4000 and the SCA components. Training can be done either at Spectrum's headquarters in Burnaby, B.C., Canada or at the customer site. For complete detail, please see the training datasheet

[Custom Application Development]

Spectrum's Application Engineering Services (AES) can assist in the development of your custom application software, including U.S. Department of Defense and ITAR-controlled projects. The scope of these services are tailored to customers' needs, ranging from complete subsystem development to support for SCA operating environment and waveforms. Spectrum's AES team partners with customers' internal application development engineers to augment their development resources. For more information, please see the Application Engineering Services datasheet.

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Specifications

[general]	FPGA Device	Xilinx Virtex-4: XC4VSX55
	External Reference Oscillator	0.75 - 2.5 Vpp drives sampling clock
	Internal Reference Oscillator	10 MHz drives sampling clock
	External Sampling Clock	Supports range of 36 MHz to 210 MHz, 0.75 - 1.8 Vpp
[analog I/O]	A/D Converter	Two Analog Devices AD6645 14-bit @ 96.0 MSPS (alternate sampling rates 36 to 105 MHz are optional)
	ADC Input	AC coupled, full scale 1.29 Vpp into a 50 ohm load @ 70 MHz IF 3 dB input bandwidth: 500 kHz – 105 MHz
	D/A Converter	Two Analog Devices AD9755 14-bit @ 192.0 MSPS (alternate sampling rates up to 300 MSPS are optional)
	DAC Output	AC coupled, max 0.47 Vpp typical into a 50 ohm load @ 70 MHz 3 dB output bandwidth: 500 kHz – 90 MHz
	ADC SFDR	@ 96.0 MSPS, -1 dBFS input; 10.7 MHz IF (10 MHz b/w) > 90 dB SFDR typical; 21.4 MHz IF (10 MHz b/w) > 85 dB SFDR typical; 70.0 MHz IF (30 MHz b/w) > 80 dB SFDR typical
	DAC SFDR	@ 192.0 MSPS, single tone 0 dBFS; 10.7 MHz IF (10 MHz b/w) > 80 dB SFDR typical; 21.4 MHz IF (10 MHz b/w) > 75 dB SFDR typical; 70.0 MHz IF (30 MHz b/w) > 72 dB SFDR typical
	SFDR note:	SFDR measurements may vary from the above based on IF frequency, sampling rates, method of tone generation and other signaling criteria
	Jitter	Less than 800 femtoseconds additive jitter through the analog clock distribution circuitry
	Phase imbalance	Less than 1 degree of phase imbalance (skew) between I/Q A/Ds at 10 MHz b/w, DC coupled
	Coupling	AC – standard, DC – optional
	Low speed A/D Converter	Quad 12-bit @ 100 Ksps
	Low speed D/A Converter	Dual 12-bit @ 100 Ksps
[external interfaces]	Analog Input/Output	SSMC receptacle 50 ohms
	External Reference Oscillator	SSMC receptacle 50 ohms
	PMC Host PCI Bus	32 bit/33 MHz PCI interface following IEEE P1386.1 specification
	JTAG Connection	JTAG connector for Virtex-4 FPGA, Xilinx Chipscope™ debugger compatible
	XMC Interface	Two Spectrum Solano links, each providing greater than 200 MB/s (full-duplex)
	GPIO	4 differential LVDS pairs or 8 single-ended lines are available via the PMC P14 connector
[compatibility]	Supported Carriers	Spectrum PRO-4600 and PRO-3500
	Operating System	Carrier dependent: Wind River® VxWorks® or Green Hills® INTEGRITY®
[development software]	Application Libraries	*quic*Comm Software Development Kit
	FPGA Code Development	ISE Foundation tools from Xilinx and ModelSim PE from Model Technology are required, Synplify Synthesis from Synplicity is recommended
	HDL Coding Language	VHDL
[electrical]	Supply Voltage (DC)	Supply Voltage +5V, 3.3V +5% / -3% (supplied by PMC connector)
	Power estimate	11.5 watts includes FPGA wrappers, receiving and transmitting (2 x DACs and 2 x ADCs) and Solano links. Power estimates do not include User application code
[environmental]	Operating Temperature	Air-cooled: Operating temperature range of 0 to 50° C, forced air @ 600 LFM Industrial conduction-cooled: -40 to +70° C card edge
	Shock and Vibration	Conduction-cooled version tested in accordance with MIL-STD-810F
	Conformal Coating	Optional. Contact Spectrum Sales for details
	RoHS	0 of 6 compliant. For other RoHS options, please contact Spectrum sales
[ordering information]	650-00548	XMC-3321 2-In/2-Out Transceiver – Industrial, Conduction-cooled
	650-00549	XMC-3321 2-In/2-Out Transceiver – Commercial, Air-cooled
	202-00925	XMC-3321 Cable kit
[custom configuration]		For custom configuration, please contact Spectrum Sales
[future options]		Future options may be implemented at the discretion of Spectrum Signal Processing Inc. based on market demand.**
	ANSI VITA 42.1 standard	Parallel RapidIO over XMC
	Alternate User FPGA size	Virtex-4 LX100/LX60/LX40
	Alternate Sampling Rates	High-speed DAC up to 300 MSPS
	Built-In-Test	PBIT, IBIT and power-up, offline and background diagnostics including loop-back tests and libraries for writing custom BIT routines

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