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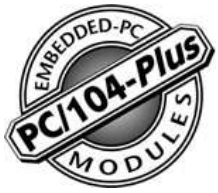
Find the *Versalogic A-EPM35S* at our website: ***Click HERE***

Reference Manual

DOC. REV. 10/17/2013

VL-EPM-35 (Leopard)

Intel Dual Core Based Dual Board Computer with Dual Gigabit Ethernet, SATA, PC/104-*Plus*, Video, Audio, and SPX





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Product Release Notes

Rev 2.00 – Minor changes to improve manufacturability. No customer impact.

Rev 1.00 – Initial commercial release.

Support Page

The **VL-EPM-35 support page**, at **http://www.versalogic.com/private/leopardsupport.asp**, contains additional information and resources for this product including:

- Reference Manual (PDF format)
- Operating system information and software drivers
- Data sheets and manufacturers' links for chips used in this product
- Photograph of the circuit board
- BIOS information and upgrades
- Utility routines and benchmark software

Note: This is a private page for VL-EPM-35 users that can be accessed only be entering this address directly. It cannot be reached from the VersaLogic homepage.

The VersaTech KnowledgeBase is an invaluable resource for resolving technical issues with your VersaLogic product.

VersaTech KnowledgeBase

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1 Introduction

Description

Features and Construction

The VL-EPM-35 is a feature-packed dual board computer (DBC) designed for OEM control projects requiring fast processing and designed-in reliability and longevity (product lifespan). Its features include:

- Intel Core 2 Duo processor, 2.26 GHz, 1066 MHz FSB, 6 MB cache
- Up to 4 GB DDR3 SO-DIMM socket
- USB MiniBlade socket
- Dual 10BaseT / 100BaseTX / 1000BaseT Ethernet interface
- Intel GMA 4500 MHD graphics core
- PC/104-*Plus* (PCI and ISA) expansion
- Two SATA 3 Gb/s ports
- Six USB 2.0 ports
- eUSB SSD site
- PS/2 keyboard and mouse interface
- TVS devices for ESD protection
- Watchdog timer
- Audio stereo line in, stereo line out
- Simultaneous VGA and LVDS outputs
- CPU temperature sensor
- Five serial ports
- V_{CC} sensing reset circuit
- PC/104-compliant footprint
- Field upgradeable BIOS with OEM enhancements
- External HD Audio compatible
- Customizing available
- SPX interface supports up to four (external) SPI devices either of user design or any of the SPX™ series of expansion boards, with clock frequencies from 1-8MHz

The VL-EPM-35 is a PC/104-*Plus*-compliant single board computer with an Intel Core 2 Duo processor. The board is compatible with popular operating systems such as Windows, Windows Embedded, QNX, VxWorks and Linux.

The VL-EPM-35 features high reliability design and construction, including voltage sensing reset circuits and current limiting external power rails.

VL-EPM-35 boards are subjected to 100% functional testing and are backed by a limited two-year warranty. Careful parts sourcing and US-based technical support ensure the highest possible quality, reliability, service and product longevity for this exceptional SBC.

Additional I/O expansion is available through the high-speed PC/104-*Plus* (PCI) and PC/104 (ISA) connectors. The VL-EPM-35 is equipped with two multifunction utility cables, VL-CBR-3406 (breakout board) and VL-CBR-8006, that provide numerous standard I/O interfaces.

Technical Specifications

Specifications are typical at 25°C with 5.0V supply unless otherwise noted.

Board Size:
3.55" x 3.775" (PC/104 standard) with connector overhangs in designated connector areas

Storage Temperature:
-40° C to 85° C

Operating Temperature: *(with Windows XP running with both CPU cores at 1.2GHz/95% utilization with active 2D and 3D video)*
VL-EPM-35S: 0° C to +60° C free air, no airflow
VL-EPM-35E: -40° C to +85° C free air

Power Requirements: *(+5V with 1 GB system DDR3 SO-DIMM, keyboard and mouse, running Windows XP)*
VL-EPM-35S, SR: Idle 2.8A (14W), typical 4.3A (21.3W), max 5.7A (28.5W)
VL-EPM-35E, ER: Idle 2.3A (11.5W), typical 3.1A (15.5W), max 3.9A (19.5W)
+3.3V or ± 12V may be required by some expansion modules

System Reset:
V_{cc} sensing, resets below 4.70V typ.

DRAM:
Up to 4 GB, DDR3 SO-DIMM, 800 MHz PC3-6400 or 1067 MHz PC3-8500

Video Interface:
Intel GMA 4500 MHD graphics core
Analog output for VGA
LVDS output for TFT FPDs
Up to 1280 x 1024 (24 bits)

SATA Interface:
Two SATA 3 Gb/s ports

Flash Interface:
One MiniBlade socket, supports USB only
USB SSD socket (eUSB)

Ethernet Interface:
PCIe based 82574IT supporting autodetect 10BaseT / 100BaseTX / 1000BaseT (top board)
PCI based 82541ER supporting autodetect 10BaseT / 100BaseTX / 1000BaseT (bottom board)

Serial Ports:
Serial Port 1 Interface: RS-232 16C550 compatible, All handshake lines implemented.
Serial Port 2 Interface: RS-232/422/485, 16C550 compatible, 4-wire RS 232 (Only CTS and RTS handshaking). Auto direction control.
Serial Port 3 Interface: RS-232/422/485, 16C550 compatible, 4-wire RS 232 (Only CTS and RTS handshaking). Auto direction control.
Serial Port 4 Interface: RS-232/422/485, 16C550 compatible, 4-wire RS 232 (Only CTS and RTS handshaking). Auto direction control.
Serial Port 5 Interface: RS-232/422/485, 16C550 compatible, 4-wire RS 232 (Only CTS and RTS handshaking).

LPT Interface:
Bi-directional/EPP/ECP compatible

BIOS:
Phoenix Embedded BIOS© with StrongFrame® Technology and OEM enhancements
Field-upgradeable with Flash BIOS Update Utility

Bus Speed:
PC/104-*Plus* (PCI): 33MHz
PC/104 (ISA): 8MHz

Compatibility:
Embedded-PCI (PC/104-*Plus* version 2.3) – full compliance, 3.3V signaling

Weight:
0.306 kg (0.675 lb)

Specifications are subject to change without notice.

VL-EPM-35 Block Diagram

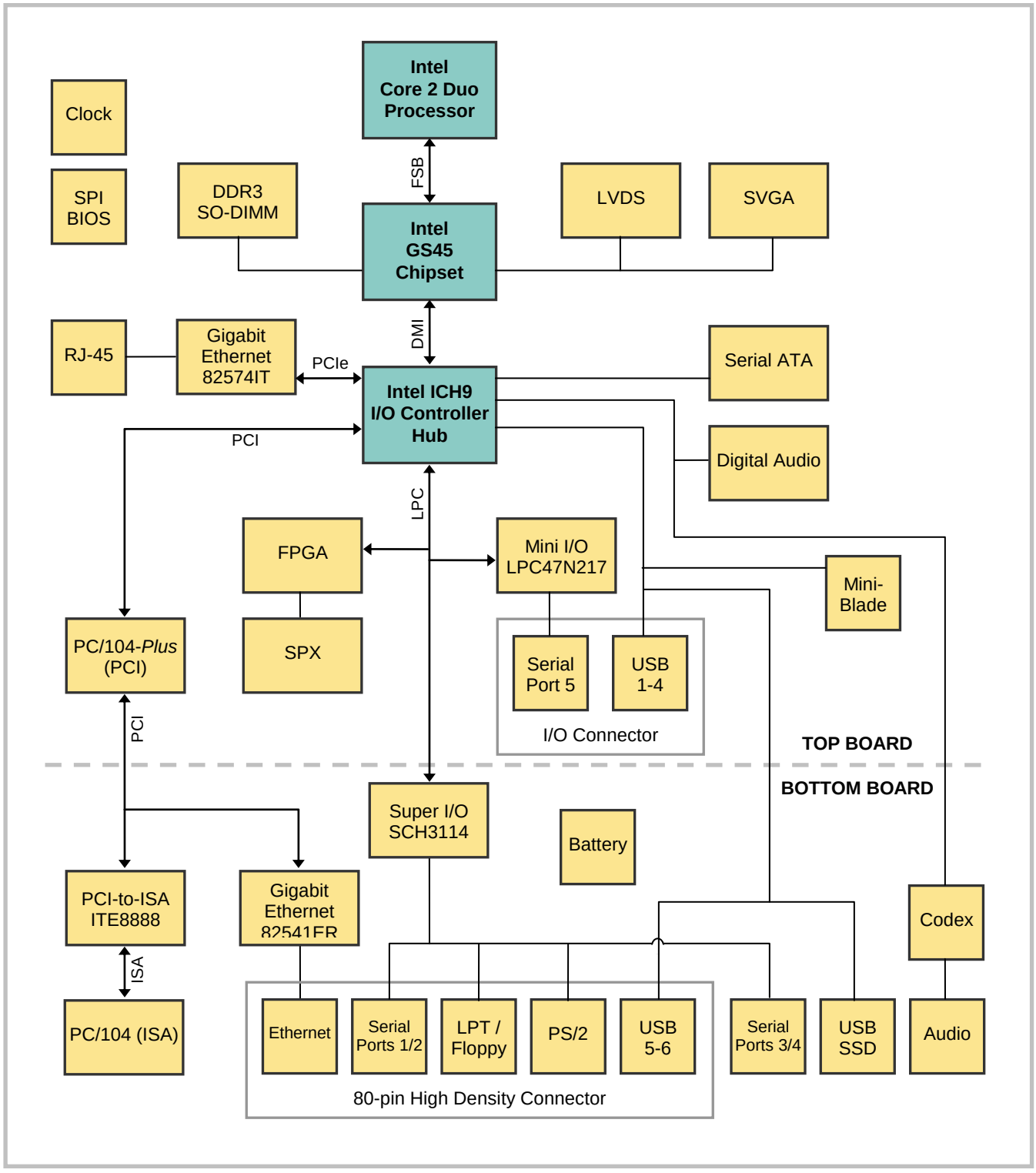


Figure 1. System Block Diagram

Thermal Considerations

CPU Die Temperature

The CPU die temperature is affected by numerous conditions, such as CPU utilization, CPU speed, ambient air temperature, air flow, thermal effects of adjacent circuit boards, external heat sources, and many others.

The CPU is protected from over temperature conditions by several mechanisms.

The CPU will automatically slow down by 50% whenever its die temperature exceeds 105° C. When the temperature falls back below 105° C, the CPU resumes full speed operation.

As a failsafe, if the CPU die temperature climbs above 115° C, the CPU will turn itself off to prevent damage to the chip.

Model Differences

VersaLogic offers both standard and extended temperature models of the VL-EPM-35. The basic operating temperature specification for both models is shown below.

- VL-EPM-35S: 0° C to +60° C free air, no airflow
- VL-EPM-35E: -40° C to +85° C free air

To reliably function at extreme temperatures the extended temperature model specifications deviate from the standard model in the following ways:

- The DRAM interface is slowed. PC3-6400 memory runs at 600 MHz. PC3-8500 memory runs at 800 MHz.
- The DRAM refresh rates are doubled.
- The Front Side Bus speed is reduced to 800 MHz.
- Maximum processor speed is limited to 1200 MHz.
- The graphics core is limited to 400 MHz.

RoHS Compliance

The VL-EPM-35 is RoHS-compliant.

About RoHS

In 2003, the European Union issued Directive 2002/95/EC regarding the Restriction of the use of certain Hazardous Substances (RoHS) in electrical and electronic equipment.

The RoHS directive requires producers of electrical and electronic equipment to reduce to acceptable levels the presence of six environmentally sensitive substances: lead, mercury, cadmium, hexavalent chromium, and the presence of polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) flame retardants, in certain electrical and electronic products sold in the European Union (EU) beginning July 1, 2006.

VersaLogic Corporation is committed to supporting customers with high-quality products and services meeting the European Union's RoHS directive.

Warnings

ELECTROSTATIC DISCHARGE

Warning! Electrostatic discharge (ESD) can damage circuit boards, disk drives and other components. The circuit board must only be handled at an ESD workstation. If an approved station is not available, some measure of protection can be provided by wearing a grounded antistatic wrist strap. Keep all plastic away from the board, and do not slide the board over any surface.

After removing the board from its protective wrapper, place the board on a grounded, static-free surface, component side up. Use an antistatic foam pad if available.

The board should also be protected inside a closed metallic anti-static envelope during shipment or storage.

Note: The exterior coating on some metallic antistatic bags is sufficiently conductive to cause excessive battery drain if the bag comes in contact with the battery.

LITHIUM BATTERY

Warning! To prevent shorting, premature failure or damage to the lithium battery, do not place the board on a conductive surface such as metal, black conductive foam or the outside surface of a metalized ESD protective pouch. The lithium battery may explode if mistreated. Do not recharge, disassemble or dispose of in fire. Dispose of used batteries promptly and in an environmentally suitable manner.

HANDLING CARE

Warning! Care must be taken when handling the board not to touch the exposed circuitry with your fingers. Though it will not damage the circuitry, it is possible that small amounts of oil or perspiration on the skin could have enough conductivity to cause the contents of CMOS RAM to become corrupted through careless handling, resulting in CMOS resetting to factory defaults.

Technical Support

If you are unable to solve a problem after reading this manual please visit the VL-EPM-35 Product Support web page below. The support page provides links to component datasheets, device drivers, and BIOS and FPGA code updates.

VL-EPM-35 Support Page

The VersaTech KnowledgeBase also contains a wealth of technical information about VersaLogic products, along with product advisories. Click the link below to see all KnowledgeBase articles related to the VL-EPM-35.

VersaTech KnowledgeBase

If you have further questions, contact VersaLogic Technical Support at (503) 747-2261. VersaLogic support engineers are also available via e-mail at Support@VersaLogic.com.

REPAIR SERVICE

If your product requires service, you must obtain a Returned Material Authorization (RMA) number by calling (503) 747-2261. Please provide the following information:

- Your name, the name of your company, your phone number, and e-mail address
- The name of a technician or engineer that can be contacted if any questions arise
- Quantity of items being returned
- The model and serial number (barcode) of each item
- A detailed description of the problem
- Steps you have taken to resolve or recreate the problem
- The return shipping address

Warranty Repair All parts and labor charges are covered, including return shipping charges for UPS Ground delivery to United States addresses.

Non-warranty Repair All non-warranty repairs are subject to diagnosis and labor charges, parts charges and return shipping fees. Please specify the shipping method you prefer and provide a purchase order number for invoicing the repair.

Note: Please mark the RMA number clearly on the outside of the box before returning.

Configuration and Setup 2

Initial Configuration

The following components are recommended for a typical development system.

- VL-EPM-35 computer
- 204-pin SO-DIMM (memory module): DDR3-800 or DDR3-1066
- ATX power supply
- SVGA video monitor
- USB keyboard
- USB mouse
- SATA hard drive
- USB CD-ROM drive

The following VersaLogic cables are recommended.

- CBR-1201 – Video adapter cable
- CBR-3406 – Utility I/O cable and breakout board
- CBR-0701 – SATA data cable
- CBR-1008 – Power adapter cable

You will also need a Windows (or other OS) installation CD.

Basic Setup

The following steps outline the procedure for setting up a typical development system. The VL-EPM-35 should be handled at an ESD workstation or while wearing a grounded antistatic wrist strap.

Before you begin, unpack the VL-EPM-35 and accessories. Verify that you received all the items you ordered. Inspect the system visually for any damaged that may have occurred in shipping. Contact Support@VersaLogic.com immediately if any items are damaged or missing.

Gather all the peripheral devices you plan to attach to the VL-EPM-35 and their interface and power cables.

It is recommended that you attach standoffs to the board (see Hardware Assembly) to stabilize the board and make it easier to work with.

Figure 2 shows a typical start-up configuration.

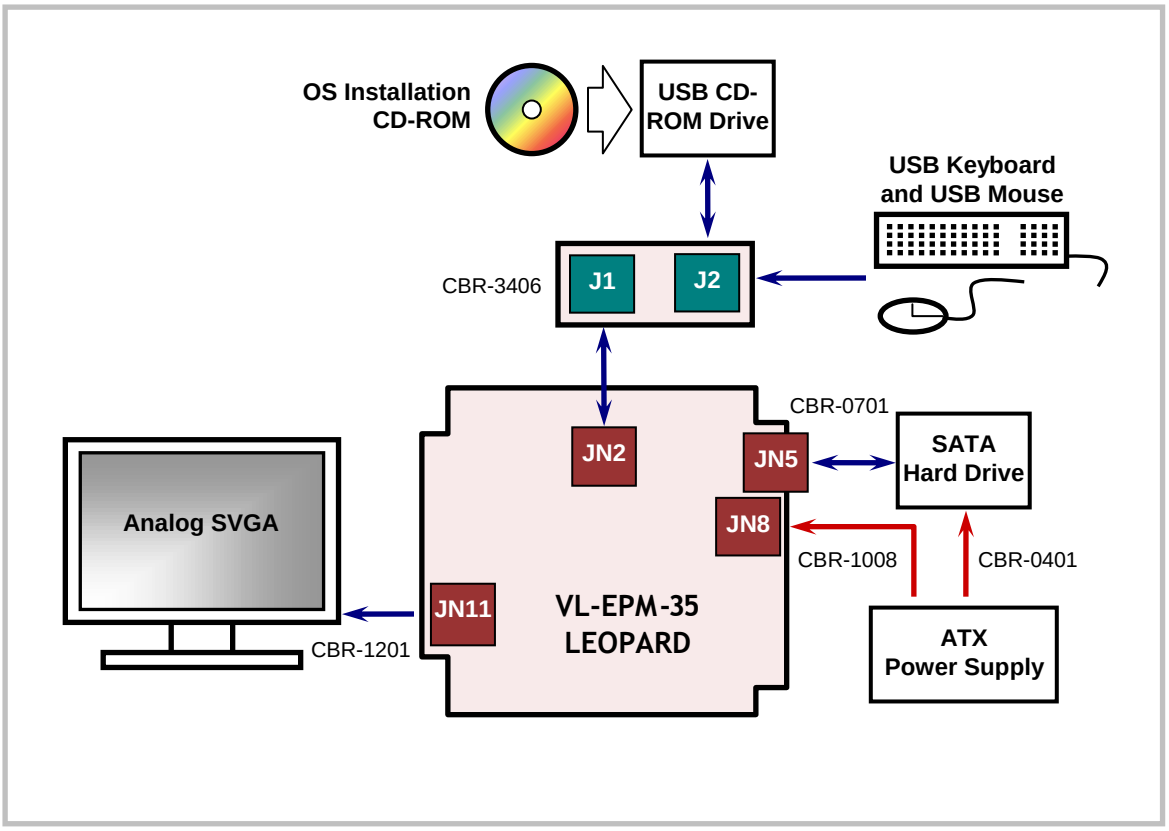


Figure 2. Typical Start-up Configuration

1. Install Memory

- Insert the DRAM module into SO-DIMM socket JN13 on the bottom of the board and latch it into place.

2. Attach Power

- Plug the power adapter cable VL-CBR-1008 into socket JN8. Attach the motherboard connector of the ATX power supply to the adapter.

3. Attach Cables and Peripherals

- Plug the video adapter cable VL-CBR-1201 into socket JN11. Attach the video monitor interface cable to the video adapter.
- Plug the breakout cable VL-CBR-3406 into socket JN2. (The cable and board are shipped attached.)
- Plug a USB keyboard, USB mouse, and USB CD-ROM drive into socket J2 of the breakout board.
- Plug the SATA hard drive data cable VL-CBR-0701 into socket JN5 (top or bottom) and attach a hard drive to the cable.
- Attach an ATX power cable to the SATA hard drive using the VL-CBR-0401 SATA power adapter cable.

4. Review Configuration

- Before you power up the system, double check all the connections. Make sure all cables are oriented correctly and that adequate power will be supplied to the VL-EPM-35 and peripheral devices.

5. Power On

- Turn on the ATX power supply and the video monitor. If the system is correctly configured, a video signal should be present.

6. Install Operating System

- Install the operating system according to the instructions provided by the OS manufacturer. (See Operating System Installation.)

  Note: If you intend to operate the VL-EPM-35 under Windows XP or Windows XP Embedded, be sure to use Service Pack 3 (SP3) for full support of the latest hardware features.

CMOS Setup

See VersaLogic KnowledgeBase article VT1638 – VL-EPM-35 Leopard CMOS Setup Reference for complete information on CMOS Setup parameters and variations for the VL-EPM-35E.

Operating System Installation

The standard PC architecture used on the VL-EPM-35 makes the installation and use of most of the standard x86 processor-based operating systems very simple. The operating systems listed on the VersaLogic OS Compatibility Chart use the standard installation procedures provided by the maker of the OS. Special optimized hardware drivers for a particular operating system, or a link to the drivers, are available at the VL-EPM-35 Product Support web page at **http://www.versalogic.com/private/leopardsupport.asp**.

Dimensions and Mounting

The VL-EPM-35 complies with all PC/104-*Plus* standards. Dimensions are given below to help with pre-production planning and layout.

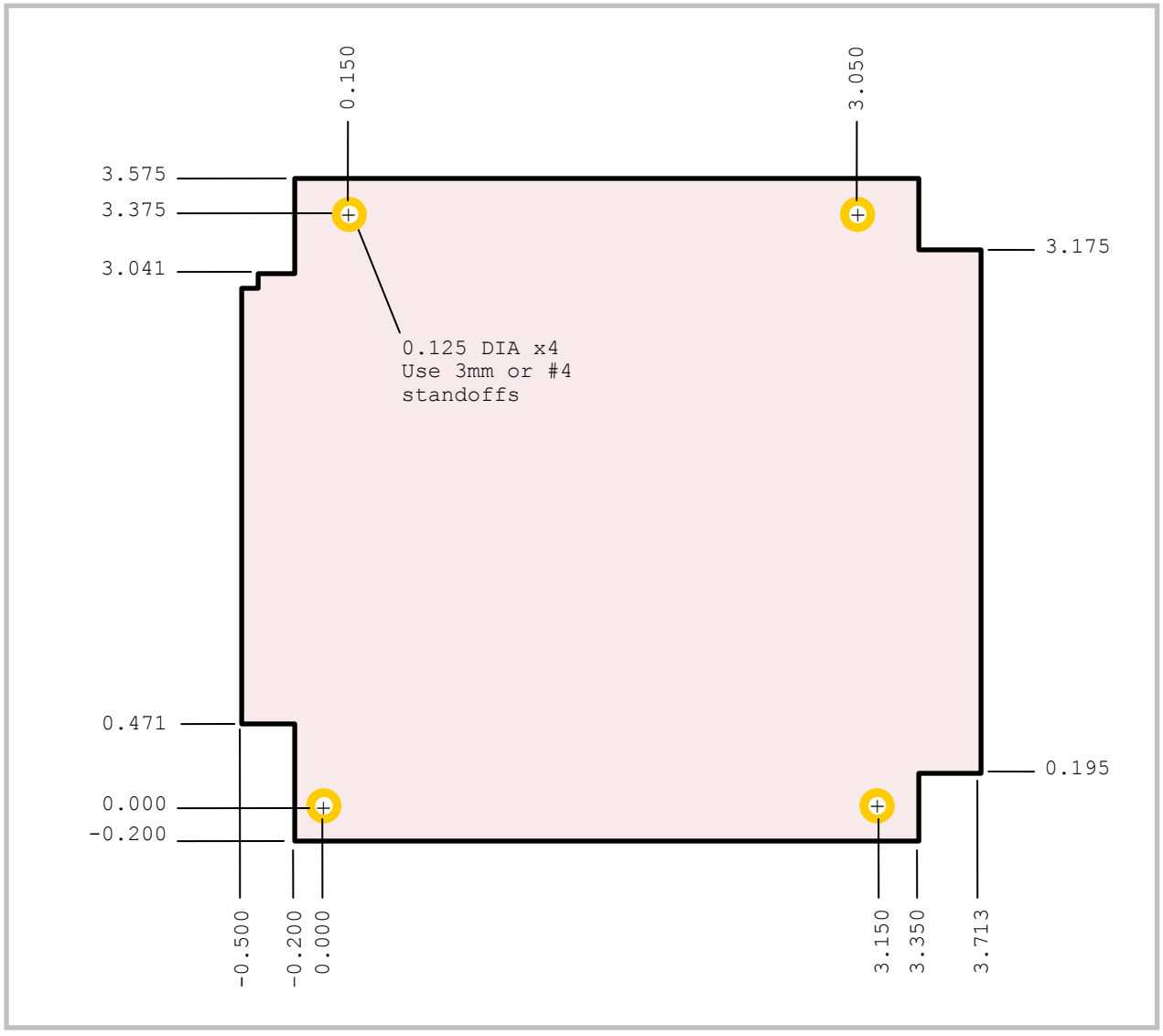


Figure 3. VL-EPM-35 Top Board Dimensions and Mounting Holes (Top View)

(Not to scale. All dimensions in inches.)

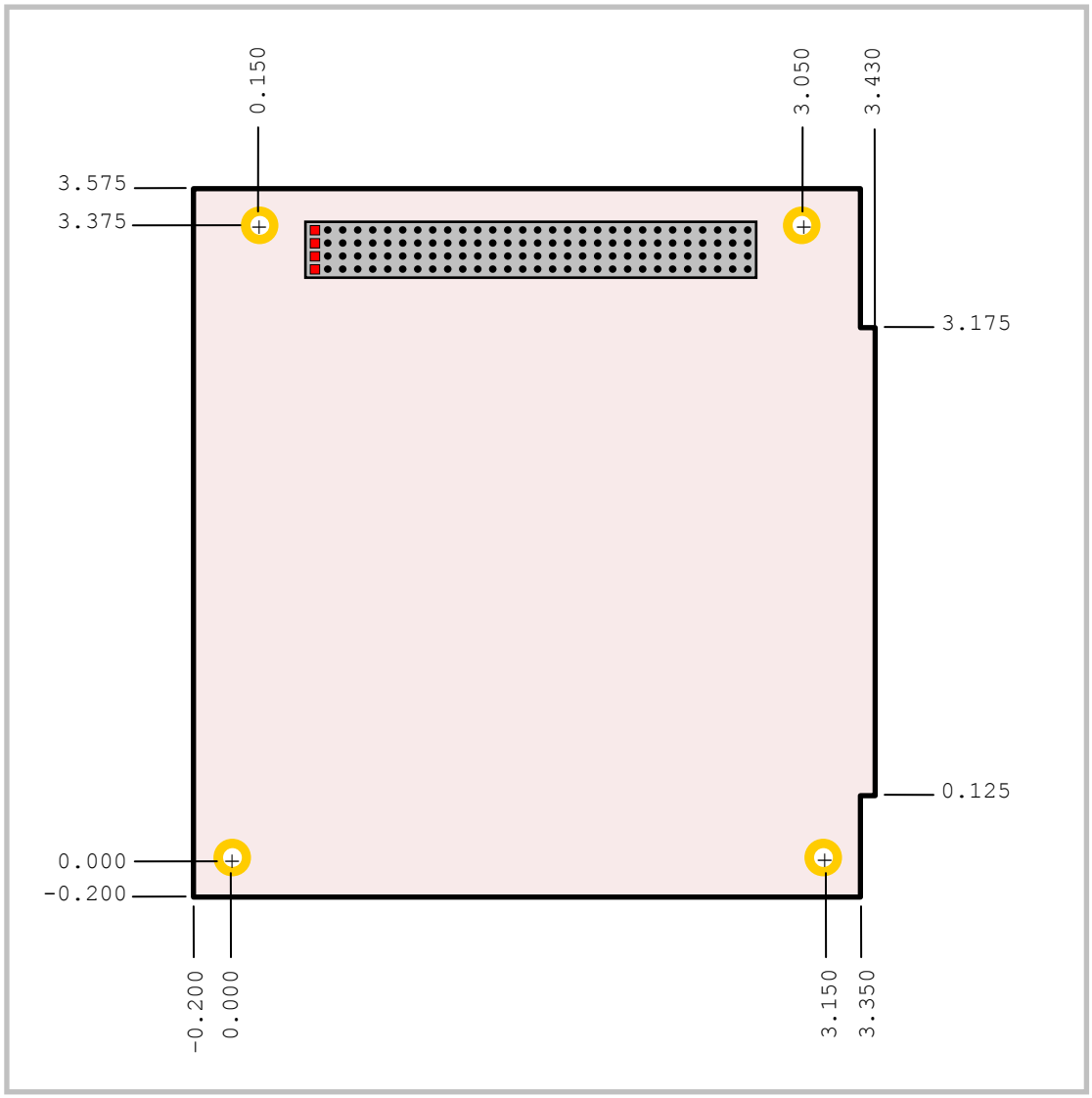


Figure 4. VL-EPM-35 Bottom Board Dimensions and Mounting Holes (Top View)

(Not to scale. All dimensions in inches.)

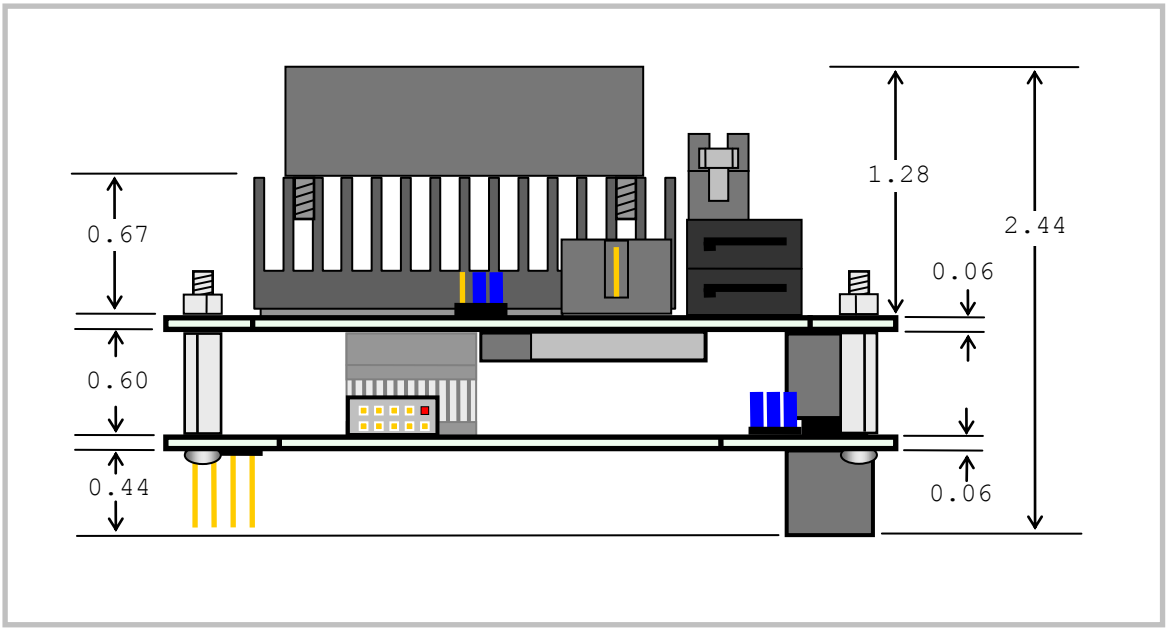


Figure 5. VL-EPM-35 Height Dimensions (Side View)

(Not to scale. All dimensions in inches.)

CBR-3406 DIMENSIONS

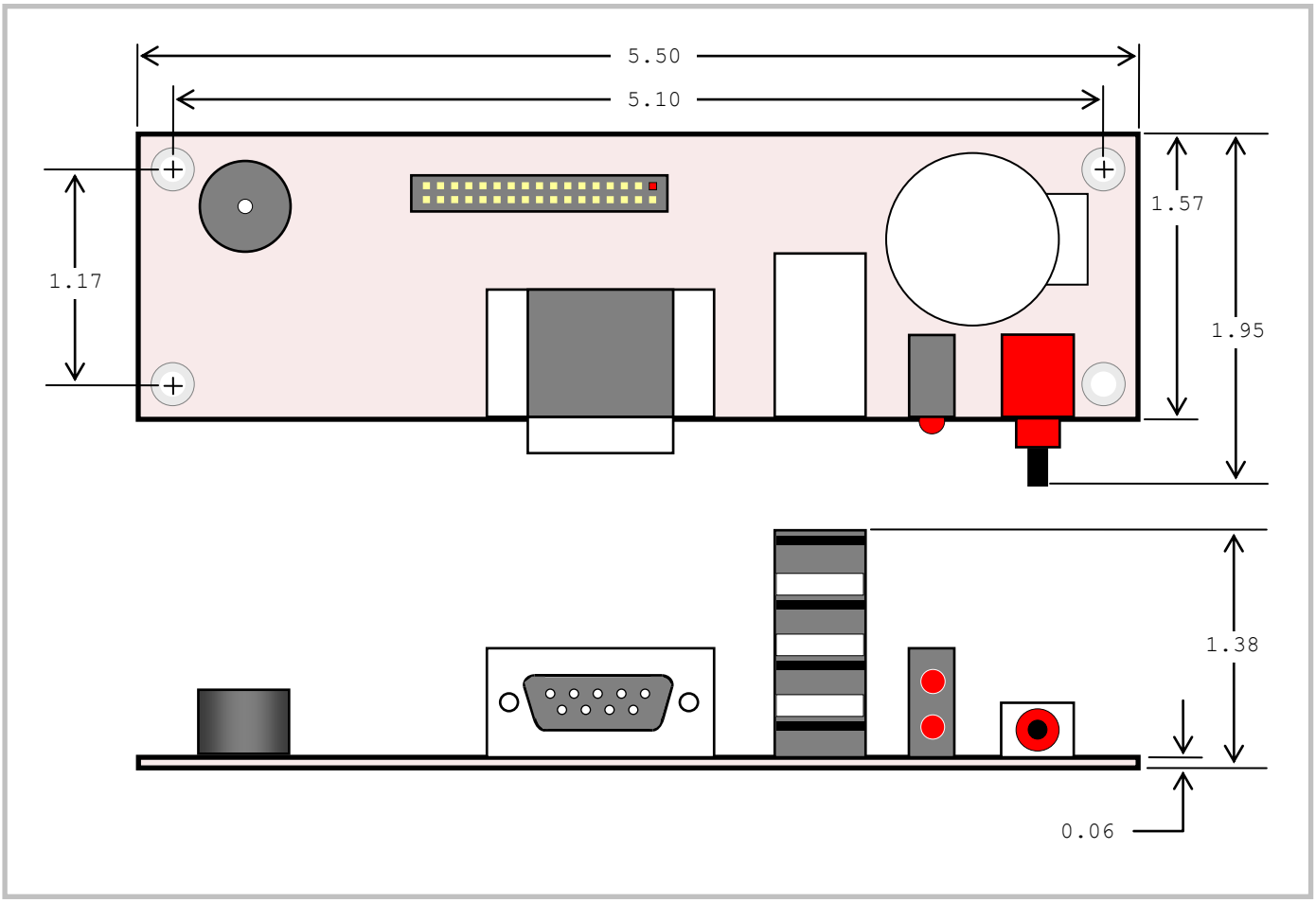


Figure 6. VL-CBR-3406 Dimensions and Mounting Holes (Top and Side Views)
(Not to scale. All dimensions in inches.)

HARDWARE ASSEMBLY

The VL-EPM-35 consists of two boards that are mounted together with four 5mm x 15.25mm M3 threaded hex male/female standoffs using the corner mounting holes. These standoffs are secured to the top circuit board using four pan head screws.

Caution: Care must be taken not to damage components near the corner mounting holes when tightening standoffs with nut driver tools.

Additional PC/104-Plus or PC/104 cards can be attached to the bottom of theVL-EPM-35 board set and secured with standoffs or 5mm nuts.

PC/104-Plus expansion modules can be secured directly to the underside of the EPM-32. PC/104 expansion modules can be secured to the underside of the EPM-32; however, the 40-pin and 64-pin ISA pass-through connectors may need to be extended, and longer standoffs might need to be used to provide adequate clearance between the PCI connector and the components on the top side of the PC/104 expansion module.

The entire assembly can sit on a table top or be secured to a base plate. When bolting the unit down, make sure to secure all four standoffs to the mounting surface to prevent circuit board flexing. Standoffs and screws are available as part number VL-HDW-105.

An extractor tool is available (part number VL-HDW-201) to separate the PC/104 modules from the stack. Use caution when using the extractor tool not to damage any board components.

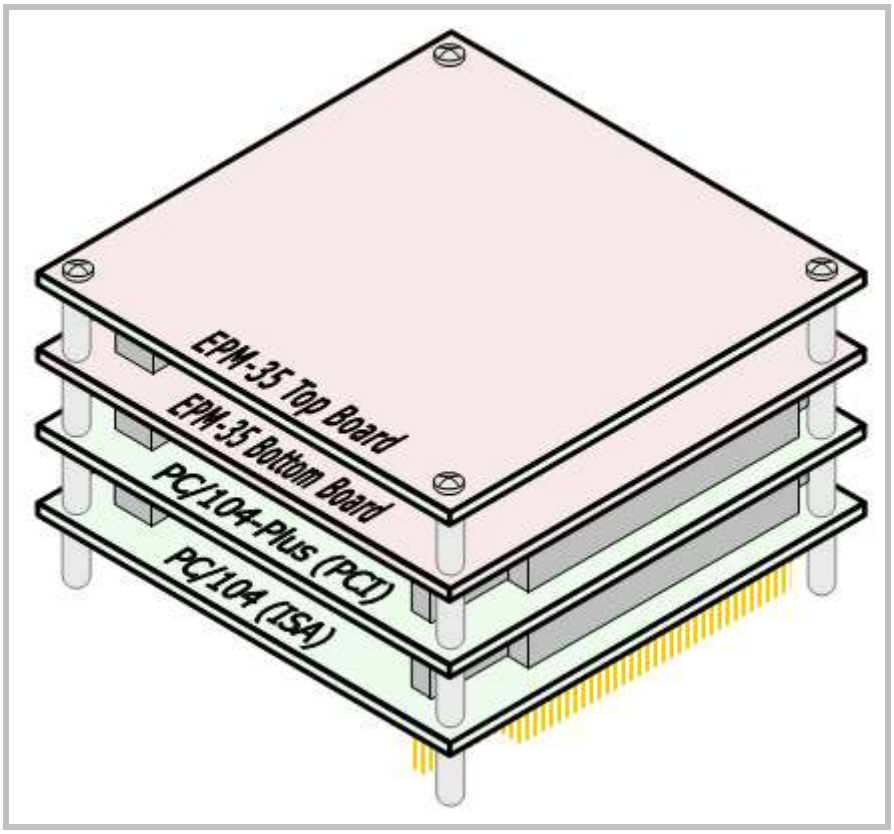


Figure 7. Stack Arrangement Example

External Connectors

VL-EPM-35 CONNECTOR LOCATIONS

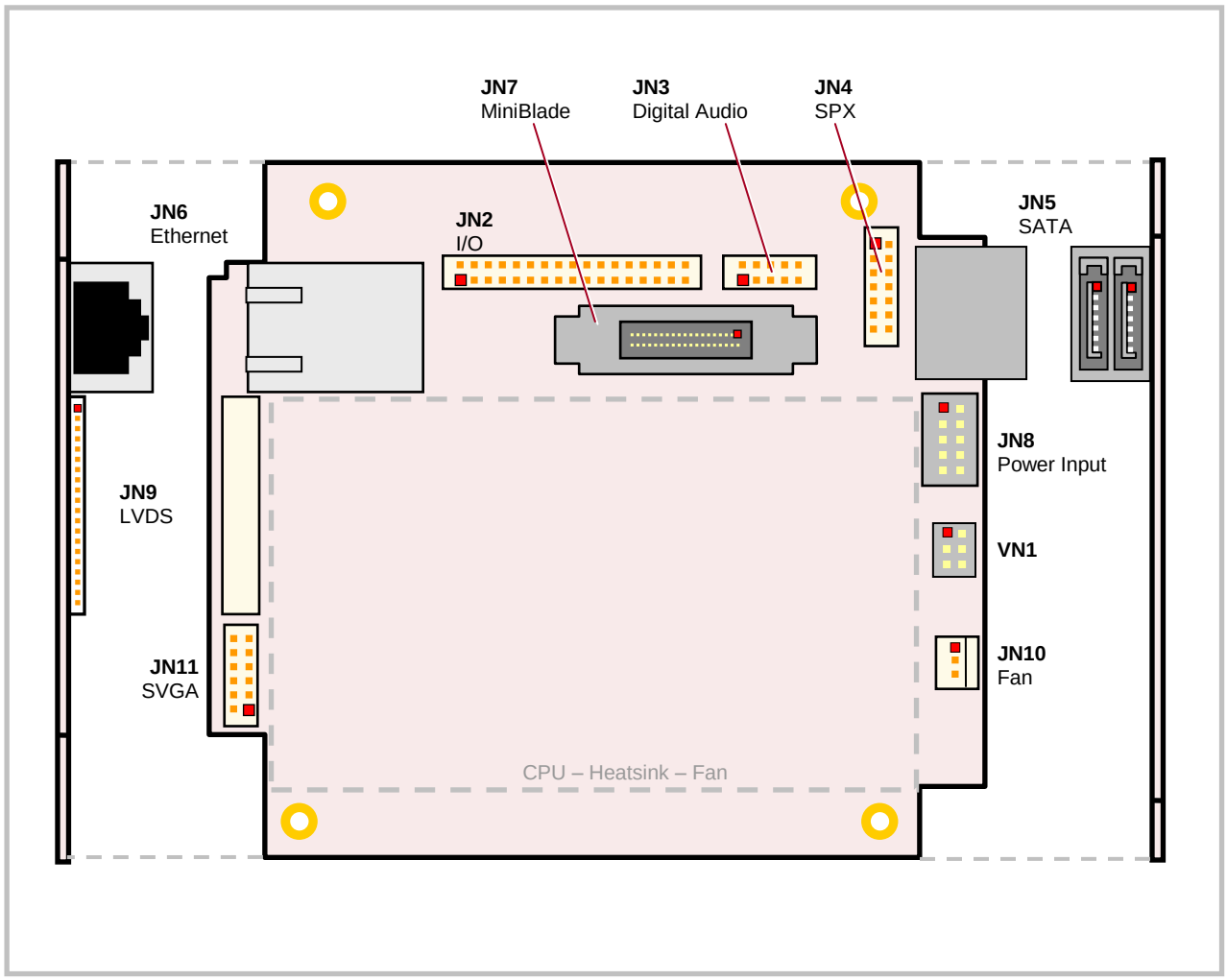


Figure 8. Connector Locations –Top Board (Top View)

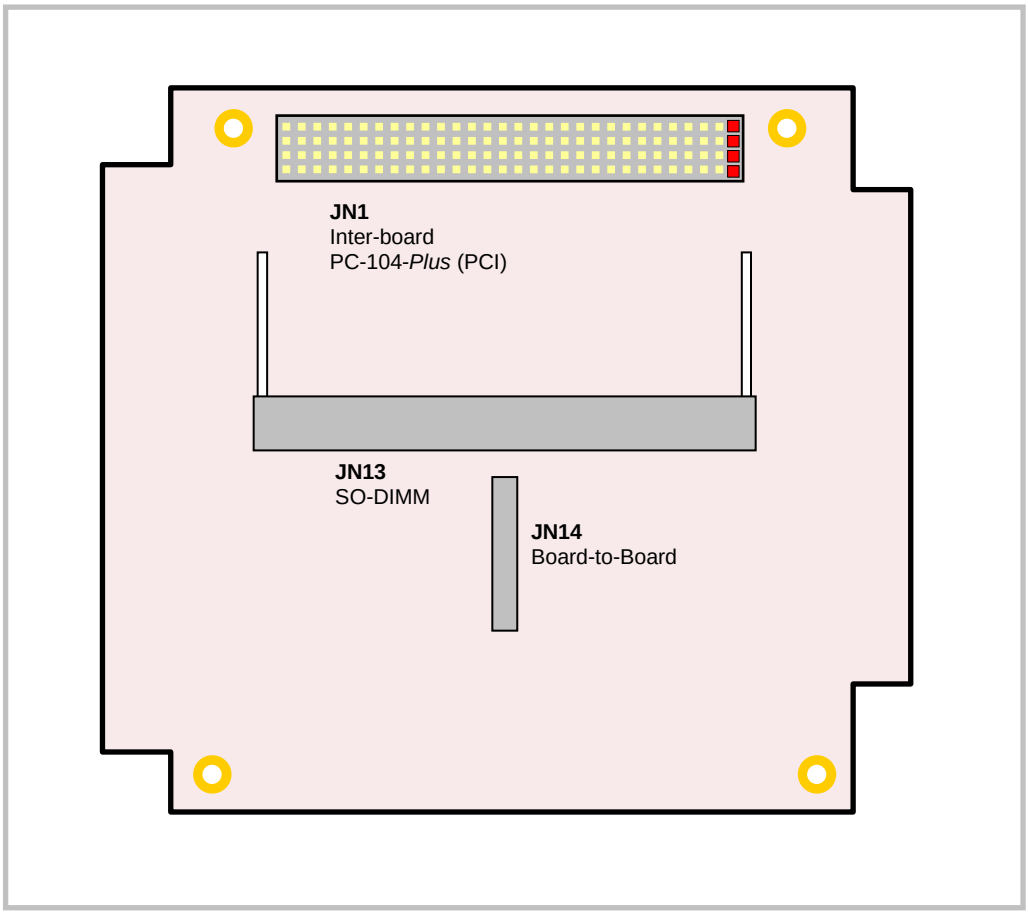


Figure 9. Connector Locations – Top Board (Bottom View)

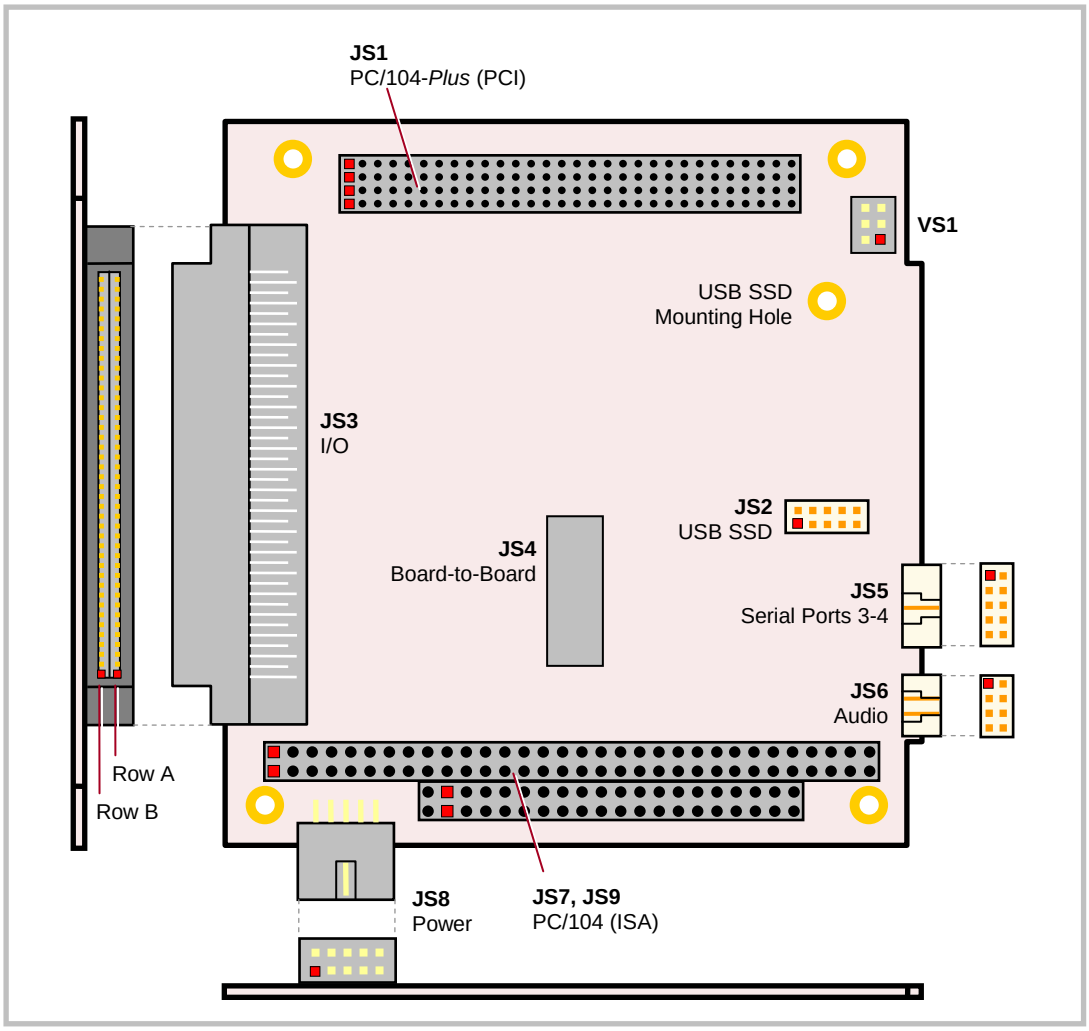


Figure 10. Connector Locations – Bottom Board (Top View)

VL-EPM-35 CONNECTOR FUNCTIONS AND INTERFACE CABLES

Table 1 provides information about the function, mating connectors, and transition cables for VL-EPM-35 connectors. Page numbers indicate where a detailed pinout or further information is available. JN connectors are located on the north board; JS designators on the south board.

Table 1: Connector Functions and Interface Cables

Connector	Function	Mating Connector	Transition Cable	Cable Description	Pin 1 Location[1] x coord.	Pin 1 Location[1] y coord.	Page
JN1	Inter-board PC/104-*Plus* (PCI)	—	—	—	0.450	3.139	45
JN2	Serial Port 5, USB 1-4, LEDs, Reset, Speaker, Battery	FCI 89947-334LF	VL-CBR-3406	34-pin latching I/O cable and breakout board	0.862	2.932	30
JN3	Digital Audio	FCI 89361710LF	—	—	2.385	2.932	36
JN4	SPX	FCI 89361714LF	VL-CBR-1401 or VL-CBR-1402	2mm 14-pin IDC, 2 or 4 SPX device cable	3.023	3.119	37
JN5	SATA0-1	Standard SATA	VL-CBR-0701 VL-CBR-0401	500mm 7-pin, straight-to-straight SATA data ATX to SATA power adapter	3.477	2.960	41
JN6	Ethernet	RJ-45 crimp-on plug	—	—	0.492	2.487	41
JN7	MiniBlade	USB Mini-Blade	—	—	2.344	2.689	42
JN8	Main Power Input	Berg 69176-010 (housing) + Berg 47715-000 (pins)	VL-CBR-1008	Interface from standard ATX power supply	3.515	2.287	23
JN9	LVDS	Molex 51146-2000 (housing), Molex 50641-8041 (pins)	VL-CBR-2010, or VL-CBR-2011, or VL-CBR-2012	18-bit TFT FPD using 20-pin Hirose, or 18-bit TFT FPD using 20-pin JAE, or 24-bit TFT FPD using 20-pin Hirose	-0.195	2.185	43
JN10	Fan	Molex 22-01-3027 or Molex 22-01-2025	Provided with assembly	—	3.565	0.9700	—
JN11	Video Output	FCI 89361-712 or FCI 89947-712	VL-CBR-1201	1’ 12-pin 2mm latching / 15-pin HD D-Sub VGA	-0.321	0.605	42
JN13	Memory	DDR3 SO-DIMM	—	—	0.473	1.974	26
JN14	Board-to-Board I/F	—	—	—	1.550	1.522	—
JS1	PC/104-*Plus* (PCI)	AMP 1375799-1	—	—	0.450	3.139	45
JS2	USB SSD	—	—	VL-F15 Series eUSB drive	2.747	1.513	45
JS3	Serial Ports 1-2, PS/2 keyboard and mouse, LPT, USB (2), GB Ethernet	3M Robinson-Nugent P50E-080S-EA	VL-CBR-8006	Breakout to standard PC device connectors	0.100	0.750	46
JS4	Board-to-Board I/F	—	—	—	1.550	1.522	—
JS5	Serial Ports 3-4	FCI 89947-334LF	VL-CBR-1012	12" dual DB9 serial port cable	3.237	1.208	31
JS6	Audio	FCI 89361710LF	VL-CBR-0803	1’ latching 8-pin 2mm to two 3.5mm stereo audio	3.237	0.633	36
JS7, JS9	PC/104 (ISA)	AMP 1375795-2	—	—	0.050	0.200	46
JS8	Power Input	Berg 69176-010 (housing) + Berg 47715-000 (pins)	VL-CBR-1008	Interface from standard ATX power supply	0.225	-0.050	23

1. The PCB Origin is the mounting hole to the lower left, as shown in Figure 8.

CONNECTOR LOCATIONS – VL-CBR-3406

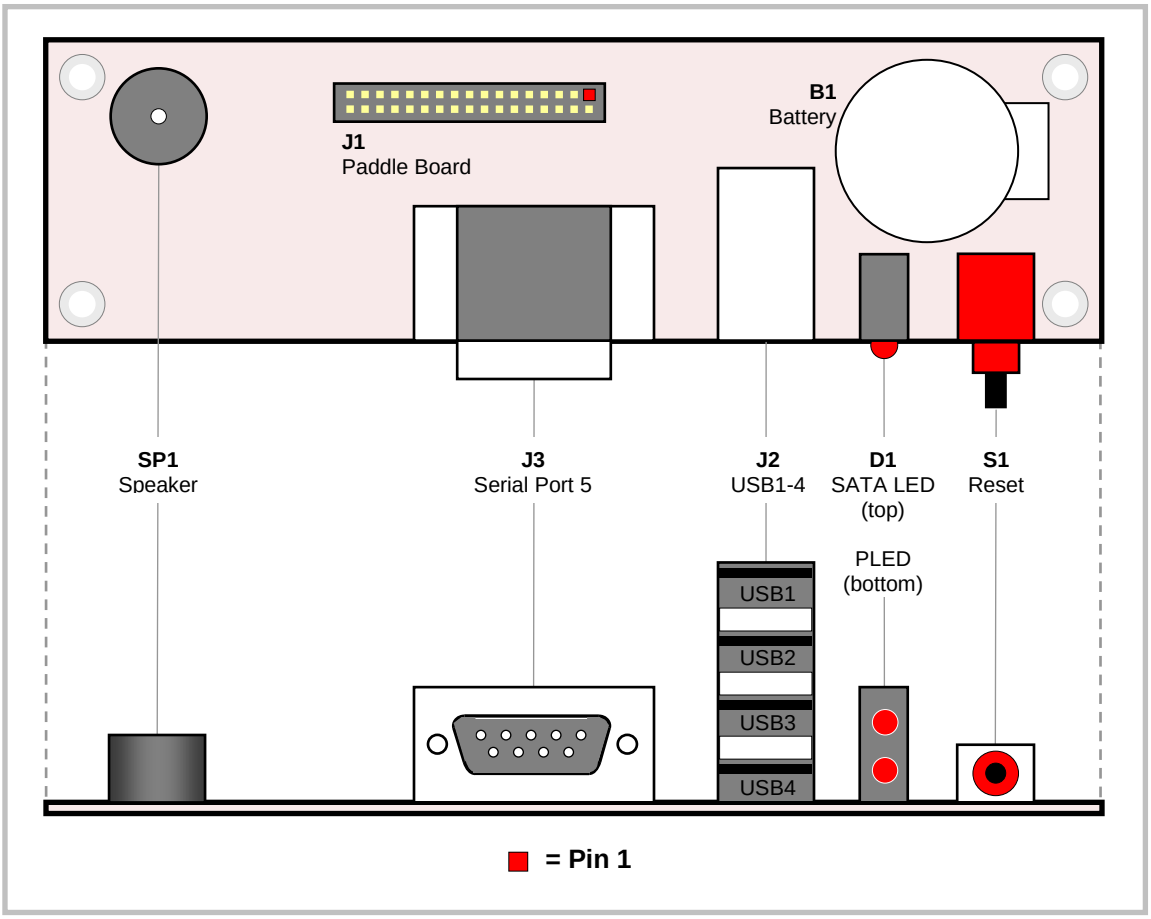


Figure 11. VL-CBR-3406 Connector Locations (Top and Side Views)

CBR-3406 CONNECTOR FUNCTIONS AND MATING CONNECTORS

Table 2: VL-CBR-3406 Connector Functions and Interface Cables

Connector	Function	PCB Connector
J1	2mm IDC Connector	FCI 98414-F06-34ULF
J2	USB 1-4	4 USB Type A
J3	Serial Port 5	DB-9 male, Kycon K22X-E9P-N
B1	Battery	Lithium coin battery, Panasonic BR2330A/GAE
D1	SATA LED / PLED	Dual LED
S1	Reset	Pushbutton
SP1	Speaker	Piezo

Jumper Blocks

JUMPERS AS-SHIPPED CONFIGURATION

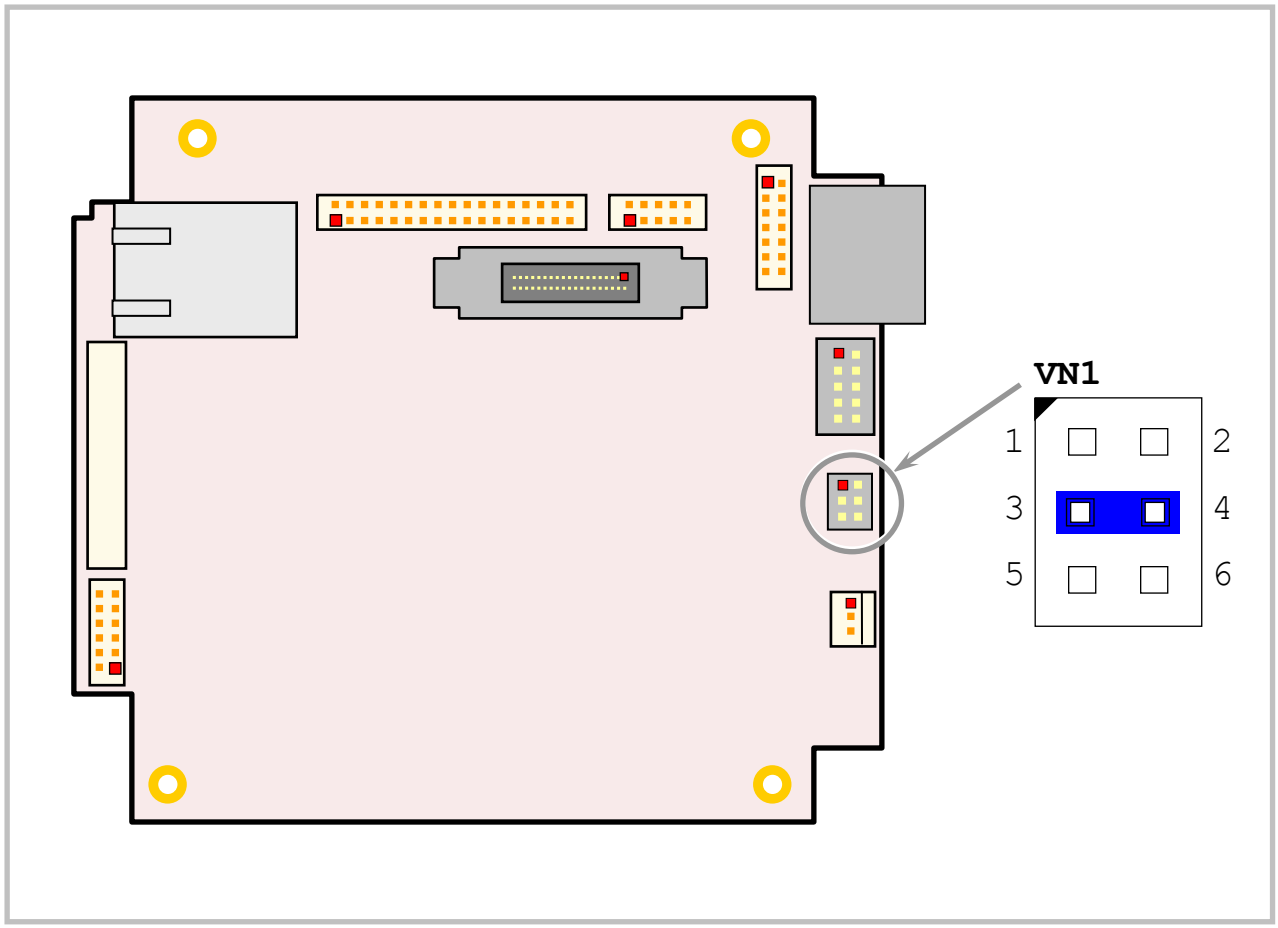


Figure 12. Jumpers As-Shipped – Top Board

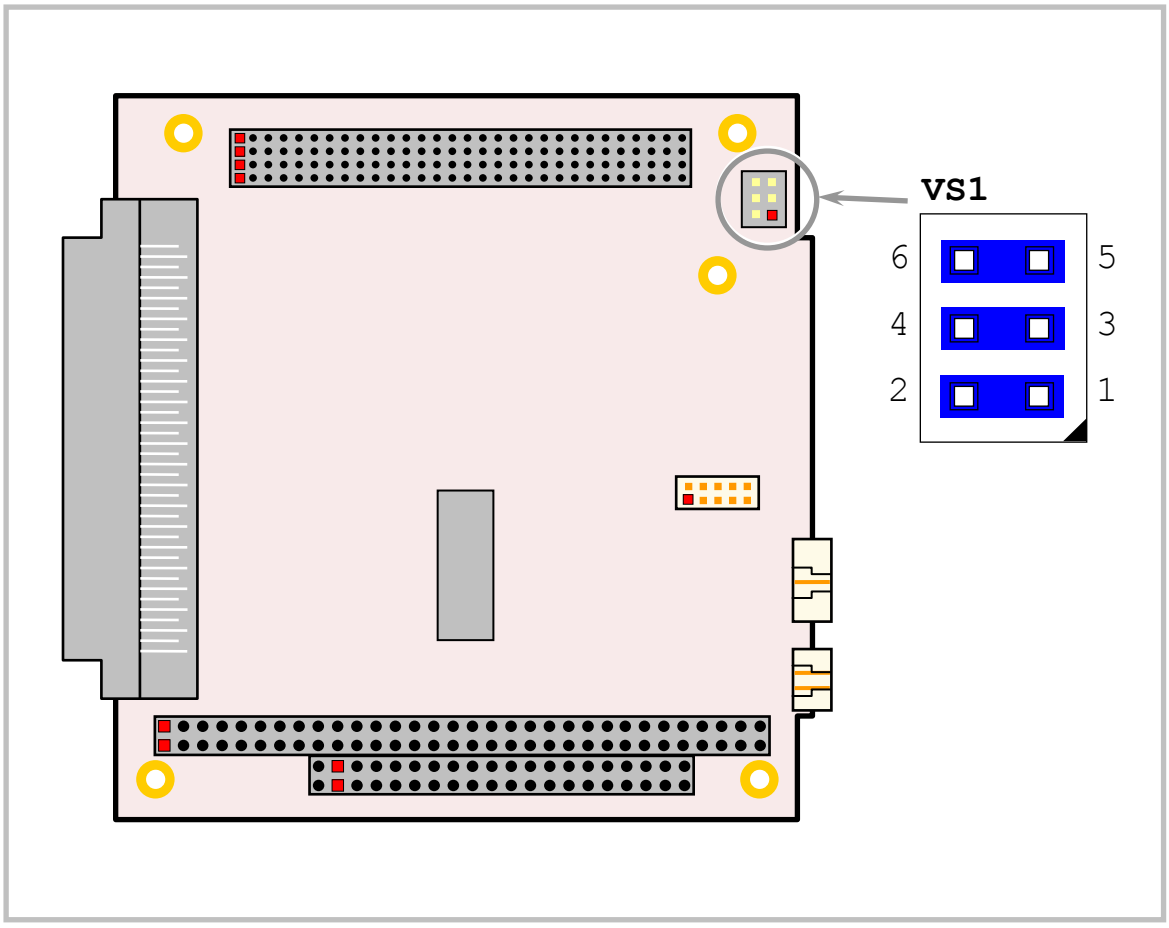


Figure 13. Jumpers As-Shipped – Bottom Board

JUMPER SUMMARY

Table 3: Jumper Summary

Jumper Block	Description	As Shipped	Page
VN1[1-2]	**System BIOS Selector** In – Backup system BIOS selected Out – Primary system BIOS selected The Primary system BIOS is field upgradeable using the BIOS upgrade utility. See http://www.VersaLogic.com/private/wildcatsupport.asp for more information.	Out	26
VN1[3-4]	**Serial Port 5 RS-422 Termination** In – Port terminated with 120 Ohms Out – No termination Places terminating resistor across Serial Port 5 RS-422 RX+/RX- differential pair.	In	32
VN1[5-6]	**CMOS RAM and Real-time Clock Erase** In – Erase CMOS RAM and real-time clock Out – Normal operation	Out	26
VS1[1-2]	**Serial Port 2 RS-422 Termination** In – Port terminated with 120 Ohms Out – No termination Places terminating resistor across Serial Port 2 RS-422 RX+/RX- differential pair.	In	32
VS1[3-4]	**Serial Port 3 RS-422 Termination** In – Port terminated with 120 Ohms Out – No termination Places terminating resistor across Serial Port 3 RS-422 RX+/RX- differential pair.	In	32
VS1[5-6]	**Serial Port 4 RS-422 Termination** In – Port terminated with 120 Ohms Out – No termination Places terminating resistor across Serial Port 4 RS-422 RX+/RX- differential pair.	In	32

Power Supply

POWER CONNECTORS

Main power is applied to the VL-EPM-35 through a 10-pin connector at either location JN8 (top board) or JS8 (bottom board). The table below shows the pinout for both connectors.

Note: Only one power connector should be used at a time. If both JN8 and JS8 are used at the same time, a ground loop may result.

Warning! To prevent possibly irreparable damage to the system, it is critical that the power connectors are wired correctly. Make sure to use all +5VDC pins and all ground pins to prevent excess voltage drop. Some manufacturers include a pin-1 indicator on the crimp housing that corresponds to pin-10 of the pinout shown in Figure 14.

Table 4: Main Power Connector Pinout

JN8/JS8 Pin	Signal Name	Description
1	GND	Ground
2	+5VDC	Power Input
3	GND	Ground
4	+12VDC	Power Input
5	GND	Ground
6	-12VDC	Power Input
7	+3.3VDC	Power Input
8	+5VDC	Power Input
9	GND	Ground
10	+5VDC	Power Input

Figure 14 shows the VersaLogic standard pin numbering for this type of 10-pin power connector and the corresponding mating connector.

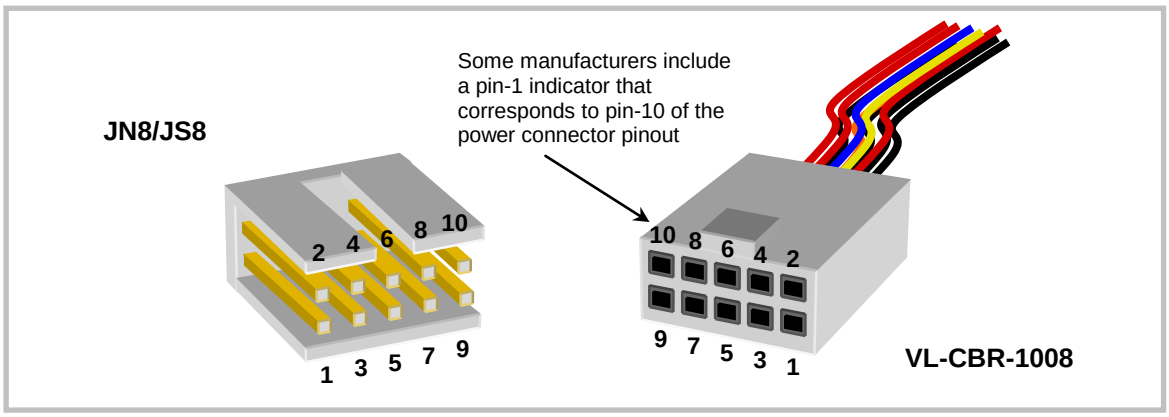


Figure 14. JN8/JS8 and VL-CBR-1008 Pin Numbering

Note: The +3.3VDC, +12VDC and -12VDC inputs are required only for expansion modules that require these voltages.

POWER REQUIREMENTS

The VL-EPM-35 requires only +5 volts (±5%) for proper operation. The higher voltages required for the RS-232 ports are generated with as needed on-board. Low-voltage supply circuits provide the many power rails required by the CPU and other on-board devices.

The exact power requirement of the VL-EPM-35 depends on several factors, including memory configuration, CPU speed, peripheral connections, type and number of expansion modules and attached devices. For example, driving long RS-232 lines at high speed can increase power demand, and USB devices can draw considerable power depending on the device.

The VL-EPM-35 is equipped with a voltage sensing reset circuit. The system will reset if voltage drops below 4.63V typically (4.50V min./4.75V max.).

POWER DELIVERY CONSIDERATIONS

The VL-EPM-35 draws up to 28.5W (5.7A) as measured on a typical time averaging ammeter. The board can experience large, short-term current transients during operation, so care must be taken to provide robust power to the board. A good power delivery method eliminates such problems as voltage drop and lead inductance. Using the VersaLogic approved power supply and power cable will ensure high quality power delivery to the board. Customers who design their own power delivery methods should take into consideration the guidelines below to ensure good power connections.

Also note that the 5V @ 21.3W (models S, SR) or 15.5W (models E, ER) typical operating current does not include any off-board power usage that may be fed through the VL- EPM-35 power connector. PC/104 boards on the expansion site and USB devices plugged into the board will source additional 5V power through the VL- EPM-35 power connector.

- Do not use wire smaller than 22 AWG. Use high quality UL 1007 compliant stranded wire.
- The length of the wire should not exceed 12".
- Avoid using any additional connectors in the power delivery system.
- The power and ground leads should be twisted together, or as close together as possible to reduce lead inductance.
- A separate conductor must be used for each of the power pins.
- All 5V pins and all ground pins must be independently connected between the power source and the power connector.
- Implement the remote sense feature on your power supply if it has one. Connect the remote sense lines in tandem with one of the power connector 5V and ground pins. This is done at the connector to compensate for losses in the power wires.

Use a high quality power supply that can supply a stable voltage while reacting to widely varying current draws.

LITHIUM BATTERY

A lithium battery is mounted on the bottom board of the VL-EPM-35. The I/O connector at JN2 provides a second battery interface. Installing the VL-CBR-3406 breakout board adds a secondary battery, effectively doubling the battery life of the VL-EPM-35. Both batteries are diode protected, so if one is damaged or drained, the other will not be affected.

Warning! To prevent shorting, premature failure, or damage to the lithium battery, do not place the board on a conductive surface such as metal, black conductive foam, or the outside surface of a metalized ESD protective pouch. The lithium battery may explode if mistreated. Do not recharge, disassemble or dispose of in fire. Dispose of used batteries promptly.

Normal battery voltage should be at least +3V. If the voltage drops below +2V, contact the factory for a replacement (part number HB3/0-1). The life expectancy under normal use is approximately 10 years.

The battery interface uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

CPU

The Intel Core 2 Duo processor combines fast performance, using Intel's 45nm technology, with advanced power savings features. The SP9300 model used on the VL-EPM-35 has a maximum clock rate of 2.26 GHz and a front side bus speed of 1066 MHz, and features 6 MB of L2 cache. Other features include DDR3 SDRAM support and an integrated display controller. For more CPU information see the VL-EPM-35 support page.

System RAM

The VL-EPM-35 has one DDR3 SO-DIMM socket with the following characteristics:

- Storage Capacity Up to 4GB
- Voltage 1.5V
- Type 800 MHz PC3-6400 or 1067 MHz PC3-8500

CMOS RAM

CLEARING CMOS RAM

You can install a jumper at VN1 pins 5-6 for a minimum of three seconds to erase the contents of the CMOS RAM and the real-time clock. When clearing CMOS RAM:

1. Power off the VL-EPM-35.
2. Install a jumper on VN1[5-6] and leave it for three seconds.
3. Remove the jumper.
4. Power on the VL-EPM-35.

CMOS Setup Defaults

The VL-EPM-35 permits users to modify CMOS Setup defaults. This allows the system to boot up with user-defined settings from cleared or corrupted CMOS RAM, battery failure or battery-less operation. All CMOS setup defaults can be changed, except the time and date. CMOS Setup defaults can be updated with the BIOS Update Utility. See the General BIOS Information page for details.

Note: If CMOS Setup default settings make the system unbootable and prevent the user from entering CMOS Setup, the system can be recovered by switching to the Backup BIOS.

DEFAULT CMOS RAM SETUP VALUES

After CMOS RAM is cleared, the system will load default CMOS RAM parameters the next time the board is powered on. The default CMOS RAM setup values will be used in order to boot the system whenever the main CMOS RAM values are blank, or when the system battery is dead or has been removed from the board.

Primary and Backup BIOS

The Primary system BIOS is field upgradeable using the BIOS upgrade utility (see the VL-EPM-35 Support Page for more information). The Backup BIOS is available if the Primary BIOS becomes corrupted. Jumper VN1[1-2] controls whether the system uses the Primary or Backup BIOS. By default the Primary BIOS is selected (jumper removed).

Real Time Clock

The VL-EPM-35 features a year 2000-compliant, battery-backed 146818-compatible real-time clock/calendar chip. Under normal battery conditions, the clock maintains accurate timekeeping functions when the board is powered off.

SETTING THE CLOCK

The CMOS Setup utility (accessed by pressing the Delete key during the early boot cycle) can be used to set the time and date of the real time clock.

Watchdog Timer

A watchdog timer circuit is included on the VL-EPM-35 board to reset the CPU if proper software execution fails or a hardware malfunction occurs.

If the watchdog timer is enabled, software must periodically refresh the watchdog timer at a rate faster than the timer is set to expire (1000 ms minimum). Writing 5Ah to the WDHOLD register resets the watchdog timeout period. (See "Special Control Register" and "Watchdog Hold Register.")

Fan/Tachometer Monitor

The VL-EPM-35 includes a fan/tachometer indicator circuit that can generate an interrupt if the CPU fan speed drops below 1 Hz. Bit D0 of the FANTACH register enables or disables the fan interrupt. Bit D7 indicates whether the fan is running at or above 1 Hz or below 1Hz. See "Fan/Tachometer Control Register" for more information.

FAN/TACH IRQ CODE EXAMPLE

```
#include <stdio.h>
#include <conio.h>
#include <stdlib.h>
#include <graph.h>
#include <dos.h>

//Definitions
#define TRUE            1
#define FALSE           0
#define ESC             27
#define FANREG1         0xC94
#define FANREG2         0xCA4
#define FANIRQEN        0x01
#define SLOWFAN         0x80

//Global Variables
volatile int int_hit;

//Function Prototypes
void (__interrupt __far *old_isr)();    // holds old interrupt handler
void __interrupt __far chain_isr(void);
```

```
//Main
void main()
{
  char keypressed = 0;
  int irq_count = 0;

   _clearscreen( _GCLEARSCREEN );
  _settextposition(2,1);
  printf( "FANTACH IRQ DEMO -- Stop the spinning fan to perform
test...\n" );

  _settextposition(4,1);
  printf( "Setting new ISR for IRQ 7...\n" );
  outp( 0x20, 0x20 );                    //Clear any pending IRQs
  old_isr = _dos_getvect( 0x0F );        //Assign function ptr to old_isr
  _dos_setvect( 0x0F, chain_isr );       //Set new ISR function ptr
  outp( 0x21, inp ( 0x21 ) & 0x7F );     //unmask IRQ 7 in the PIC

  //Ensure slow fan status bit is cleared...
  outp ( FANREG1, inp ( FANREG1 ) | SLOWFAN );
  outp ( FANREG2, inp ( FANREG2 ) | SLOWFAN );

  //Enable Slow/Stalled Fan Interrupt output...
  outp( FANREG1, inp( FANREG1 ) | FANIRQEN );
  outp( FANREG2, inp( FANREG2 ) | FANIRQEN );


  _settextposition(5,1);
  printf( "Listening for IRQ7...(press ESC to quit)\n" );
  while (keypressed != ESC)
  {
    if (kbhit())
    {
      keypressed = getch();
    }

    //Check for IRQ...
    if ( int_hit )
    {
      _settextposition(6,1);
      irq_count++;
      printf( "%d Slow/Stalled Fan IRQs Detected!\n", irq_count );
      int_hit = FALSE;
    }
  }
  _settextposition(7,1);
  printf( "Original IRQ7 ISR restored...\n\n" );
  _dos_setvect( 0x0F, old_isr );         //restore original ISR

  //Turn off Slow/Stalled Fan IRQ output...
  outp( FANREG1, inp( FANREG1 ) & !FANIRQEN );
  outp( FANREG2, inp( FANREG2 ) & !FANIRQEN );

  exit( 0 );
}

void __interrupt __far chain_isr(void)
```

```
{
  int_hit = TRUE;

  //clear slow fan status bit...(this will trigger a new IRQ,
  //if the fan is still stalled.)
  outp ( FANREG1, inp ( FANREG1 ) | SLOWFAN );
  outp ( FANREG2, inp ( FANREG2 ) | SLOWFAN );

  outp( 0x20, 0x20 );                    //EOI

  (*old_isr)();                          //call old isr
}
```

34-Pin I/O Connector (JN2)

The JN2 34-pin I/O connector incorporates one serial port, USB ports, LEDs, speaker, and the reset button. Table 5 illustrates the function of each pin and the pinout assignments to connectors on the VL-CBR-3406 breakout board.

Table 5: JN2 I/O Connector Pinout

JN2 Pin	CBR-3406 Connector	Signal
1	**Serial Port 5**	Transmit +
2	J3	Transmit –
3		Ground
4		Receive +
5		Receive –
6		Ground
7	**USB0**	Ground
8	J2 Top	USB0 Power
9		USB0 Data –
10		USB0 Data +
11	**USB1**	Ground
12	J2 Middle	USB1 Power
13	Top	USB1 Data –
14		USB1 Data +
15	**USB2**	Ground
16	J2 Middle	USB2 Power
17	Bottom	USB6 Data –
18		USB6 Data +
19	**USB3**	Ground
20	J2 Bottom	USB3 Power
21		USB7 Data –
22		USB7 Data +
23	**PLED**	3.3V (protected)
24	**D1 Bottom**	Programmable LED
25	**IDE LED**	3.3V (protected)
26	D1 Top	IDE LED
27	**Speaker**	3.3V (protected)
28	SP1	Speaker
29		3.3V (protected)
30		Reserved
31	**Battery**	Ground
32	B1	Battery In
33	**Reset**	Ground
34	S1	System Reset

All user I/O ports on this connector are protected against ESD damage.

Serial Ports (JN2, JS3, JS5)

The VL-EPM-35 features five 16550-based serial ports, as described below.

Table 6: VL-EPM-35 Serial Ports

Port	Type	Connector
Serial Port 1	RS-232,16C550 compatible, all handshake lines implemented	JS3 to VL-CBR-8006 DB-9 (labeled COM1)
Serial Port 2	RS-232/422/485,16C550 compatible, 4-wire RS-232 (only CTS and RTS handshaking), auto direction control	JS3 to VL-CBR-8006 DB-9 (labeled COM2)
Serial Port 3	RS-232/422/485,16C550 compatible, 4-wire RS-232 (only CTS and RTS handshaking), auto direction control	JS5
Serial Port 4	RS-232/422/485,16C550 compatible, 4-wire RS-232 (only CTS and RTS handshaking), auto direction control	JS5
Serial Port 5	RS-232/422/485, 16C550 compatible, 4-wire RS-232 (only CTS and RTS handshaking), manual direction control	JN2 to VL-CBR-3406 J3 DB-9

Serial Port 1 operates in RS-232 mode only with all handshaking lines implemented.

Serial ports 2-5 are 4-wire connections and can operate in RS-232, RS-422, and RS-485 modes, with only CTS and RTS handshaking. For these ports, additional non-standard baud rates are also available (programmable in the normal baud registers) of up to 460K baud.

Serial ports 2-4 operate with automatic direction control. Serial port 5 operates with manual direction control.

Interrupt assignment, I/O address, and mode for serial ports are handled in CMOS Setup. Ports can be enabled or disabled in CMOS setup.

These connectors are protected against ESD damage.

SERIAL PORT CONNECTORS

Serial Ports 1 and 2

The interface to Serial Ports 1 and 2 are provided by connector JS3 on the bottom board. (See "80-Pin I/O Connector (JS3)" for a pinout of connector JS3.) VL-CBR-8006 provides two DB-9 connectors labeled COM1 and COM2. The pinouts of these connectors are shown below.

Table 7: Serial Port 1 Pinout

JS3 Pin	RS-232	VL-CBR-8006 DB-9 COM1 Pin
B21	DCD	1
B22	DSR	6
B23	RXD*	2
B24	RTS	7
B25	TXD*	3
B26	CTS	8
B27	DTR	4
B28	RI	9
B29	Ground	5

Table 8: Serial Port 2 Pinout

JS3 Pin	RS-232	RS-422	RS-485	VL-CBR-8006 DB-9 COM2 Pin
B31	NC	NC	NC	1
B32	NC	NC	NC	6
B33	RXD	RxD–	RxD–	2
B34	RTS	TxD+	TxD+	7
B35	TXD	TxD–	TxD–	3
B36	CTS	RxD+	RxD+	8
B37	Ground	Ground	Ground	4
B38	NC	NC	NC	9
B39	Ground	Ground	Ground	5

Serial Ports 3 and 4

The interface to Serial Ports 3 and 4 are provided by connector JS5 on the bottom board. VL-CBR-1012 provides two DB-9 connectors. The pinouts of the JS5 connector and the DB-9 connectors on the VL-CBR-1012 cable are shown below.

Table 9: Serial Port 3 and 4 Pinout

JS5 Serial Port 3 Pin	RS-232	RS-422	RS-485	VL-CBR-1012 DB-9 Pin
1	RXD	RxD–	RxD–	2
2	CTS	RxD+	RxD+	8
3	TXD	TxD–	TxD–	3
4	RTS	TxD+	TxD+	7
5	Ground	Ground	Ground	5
–	NC	NC	NC	1
–	NC	NC	NC	4
–	NC	NC	NC	6
–	NC	NC	NC	9

JS5 Serial Port 4 Pin	RS-232	RS-422	RS-485	VL-CBR-1012 DB-9 Pin
6	Ground	Ground	Ground	5
7	RXD	RxD–	RxD–	2
8	CTS	RxD+	RxD+	8
9	TXD	TxD–	TxD–	3
10	RTS	TxD+	TxD+	7
–	NC	NC	NC	1
–	NC	NC	NC	4
–	NC	NC	NC	6
–	NC	NC	NC	9

Serial Port 5

The interface to Serial Port 5 is provided by connector JN2 on the top board. (See "34-Pin I/O Connector (JN2)" for a pinout of the JN2 connector.) VL-CBR-3406 provides a DB-9 connector at J3. The pinout of this connector is shown below.

Table 10: Serial Port 5 Pinout

JN2 Pin	RS-232	RS-422	RS-485	VL-CBR-3406 DB-9 (J3) Pin
1	RTS	TxD+	TxD+	7
2	TXD	TxD–	TxD–	3
3	Ground	Ground	Ground	4*
4	CTS	RxD+	RxD+	8
5	RXD	RxD–	RxD–	2
6	Ground	Ground	Ground	5
–	NC	NC	NC	1
–	NC	NC	NC	6
–	NC	NC	NC	9

* Pin 4 of CBR-3406 connector J3 is not connected.

COM Port Configuration

Jumper block VN1[3-4] sets the serial port 5 termination of the RS-422 differential pairs. Jumper block VS1 sets the termination for serial ports 2-4. See the Jumper Summary on page 22 for details on termination configuration.

RS-485 Mode Line Driver Control

The TxD+/TxD– differential line driver can be turned on and off by manipulating the RS-485/422 Transmit/Receive Control Register. Refer to page 53 for more information. Serial ports 2-4 can be configured with CMOS Setup to operate with automatic direction control.

USB Interface (JN2, JS3)

The USB interface on the VL-EPM-35 is UHCI (Universal Host Controller Interface) and EHCI (Enhance Host Controller Interface) compatible, which provides a common industry software/hardware interface.

Connector JN2 includes interfaces for four USB ports. There are four Type A USB connectors on the VL-CBR-3406 breakout board.

Connector JS3 includes interfaces for two USB ports. There are two Type A USB connectors on the VL-CBR-8006 breakout cable.

These connectors are protect against ESD damage.

BIOS CONFIGURATION

The USB channels use a number of PCI interrupts (see “Interrupt Configuration”). CMOS Setup is used to select the IRQ line routed to each PCI interrupt line.

Programmable LED (JN2, JS3)

Connectors JN2 and JS3 include a output signals for a software controlled LED. For connector JN2, connect the cathode of the LED to JN2 pin 24; connect the anode to +3.3V. An on-board 200 ohm resistor limits the current. A programmable LED is provided on the VL-CBR-3406 breakout board and on the VL-CBR-8006 cable.

These connectors are protect against ESD damage.

To turn the LED on and off, set or clear bit D7 in I/O port CA0h. When changing the register, make sure not to alter the value of the other bits.

The following code examples show how to turn the LED on and off. See page 50 for more information:

LED On

```
MOV    DX,CA0H
IN     AL,DX
OR     AL,80H
OUT    DX,AL
```

LED Off

```
MOV    DX,CA0H
IN     AL,DX
AND    AL,7FH
OUT    DX,AL
```

Note: The LED is turned on by the BIOS during system startup. This causes the light to function as a "power on" indicator if it is not otherwise controlled by user code.

HD LED (JN2, JS3)

Connectors JN2 and JS3 include output signals for a SATA activity LED. For JN2, connect the cathode of the LED to JN2 pin 26, and connect the anode to +5V. An on-board 200 Ohm resistor limits the current. A SATA LED is provided on the VL-CBR-3406 board and the VL-CBR-8006 cable. These interfaces are protected against ESD damage.

Internal Speaker (JN2, JS3)

Connectors JN2 and JS3 include speaker output signals. The VL-CBR-3406 breakout board and VL-CBR-8006 each provide a Piezo electric speaker. These interfaces are protected against ESD damage.

Pushbutton Reset (JN2, JS3)

Connectors JN2 and JS3 include inputs for a pushbutton reset switch. Shorting JN2 pin 34 to ground causes the VL-EPM-35 to reboot. These interfaces are protected against ESD damage.

Audio (JN3, JS6)

DIGITAL AUDIO (JN3)

The digital audio interface on the VL-EPMp-34 allows you to connect an external audio codec to the system. Contact VersaLogic Sales for available external codecs**.** This interface is protected against ESD damage.

Table 11: JN3 Audio Connector

JN3 Pin	Signal Name	Function
1	HDA_BIT_CLK_0	Clock
2	Ground	Ground
3	HDA_SDOUT_0	Line Out
4	Ground	Ground
5	HDA_SDIN_0	Line In
6	Ground	Ground
7	HDA_SYNC_0	Frame sync
8	V3_3	+3.3V (protected)
9	HDA_RST_0#	Reset
10	V3_3	+3.3V (protected)

AUDIO LINE IN/OUT (JS6)

Connector JS6 provides an audio interface using the IDT 92HD75B Audio Codec. Drivers are available for most Windows-based operating systems (see the VL-EPM-35 support page). The interface provides the line-level stereo input and line-level stereo output connection points. The outputs will drive any standard-powered PC speaker set. This interface is protected against ESD damage.

Table 12: JS6 Audio Connector Pinout

JS6 Pin	Signal Name	Function
1	LINE_OUTR	Line-Out Right
2	Ground	Ground
3	LINE_OUTL	Line-Out Left
4	Ground	Ground
5	LINE_INR	Line-In Right
6	Ground	Ground
7	LINE_INL	Line-In Left
8	Ground	Ground

SPX™ Expansion Bus (JN4)

Up to four serial peripheral expansion (SPX) devices can be attached to the VL-EPM-35 at connector JN4 using the VL-CBR-1401 or VL-CBR-1402 cable. The SPX interface provides the standard serial peripheral interface (SPI) signals: SCLK, MISO, and MOSI, as well as four chip selects, SS0# to SS3#, and an interrupt input, SINT#.

The 5.0V power provided to pins 1 and 14 of JN4 is protected by a 1 Amp fuse.

Table 13: SPX Expansion Bus Pinout

JN4 Pin	Signal Name	Function
1	V5_0	+5.0V (Protected)
2	SCLK	Serial Clock
3	GND	Ground
4	MISO	Serial Data In
5	GND	Ground
6	MOSI	Serial Data Out
7	GND	Ground
8	SS0#	Chip Select 0
9	SS1#	Chip Select 1
10	SS2#	Chip Select 2
11	SS3#	Chip Select 3
12	GND	Ground
13	SINT#	Interrupt Input
14	V5_0	+5.0V (Protected)

SPI is, in its simplest form, a three wire serial bus. One signal is a Clock, driven only by the permanent Master device on-board. The others are Data In and Data Out with respect to the Master. The SPX implementation adds additional features, such as chip selects and an interrupt input to the Master. The Master device initiates all SPI transactions. A slave device responds when its Chip Select is asserted and it receives Clock pulses from the Master.

The SPI clock rate can be software configured to operate at speeds between 1 MHz and 8 MHz. Please note that since this clock is divided from a 33 MHz PCI clock, the actual generated frequencies are not discrete integer MHz frequencies. All four common SPI modes are supported through the use of clock polarity and clock idle state controls.

VERSALOGIC SPX EXPANSION MODULES

VersaLogic offers a number of SPX modules that provide a variety of standard functions, such as analog input, digital I/O, CANbus controller, and others. These are small boards (1.2” x 3.775”) that can mount on the PC/104 stack, using standard PC/104 stand-offs, or up to two feet away from the base board. For more information, contact VersaLogic at info@VersaLogic.com.

SPI REGISTERS

A set of control and data registers are available for SPI transactions. The following tables describe the SPI control registers (SPICONTROL and SPISTATUS) and data registers (SPIDATA3-0).

SPICONTROL (READ/WRITE) CA8h (or C98h)

D7	D6	D5	D4	D3	D2	D1	D0
CPOL	CPHA	SPILEN1	SPILEN0	MAN_SS	SS2	SS1	SS0

Table 14: SPI Control Register 1 Bit Assignments

Bit	Mnemonic	Description
D7	CPOL	**SPI Clock Polarity –** Sets the SCLK idle state. 0 = SCLK idles low 1 = SCLK idles high
D6	CPHA	**SPI Clock Phase –** Sets the SCLK edge on which valid data will be read. 0 = Data read on rising edge 1 = Data read on falling edge
D5-D4	SPILEN	**SPI Frame Length –** Sets the SPI frame length. This selection works in manual and auto slave select modes. **SPILEN1 SPILEN0 Frame Length** 0 0 8-bit 0 1 16-bit 1 0 24-bit 1 1 32-bit
D3	MAN_SS	**SPI Manual Slave Select Mode –** This bit determines whether the slave select lines are controlled through the user software or are automatically controlled by a write operation to SPIDATA3 (CADh). If MAN_SS = 0, then the slave select operates automatically; if MAN_SS = 1, then the slave select line is controlled manually through SPICONTROL bits SS2, SS1, and SS0. 0 = Automatic, default 1 = Manual
D2-D0	SS	**SPI Slave Select –** These bits select which slave select will be asserted. The SSx# pin on the base board will be directly controlled by these bits when MAN_SS = 1. **SS2 SS1 SS0 Slave Select** 0 0 0 None, port disabled 0 0 1 SPX Slave Select 0, JN4 pin-8 0 1 0 SPX Slave Select 1, JN4 pin-9 0 1 1 SPX Slave Select 2, JN4 pin-10 1 0 0 SPX Slave Select 3, JN4 pin-11 1 0 1 Reserved 1 1 0 Reserved 1 1 1 Reserved

SPISTATUS (READ/WRITE) CA9h (or C99h)

D7	D6	D5	D4	D3	D2	D1	D0
IRQSEL1	IRQSEL0	SPICLK1	SPICLK0	HW_IRQ_EN	LSBIT_1ST	HW_INT	BUSY

Table 15: SPI Control Register 2 Bit assignments

Bit	Mnemonic	Description
D7-D6	IRQSEL	**IRQ Select** – These bits select which IRQ will be asserted when a hardware interrupt from a connected SPI device occurs. The HW_IRQ_EN bit must be set to enable SPI IRQ functionality. **IRQSEL1 IRQSEL0 IRQ** 0 0 IRQ3 0 1 IRQ4 1 0 IRQ5 1 1 IRQ10
D5-D4	SPICLK	**SPI SCLK Frequency –** These bits set the SPI clock frequency. **SPICLK1 SPICLK0 Frequency** 0 0 1.042 MHz 0 1 2.083 MHz 1 0 4.167 MHz 1 1 8.333 MHz
D3	HW_IRQ_EN	**Hardware IRQ Enable** – Enables or disables the use of the selected IRQ (IRQSEL) by an SPI device. 0 = SPI IRQ disabled, default 1 = SPI IRQ enabled **Note:** The selected IRQ is shared with PC/104 ISA bus devices. CMOS settings must be configured for the desired ISA IRQ.
D2	LSBIT_1ST	**SPI Shift Direction** – Controls the SPI shift direction of the SPIDATA registers. The direction can be shifted toward the least significant bit or the most significant bit. 0 = SPIDATA data is left-shifted (MSbit first), default 1 = SPIDATA data is right-shifted (LSbit first)
D1	HW_INT	**SPI Device Interrupt State –** This bit is a status flag that indicates when the hardware SPX signal SINT# is asserted. 0 = Hardware interrupt on SINT# is deasserted 1 = Interrupt is present on SINT# This bit is read-only and is cleared when the SPI device's interrupt is cleared.
D0	BUSY	**SPI Busy Flag** – This bit is a status flag that indicates when an SPI transaction is underway. 0 = SPI bus idle 1 = SCLK is clocking data in and out of the SPIDATA registers This bit is read-only.

SPIDATA0 (READ/WRITE) CAAh (or C9Ah)

D7	D6	D5	D4	D3	D2	D1	D0
MSbit							LSbit

SPIDATA1 (READ/WRITE) CABh (or C9Bh)

D7	D6	D5	D4	D3	D2	D1	D0
MSbit							LSbit

SPIDATA2 (READ/WRITE) CACh (or C9Ch)

D7	D6	D5	D4	D3	D2	D1	D0
MSbit							LSbit

SPIDATA3 (READ/WRITE) CADh (or C90h)

D7	D6	D5	D4	D3	D2	D1	D0
MSbit							LSbit

SPIDATA3 contains the most significant byte (MSB) of the SPI data word. A write to this register will initiate the SPI clock and, if the MAN_SS bit = 0, will also assert a slave select to begin an SPI bus transaction. Increasing frame sizes from 8-bit use the lowest address for the least significant byte of the SPI data word; for example, the LSB of a 24-bit frame would be SPIDATA1. Data is sent according to the LSBIT_1ST setting. When LSBIT_1ST = 0, the MSbit of SPIDATA3 is sent first, and received data will be shifted into the LSbit of the selected frame size set in the SPILEN field. When LSBIT_1ST = 1, the LSbit of the selected frame size is sent first, and the received data will be shifted into the MSbit of SPIDATA3.

Data returning from the SPI target will normally have its most significant data in the SPIDATA3 register. An exception will occur when LSBIT_1ST = 1 to indicate a right-shift transaction. In this case the most significant byte of an 8-bit transaction will be located in SPIDATA0, a 16-bit transaction's most significant byte will be located in SPIDATA1, and a 24-bit transaction's most significant byte will be located in SPIDATA2.

SATA Ports (JN5)

The VL-EPM-35 provides two serial ATA (SATA) ports, which communicate at a rate of up to 3.0 gigabits per second. The SATA connectors at location JN5 are standard 7-pin straight SATA friction latching connectors.

Power to SATA drives is supplied by the ATX power supply. Note that the standard SATA drive power connector is different than the common 4-pin Molex connector used on IDE drives. Most current ATX power supplies provide SATA connectors, and many SATA drives provide both types of power connectors. If the power supply you are using does not provide SATA connectors, adapters are available.

Table 16: SATA Port Pinout (JN5)

JN5 Pin Bottom	JN5 Pin Top	Signal Name	Function
1	8	GND	Ground
2	9	TX+	Transmit +
3	10	TX-	Transmit -
4	11	GND	Ground
5	12	RX-	Receive -
6	13	RX+	Receive +
7	14	GND	Ground

Ethernet Interface (JN6, JS3)

The VL-EPM-35 features two on-board gigabit Ethernet controllers, an Intel 82574IT and an Intel 82541ER. Both controllers provide a standard IEEE 802.3 Ethernet interface for 1000Base-T, 100Base-TX, and 10Base-T applications. The RJ-45 connector JN6 on the top board is controlled by the 82574IT. Connector JS3 on the bottom board is controlled by the 82541ER. The VL-CBR-8006 breakout cable includes an RJ-45 connector.

These interfaces are protected against ESD damage.

While these controllers are not NE2000-compatible, it is widely supported. Drivers are readily available to support a variety of operating systems. See VersaLogic website for latest OS support.

BIOS CONFIGURATION

Both Ethernet controllers use PCI interrupt INTA#. Use CMOS Setup to select the IRQ line routed to each PCI interrupt line.

ETHERNET STATUS LEDS

The JN6 RJ-45 connector has two built-in LEDs to provide an indication of the Ethernet status as shown in the following table.

Table 17: JN6 Ethernet Status LEDs

LED	State	Description
Green/Orange (Link Speed)	Orange	1 Gbps speed
	Green	100 Mbps speed
	Off	10 Mbps speed or cable not plugged into active hub
Yellow (Activity)	On	Activity detected on cable (intermittent with activity)
	Off	No activity detected on cable

On-board LEDs provide an indication of the JS3 Ethernet interfaces, as shown below.

Table 18: JS3 Ethernet Status LEDs

LED	State	Description
Green	On	Active Ethernet cable plugged in
	Off	Active cable not plugged in or cable not plugged into active hub
Yellow	On	Activity detected on cable (intermittent with activity)
	Off	No activity detected on cable

Solid State Drives (JN7, JS2)

MINIBLADE (JN7)

A vertical MiniBlade socket is provided at position JN7 for solid state storage. The MiniBlade interface on the VL-EPM-35 supports only USB devices. The VL-F23 series of MiniBlade devices are available from VersaLogic in sizes of 1 GB, 2 GB, and 4 GB. Contact VersaLogic Sales to order.

EUSB SOLID STATE DRIVE (JS2)

Connector JS2 on the bottom board provides an interface for an eUSB solid state drive (SSD). The VersaLogic VL-F15 series of eUSB SSDs come in sizes of 2 GB and 4 GB, as well as standard and extended temperature ratings. Contact VersaLogic Sales for information. eUSB modules are secured to the board using the VL-HDW-109 hardware kit from VersaLogic. The kit contains one M2.5 x 6mm round aluminum standoff and two M2.5 x 4mm pan head Philips screws.

Video Interface (JN9, JN11)

An on-board video controller integrated into the chipset provides high performance video output for the VL-EPM-35. The VL-EPM-35 can also be operated without video attached. See "Console Redirection."

CONFIGURATION

The VL-EPM-35 uses a shared-memory architecture. It supports two types of video output, SVGA and LVDS Flat Panel Display.

SVGA OUTPUT CONNECTOR (JN11)

See the *Connector Location Diagram* on page 15 for connector location information. An adapter cable, part number VL-CBR-1201, is available to translate JN11 into a standard 15-pin D-Sub SVGA connector.

This connector is protected against ESD damage.

Table 19: Video Output Pinout

JN11 Pin	Signal Name	Function	Mini DB15 Pin
1	GND	Ground	6
2	CRED	Red video	1
3	GND	Ground	7
4	CGRN	Green video	2
5	GND	Ground	8
6	CBLU	Blue video	3
7	GND	Ground	5
8	CHSYNC	Horizontal Sync	13
9	GND	Ground	10
10	CVSYNC	Vertical Sync	14
11	DDC_CLK	DDC Clock Signal	15
12	DDC_DATA	DDC Data Control	12

LVDS FLAT PANEL DISPLAY CONNECTOR (JN9)

The integrated LVDS Flat Panel Display in the VL-EPM-35 is an ANSI/TIA/EIA-644-1995 specification-compliant interface. It can support up to 24 bits of RGB pixel data plus 3 bits of timing control (HSYNC/VSYNC/DE) on the 4 differential data output pairs.

The 3.3V power provided to pins 19 and 20 of JN9 is protected by a 1 Amp fuse.

See the *Connector Location Diagram* on page 15 for connector location information.

Table 20: LVDS Flat Panel Display Pinout

JN9 Pin	Signal Name	Function
1	GND	Ground
2	NC	No Connection
3	LVDSA3	Diff. Data 3 (+)
4	LVDSA3#	Diff. Data 3 (–)
5	GND	Ground
6	LVDSCLK0	Differential Clock (+)
7	LVDSCLK0#	Differential Clock (–)
8	GND	Ground
9	LVDSA2	Diff. Data 2 (+)
10	LVDSA2#	Diff. Data 2 (–)
11	GND	Ground
12	LVDSA1	Diff. Data 1 (+)
13	LVDSA1#	Diff. Data 1 (–)
14	GND	Ground
15	LVDSA0	Diff. Data 0 (+)
16	LVDSA0#	Diff. Data 0 (–)
17	GND	Ground
18	GND	Ground
19	+3.3V	Protected Power Supply
20	+3.3V	Protected Power Supply

COMPATIBLE LVDS PANEL DISPLAYS

The following list of flat panel displays is reported to work properly with the integrated graphics video controller chip used on the VL-EPM-35.

Table 21: Compatible Flat Panel Displays

Manufacture	Model Number	Panel Size	Resolution	Interface	Panel Technology
eVision Displays	xxx084S01 series	8.4”	800 x 600 18-bit	LVDS	TFT
au Optronix	B084SN01	8.4”	800 x 600 18-bit	LVDS	TFT
eVision Displays	xxx104S01 series	10.4”	800 x 600 18-bit	LVDS	TFT
au Optronix	B104SN01	10.4”	800 x 600 18-bit	LVDS	TFT
Sharp	LQ121S1LG411	12.1”	800 x 600 18-bit	LVDS	TFT
eVision Displays*	xxx141X01 series	14.1”	1024 x 768 18-bit	LVDS	TFT

CONSOLE REDIRECTION

The VL-EPM-35 can be operated without using the on-board video output by redirecting the console to a serial communications port. CMOS Setup and some operating systems such as DOS can use this console for user interaction.

Console redirection settings are configured on the Features tab of CMOS Setup. The default setting (On Remote User Detect) causes the console not to be redirected to the serial port unless a signal (a Ctrl-C character) is detected from the terminal. Console redirection can also be set to Always or Never. Notes on console redirection:

- When console redirection is enabled, you can access CMOS Setup by typing Ctrl-C.
- The decision to redirect the console is made early in BIOS execution, and cannot be changed later.
- The redirected console uses 115200 baud, 8 data bits, 1 stop bit, no parity, and no flow control.

Null Modem

The following diagram illustrates a typical DB9 to DB9 RS-232 null modem adapter.

```
System 1    <-->  System 2
Name  Pin         Pin   Name
-----------------------------------
TX    3     <-->  2     RX
RX    2     <-->  3     TX
RTS   7     <-->  1     DCD
CTS   8
DSR   6     <-->  4     DTR
DCD   1     <-->  7     RTS
                  8     CTS
DTR   4     <-->  6     DSR
```

Pins 7 and 8 are shorted together on each connector. Unlisted pins have no connection.

Expansion Bus (JS1, JS7/JS9)

PC/104-*PLUS* – PCI (JS1)

PC/104-*Plus* modules can be secured directly to the bottom of the VL-EPM-35. The bottom board of the VL-EPM-35 set consumes the first slot position on the PC/104-*Plus* stack. Make sure to correctly configure the slot position jumpers on each PC/104-*Plus* module appropriately.

The VL-EPM-35 is compliant with revision 2.3 of the PC/104-*Plus* specification and can support three bus master capable PC/104-*Plus* modules.

The BIOS automatically allocates I/O and memory resources. CMOS Setup may be used to select IRQ assignment.

PC/104 – ISA (JS7/JS9)

The VL-EPM-35 provides full support of the PC/104 (ISA) bus, including support of 16-bit I/O and memory transfers. PC/014 modules can be added to the stack below the VL-EPM-35. Most PC/104 cards will work, but be sure to check the requirements of your PC/104 card against the limitations listed below.

Available I/O Ranges

The following I/O ranges are available on the ISA bus:

- 0x200 – 0x2FF (except 0x208 – 0x20F and any on-board devices assigned in CMOS Setup to the 0x200 – 0x2FF range; see note below)
- 0x300 – 0x37F
- 0x400 – 0x47F
- 0x600 – 0xBFF

Note: By default, Serial Port 2 is assigned to 0x2F8 – 0x2FF in CMOS Setup, but the base address for this device can be moved outside the 0x200 – 0x2FF range. See KnowledgeBase article VT1638 for information on serial port settings in CMOS Setup.

Available Memory Ranges

The following memory range is available on the ISA bus:

- D000:0h – DFFF:Fh

DMA and Bus Master Support

The VL-EPM-35 does not support PC/104 DMA or bus mastering.

80-Pin I/O Connector (JS3)

Connector JS3 provides interfaces for the following VL-EPM-35 ports:

- Parallel port
- Serial ports 1-2
- PS/2 (keyboard and mouse)
- USB (two devices)
- Ethernet

The connector also provides interfaces to a programmable LED, IDE LED, reset button, and external speaker. Table 22 shows the pinout for the cable assembly.

To connect devices to any of these ports, connect the 80-pin connector of the VL-CBR-8006 transition cable to connector JS3 on the VL-EPM-35, then plug the devices into the appropriate connector on the breakout cable. Optionally, you can manufacture a cable based on the pinout information provided for each interface.

All user I/O ports on this connector are protected against ESD damage.

Table 22: 80-Pin I/O Connector Pinout

JS3 Pin	External Connector	Signal
A1	**LPT1**	Strobe
A2	JA	Auto feed
A3	DB-25F	Data bit 1
A4		Printer error
A5		Data bit 2
A6		Reset
A7		Data bit 3
A8		Select input
A9		Data bit 4
A10		Ground
A11		Data bit 5
A12		Ground
A13		Data bit 6
A14		Ground
A15		Data bit 7
A16		Ground
A17		Data bit 8
A18		Ground
A19		Acknowledge
A20		Ground
A21		Port Busy
A22		Ground
A23		Paper End
A24		Ground
A25		Select
A26	**MISC**	No Connect
A27		Programmable LED +
A28		Programmable LED –
A29		Speaker +
A30		Speaker –
A31		IDE Data LED –
A32		IDE Data LED +
A33	**MOUSE**	+5V (Protected)
A34	JB	Mouse Data
A35	6-pin	Ground
A36	Mini-DIN	Mouse Clock
A37	**KBD**	+5V (Protected)
A38	JC	Keyboard Data
A39	6-pin	Ground
A40	Mini-DIN	Keyboard Clock

JS3 Pin	External Connector	Signal
B1	**USB CH0**	+5V (Protected)*
B2	**USB CH1**	Channel 0 Data +
B3	JD	Channel 0 Data –
B4	10-pin	Ground
B5	.1" Male	Cable Shield
B6	Header	Cable Shield
B7		Ground
B8		Channel 1 Data –
B9		Channel 1 Data +
B10		+5V (Protected)*
B11	**ETHERNET**	Bi-directional pair +C
B12	JE	Bi-directional pair -C
B13	8-pin	Bi-directional pair -B
B14	RJ-45	Bi-directional pair +B
B15	Jack	Bi-directional pair +D
B16		Bi-directional pair -D
B17		Bi-directional pair -A
B18		Bi-directional pair +A
B19	**PBRESET**	Pushbutton Reset
B20		Ground
B21	**Serial Port 1**	Data Carrier Detect
B22	JF	Data Set Ready
B23	DB-9M	Receive Data
B24		Request to Send
B25		Transmit Data
B26		Clear to Send
B27		Data Terminal Ready
B28		Ring Indicator
B29		Ground
B30		No Connect
B31	**Serial Port 2**	No Connect
B32	JG	No Connect
B33	DB-9M	Receive Data
B34		Request to Send
B35		Transmit Data
B36		Clear to Send
B37		Ground
B38		No Connect
B39		Ground
B40		No Connect

* The 5V power supplied to pins on this connector is protected by current limiting circuitry.

6 Interrupt Configuration

The VL-EPM-35 has the standard complement of PC type interrupts. Up to six IRQ lines can be allocated as needed to PCI devices. There are no interrupt configuration jumpers. All configuration is handled through CMOS Setup.

Table 23: VL-EPM-35 IRQ Settings

● = default setting ○ = allowed setting

Source	IRQ															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Timer 0	●															
Keyboard		●														
Slave PIC			●													
Serial Port 1				○	●	○		○								
Serial Port 2				●	○	○		○								
Serial Port 3				○	○	○		○								
Serial Port 4				○	○	○		○								
Serial Port 5				○	○	○		○								
Parallel Port							●									
RTC									●							
Mouse													●			
Math Chip														●		
Primary IDE															●	
Secondary IDE																●
LPT1						○		○								
SPX				○	○	○					○					
Fan Tachometer								○								
PCI INTA#						○				○	○	●				
PCI INTB#						○				○	○	●				
PCI INTC#						○				○	○	●				
PCI INTD#						○				●	○	○				
PCI INTE#						○				●	○	○				
PCI INTF#						○				●	○	○				

Table 24: PCI Interrupt Settings

● = default setting ○ = allowed setting

Source	PCI Interrupt					
	INTA#	INTB#	INTC#	INTD#	INTE#	INTF#
82541ER Ethernet	●					
82574IT Ethernet	●					
Audio	●					
SATA		●				
USB EHCI 1					●	
USB EHCI 2			●			
USB UHCI 1					●	
USB UHCI 2						●
USB UHCI 3			●			
USB UHCI 4	●					
USB UHCI 5		●				
USB UHCI 6			●			
Video	●					

Product Code Register

PRODCODE (Read/Write) CA0h (or C90h)

D7	D6	D5	D4	D3	D2	D1	D0
PLED	PC6	PC5	PC4	PC3	PC2	PC1	PC0

Table 25: Product Code Register Bit Assignments

Bit	Mnemonic	Description
D7	PLED	**Light Emitting Diode** — Controls the programmable LED on connector JN2 and JS3. 0 = Turns LED on 1 = Turns LED off
D6-D0	PC	**Product Code** — These bits are hard-coded to represent the product type. The VL-EPMp-34 always reads as 0000001. Other codes are reserved for future products. **PC6 PC5 PC4 PC3 PC2 PC1 PC0 — Product Code** 0 0 0 0 0 0 1 — VL-EPMp-34 and VL-EPM-35 These bits are read-only.

Revision Level Register

REVLEV (Read Only) CA1h (or C91h)

D7	D6	D5	D4	D3	D2	D1	D0
RL4	RL3	RL2	RL1	RL0	EXT	CUST	BETA

Table 26: Revision Level Register Bit Assignments

Bit	Mnemonic	Description
D7-D3	RL	**FPGA Revision Level** — These bits are hard-coded to represent the FPGA revision. Contact VersaLogic Support for further information. These bits are read-only.
D2	EXT	**Extended Temperature** — Indicates operating temperature range. 0 = Standard temperature range 1 = Extended temperature range This bit is read-only.
D1	CUSTOM	**Custom Flag –** Indicates whether this is a custom FPGA. 0 = Standard 1 = Custom This bit is read-only.
D0	REV	**Beta Flag** — Indicates whether this is a Beta product. 0 = Standard 1 = Beta This bit is read-only.

Special Control Register

SCR (Read/Write) CA2h (or C92h)

D7	D6	D5	D4	D3	D2	D1	D0
BIOS_JMP	BIOS_OR	BIOS_SEL	CMOD1	CMOD0	WDOG_STAT	WDOG_RST	Reserved

Table 27: Special Control Register Bit Assignments

Bit	Mnemonic	Description
D7	BIOS_JMP	**System BIOS Selector Jumper Status —** Indicates the status of the system BIOS selector jumper at VN1[1-2]. 0 = Jumper installed – backup system BIOS selected 1 = No jumper installed – primary system BIOS selected This bit is read-only.
D6	BIOS_OR	**BIOS Jumper Override —** Overrides the system BIOS selector jumper and selects the BIOS with BIOS_SEL. 0 = No BIOS override 1 = BIOS override
D5	BIOS_SEL	**BIOS Select —** Selects the system BIOS when BIOS_OR is set. 0 = Backup BIOS selected 1 = Primary BIOS selected
D4-D3	CMOD	**Serial Port 5 Mode —** Sets the operation mode of Serial Port 5. **CMOD1 CMOD0 Serial Port 5 Mode** 0 0 RS-232 0 1 RS-422 1 0 RS-485 1 1 Reserved
D2	WDOG_STAT	**Watchdog Status —** Indicates if the watchdog timer has expired. 0 = Timer has not expired. 1 = Timer has expired. This bit is read-only.
D1	WDOG_RST	**Watchdog Reset Enable —** Enables and disables the watchdog timer reset circuit. 0 = Disables 1 = Enables
D0	Reserved	This bit has no function.

Watchdog Hold Register

WDHOLD (Write Only) CA3h (or C93h)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	0

If the watchdog timer is enabled, software must periodically refresh the watchdog timer at a rate faster than the timer is set to expire (1000 ms minimum). Writing 5Ah to WDHOLD resets the watchdog timeout period.

Fan/Tachometer Control Register

FANTACH (Read/Write) CA4h (or C94h)

D7	D6	D5	D4	D3	D2	D1	D0
SLOWFAN	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	FANINT

Table 28: Fan/Tachometer Control Register Bit Assignments

Bit	Mnemonic	Description
D7	SLOWFAN	**Slow Fan Speed Indicator** – Indicates whether the fan is running below 1 Hz. 0 = Fan is running at or above 1 Hz. 1 = Fan is running below 1 Hz. This bit is read-only.
D6-D1	Reserved	These bits have no function.
D0	FANINT	**Fan Interrupt Enable** — Enables or disables fan interrupt. 0 = Disables fan interrupt 1 = Enables fan interrupt – IRQ7

Appendix A – References



CPU	
Intel Core 2 Duo	Intel Core 2 Duo Datasheet
Chipset	
Intel GS45	Intel GS45 Datasheet
Intel ICH9	Intel ICH9 Datasheet
Ethernet Controller	
Intel 82574IT Ethernet Controller	Intel 82574IT Datasheet
Intel 82541ER Ethernet Controller	Intel 82541ER Datasheet
Super I/O Chip	
SMSC LPC47N217	LPCC47N217 Datasheet
SMSC SCH3114	SCH3114 Datasheet
PC/104-*Plus* Interface	PC/104-*Plus* Specification
General PC Documentation	
The Programmer's PC Sourcebook	Amazon.com
General PC Documentation	
The Undocumented PC	Amazon.com

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