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# Reference Manual

**DOC. REV. 12/29/2006**

# EPM-CPU-6
# EPM-CPU-7

Pentium/K6 and Intel Tillamook processor module with 10/100 Ethernet, Video, and PC/104-Plus interface.






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# EPM-CPU-6
# EPM-CPU-7

Pentium/K6 and Intel Tillamook processor module with 10/100 Ethernet, Video, and PC/104-*Plus* interface

**MEPM-CPU-6**

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# Product Release Notes

This page includes recent changes or improvements that have been made to this product. These changes may affect its operation or physical installation in your application. Please read the following information.

### *Rev 3 Release (EPM-CPU-7 only)*

- BIOS. EPM-CPU-7 with BIOS version 4.3.105
- CPU. EPM-CPU-7 designed to support the Intel Tillamook chip.

### *Rev 2 Release*

- Initial public release.

# Support Page

The **EPM-CPU-6/7 Support Page**, at **http://www.VersaLogic.com/private/panthersupport.asp**, contains additional information and resources for this product including:

- Reference Manual (PDF format)
- Operating system information and software drivers
- Data sheets and manufacturers' links for chips used in this product
- BIOS information and upgrades
- Utility routines and benchmark software

**Note:** This is a private page for EPM-CPU-6/7 users only. It cannot be reached through our web site. You must enter this address directly to find the support page.

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# Model EPM-CPU-6/7

Pentium/K6 and Intel Tillamook processor module
with 10/100 Ethernet,
Video, and PC/104-*Plus* interface

## REFERENCE MANUAL




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# Introduction 1

## Description

The EPM-CPU-6/7 is a performance-oriented processor board in a compact PC/104-Plus format. It is specifically designed for OEM control projects requiring fast processing, compact size, flexible memory options, high reliability, and long product lifespan / availability. It's features include:

- Full Socket 7 CPU Support - to 400 MHz
  - Intel Pentium MMX
  - AMD K6-2 3D
  - AMD K6-2e low power
  - Intel Tillamook (EPM-CPU-7 only)
- 512 KB Level 2 cache
- 8 to 256 MB system RAM
- 10 / 100 dual-speed Ethernet
- PCI based video
  2 MB VRAM on EPM-CPU-6
  4 MB VRAM on EPM-CPU-7
- Flat panel display support
- 32-pin DOC Flash support
- PC/104-*Plus* high speed expansion interface
- PCI based IDE controller
- Dual USB 1.0 interfaces
- 2 COM + 1 LPT port
- Keyboard and PS/2 mouse port
- RS-232/422/485 COM port
- CPU temperature sensor
- Watchdog timer
- Vcc sensing reset circuit
- Flash BIOS with OEM enhancements
- Ethernet Remote boot option
- Single supply (+5V) operation
- Latching I/O connectors
- Customizing available
- Fanless option

The EPM-CPU-6/7 is a complete computer system in a compact two board set. It may be used alone or with expansion modules. It features a PC/104-*Plus* expansion interface for fast PCI-based interface to a wide variety of PC/104 and PC/104-*Plus* stacking modules.

It is fully compatible with popular operating systems including Windows operating systems, QNX, Linux, RT-Linux, OS-9, and other Real Time Operating Systems.

On-board I/O includes 10/100 Mbit Ethernet, CRT / Flat Panel interface, IDE, USB 1.0, two COM and one LPT port. In addition, one of the COM ports is convertible to RS-232/422/485.

Up to 256 MB of low power system RAM is supported in a high-reliability latching 144-pin SODIMM socket. Up to 72 MB of bootable DiskOnChip Flash space is support for non-volatile program and data file storage without the use of mechanical disk drives.



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The high reliability design and construction of this board also features latching I/O connectors, watchdog timer, voltage sensing reset circuit, and self-resetting fuse on the 5V supply to the keyboard, mouse, and USB 1.0 ports. An onboard programmable CPU temperature sensor is included for use in difficult thermal situations. The sensor output can be used to turn on additional fans, create local or remote warnings, or take other action through software triggers.

The EPM-CPU-6/7 delivers both full performance and product longevity by utilizing only standardized components in its design. Features such as full socket 7 compatibility were made possible by its unique 2-board design with PC/104-Plus interconnect. The EPM-CPU-6/7 is designed to mount at the top of a PC/104 stack due to fan / heat sink height. Other configurations are possible depending on the environmental characteristics of the application.

This exceptional processor card was designed from the ground up for OEM applications with longevity and reliability as the focus. It is fully supported by the VersaLogic design team. Both hardware and software (BIOS) customization are available in quantities as low as 25 pieces. Each board is subjected to a 48-hour burn-in and 100% functional testing and backed by a limited two-year warranty.



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# Technical Specifications

*Specifications are typical at 25°C with 5.0V supply unless otherwise noted.*

**Board Size:**
3.55" x 3.775" (PC/104 standard). Two board set.

**Storage Temperature:**
–40° C to 85° C

**Free Air Operating Temperature:**
0° C to +60° C (free air, CPU fan with heatsink attached and operating)

**Power Requirements:** *(with 32 MB SDRAM, keyboard, mouse, running Win95 with Ethernet)*

| | | |
|---|---|---|
| EPM-CPU-6/7bj | 266 MHz K6-2 CPU | 5V ±5% @ 3.30 A (16.5 W) typ. |
| EPM-CPU-6c | 233 MHz Pentium CPU | 5V ±5% @ 3.50 A (17.5 W) typ |
| EPM-CPU-6/7g | 400 MHz K6-2 CPU | 5V ±5% @ 4.25 A (21.3 W) typ. |
| EPM-CPU-6/7h | 266 MHz K6-2E CPU | 5V ±5% @ 2.55 A (12.8 W) typ. |
| EPM-CPU-7s | 266 MHz Tillamook | 5V ±5% @ 1.95 A (9.7 W) typ. |
| EPM-CPU-7t | 266 MHz Tillamook | 5V ±5% @ 2.05 A (10.3 W) typ. |

+3.3V or ±12V may be required by some expansion modules

**System Reset:**
$V_{CC}$ sensing, resets below 4.37V typ. Watchdog timeout

**DRAM Interface:**
One 144-pin SODIMM socket, 8 to 256 MB, EDO (60 ns) or
SDRAM (66 MHz or PC-100 compatible, runs at 66 MHz).

**Flash / BBSRAM Interface:**
One 32-pin JEDEC DIP socket.
Accepts one 8 to 96 MB DiskOnChip device or 512 KB battery-backed static RAM chip. Height limit of 0.0330”

**Video Interface:**

| | |
|---|---|
| EPM-CPU-6: | Based on Intel/C&T 69000 chip. 2 MB VRAM. Resolutions to 1600 x 1200. |
| EPM-CPU-7: | Based on Intel/C&T 69030 chip. 4 MB VRAM. Resolutions to 1600 x 1200 |

44-pin flat panel display interface compatible with common panels.

**IDE Interface:**
One PCI-based IDE channel, 40-pin interface, compatble with enhanced IDE mode 4 and Ultra DMA only.
Supports up to two IDE devices (hard drives, CD-ROM, etc.)

**Floppy Disk Interface:**
Supports two floppy drives

**Ethernet Interface:**
Autodetect 10BaseT/100BaseTX based on AMD 79C973. 12K transmit/receive buffer.

**COM1 Interface:**
RS-232, 16C550 compatible, 115K baud max.

**COM2 Interface:**
RS-232/422/485, 16C550 compatible, 460K baud max.

**LPT Interface:**
Bi-directional/EPP/ECP compatible

**Connectors:**

| | |
|---|---|
| I/O: | Two high-density 80-pin (break out to standard .1" IDC and PC connectors). |
| Video: | 10-pin 2mm SVGA connector,44-pin 2mm FPD connector |
| Power: | 10-pin .1" |

**BIOS:** General Software embedded BIOS with OEM enhancements
Field upgradable with Flash BIOS Upgrade Utility

**Bus Speed:**

| | |
|---|---|
| CPU External: | 66 MHz |
| PCI, PC/104-*Plus*: | 33 MHz |
| PC/104: | 8 MHz |

**Compatibility:**
PC/104 – Full compliance
Embedded-PCI (PC/104-*Plus*) – Full compliance, 3.3V or 5V modules

Specifications are subject to change without notice.



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# Technical Support

If you have problems that this manual can't help you solve, first visit the EPM-CPU-6/7 Product Support web page at **http://www.VersaLogic.com/private/panthersupport.asp**. If you have further questions, contact VersaLogic for technical support at (541) 485-8575. You can also reach our technical support engineers via e-mail at Support@VersaLogic.com.

**EPM-CPU-6/7 Support Website**

*http://www.VersaLogic.com/private/panthersupport.asp*

### REPAIR SERVICE

If your product requires service, you must obtain a Returned Material Authorization (RMA) number by calling (541) 485-8575. Our standard turn-around time for repairs is five working days after we receive the product.

Please provide the following information:

- Your name, the name of your company, and your phone number
- The name of a technician or engineer who we can contact if we have questions
- Quantity of items being returned
- The model and serial number (bar code) of each item.
- A description of the problem
- Steps you have taken to resolve or repeat the problem
- The return shipping address

**Warranty Repair** All parts and labor charges are covered, including return shipping charges for UPS 3rd Day Select delivery to United States addresses.

**Non-warranty Repair** All non-warranty repairs are subject to diagnosis and labor charges, parts charges, and return shipping fees. We will need to know what shipping method you prefer for return back to your facility, and we will need to secure a purchase order number for invoicing the repair.

**Note:** Please mark the RMA number clearly on the outside of the box before returning. Failure to do so can delay the processing of your return.



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# Configuration / Operation 2

## Overview

### ELECTROSTATIC DISCHARGE

***Warning!*** Electrostatic discharge (ESD) can damage boards, disk drives, and other components. The circuit board must be only be handled at an ESD workstation. If an approved station is not available, some measure of protection can be provided by wearing a grounded antistatic wrist strap. Keep all plastic away from the board, and do not slide the board over any surface.

After removing the board from its protective wrapper, place the board on a grounded, static-free surface, component side up. Use an anti-static foam pad if available.

The board should also be protected during shipment or storage by keeping inside a closed metallic anti-static envelope.

**Note:** The exterior coating on some metallic anti-static bags is sufficiently conductive to cause excessive battery drain if the bag comes in contact with the bottom side of the EPM-CPU-6/7.

### LITHIUM BATTERY

***Warning!*** To prevent shorting, premature failure, or damage to the lithium battery, do not place the board on a conductive surface such as metal, black conductive foam, or the outside surface of a metalized ESD protective pouch. The lithium battery may explode if mistreated. Do not recharge, disassemble, or dispose of in fire. Dispose of used batteries promptly.



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# Initial Configuration and Setup

The following list describes the recommended components and gives an abbreviated outline for setting up a typical development system.

### RECOMMENDED COMPONENTS

- EPM-CPU-6/7 Board Set
- 144-pin SODIMM SDRAM Memory Module (66 MHz or PC-100)
- ATX Power Supply
- SVGA Video Monitor
- Keyboard with PS2 connector
- 3.5" Floppy Disk Drive
- IDE Hard Drive
- IDE CD ROM Drive (optional)

### DRAM MODULE

- Insert DRAM module into the SODIMM socket. Latch into place.

### CABLES / PERIPHERAL DEVICES

- Plug video adapter cable (p/n VL-CBL-1007) into socket JN2 and attach video monitor.
- Plug keyboard into socket JS1[JC].
- Plug floppy data connector JS3[JK] into floppy drive.

**Note:** The floppy drive used to boot the system (Drive A) should be connected after the twist in the cable (connector JS3[JK]).

- Plug hard drive data connector JS3[JH] into IDE hard drive.
- Optionally, a CD ROM can be connected to JS3[JJ].
- Plug power supply into JS4.
- Attach power supply cables to external drives.
- Jumper hard drive to operate as a master device.



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# CMOS Setup / Boot Procedure for EPM-CPU-6x

- Turn power on.
- Press the DEL key the instant that video is displayed (during the memory test).
- Verify correct CMOS Setup information as shown below.
- Insert bootable floppy disk into floppy drive.
- Reset computer using push button reset.

**Basic CMOS Configuration**

```
+---------------------------------------------------------------------------+
|               System Bios Setup - Basic CMOS Configuration                |
|          (C) 1999 General Software, Inc. All rights reserved              |
+--------------------------+--------------------+-----------------------+---+
| DRIVE ASSIGNMENT ORDER:  | Date:>Jan 01, 1980 | Typematic Delay  : 250 ms |
| Drive A: Floppy 0        | Time: 00 : 00 : 00 | Typematic Rate   : 30 cps |
| Drive B: (None)          | NumLock:  Disabled | Seek at Boot     : Floppy |
| Drive C: (None)          +--------------------+ Show "Hit Del"   : Enabled |
| Drive D: (None)          | BOOT ORDER:        | Config Box       : Enabled |
| Drive E: (None)          | Boot 1st: Drive A: | F1 Error Wait    : Enabled |
| Drive F: (None)          | Boot 2nd: (None)   | Parity Checking  : (Unused)|
| Drive G: (None)          | Boot 3rd: (None)   | Memory Test Tick : Enabled |
| Drive H: (None)          | Boot 4th: (None)   | Test Above 1 MB  : Disabled|
| Drive I: (None)          | Boot 5th: (None)   | Long Memory Test : (Unused)|
| Drive J: (None)          | Boot 6th: (None)   | Hexadecimal Case : Upper   |
| Drive K: (None)          +--------------------+-----------------+-----------+
| (Loader): (Unused)       | IDE DRIVE GEOMETRY:  Sect  Hds  Cyls | Memory    |
+--------------------------+ Ide 0: Not installed                 |  Base:    |
| FLOPPY DRIVE TYPES:      | Ide 1: Not installed                 |           |
| Floppy 0: 1.44 MB, 3.5"  | Ide 2: Not installed                 |  Ext:     |
| Floppy 1: Not installed  | Ide 3: Not installed                 |           |
+--------------------------+--------------------------------------+-----------+
```

**Custom Configuration**

```
+---------------------------------------------------------------------------+
|              System BIOS Setup - Advanced Configuration                   |
|          (C) 1999 General Software, Inc. All rights reserved              |
+-------------------------------------+-------------------------------------+
| Cache (L1 and L2)          : Enabled| COM1 (03F8) Enable/IRQ    : IRQ4    |
| Ethernet                   : Enabled| COM2 (02F8) Enable/IRQ    : IRQ3    |
| Parallel Port Mode         : SPP    | LPT1 (0378) Enable/IRQ    : IRQ7    |
| I/O Register Base Address  : 0E0h   | External Interrupt        : No IRQ  |
| 32Pin Socket (DOC/BBSRAM)  : Disabled| PC/104 (ISA)              : No IRQ  |
| USB Controller             : Disabled| PC/104 (ISA)              : No IRQ  |
| Interrupt Vector Restore   : 19h & 40h| PC/104 (ISA)              : No IRQ  |
| 32-Bit PCI BIOS Extension  : Enabled| PC/104 (ISA)              : No IRQ  |
| Display Type               : CRT    | IDE 0 PIO Mode            : Auto    |
| CPU Temperature Threshold  : 70C    | IDE 1 PIO Mode            : Auto    |
+-------------------------------------+-------------------------------------+
```

**Shadow Configuration**

```
+---------------------------------------------------------------------------+
|              System BIOS Setup - Shadow/Cache Configuration               |
|          (C) 1999 General Software, Inc. All rights reserved              |
+-------------------------------------+-------------------------------------+
| Shadowing                  : None   | Shadow 16KB ROM at C000   : Enabled |
| Shadow 16KB ROM at C400    : Enabled| Shadow 16KB ROM at C800   : Enabled |
| Shadow 16KB ROM at CC00    : Disabled| Shadow 16KB ROM at D000   : Disabled|
| Shadow 16KB ROM at D400    : Disabled| Shadow 16KB ROM at D800   : Disabled|
| Shadow 16KB ROM at DC00    : Disabled| Shadow 16KB ROM at E000   : Disabled|
| Shadow 16KB ROM at E400    : Disabled| Shadow 16KB ROM at E800   : Disabled|
| Shadow 16KB ROM at EC00    : Disabled| Shadow 64KB ROM at F000   : Enabled |
+-------------------------------------+-------------------------------------+
```

**Note:** Due to changes and improvements in the system BIOS, the information on your monitor may differ from that shown above. Above screen version is Version 4.3.104



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# CMOS Setup / Boot Procedure for EPM-CPU-7x

- Turn power on.
- Press the DEL key the instant that video is displayed (during the memory test).
- Verify correct CMOS Setup information as shown below.
- Insert bootable floppy disk into floppy drive.
- Reset computer using push button reset.

**Basic CMOS Configuration**

```
+--------------------------------------------------------------------------+
|                 System Bios Setup - Basic CMOS Configuration             |
|           (C) 2000 General Software, Inc. All rights reserved            |
+--------------------------+--------------------+--------------------------+
| DRIVE ASSIGNMENT ORDER:  | Date:>Jan 01, 1980 | Typematic Delay  : 250 ms  |
| Drive A: Floppy 0        | Time: 00 : 00 : 00 | Typematic Rate   : 30 cps  |
| Drive B: (None)          | NumLock:  Disabled | Seek at Boot     : None    |
| Drive C: (None)          +--------------------+ Show "Hit Del"   : Enabled |
| Drive D: (None)          | BOOT ORDER:        | Config Box       : Enabled |
| Drive E: (None)          | Boot 1st: Drive A: | F1 Error Wait    : Enabled |
| Drive F: (None)          | Boot 2nd: (None)   | Parity Checking  : (Unused)|
| Drive G: (None)          | Boot 3rd: (None)   | Memory Test Tick : Enabled |
| Drive H: (None)          | Boot 4th: (None)   | Test Above 1 MB  : Disabled|
| Drive I: (None)          | Boot 5th: (None)   | Debug Breakpoints: (Unused)|
| Drive J: (None)          | Boot 6th: (None)   | Splash Screen    : Disabled|
| Drive K: (None)          +--------------------+-----------------+-----------+
| (Loader): (Unused)       | IDE DRIVE GEOMETRY:  Sect  Hds  Cyls | Memory    |
+--------------------------+ Ide 0: Not installed                 |  Base:    |
| FLOPPY DRIVE TYPES:      | Ide 1: Not installed                 |   640KB   |
| Floppy 0: 1.44 MB, 3.5"  | Ide 2: Not installed                 |  Ext:     |
| Floppy 1: Not installed  | Ide 3: Not installed                 |   15MB    |
+--------------------------+--------------------------------------+-----------+
```

**Custom Configuration**

```
+--------------------------------------------------------------------------+
|                 System BIOS Setup - Custom Configuration                 |
|           (C) 2000 General Software, Inc. All rights reserved            |
+--------------------------------------+-----------------------------------+
| Cache (L1 and L2)         : Enabled  | COM1 (03F8) Enable/IRQ   : IRQ4   |
| Ethernet                  : Enabled  | COM2 (02F8) Enable/IRQ   : IRQ3   |
| Parallel Port Mode        : SPP      | LPT1 (0378) Enable/IRQ   : IRQ7   |
| I/O Register Base Address : 0E0h     | External Interrupt       : No IRQ |
| DiskOnChip                : Disabled | PCI INTA                 : IRQ11  |
| USB Controller            : Disabled | PCI INTB                 : IRQ11  |
| Interrupt Vector Restore  : Disabled | PCI INTC                 : IRQ11  |
| BIOS Extension            : Disabled | PCI INTD                 : IRQ11  |
| Display Type              : CRT      | IDE 0 PIO Mode           : Auto   |
| CPU Temperature Monitor   : 70 C     | IDE 1 PIO Mode           : Auto   |
+--------------------------------------+-----------------------------------+
```

**Shadow Configuration**

```
+--------------------------------------------------------------------------+
|                 System BIOS Setup - Shadow/Cache Configuration           |
|           (C) 2000 General Software, Inc. All rights reserved            |
+--------------------------------------+-----------------------------------+
| Shadowing                 : >Chipset | Shadow 16KB ROM at C000  : Disabled|
| Shadow 16KB ROM at C400   : Disabled | Shadow 16KB ROM at C800  : Disabled|
| Shadow 16KB ROM at CC00   : Disabled | Shadow 16KB ROM at D000  : Disabled|
| Shadow 16KB ROM at D400   : Disabled | Shadow 16KB ROM at D800  : Disabled|
| Shadow 16KB ROM at DC00   : Disabled | Shadow 16KB ROM at E000  : Disabled|
| Shadow 16KB ROM at E400   : Disabled | Shadow 16KB ROM at E800  : Disabled|
| Shadow 16KB ROM at EC00   : Disabled | Shadow 64KB ROM at F000  : Enabled |
+--------------------------------------+-----------------------------------+
```

**Note:** Due to changes and improvements in the system BIOS, the information on your monitor may differ from that shown above. Above screen version is Version 4.3.105



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# Operating System Installation

The standard PC architecture used on the EPM-CPU-6/7 makes the installation and use of most of the standard x86 processor-based operating systems simple. The operating systems listed on the VersaLogic OS Compatibility Chart (http://www.versalogic.com/kb/KB.asp?KBID=1487) use the standard installation procedures provided by the maker of the OS. Special optimized hardware drivers for a particular operating system, or a link to the drivers, are available at the EPM-CPU-6/7 support web page: http://www.VersaLogic.com/private/panthersupport.asp.

# Creating a Bootable DOS DiskOnChip

The DiskOnChip is shipped pre-formatted, non-bootable, without any files on it. The DiskOnChip will appear as Drive D in systems with an installed hard drive. If a hard drive is not installed, the DOC will appear as Drive C:

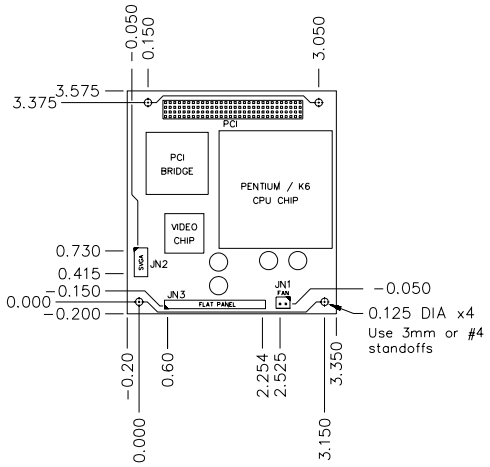
1. Boot your system under DOS or Windows (if using Windows, start a DOS session)
2. Type SYS C: (or SYS D: if appropriate)



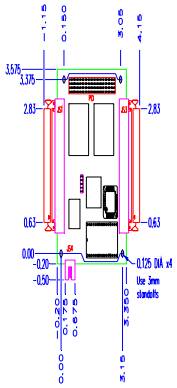
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# Physical Dimensions

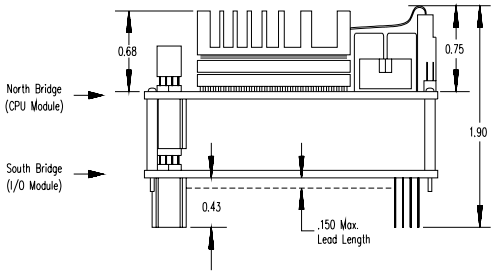
The EPM-CPU-6/7 is a two board set consisting of a CPU Module (North Bridge) and an I/O Module (South Bridge). Dimensions are given below to help with pre-production planning and layout.



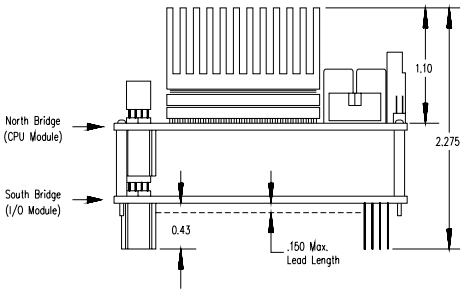

**CPU Module (North Bridge)**



**I/O Module (South Bridge)**




**Overall Height (Both Cards)**




**Overall Height (Fanless Model)**

**Figure 1. Dimensions**

*(Not to scale. All dimensions in inches.)*



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### HARDWARE ASSEMBLY

The EPM-CPU-6/7 consists of two boards which are mounted together with eight 5mm x 15mm M3 threaded hex male/female standoffs (p/n VL-HDW-101) using the corner mounting holes. These standoffs are secured to the top circuit board using four pan head screws.

***Caution*** Extreme care must be taken not to damage components near the corner mounting holes when tightening standoffs with nut driver tools.

Additional PC/104-*Plus* or PC/104 cards can be attached to the bottom of the EPM-CPU-6/7 board set and secured with standoffs or 5mm nuts.

PC/104-*Plus* expansion modules can be secured directly to the underside of the EPM-CPU-6/7.

PC/104 expansion modules can be secured to the underside of the EPM-CPU-6/7, however, the 40-pin and 64-pin ISA feedthrough connectors may need to be extended, and longer standoffs might need to be used to provide adequate clearance between the PCI connector and the components on the top side of the PC/104 module.

The entire assembly can sit on a table top or it can be secured to a base plate. When bolting the unit down, make sure to secure all four standoffs to the mounting surface to prevent circuit board flexing. Refer to the drawing on page 11 for dimensional details.

An extractor tool is available (part number VL-HDW-201) to separate the modules from the stack.

### STACK ARRANGEMENT

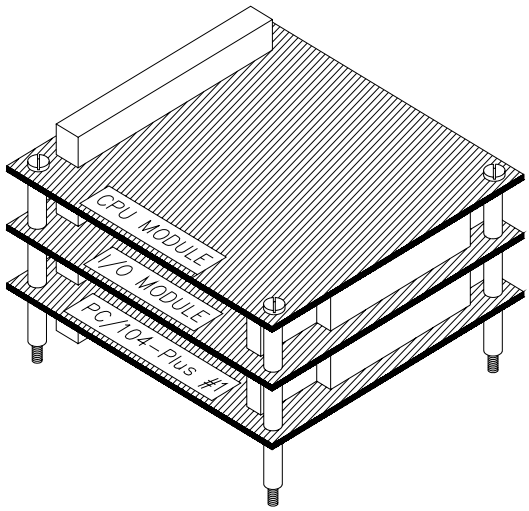



**Figure 2. PC/104-*Plus* Card Added to Bottom of Stack**



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# External Connectors

## CONNECTOR LOCATION DIAGRAMS

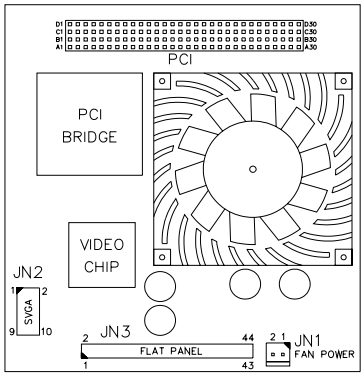



**Figure 3. Connector Location Diagram (CPU Module)**

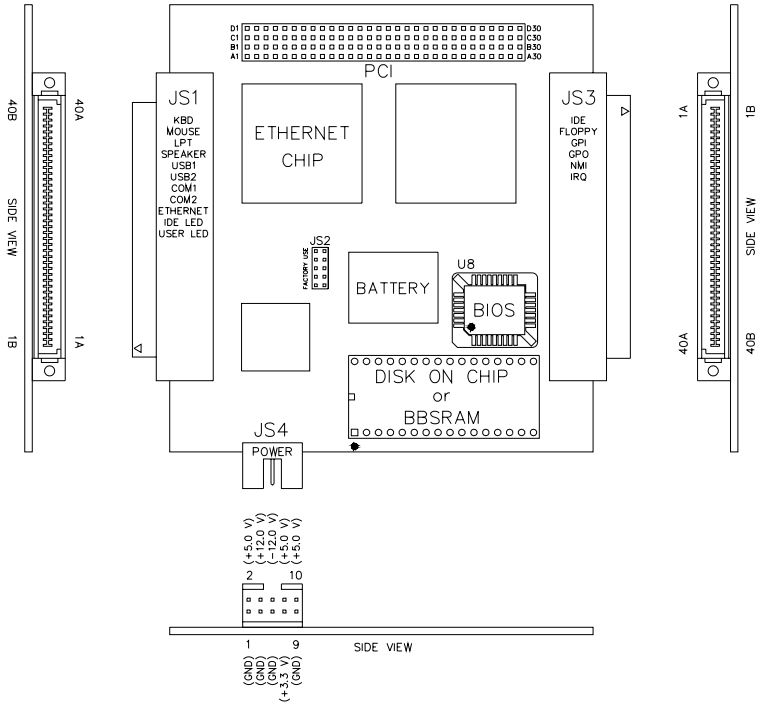



**Figure 4. Connector Location Diagram (I/O Module)**



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## CONNECTOR FUNCTIONS AND INTERFACE CABLES

The table below notes the function of each connector, as well as mating connectors and cables, and the page where a detailed pinout or further information is available.

**Table 1: Connector Functions and Interface Cables**

| Connector | Function | Mating Connector | Transition Cable | Cable Description | Page |
|---|---|---|---|---|---|
| JN1 | Fan Power Output (+5V) | Molex 22-01-3027 or Molex 22-01-2025 | Provided with fan assembly | — | 22 |
| JN2 | SVGA Video Output | Samtec TCSD-05-12.00-01 ‡ | VersaLogic VL-CBL-1007 | | 32 |
| JN3 | Flat Panel Interface | Adam Tech 2CH-A2-44<br>Adam Tech 2CTA* | — | Contact Factory | 33 |
| JS1 | Keyboard, Mouse, LPT1, Speaker, USB1, USB2, COM1, COM2, Ethernet, IDE Data LED, Programmable LED | Robinson-Nugent P50E-080S-TG | VersaLogic VL-CBL-8001 | Breakout to standard PC device connectors | 20 |
| JS2 | PLD Reprogramming Port *(Factory use Only)* | — | — | — | — |
| JS3 | IDE0, Floppy, General Purpose Input, General Purpose Output, NMI, IRQ | Robinson-Nugent P50E-080S-TG | VersaLogic VL-CBL-8002 | Breakout to standard PC device connectors | 35 |
| JS4 | Main Power Input | Berg 69176-010 (Housing) + Berg 47715-000 (Pins) | VersaLogic VL-CBR-1008 | Interface from industry standard ATX power supply | 20 |

* **Note:** This connector is a 2.00mm housing and crimp terminal, discrete wire style. Number of crimp terminals depends upon flat panel display model being used. Insulation displacement connector (IDC) for ribbon cable not recommended due to lack of clearance between connector JN3 and jumper header VN3.

‡ **Note:** The 12.00 in this part number specifies cable length. This part number has a 12" cable attached to the 10-pin 2mm connector.



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### HIGH DENSITY 80-PIN CABLE (JS1)

Cable assembly VL-CBL-8001 is used to break-out this high density connector into standard PC I/O connectors. This chart shows the pinout for the cable assembly.

**Table 2: JS1 High Density 80-Pin Connector Pinout**

| JS1 Pin | External Connector | Pin | Signal |
|---|---|---|---|
| 1A | **LPT1** | 1 | Strobe |
| 2A | JA | 14 | Auto feed |
| 3A | | 2 | Data bit 1 |
| 4A | | 15 | Printer error |
| 5A | | 3 | Data bit 2 |
| 6A | | 16 | Reset |
| 7A | | 4 | Data bit 3 |
| 8A | | 17 | Select input |
| 9A | | 5 | Data bit 4 |
| 10A | | 18 | Ground |
| 11A | | 6 | Data bit 5 |
| 12A | | 19 | Ground |
| 13A | | 7 | Data bit 6 |
| 14A | | 20 | Ground |
| 15A | | 8 | Data bit 7 |
| 16A | | 21 | Ground |
| 17A | | 9 | Data bit 8 |
| 18A | | 22 | Ground |
| 19A | | 10 | Acknowledge |
| 20A | | 23 | Ground |
| 21A | | 11 | Port Busy |
| 22A | | 24 | Ground |
| 23A | | 12 | Paper End |
| 24A | | 25 | Ground |
| 25A | | 13 | Select |
| 26A | **MISC** | — | No Connect |
| 27A | | — | Programmable LED+ |
| 28A | | — | Programmable LED– |
| 29A | | — | Speaker + |
| 30A | | — | Speaker – |
| 31A | | — | IDE Data LED– |
| 32A | | — | IDE Data LED+ |
| 33A | **MOUSE** | 4 | +5V (Protected) |
| 34A | JB | 1 | Mouse Data |
| 35A | | 3 | Ground |
| 36A | | 5 | Mouse Clock |
| 37A | **KBD** | 4 | +5V (Protected) |
| 38A | JC | 1 | Keyboard Data |
| 39A | | 3 | Ground |
| 40A | | 5 | Keyboard Clock |

| JS1 Pin | External Connector | Pin | Signal |
|---|---|---|---|
| 1B | **USB CH0** | 1 | +5V (Protected) |
| 2B | JD | 6 | Ground |
| 3B | | 2 | Channel 0 Data – |
| 4B | | 7 | Cable Shield |
| 5B | | 3 | Channel 0 Data + |
| 6B | | 8 | Channel 1 Data + |
| 7B | | 4 | Cable Shield |
| 8B | | 9 | Channel 1 Data – |
| 9B | | 5 | Ground |
| 10B | | 10 | +5V (Protected) |
| 11B | **ETHERNET** | 4 | Isolated Ground |
| 12B | JE | 5 | Isolated Ground |
| 13B | | 6 | Receive Data – |
| 14B | | 3 | Receive Data + |
| 15B | | 7 | Isolated Ground |
| 16B | | 8 | Isolated Ground |
| 17B | | 2 | Transmit Data – |
| 18B | | 1 | Transmit Data + |
| 19B | **PBRESET** | — | Pushbutton Reset |
| 20B | | — | Ground |
| 21B | **COM1** | 1 | Data Carrier Detect |
| 22B | JF | 6 | Data Set Ready |
| 23B | | 2 | Receive Data |
| 24B | | 7 | Request to Send |
| 25B | | 3 | Transmit Data |
| 26B | | 8 | Clear to Send |
| 27B | | 4 | Data Terminal Ready |
| 28B | | 9 | Ring Indicator |
| 29B | | 5 | Ground |
| 30B | | — | No Connect |
| 31B | **COM2** | 1 | Data Carrier Detect |
| 32B | JG | 6 | Data Set Ready |
| 33B | | 2 | Receive Data |
| 34B | | 7 | Request to Send |
| 35B | | 3 | Transmit Data |
| 36B | | 8 | Clear to Send |
| 37B | | 4 | Data Terminal Ready |
| 38B | | 9 | Ring Indicator |
| 39B | | 5 | Ground |
| 40B | | — | No Connect |



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### HIGH DENSITY 80-PIN CABLE (JS3)

Cable assembly VL-CBL-8002 is used to break-out this high density connector into standard PC I/O connectors. This chart shows the pinout for the cable assembly.

**Table 3: JS3 High Density 80-Pin Connector Pinout**

| JS3 Pin | External Connector | Pin | Signal |
|---|---|---|---|
| 1A | **IDE CH0** | 1 | Reset |
| 2A | JH/JJ | 2 | Ground |
| 3A | | 3 | Data bit 7 |
| 4A | | 4 | Data bit 8 |
| 5A | | 5 | Data bit 6 |
| 6A | | 6 | Data bit 9 |
| 7A | | 7 | Data bit 5 |
| 8A | | 8 | Data bit 10 |
| 9A | | 9 | Data bit 4 |
| 10A | | 10 | Data bit 11 |
| 11A | | 11 | Data bit 3 |
| 12A | | 12 | Data bit 12 |
| 13A | | 13 | Data bit 2 |
| 14A | | 14 | Data bit 13 |
| 15A | | 15 | Data bit 1 |
| 16A | | 16 | Data bit 14 |
| 17A | | 17 | Data bit 0 |
| 18A | | 18 | Data bit 15 |
| 19A | | 19 | Ground |
| 20A | | 20 | No connection |
| 21A | | 21 | No connection |
| 22A | | 22 | Ground |
| 23A | | 23 | I/O write |
| 24A | | 24 | Ground |
| 25A | | 25 | I/O read |
| 26A | | 26 | Ground |
| 27A | | 27 | I/O Channel Ready |
| 28A | | 28 | No connection |
| 29A | | 29 | No connection |
| 30A | | 30 | Ground |
| 31A | | 31 | IRQ14 |
| 32A | | 32 | Drive 16-bit I/O |
| 33A | | 33 | Address bit 1 |
| 34A | | 34 | No connection |
| 35A | | 35 | Address bit 0 |
| 36A | | 36 | Address bit 2 |
| 37A | | 37 | Chip select 0 |
| 38A | | 38 | Chip select 1 |
| 39A | | 39 | Light Emitting Diode – |
| 40A | | 40 | Ground |

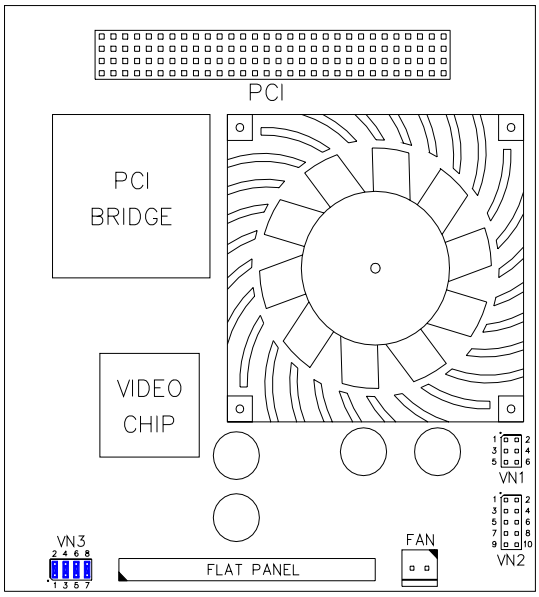
| JS3 Pin | External Connector | Pin | Signal |
|---|---|---|---|
| 1B | **FLOPPY** | 1 | Ground |
| 2B | JK/JL | 2 | Load Head |
| 3B | | 3 | Ground |
| 4B | | 4 | No Connection |
| 5B | | 5 | Ground |
| 6B | | 6 | No Connection |
| 7B | | 7 | Ground |
| 8B | | 8 | Beginning Of Track |
| 9B | | 9 | Ground |
| 10B | | 10 | Motor Enable 1 |
| 11B | | 11 | Ground |
| 12B | | 12 | Drive Select 0 |
| 13B | | 13 | Ground |
| 14B | | 14 | Drive Select 1 |
| 15B | | 15 | Ground |
| 16B | | 16 | Motor Enable 0 |
| 17B | | 17 | Ground |
| 18B | | 18 | Direction Select |
| 19B | | 19 | Ground |
| 20B | | 20 | Motor Step |
| 21B | | 21 | Ground |
| 22B | | 22 | Write Data Strobe |
| 23B | | 23 | Ground |
| 24B | | 24 | Write Enable |
| 25B | | 25 | Ground |
| 26B | | 26 | Track 0 Indicator |
| 27B | | 27 | Ground |
| 28B | | 28 | Write Protect |
| 29B | | 29 | Ground |
| 30B | | 30 | Read Data |
| 31B | | 31 | Ground |
| 32B | | 32 | Head Select |
| 33B | | 33 | Ground |
| 34B | | 34 | Drive Door Open |
| 35B | **MISC** | 1 | Ground |
| 36B | JM | 2 | +5V (Protected) |
| 37B | | 3 | General Purpose Output |
| 38B | | 4 | General Purpose Input |
| 39B | | 5 | Non Maskable Interrupt |
| 40B | | 6 | Interrupt Request Input |



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# Jumper Block Locations

**Note:** Jumpers shown in as-shipped configuration.




| EPM-CPU-6b | EPM-CPU-6c | EPM-CPU-6g<br>EPM-CPU-7g | EPM-CPU-6h<br>EPM-CPU-6j<br>EPM-CPU-7h<br>EPM-CPU-7j | EPM-CPU-7s<br>EPM-CPU-7t | |
|---|---|---|---|---|---|
| 266 MHz | 233 MHz | 400 MHz | 266 MHz | 266 MHz | |
| 1 2<br>3 4<br>5 6 | 1 2<br>3 4<br>5 6 | 1 2<br>3 4<br>5 6 | 1 2<br>3 4<br>5 6 | 1 2<br>3 4<br>5 6 | VN1 |
| 1 2<br>3 4<br>5 6<br>7 8<br>9 10 | 1 2<br>3 4<br>5 6<br>7 8<br>9 10 | 1 2<br>3 4<br>5 6<br>7 8<br>9 10 | 1 2<br>3 4<br>5 6<br>7 8<br>9 10 | 1 2<br>3 4<br>5 6<br>7 8<br>9 10 | VN2 |

**Figure 5. Jumper Block Locations (CPU Module)**

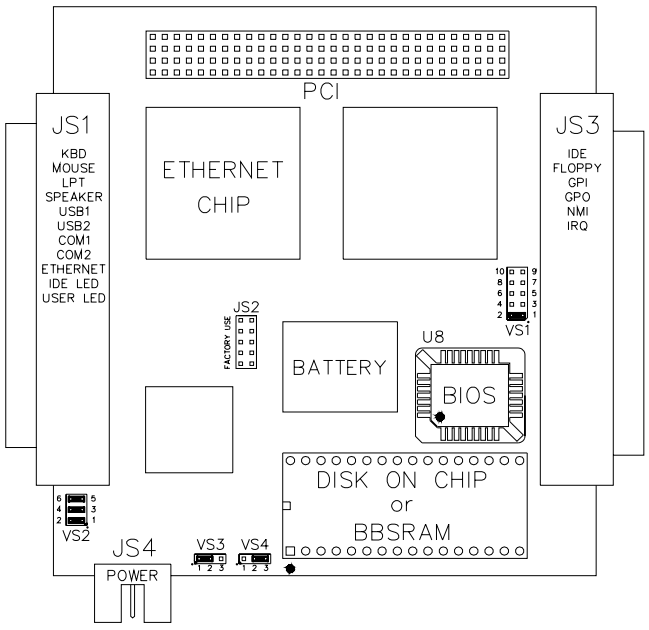



**Figure 6. Jumper Block Locations (I/O Module)**



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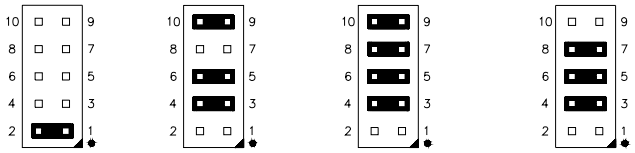
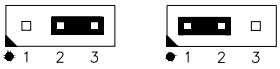
## JUMPER SUMMARY

**Table 4: Jumper Summary**

| Jumper Block | Description | As Shipped | Page |
|---|---|---|---|
| VN1 | **CPU Clock Speed Multiplier**<br>**VN1[5-6] / VN1[3-4] / VN1[1-2] / Multiplier / Speed**<br>Out / Out / In / 6.0 / 400 MHz<br>Out / In / In / 2.5 / 166 MHz<br>Out / In / Out / 3.0 / 200 MHz<br>Out / Out / Out / 3.5 / 233 MHz<br>In / Out / In / 4.0 / 266 MHz<br>Out / In / In / 4.0 / 266 MHz*<br>In / In / In / 4.5 / 300 MHz<br>In / In / Out / 5.0 / 333 MHz<br>In / Out / Out / 5.5 / 366 MHz<br>**Note: For the Intel Tillamook 266 MHz CPU chips only.* | Varies | 22 |
| VN2 | **CPU Core Voltage Selection**<br>**VN2[9-10] / VN2[7-8] / VN2[5-6] / VN2[3-4] / VN2[1-2] / Voltage**<br>In / In / Out / In / Out / 1.80 V<br>**In / In / Out / In / In / 1.85 V**<br>In / In / In / Out / Out / 1.90 V<br>In / In / In / Out / In / 1.95 V<br>In / In / In / In / Out / 2.00 V<br>In / In / In / In / In / 2.05 V<br>Out / Out / Out / Out / Out / 2.00 V<br>Out / Out / Out / Out / In / 2.10 V<br>**Out / Out / Out / In / Out / 2.20 V**<br>Out / Out / Out / In / In / 2.30 V<br>**Out / Out / In / Out / Out / 2.40 V**<br>Out / Out / In / Out / In / 2.50 V<br>Out / Out / In / In / Out / 2.60 V<br>Out / Out / In / In / In / 2.70 V<br>**Out / In / Out / Out / Out / 2.80 V**<br>Out / In / Out / Out / In / 2.90 V<br>Out / In / Out / In / Out / 3.00 V<br>Out / In / Out / In / In / 3.10 V<br>Out / In / In / Out / Out / 3.20 V<br>Out / In / In / Out / In / 3.30 V<br>Out / In / In / In / Out / 3.40 V<br>Out / In / In / In / In / 3.50 V<br>***Note:*** *Do not confuse CPU Core Voltage with CPU I/O voltage. The EPM-CPU-6/7 will only work with CPU chips with an I/O voltage of 3.3V.* | Varies | 22 |
| VN3 | **Flat Panel Selection**<br>**VN3[7-8] / VN3[5-6] / VN3[3-4] / VN3[1-2] / Number / Type**<br>In / In / In / In / — / —<br>In / In / In / Out / 1 / 1024x768 Dual Scan STN Color<br>In / In / Out / In / 2 / 128x1024 TFT Color<br>In / In / Out / Out / 3 / 640x480 Dual Scan STN Color<br>In / Out / In / In / 4 / 800x600 Dual Scan STN Color<br>In / Out / In / Out / 5 / 640x480 Sharp TFT Color<br>In / Out / Out / In / 6 / 640x480 18-bit TFT Color<br>In / Out / Out / Out / 7 / 1024x768 TFT Color<br>Out / In / In / In / 8 / 800x600 TFT Color<br>Out / In / In / Out / 9 / 800x600 TFT Color<br>Out / In / Out / In / 10 / 800x600 TFT Color<br>Out / In / Out / Out / 11 / 800x600 Dual Scan STN Color<br>Out / Out / In / In / 12 / 800x600 Dual Scan STN Color<br>Out / Out / In / Out / 13 / 1024x768 TFT Color<br>Out / Out / Out / In / 14 / 1280x1024 Dual Scan STN Color<br>Out / Out / Out / Out / 15 / 1024x600 Dual Scan STN Color | — | — |



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| Jumper Block | Description | As Shipped | Page |
|---|---|---|---|
| VS1 | **COM2 Configuration**<br>RS-232 RS-422 RS-485 Endpoint Station RS-485 Intermediate Station<br> | RS-232 | 26 |
| VS2[1-2] | **System BIOS Selector**<br>In — Primary System BIOS occupies F0000h to FFFFFh<br>Out — Secondary System BIOS occupies F0000h to FFFFFh<br>***Note:*** *The secondary System BIOS is field upgradable using the BIOS upgrade utility. See www.VersaLogic.com/private/panthersupport.asp for further information.* | In | — |
| VS2[3-4] | **Video BIOS Selector**<br>In — Primary Video BIOS occupies C0000h to C9FFFh<br>Out — Secondary Video BIOS occupies C0000h to C9FFFh<br>***Note:*** *The secondary System BIOS is field upgradable using the BIOS upgrade utility. See www.VersaLogic.com/private/panthersupport.asp for further information.* | In | — |
| VS2[5-6] | **General Purpose Input Bit**<br>In — Bit D1 in SCR register reads as 1<br>Out — Bit D1 in SCR register reads as 0 | In | 35,39 |
| VS3 | **32-Pin DIP Memory Socket Device Type Selector**<br>BBSRAM DOC<br><br>***Note:*** *The 32-pin socket must be enabled in CMOS Setup.* | DOC | 25 |
| VS4 | **CMOS RAM and Real Time Clock Erase**<br>Normal Operation Erase<br><br>***Note:*** *Do not operate the board with the jumper in the erase position. Leave the jumper in position VS4[1-2] for at least one full minute to fully erase CMOS RAM.* | Normal | 23 |



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# Power Supply

### POWER CONNECTORS

Main power is applied to the *EPM-CPU-6/7* through a 10-pin polarized connector. Mating connector Berg 69176-010 (Housing) + Berg 47715-000 (Pins).

See page 13 for connector location information.

***Warning!*** To prevent severe and possibly irreparable damage to the system, it is critical that the power connectors be wired correctly. Make sure to use all three +5VDC pins and all four ground pins to prevent excess voltage drop.

**Table 5: Main Power Connector Pinout**

| JS4 Pin | Signal Name | Description |
|---|---|---|
| 1 | Ground | Ground |
| 2 | +5VDC | Power Input |
| 3 | Ground | Ground |
| 4 | +12VDC | Power Input |
| 5 | Ground | Ground |
| 6 | –12VDC | Power Input |
| 7 | +3.3VDC | Power Input |
| 8 | +5VDC | Power Input |
| 9 | Ground | Ground |
| 10 | +5VDC | Power Input |

**Note:** The +3.3VDC, +12VDC, and –12VDC inputs are only required for expansion modules that require these voltages.



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### POWER REQUIREMENTS

The *EPM-CPU-6/7* only requires +5 volts (±5%) for proper operation. The voltage required for the RS-232 ports and analog input sections are generated with an on-board DC/DC converter. A variable low-voltage supply circuit provides power to the CPU and other on-board devices.

The exact power requirement of the *EPM-CPU-6/7* depends on several factors, including memory configuration, CPU speed, peripheral connections, type and number of expansion modules, and attached devices. For example, PS/2 keyboards typically draw their power directly from the *EPM-CPU-6/7*, and driving long RS-232 lines at high speed can increase power demand.

### LITHIUM BATTERY

***Warning!*** To prevent shorting, premature failure, or damage to the lithium battery, do not place the unit on a conductive surface such as metal, black conductive foam, or the outside surface of a metalized ESD protective pouch. The lithium battery may explode if mistreated. Do not recharge, disassemble, or dispose of in fire. Dispose of used batteries promptly.

Normal battery voltage should be at least 3.0V. If the voltage drops below 3.0V, contact the factory for a replacement (part number T-HB3/5-2). Life expectancy under normal use is approximately 10 years.



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# CPU

### CPU Clock Speed Multiplier

Jumper block VN1 is used to multiply the on-board 66 MHz bus clock to match the internal clock speed of the CPU chip. For example, the 200 MHz CPU shown shown below uses a multiplier of 3.0

See page 17 for jumper configuration details.

### CPU Core Voltage Selection

Jumper block VN2 is used to program a variable output voltage regulator to match the $V_{CORE}$ power supply requirements of the CPU chip.

### Heat Sink

A heat sink and cooling fan must be in place whenever power is applied to the CPU. The fan connects to header JN1 for power.

**Table 6: Fan Power Connector**

| JN1 Pin | Signal Name | Function |
|---|---|---|
| 1 | GND | Ground |
| 2 | +5V | Fan Power |

**Note:** A fan is not required for the low-power K6-2E model (h version) or Intel Tillamook (s version) models.

### L2 Cache Memory

No configuration is required for the L2 Cache memory. The *EPM-CPU-6/7* is shipped with 512 MB of cache memory.

# System RAM

### Compatible Memory Modules

The *EPM-CPU-6/7* will accept one 144-pin SODIMM memory module with the following characteristics:

- Storage Capacity 8 to 256 MB
- Voltage 3.3 Volt
- Error Detection Not supported
- Error Correction Not supported
- Type EDO, 60 ns or SDRAM, 66 MHz or PC-100



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# CMOS RAM

### CLEARING CMOS RAM

Jumper VS4 can be moved to position [1-2] for 30 seconds to erase the contents of the CMOS RAM. Be sure to move the jumper back to position [2-3] for normal operation.

**Note:** Operation with the jumper in the erase position [1-2] will cut-off all battery power to the CMOS RAM and Real Time Clock chip. The board will operate in this condition, however, this will force the board to use the factory default parameters as shown on page 7. For custom programming of the Factory Default Parameters, please contact the Customization Department at VersaLogic.

### DEFAULT CMOS RAM SETUP VALUES

After the CMOS RAM is cleared, the system will load default CMOS RAM parameters the next time the board is powered on. The default CMOS RAM setup values will be used in order to boot the system whenever the main CMOS RAM values are blank, or when the system battery is dead or has been removed from the board.

### USER DEFAULT CMOS RAM SETUP VALUES

Jumper V9 determines whether the factory defined default values, or a set of user default values are loaded when CMOS RAM values are corrupted or blank. In order for a custom (user defined) set of values to be used as the backup (default) CMOS RAM values, it is necessary to:

1. Use CMOS Setup to configure the CMOS RAM values exactly the way you want them to be permanently stored
2. Select "Save CMOS Settings to FLASH" on the main CMOS Setup screen.
3. Remove jumper V9[1-2]

# Real Time Clock

The *EPM-CPU-6/7* features a year 2000 compliant, battery-backed 146818 compatible real time clock/calendar chip. Under normal battery conditions, the clock will maintain accurate timekeeping functions during periods when the board is powered off.

### SETTING THE CLOCK

The CMOS Setup utility (accessed by pressing the [DEL] key during a system boot) can be used to set the time/date of the real time clock.



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# Battery Backed Static RAM

A 32-pin socket (U9 on the I/O module) will accept a battery-backed static RAM chip for non-volatile storage. We recommend using the Dallas 128Kx8 DS1645 series or the 512Kx8 DS1650/DS1250 series memory devices. They need to be a 32-pin, 0.6" DIP, 200nS or faster part. Make sure that jumper VS3 is in the [2-3] position, and the socket is enabled in CMOS Setup.



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# Disk on Chip

A 32-pin socket (U9 on the I/O module) will accept an M-Systems DiskOnChip (DOC) Flash Disk for non-volatile, read/write data storage. The DOC can be configured as a boot device

### ENABLE / DISABLE

The DOC can be enabled or disabled through CMOS Setup by going into the Advanced Configuration screen and setting "32 Pin Socket" to "DOC" or "Disabled". When enabled, the DOC appears in the upper memory region as an 8K page frame from CE000h to CFFFFh.

When disabled, this memory range is freed up for other devices to use.

### COMPATIBLE DEVICES

Any 5 Volt, M-Systems series rev 1.10 or later DOC device will work.

**Note:** DOC chips used must be low profile.

### INSTALLING THE DOC CHIP

1. Align pin 1 on the DOC with pin 1 of socket U9 on the I/O module.
2. Push the DOC into the socket carefully until it is fully seated.
3. Make sure jumper VS3[1-2] is installed.

***Warning!*** ***The DOC will be permanently damaged if installed incorrectly!*** When installing or removing the DOC, be sure to align pin-1 on the the chip with pin-1 on the socket. To prevent electrostatic damage, first touch a grounded surface to discharge any static electricity from your body.

### CMOS SETUP

To enable the DOC as drive C on a system without a hard disk, set the CMOS setup of drive C to “not installed”, and reboot the computer.

**Note:** The DOC needs to be formatted with the System files in order for it to be a bootable drive. Refer to the M-Systems web site (www.m-sys.com) for documentation on the DOC 2000 and details on making it a bootable device.



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# Serial Ports

The *EPM-CPU-6/7* features two on-board 16550 based serial channels located at standard PC I/O addresses. COM1 is an RS-232 (115.2K baud) serial port.

COM2 can be operated in RS-232, RS-422, or RS-485 modes. Two additional non-standard baud rates are also available (programmable in the normal baud rate registers) of 230K and 460K baud.

Interrupt assignment for each COM port is handled in CMOS Setup, and each port can be independently enabled or disabled.

### COM Port Configuration

There are no configuration jumpers for COM1 because it only operates in RS-232 mode.

Jumper VS1 is used to configure COM2 for RS-232/422/485 operation. See page 17 for jumper configuration details.

### COM2 RS-485 Mode Line Driver Control

The TxD+/TxD– differential line driver can be turned on and off by manipulating the DTR handshaking line.

The following code example shows how to turn the line driver for COM2 on and off:

```
mov   dx,02FCh   ; Point to COM2 Modem Control register
in    al,dx      ; Fetch existing value
or    al,01h     ; Set bit D0
out   dx,al      ; Turn DTR on (enables line driver)

in    al,dx      ; Fetch existing value
and   al,0FEh    ; Clear bit D0
out   dx,al      ; Turn DTR off (disables line driver)
```



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### SERIAL PORT CONNECTORS

See the *Connector Location Diagram* on pages 13 and 14 for connector and cable information. The pinout of the DB9 connector applies to use of the VersaLogic transition cable #VL-CBL-8001.

**Table 7: Connectors JF / JG — Serial Port Pinout**

| COM1 JS1 Pin | COM2 JS1 Pin | RS-232 | RS-422 | RS-485 | JF/JG DB9 Pin |
|---|---|---|---|---|---|
| 21B | 31B | DCD | — | — | 1 |
| 22B | 32B | DSR | — | — | 6 |
| 23B | 33B | RXD* | TxD+ | TxD+ | 2 |
| 24B | 34B | RTS | TxD– | TxD– | 7 |
| 25B | 35B | TXD* | — | — | 3 |
| 26B | 36B | CTS | Ground | Ground | 8 |
| 27B | 37B | DTR | RxD– | TxD/RxD– | 4 |
| 28B | 38B | RI | RxD+ | TxD/RxD+ | 9 |
| 29B | 39B | Ground | Ground | Ground | 5 |
| 30B | 40B | N/C | — | — | — |



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# Parallel Port

The *EPM-CPU-6/7* includes a standard bi-directional/EPP/ECP compatible LPT port which resides at the PC standard address of 378h. The port can be enabled/disabled and interrupt assignments can be made via the CMOS Setup screen. The pinout of the JA connector applies to use of the VersaLogic transition cable #VL-CBL-8001.

**Table 8: LPT1 Parallel Port Pinout**

| JS1 Pin | Centronics Signal | Signal Direction | JA Pin |
|---|---|---|---|
| 1A | Strobe | Out | 1 |
| 2A | Auto feed | Out | 14 |
| 3A | Data bit 1 | In/Out | 2 |
| 4A | Printer error | In | 15 |
| 5A | Data bit 2 | In/Out | 3 |
| 6A | Reset | Out | 16 |
| 7A | Data bit 3 | In/Out | 4 |
| 8A | Select input | Out | 17 |
| 9A | Data bit 4 | In/Out | 5 |
| 10A | Ground | — | 18 |
| 11A | Data bit 5 | In/Out | 6 |
| 12A | Ground | — | 19 |
| 13A | Data bit 6 | In/Out | 7 |
| 14A | Ground | — | 20 |
| 15A | Data bit 7 | In/Out | 8 |
| 16A | Ground | — | 21 |
| 17A | Data bit 8 | In/Out | 9 |
| 18A | Ground | — | 22 |
| 19A | Acknowledge | In | 10 |
| 20A | Ground | — | 23 |
| 21A | Port Busy | In | 11 |
| 22A | Ground | — | 24 |
| 23A | Paper End | In | 12 |
| 24A | Ground | — | 25 |
| 25A | Select | In | 13 |



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# EIDE Hard Drive / CD-ROM Interfaces

One EIDE interface is available to connect up to two hard disk or CD-ROM drives. Use CMOS Setup to specify the drive parameters of the attached drives.

Some older IDE drives, such as those that are PIO Mode 0-1, do not operate reliably with this product. VersaLogic recommends the use of only PIO Mode 2-3 and Ultra DMA type drives with this product.

***Warning!*** Cable length must be 18" or less to maintain proper signal integrity. The grounds in this connector should not be used to carry motor current.

**Table 9: EIDE Hard Drive Connector Pinout**

| JS3 Pin | Signal Name | EIDE Signal Name | Function | JH/JJ Pin |
|---|---|---|---|---|
| 1A | HRST* | Host Reset | Reset signal from CPU | 1 |
| 2A | Ground | Ground | Ground | 2 |
| 3A | IDE7 | DATA 7 | Data bit 7 | 3 |
| 4A | HD8 | DATA 8 | Data bit 8 | 4 |
| 5A | HD6 | DATA 6 | Data bit 6 | 5 |
| 6A | HD9 | DATA 9 | Data bit 9 | 6 |
| 7A | HD5 | DATA 5 | Data bit 5 | 7 |
| 8A | HD10 | DATA 10 | Data bit 10 | 8 |
| 9A | HD4 | DATA 4 | Data bit 4 | 9 |
| 10A | HD11 | DATA 11 | Data bit 11 | 10 |
| 11A | HD3 | DATA 3 | Data bit 3 | 11 |
| 12A | HD12 | DATA 12 | Data bit 12 | 12 |
| 13A | HD2 | DATA 2 | Data bit 2 | 13 |
| 14A | HD13 | DATA 13 | Data bit 13 | 14 |
| 15A | HD1 | DATA 1 | Data bit 1 | 15 |
| 16A | HD14 | DATA 14 | Data bit 14 | 16 |
| 17A | HD0 | DATA 0 | Data bit 0 | 17 |
| 18A | HD15 | DATA 15 | Data bit 15 | 18 |
| 19A | Ground | Ground | Ground | 19 |
| 20A | NC | NC | No connection | 20 |
| 21A | NC | NC | No connection | 21 |
| 22A | Ground | Ground | Ground | 22 |
| 23A | HWR* | HOST IOW* | I/O write | 23 |
| 24A | Ground | Ground | Ground | 24 |
| 25A | HRD* | HOST IOR* | I/O read | 25 |
| 26A | Ground | Ground | Ground | 26 |
| 27A | NC | NC | No connection | 27 |
| 28A | HAEN | ALE | Address latch enable | 28 |
| 29A | NC | NC | No connection | 29 |
| 30A | Ground | Ground | Ground | 30 |
| 31A | HINT | HOST IRQ14 | IRQ14 | 31 |
| 32A | XI16* | HOST IOCS16* | Drive register enabled | 32 |
| 33A | HA1 | HOST ADDR1 | Address bit 1 | 33 |
| 34A | NC | NC | No connection | 34 |
| 35A | HA0 | HOST ADDR0 | Address bit 0 | 35 |
| 36A | HA2 | HOST ADDR2 | Address bit 2 | 36 |
| 37A | HCS0* | HOST CS0* | Reg. access chip select 0 | 37 |
| 38A | HCS1* | HOST CS1* | Reg. access chip select 1 | 38 |
| 39A | NC | NC | No connection | 39 |
| 40A | Ground | Ground | Ground | 40 |



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# Utility Connector

### KEYBOARD/MOUSE INTERFACE

A standard PS/2 keyboard and mouse interface is accessible through connector JS1. In addition, you will find a programmable LED output, hard drive activity LED, and a speaker output as shown in the table below. The pinout of the PS/2 connectors applies to use of the VersaLogic transition cable #VL-CBL-8001.

**Table 10: Utility Connector**

| JS1 Pin | Description | PS/2 Pin | |
|---|---|---|---|
| 27A | Programmable LED + | | |
| 28A | Programmable LED – | | |
| 29A | Speaker + | | |
| 30A | Speaker – | | |
| 31A | IDE Drive Indicator LED – | | |
| 32A | IDE Drive Indicator LED + | | |
| 33A | Protected +5V | 4 | |
| 34A | Mouse Data | 1 | |
| 35A | Ground | 3 | ← (JB) Mouse Connector |
| 36A | Mouse Clock | 5 | |
| 37A | Protected +5V | 4 | |
| 38A | Keyboard Data | 1 | |
| 39A | Ground | 3 | ← (JC) Keyboard Connector |
| 40A | Keyboard Clock | 5 | |

### PROGRAMMABLE LED

The high-density I/O connector JS1 includes an output signal for attaching a software controlled LED. Connect the cathode of the LED to JS1[28A]; anode to JS1[27A]. An on-board resistor limits the current to 15 mA when the circuit is turned on.

To turn the LED on and off, set or clear bit D7 in I/O port 0E0h (or 1E0h if selected in CMOS Setup). When changing the register, make sure not to alter the value of the other bits.

The following code examples show how to turn on and off the LED. Refer to page 42 for further information:

**LED On**

```
in    al,E0h
or    al,80h
out   E0h,al
```

**LED Off**

```
in    al,E0h
and   al,7Fh
out   E0,al
```

**Note:** The LED is turned on by the BIOS during system startup. This causes the light to function as a "power on" indicator if it is not otherwise controlled by user code.

### EXTERNAL SPEAKER

A miniature 8 ohm speaker can be connected between JS1[29A] and JS1[30A].



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### PUSH-BUTTON RESET

A normally open, momentary action push-button reset switch can be connected between JS1[19B] and JS1[20B]. Shorting JS1[19B] to ground will cause the *EPM-CPU-6/7* to reboot.

## Floppy Drive Interface

The *EPM-CPU-6/7* supports a standard 34-pin PC/AT style floppy disk interface via connector JS3[JK] and JS3[JL]. Up to two floppy drives can be attached. CMOS Setup can be used to enable or disable the floppy disk interface.

**Note:** The floppy drive used to boot the system (Drive A) should be connected after the twist in the cable, JS3[JK].

***Warning!*** Cable length must be 18" or less to maintain proper signal integrity. The grounds in this connector should not be used to carry motor current.

**Table 11: Floppy Disk Interface Connector Pinout**

| JS3 Pin | Signal Name | Function | JK/JL Pin |
|---|---|---|---|
| 1B | Ground | Ground | 1 |
| 2B | R/LC | Load Head | 2 |
| 3B | Ground | Ground | 3 |
| 4B | NC | No Connection | 4 |
| 5B | Ground | Ground | 5 |
| 6B | NC | No Connection | 6 |
| 7B | Ground | Ground | 7 |
| 8B | INDX* | Beginning Of Track | 8 |
| 9B | Ground | Ground | 9 |
| 10B | MTR1* | Motor Enable 1 | 10 |
| 11B | Ground | Ground | 11 |
| 12B | DRV0* | Drive Select 0 | 12 |
| 13B | Ground | Ground | 13 |
| 14B | DRE1* | Drive Select 1 | 14 |
| 15B | Ground | Ground | 15 |
| 16B | MTR0* | Motor Enable 0 | 16 |
| 17B | Ground | Ground | 17 |
| 18B | DIR | Direction Select | 18 |
| 19B | Ground | Ground | 19 |
| 20B | STEP* | Motor Step | 20 |
| 21B | Ground | Ground | 21 |
| 22B | WDAT* | Write Data Strobe | 22 |
| 23B | Ground | Ground | 23 |
| 24B | WGAT* | Write Enable | 24 |
| 25B | Ground | Ground | 25 |
| 26B | TRK0* | Track 0 Indicator | 26 |
| 27B | Ground | Ground | 27 |
| 28B | WPRT* | Write Protect | 28 |
| 29B | Ground | Ground | 29 |
| 30B | RDAT* | Read Data | 30 |
| 31B | Ground | Ground | 31 |
| 32B | HDSL | Head Select | 32 |
| 33B | Ground | Ground | 33 |
| 34B | DCHG | Drive Door Open | 34 |



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# Video Interface

An on-board Asiliant Technologies 690X0 controller with 2MB video RAM on the EPM-CPU-6 and 4MB video RAM on the EPM-CPU-7 provides full SVGA video output capabilities for the *EPM-CPU-6/7*.

Windows 95/98/NT automatically detects the 65550 and installs native driver support for all resolutions and color depths. The 65550 is also supported by QNX and VXWorks operating systems.

### VIDEO RESOLUTIONS

This table displays the *EPM-CPU-6/7* standard VESA SVGA modes and color depths.

**Table 12: Video Resolutions**

| **2 MB Video RAM** *(EPM-CPU-6)* | **4 MB Video RAM** *(EPM-CPU-7)* |
|---|---|
| 640 x 480, 16M colors | 640 x 480, 16M colors |
| 800 x 600, 16M colors | 800 x 600, 16M colors |
| 1024 x 768, 64K colors | 1024 x 768, 16M colors |
| 1280 x 1024, 256 colors | 1280 x 1024, 64K colors |
| 1600 X 1200, 16 colors | 1600 X 1200, 64K colors |

### VIDEO OUTPUT CONNECTOR

See the *Connector Location Diagram* on page 13 for pin and connector location information. An adapter cable, part number VL-CBL-1007 is available to translate JN2 into a standard 15-pin D-Sub SVGA connector.

**Table 13: Video Output Pinout**

| JN2 Pin | Signal Name | Function | Mini DB15 Pin |
|---|---|---|---|
| 1 | GND | Ground | 6 |
| 2 | CRED | Red Video | 1 |
| 3 | GND | Ground | 7 |
| 4 | CGRN | Green Video | 2 |
| 5 | GND | Ground | 8 |
| 6 | CBLU | Blue Video | 3 |
| 7 | GND | Ground | 5 |
| 8 | CHSYNC | Horizontal Sync | 13 |
| 9 | GND | Ground | 10 |
| 10 | CVSYNC | Vertical Sync | 14 |



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### FLAT PANEL DISPLAY CONNECTOR

See the *Connector Location Diagram* on page 13 for pin and connector location information.

**Table 14: Flat Panel Display Pinout**

| JN3 Pin | Signal Name | Function | Mono SS 8-bit | Mono DD 8-bit | Mono DD 16-bit | Color TFT 9/12/ 16-bit | Color TFT 18/24 bit | Color TFT HR 18/24 bit | Color STN STN SS 8-bit (X4bP) | Color STN SS 16-bit (4bP) | Color STN DD 8-bit (4bP) | Color STN DD 16-bit (4bP) | Color STN DD 24-bit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | +12V | Power Supply | | | | | | | | | | | |
| 2 | +12V | Power Supply | | | | | | | | | | | |
| 3 | GND | Ground | | | | | | | | | | | |
| 4 | GND | Ground | | | | | | | | | | | |
| 5 | +5V | Power Supply | | | | | | | | | | | |
| 6 | +5V | Power Supply | | | | | | | | | | | |
| 7 | ENAVEE | Power sequencing control for LCD bias voltage | | | | | | | | | | | |
| 8 | GND | Ground | | | | | | | | | | | |
| 9 | P0 | Data Output | | UD3 | UD7 | B0 | B0 | B00 | R1 | R1 | UR1 | UR0 | UR0 |
| 10 | P1 | " " | | UD2 | UD6 | B1 | B1 | B01 | B1 | G1 | UG1 | UG0 | UG0 |
| 11 | P2 | " " | | UD1 | UD5 | B2 | B2 | B02 | G2 | B1 | UB1 | UB0 | UB0 |
| 12 | P3 | " " | | UD0 | UD4 | B3 | B3 | B03 | R3 | R2 | UR2 | UR1 | LR0 |
| 13 | P4 | " " | | LD3 | UD3 | B4 | B4 | B10 | B3 | G2 | LR1 | LR0 | LG0 |
| 14 | P5 | " " | | LD2 | UD2 | G0 | B5 | B11 | G4 | B2 | LG1 | LG0 | LB0 |
| 15 | P6 | " " | | LD1 | UD1 | G1 | B6 | B12 | R5 | R3 | LB1 | LB0 | UR1 |
| 16 | P7 | " " | | LD0 | UD0 | G2 | B7 | B13 | B5 | G3 | LR2 | LR1 | UG1 |
| 17 | P8 | " " | P0 | | LD7 | G3 | G0 | G00 | SHF CLKU | B3 | | UG1 | UB1 |
| 18 | P9 | " " | P1 | | LD6 | G4 | G1 | G01 | | R4 | | UB1 | LR1 |
| 19 | P10 | " " | P2 | | LD5 | G5 | G2 | G02 | | G4 | | UR2 | LG1 |
| 20 | P11 | " " | P3 | | LD4 | R0 | G3 | G03 | | B4 | | UG2 | LB1 |
| 21 | P12 | " " | P4 | | LD3 | R1 | G4 | G10 | | R5 | | LG1 | UR2 |
| 22 | P13 | " " | P5 | | LD2 | R2 | G5 | G11 | | G5 | | LB1 | UG2 |
| 23 | P14 | " " | P6 | | LD1 | R3 | G6 | G12 | | B5 | | LR2 | UB2 |
| 24 | P15 | " " | P7 | | LD0 | R4 | G7 | G13 | | R6 | | LG2 | LR2 |
| 25 | P16 | " " | | | | | R0 | R00 | | | | | LG2 |
| 26 | P17 | " " | | | | | R1 | R01 | | | | | LB2 |
| 27 | P18 | " " | | | | | R2 | R02 | | | | | UR3 |
| 28 | P19 | " " | | | | | R3 | R03 | | | | | UG3 |
| 29 | P20 | " " | | | | | R4 | R10 | | | | | UB3 |
| 30 | P21 | " " | | | | | R5 | R11 | | | | | LR3 |
| 31 | P22 | " " | | | | | R6 | R12 | | | | | LG3 |
| 32 | P23 | " " | | | | | R7 | R13 | | | | | LB3 |
| 33 | GND | Ground | | | | | | | | | | | |
| 34 | GND | Ground | | | | | | | | | | | |
| 35 | SHFCLK | Shift Clock. Pixel clock for flat panel data. | SHF CLK | SHF CLK | SHF CLK | SHF CLK | SHF CLK | SHF CLK | SHF CLK | SHF CLK | SHF CLK | SHF CLK | SHF CLK |
| 36 | FLM | First Line Marker. Flat panel equivalent of VSYNC. | | | | | | | | | | | |
| 37 | DE | Display Enable or M signal (ADCCLK) or BLANK# | | | | | | | | | | | |
| 38 | LP | Latch Pulse. Flat panel equivalent of HSYNC. | | | | | | | | | | | |
| 39 | GND | Ground | | | | | | | | | | | |
| 40 | ENABKL | Enable Backlight. Can be programmed for other functions. | | | | | | | | | | | |
| 41 | DDCDATA | Serial Data | | | | | | | | | | | |
| 42 | DDCCLK | Serial Data | | | | | | | | | | | |
| 43 | +3V | Power Supply | | | | | | | | | | | |
| 44 | +3V | Power Supply | | | | | | | | | | | |



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### COMPATIBLE FLAT PANEL DISPLAYS

The following list of flat panel displays are reported to work properly with the Asiliant Technologies 690X0 video controller chip used on the *EPM-CPU-6/7*:

- Fujitsu FLC31SVC6S
- Hitachi D01VC1CAA
- Hitachi LMG9970ZWCC
- Hitachi LMG9972ZWCC
- Hitachi TX34D61VC1CAD
- NEC NL8060BC31-01
- Optrex DMF-50714NCU-FW (1024x768 DSTN)
- Samsung LT121-103
- Samsung LT133X1-104
- Samsung LT133X1-124
- Sanyo LM-GK53-22NTX (DSTN)
- Sanyo LM-GD53-22NAZ
- Sharp LM15X80 (XGA DSTN)
- Sharp LQ14X01
- Sharp LQ9D03B (640x480 TFT)
- Toshiba LTM12C016
- Toshiba LTM10C209

### FLAT PANEL DISPLAY SELECTION

The video BIOS shipped with the *EPM-CPU-6/7* supports up to 15 different flat panel configurations. Use jumper block VN3 to select which type of panel is used, and make sure to configure CMOS Setup to enable flat panel support.

See page 18 for jumper configuration details.



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# Ethernet Interface

The *EPM-CPU-6/7* features an industry-standard 10baseT / 100baseTX Ethernet interface based on the AMD AM97C973 interface chip. While this interface is not NE2000 compatible, the AM97C9xx series is widely supported. Drivers are readily available to support a variety of operating systems such as QNX, VxWorks and other RTOS vendors. Win95/98/NT ship with built-in support for this Ethernet interface. The drivers load automatically when the operating system is installed.

### SOFTWARE CONFIGURATION

The CMOS Setup screen is used to enable or disable the Ethernet interface.

### ETHERNET CONNECTOR

**Table 15: RJ45 Ethernet Connector**

| JS1 Pin | Signal Name | Function | JE Pin |
|---|---|---|---|
| 11B | IGND | Isolated Ground | 4 |
| 12B | IGND | Isolated Ground | 5 |
| 13B | R– | Receive Data – | 6 |
| 14B | R+ | Receive Data + | 3 |
| 15B | IGND | Isolated Ground | 7 |
| 16B | IGND | Isolated Ground | 8 |
| 17B | T– | Transmit Data – | 2 |
| 18B | T+ | Transmit Data + | 1 |

# Ethernet Status

LED D1 provides an onboard indication of the current condition of the board's Ethernet functionality.

Yellow = 10/100
On = 10 Base T
Off = 100 Base T
Green = Link/Activity
On = (solid) Link
Off = (Flickers) Blinks Activity



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# Watchdog Timer

A watchdog timer circuit is included on the *EPM-CPU-6/7* to reset the CPU if proper software execution fails or a hardware malfunction occurs.

### ENABLING THE WATCHDOG

To enable or disable the watchdog, set or clear bit D0 in I/O port 0E0h (or 1E0h if selected in CMOS Setup). When changing the contents of the register, make sure not to alter the value of the other bits.

The following code example enables the watchdog:

```
in    al,E0h
or    al,01h
out   E0h,al
```

The Watchdog will be enabled after the first Watchdog refresh is performed.

**Note:** The watchdog timer powers up in a disabled state.

### REFRESHING THE WATCHDOG

If the watchdog timer is enabled, software must periodically refresh the watchdog timer at a rate faster than the timer is set to expire (250 ms minimum). Outputting a 5Ah to the *Watchdog Timer Hold-Off Register* at 0E1h (or 1E1h if selected in CMOS Setup) resets the watchdog time-out period, preventing the CPU from being reset for the next 250 ms. See page 43 for additional information.

The following code example refreshes the watchdog:

```
mov   al,5Ah
out   E1h,al
```

# CPU Temperature Monitor

A thermometer circuit is located directly under the CPU chip which constantly monitors the case temperature of the CPU. This circuit can be used to detect over-temperature conditions which can result from fan or heat sink failure or excessive ambient temperatures.

CMOS Setup is used to set the temperature detection threshold. A status bit in the *Special Control Register* can be read to determine if the case temperature is above or below the threshold.

The system can be configured to generate a Non-Maskable Interrupt (NMI) when the temperature exceeds the threshold.

See page 42 for additional information.



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# USB1.0 Interface

A USB 1.0 (Universal Serial Bus) connector provides a common interface to connect a wide variety of keyboards, modems, mice, and telephony devices to the *EPM-CPU-6/7*. With USB 1.0, there is no need to have separate connectors for many common PC peripherals.

The USB 1.0 interface on the *EPM-CPU-6/7* is OHCI (Open Host Controller Interface) compatible, which provides a common industry software/hardware interface.

**Note:** The USB 1.0 interface must be enabled in CMOS Setup.

**Table 16: USB 1.0 Interface Connector**

| JS1 Pin | Signal Name | Function | JD Pin |
|---|---|---|---|
| 1B | USBPWR1 | +5V (Protected) | 1 |
| 2B | GND | Cable Shield | 6 |
| 3B | USBP00 | Channel 0 Data – | 2 |
| 4B | GND1 | Digital Ground | 7 |
| 5B | USBP01 | Channel 0 Data + | 3 |
| 6B | USBP11 | Channel 1 Data + | 8 |
| 7B | GND1 | Digital Ground | 4 |
| 8B | USBP10 | Channel 1 Data – | 9 |
| 9B | GND | Cable Shield | 5 |
| 10B | USBPWR1 | +5V (Protected) | 10 |

***Warning!*** Connector JD is not numbered in the conventional manner as most dual-row headers. Care must be taken to attach the USB 1.0 adapter cables as shown below to prevent voltage reversal.

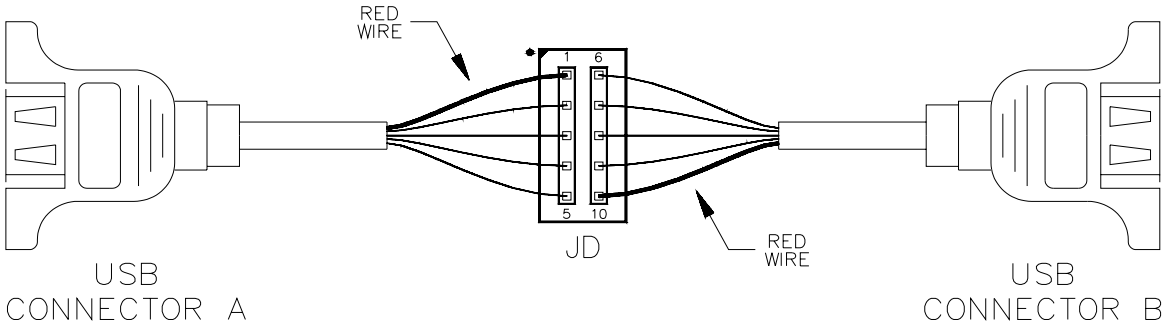



**Figure 7. USB 1.0 Connector Orientation Diagram**



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# Expansion Bus

The *EPM-CPU-6/7* will accept up to four PC/104 and/or two PC/104-*Plus* expansion modules. Both 3.3V and 5.0V modules are supported.

### PC/104-*PLUS*

PC/104-*Plus* modules can be secured directly to the underside of the *EPM-CPU-6/7*. Since circuitry on the *EPM-CPU-6/7* takes up PCI slot positions 2 and 3, the first added module is called "Slot 0", the next module is "Slot 1". Make sure to correctly configure the "slot position" jumpers on each PC/104-*Plus* module appropriately.

The BIOS automatically configures the I/O ports and Memory map allocation, including allocation of interrupts.

### PC/104

PC/104 modules are stacked under the *EPM-CPU-6/7* (under any PC/104-*Plus* modules); 16-bit modules first followed by 8-bit PC/104 modules. If necessary, a 40-pin and 64-pin ISA feedthrough connector "extender", and long standoffs may need to be used to provide adequate clearance between the PCI connector and the components on the top side of the PC/104 module.

#### I/O CONFIGURATION

#### PC/104–*Plus* Modules

No configuration is necessary except to jumper the expansion module for the correct slot number.

#### PC/104 Modules

PC/104 I/O modules should be addressed in the 100h – 3FFh address range. Care must be taken to avoid the I/O addresses shown in the *On-Board I/O Devices* table on page 40. These ports are used by on-board peripherals and video devices.



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# Memory and I/O Map

### MEMORY MAP

The lower 1 MB memory map of the *EPM-CPU-6/7* is arranged as shown in the following table.

Various blocks of memory space between A0000h and FFFFFh can be shadowed. CMOS setup is used to enable or disable this feature.

**Table 17: Memory Map**

| Start Address | End Address | Comment |
|---|---|---|
| F0000h | FFFFFh | System BIOS |
| E0000h | EFFFFh | BBSRAM, or Flash Page Frame |
| D0000h | DFFFFh | PC/104 |
| CE000h | CFFFFh | DOC |
| CC000h | CDFFFh | Nothing |
| C0000h | CBFFFh | Video BIOS |
| A0000h | BFFFFh | Video RAM |
| 00000h | 9FFFFh | System DRAM |

**Note:** The memory region from E0000h-EFFFFh is controlled by the Map and Paging Control Register.



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### I/O MAP

The following table lists the common I/O devices in the *EPM-CPU-6/7* I/O map. User I/O devices should be added in the 100h – 3FFh range, using care to avoid the devices already in the map as shown below.

**Table 18: On-Board I/O Devices**

| I/O Device | Standard I/O Addresses | Alternate * I/O Addresses |
|---|---|---|
| Special Control Register | 0E0h | 1E0h |
| Watchdog Hold-Off Register | 0E1h | 1E1h |
| Digital Control / Analog Status Register | 0E2h | 1E2h |
| Map and Paging Control Register | 0E3h | 1E3h |
| Primary Hard Drive Controller | 1F0h – 1F7h | |
| COM2 Serial Port | 2F8h – 2FFh | |
| LPT1 Parallel Port | 378h – 37Fh | |
| SVGA Video | 3B0h – 3DFh | |
| Floppy Disk Controller | 3F0h – 3F7h | |
| COM1 Serial Port | 3F8h – 3FFh | |

* User selectable via CMOS Setup.

**Note:** I/O ports occupied by on-board devices are freed up when the device is disabled in CMOS Setup.



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# Interrupt Configuration

The *EPM-CPU-6/7* has the standard complement of PC type interrupts. Ten non-shared interrupts are routed to the PC/104 bus, and up to four IRQ lines are automatically allocated as needed to PCI devices.

There are no interrupt configuration jumpers. All configuration is handled through CMOS setup. The switches in the diagram below indicate the various CMOS Setup options. Closed switches show factory default settings.

The temperature monitor interrupt is enabled/disabled with bit D3 (NMIEN) in the *Special Control Register*.

**Note:** If your design needs to use interrupt lines on the PC/104 bus, we recommend using IRQ5, IRQ9, and/or IRQ10. Make sure to configure CMOS Setup with the chosen PC/104 interrupts. This prevents their allocation to PCI devices.

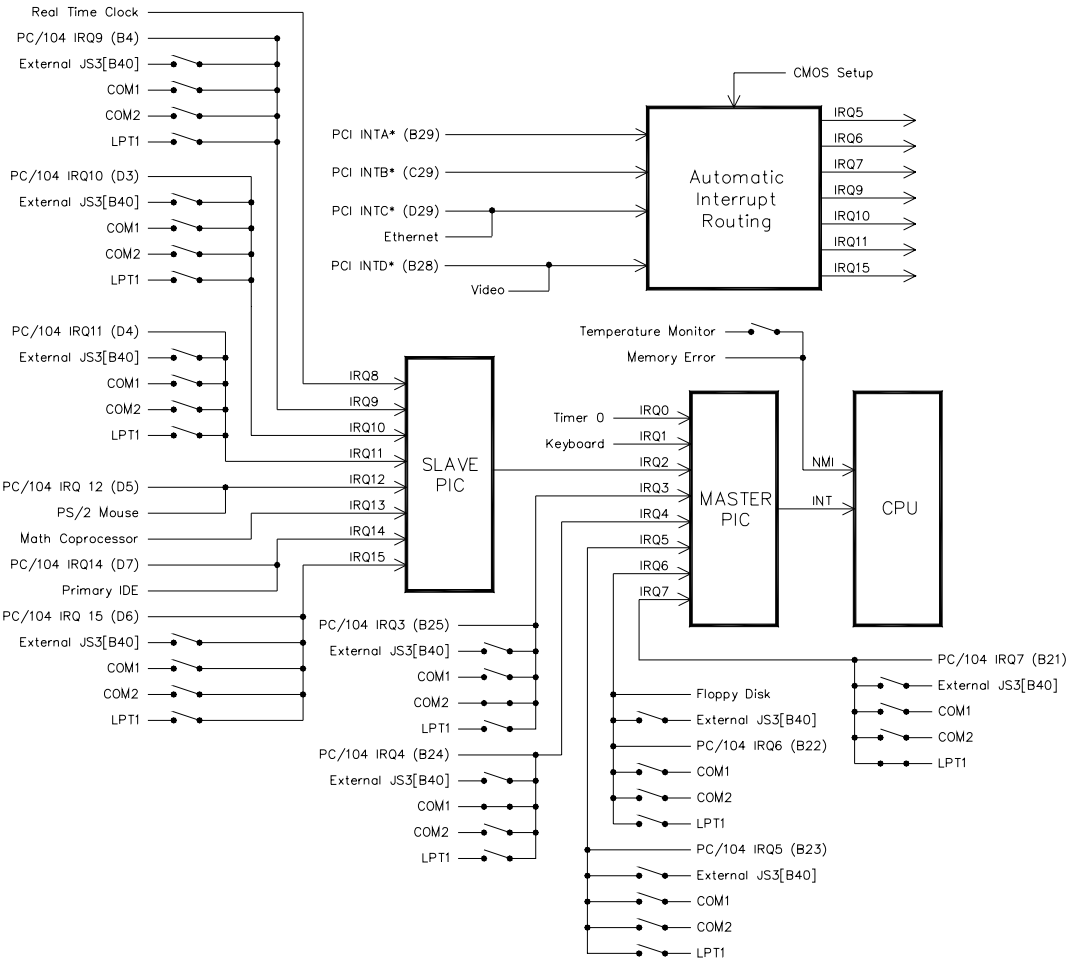



**Figure 8. Interrupt Circuit Diagram**



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# Special Control Register

**SCR (READ/WRITE) 00E0h (or 01E0h via CMOS Setup)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| LED | TEMP | GPI | GPO | NMIEN | ETHDIS | JPI | WDOGEN |

**Table 19: Special Control Register Bit Assignments**

| Bit | Mnemonic | Description |
|---|---|---|
| D7 | LED | **Light Emitting Diode** — Controls the programmable LED connected to JS1[27A/28A]<br>LED = 0 Turns LED off.<br>LED = 1 Turns LED on. |
| D6 | TEMP | **Temperature Status** — Indicates CPU case temperature.<br>TEMP = 0 CPU case temperature is below value set in CMOS Setup<br>TEMP = 1 CPU case temperature is above value set in CMOS Setup<br>***Note:*** *This bit is a read-only bit.* |
| D5 | GPI | **General Purpose Input** — Indicates the status of TTL input at JS3[B38].<br>GPI = 0 Logic High<br>GPI = 1 Logic Low<br>***Note:*** *This bit is a read-only bit.* |
| D4 | GPO | **General Purpose Output** — Controls TTL output at JS3[37B].<br>GPO = 0 Logic High<br>GPO = 1 Logic Low |
| D3 | NMIEN | **Non-Maskable Interrupt Enable** — Controls the generation of Non-Maskable Interrupts whenever the CPU temperature sensor detects an over-temperature condition.<br>NMIEN = 0 Disable<br>NMIEN = 1 Enable |
| D2 | ETHDIS | **Ethernet Disable** — Enables and disables the Ethernet port.<br>ETHDIS = 0 Enables Ethernet port.<br>ETHDIS = 1 Disables Ethernet port. |
| D1 | JPI | **Jumper Input** — Indicates the status of jumper VS2[5-6]<br>JPI = 0 Jumper VS2[5-6] = Out<br>JPI = 1 Jumper VS2[5-6] = In<br>***Note:*** *This general purpose bit is read-only.* |
| D0 | WDOGEN | **Watchdog Enable** — Enables and disables the watchdog timer reset circuit.<br>WDOGEN = 0 Disables the watchdog timer.<br>WDOGEN = 1 Enables the watchdog timer. |



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# Revision Indicator Register

**REVIND (READ ONLY) 00E1h (or 01E1h via CMOS Setup)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| PC4 | PC3 | PC2 | PC1 | PC0 | REV2 | REV1 | REV0 |

This register is used to indicate the revision level of the *EPM-CPU-6/7* product.

| Bit | Mnemonic | Description |
|---|---|---|
| D7-D3 | PC4-PC0 | **Product Code** — These bits are hard coded to represent the product type. The EPM-CPU-6/7 will always read as 11100. Other codes are reserved for future products.<br>**PC4 PC3 PC2 PC1 PC0 Product Code**<br>1 1 1 0 0 EPM-CPU-6/7<br>***Note:*** *This bits are read-only.* |
| D2-D0 | REV2-REV0 | **Revision Level** — These bits are represent the EPM-CPU-6/7 circuit revision level.<br>**REV2 REV1 REV0 Revision Level**<br>0 0 0 Rev 2 (Initial product release)<br>0 0 1 Rev 3 (EPM-CPU-7 only)<br>0 1 0 Reserved<br>0 1 1 Reserved<br>1 0 0 Reserved<br>1 0 1 Reserved<br>1 1 0 Reserved<br>1 1 1 Reserved<br>***Note:*** *This bits are read-only.* |

# Watchdog Timer Hold-Off Register

**WDHOLD (WRITE ONLY) 00E1h (or 01E1h via CMOS Setup)**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |

A watchdog timer circuit is included on the EPM-CPU-6/7 board to reset the CPU if proper software execution fails or a hardware malfunction occurs. The watchdog timer is enabled/disabled by writing to bit D0 of SCR

If the watchdog timer is enabled, software must periodically refresh the watchdog timer at a rate faster than the timer is set to expire (250 ms minimum). Writing a 5Ah to WDHOLD resets the watchdog timeout period, preventing the CPU from being reset for the next 250 ms.

# Map and Paging Control Register

{xe "Memory:Control Registers:Map and Paging Control (MPCR)"}
{xe "Memory:FLASH Page Frame"}



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### MPCR (READ/WRITE) 00E3H (or 01E3h via CMOS Setup)

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| FPGEN | Reserved | SPGEN | DPGEN | Reserved | PG2 | PG1 | PG0 |

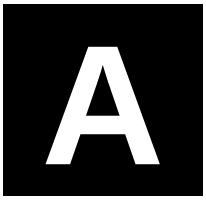
**Table 20: Map and Paging Control Register Bit Assignments**

| Bit | Mnemonic | Description |
|---|---|---|
| D7 | FPGEN | **FLASH Paging Enable** — Enables a 64K page frame from E0000h to EFFFFh. Used to gain access to the on-board FLASH memory.<br>FPGEN = 0 FLASH page frame disabled.<br>FPGEN = 1 FLASH page frame enabled.<br>***Note:*** *This bit is for factory use only. It is used to write user default CMOS setup values to FLASH and to upgrade the system BIOS. When FPGEN = 1, the Page Select bits are used to access various blocks within the FLASH.* |
| D6 | — | **Reserved** — This bit has no function. |
| D5 | SPGEN | **Battery Backed Static RAM Paging Enable** — Enables a 64K page frame from E0000h to EFFFFh. Used to gain access to an optional Dallas Semiconductor Battery-Backed Static RAM chip plugged into socket U9 (512KB max.)<br>SPGEN = 0 BBSRAM page frame disabled.<br>SPGEN = 1 BBSRAM page frame enabled.<br>***Note:*** *When SPGEN = 1, the Page Select bits are used to access various 64K blocks within the BBSRAM chip.* |
| D4 | DPGEN | **DiskOnChip Enable** — Enables a 8K page frame from CE000h to CFFFFh. Used to gain access to the Disk on Chip<br>DPGEN = 0 DOC page frame disabled.<br>DPGEN = 1 DOC page frame enabled.<br>***Note:*** *The Page Select bits are not used when accessing the DOC.* |
| D3 | — | **Reserved** — This bit has no function. |
| D2-D0 | PG2-PG0 | **Page Select** — Selects which 64K block of FLASH or BBSRAM will be mapped into the page frame at E0000h to EFFFFh<br>**PG2 PG1 PG0 — Memory Range within FLASH or BBSRAM**<br>0 0 0 — 000000h to 00FFFFh<br>0 0 1 — 010000h to 01FFFFh<br>0 1 0 — 020000h to 02FFFFh<br>0 1 1 — 030000h to 03FFFFh<br>1 0 0 — 040000h to 04FFFFh<br>1 0 1 — 050000h to 05FFFFh<br>1 1 0 — 060000h to 06FFFFh<br>1 1 1 — 070000h to 07FFFFh |



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# Appendix A — Other References



| | |
|---|---|
| PC Chipset<br>*ALi Aladdin IV+ Chipset* | Acer Laboratories Inc., (www.acerlabs.com) |
| Ethernet Controller<br>*AMD 79C973 (from the PC Net Family of devices)* | Advanced Micro Devices, (www.amd.com) |
| Video Controller<br>*690X0* | Asiliant Technologies., (www.asiliant.com) |
| Disk On Chip<br>*DOC2000* | M-Systems Inc., (www.m-sys.com) |
| PC/104 Specification<br>*PC/104 Resource Guide* | PC/104 Consortium, (www.controlled.com/pc104) |
| PC/104-*Plus* Specification<br>*PC/104 Resource Guide* | VersaLogic Corp., (www.VersaLogic.com) |
| CPU Chips<br>*K6 & K6-2*<br>*Pentium* | <br>Advanced Micro Devices, (www.amd.com)<br>Intel Corporation, (www.intel.com) |
| General PC Documentation<br>*The Programmer's PC Sourcebook* | Microsoft Press, mspress.microsoft.com |
| General PC Documentation<br>*The Undocumented PC* | www.amazon.com |



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