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Reference Manual

DOC. REV. 12/13/2013

EPM-32 (Cheetah)

Pentium M® Based Processor Board with Ethernet, Video, Audio, and PC/104-*Plus* Interface

VersaLogic Corporation



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Product Release Notes

Rev 3 Release

- Release of RoHS, fanless model EPM-32v.

Rev 2 Release

- Release of RoHS models EPM-32p and EPM-32t.

Rev 1 Release

Initial product release.

Support Page

The **EPM-32 support page**, at **http://www.VersaLogic.com/private/cheetahsupport.asp**, contains additional information and resources for this product including:

- Reference Manual (PDF format)
- Operating system information and software drivers
- Datasheets and manufacturers' links for chips used in this product
- BIOS information and upgrades
- Utility routines and benchmark software

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1 Introduction

Description

The EPM-32 is a feature-packed processor board in a compact PC/104-*Plus* format. It is designed for OEM control projects requiring fast processing, compact size, flexible memory options, and designed-in reliability and longevity. Its features include:

- Intel Pentium M® 1.0 to 1.8 GHz
- Up to 1 GB system RAM
- Intel 855GME / ICH4 chipset
- CompactFlash site
- 10/100 Ethernet interface
- Intel Extreme Graphics 2
- Flat panel display support
- PC/104-Plus high-speed expansion site
- ATA100 IDE controller
- Two USB 2.0 ports
- TVS devices for ESD protection
- Audio
- Two COM ports and one LPT port
- CPU temperature sensor
- PS/2 keyboard and mouse ports
- Watchdog timer
- Vcc sensing reset circuit
- Field upgradeable BIOS with OEM enhancements
- Latching I/O connectors
- Customizing available

The EPM-32 is a complete computer system in a compact two-board set. It may be used alone or with expansion modules. It features a PC/104-*Plus* expansion interface for fast PCI-based interface to a wide variety of PC/104 (ISA) and PC/104-*Plus* (PCI) stacking modules.

The board is compatible with popular operating systems such as Windows, QNX, VxWorks and Linux.

System memory expansion is supported with one high-reliability latching 200-pin SODIMM sockets. Low power 2.5V 200-pin SODIMM modules up to 1 GB are available.

The EPM-32 features high reliability design and construction, including latching I/O connectors. It also features a watchdog timer, voltage sensing reset circuits, and a self-resetting fuse on the 5V supply to the keyboard, mouse, and USB.

EPM-32 boards are subjected to 100% functional testing and are backed by a limited two-year warranty.

Careful parts sourcing and US-based technical support ensure the highest possible quality, reliability, service, and product longevity for this exceptional module.

Technical Specifications

Specifications are typical at 25°C with 5.0V supply unless otherwise noted.

Board Size: 4.10" x 3.775" PCB dimensions. 4.80" x 3.775" including connectors. Two board set.
Storage Temperature: -40° C to 85° C
Free Air Operating Temperature:
EPM-32c, p, v 0° C to +60° C
EPM-32e, t -40° C to +85° C
Power Requirements: *(with 256 MB DDR SODIMM, keyboard and mouse, running WinXP)*
EPM-32c 1.6 GHz Pentium M® CPU 5V ± 5% (12-25 W) typ.
EPM-32e, t, v 1.0 GHz Pentium M® CPU 5V ± 5% (8-12 W) typ.
EPM-32p 1.8 GHz Pentium M® CPU 5V ± 5% (12-25 W) typ.
+3.3V or ±12V may be required by some expansion modules
System Reset:
V_{cc} sensing, resets below 4.70V typ.
Watchdog timeout
DRAM Interface:
One 200-pin DDR SODIMM socket
Up to 1 GB, 2.50V, non-parity, PC2700
Video Interface:
Intel Extreme Graphics 2, 855GME
3.3V LVDS flat panel display interface
CRT
IDE Interface:
Single channel, 44-pin. 2mm connector. Supports up to and including UDMA5.
Supports up to two IDE devices (hard drives, CD-ROM, etc.).
(CompactFlash on separate channel.)
Ethernet Interface:
One Intel 82551ER based Fast Ethernet Controller
Audio Interface:
Standard Line Out and Line In support
COM1 Interface:
RS-232, 16C550 compatible, 115k baud max.
COM2 Interface:
RS-232/422/485, 16C550 compatible, 460k baud max.
LPT Interface:
Bi-directional/EPP/ECP compatible. Floppy disk interface with CBR-2501.
BIOS: General Software embedded BIOS with OEM enhancements
Field-upgradeable with Flash BIOS Update Utility
Bus Speed:
CPU Bus: 400MHz
DRAM: 200 MHz/266 MHz/333 MHz
PC/104-*Plus* (PCI): 33MHz
PC/104 (ISA): 8MHz
Compatibility:
PC/104 – full compliance
Embedded-PCI (PC/104-*Plus*) – full compliance, 3.3V signaling
Weight:
EPM-32c, e with standoffs installed – 0.266 kg (0.586 lbs)
EPM-32p, t with standoffs installed – 0.250 kg (0.553 lbs)
EPM-32v with standoffs installed – 0.243 kg (0.537 lbs)
No memory installed
Generated Frequencies:
100, 133, or 166 MHz (memory), 125 MHZ, 66MHz, 33.3 MHz, 25 MHz, 24.576 MHz, 14.318 MHz, 8.25 MHz, 2.5 MHz, 350 kHz, 32.768 kHz

Specifications are subject to change without notice.

EPM-32 Block Diagram

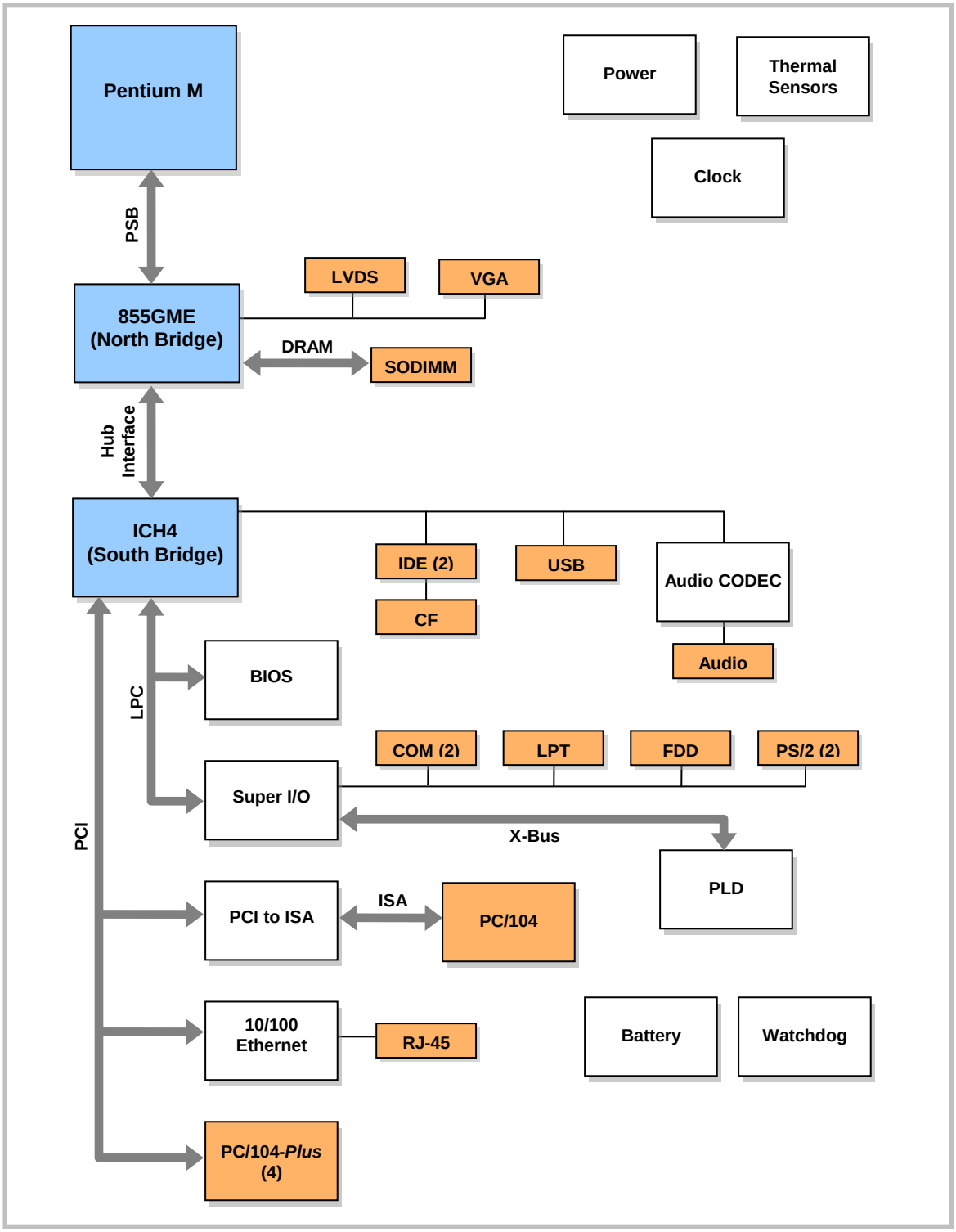


Figure 1. EPM-32 Block Diagram

RoHS Compliance

The EPM-32p, t, and v are RoHS-compliant.

About RoHS

In 2003, the European Union issued Directive 2002/95/EC regarding the Restriction of the use of certain Hazardous Substances (RoHS) in electrical and electronic equipment.

The RoHS directive requires producers of electrical and electronic equipment to reduce to acceptable levels the presence of six environmentally sensitive substances: lead, mercury, cadmium, hexavalent chromium, and the presence of polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) flame retardants, in certain electrical and electronic products sold in the European Union (EU) beginning July 1, 2006.

VersaLogic Corporation is committed to supporting customers with high-quality products and services meeting the European Union's RoHS directive.

Warnings

Electrostatic Discharge

Warning! Electrostatic discharge (ESD) can damage circuit boards, disk drives and other components. The circuit board must only be handled at an ESD workstation. If an approved station is not available, some measure of protection can be provided by wearing a grounded antistatic wrist strap. Keep all plastic away from the product, and do not slide it over any surface.

After removing the product from its protective wrapper, place it on a grounded, static-free surface,. Use an antistatic foam pad if available.

The product should also be protected inside a closed metallic anti-static envelope during shipment or storage.

Note: The exterior coating on some metallic antistatic bags is sufficiently conductive to cause excessive battery drain if the bag comes in contact with the bottom-side of the EPM-32.

Lithium Battery

Warning! To prevent shorting, premature failure or damage to the lithium battery, do not place the EPM-32 on a conductive surface such as metal, black conductive foam or the outside surface of a metalized ESD protective pouch. The lithium battery may explode if mistreated. Do not recharge, disassemble or dispose of in fire. Dispose of used batteries promptly and in an environmentally suitable manner.

CONNECTING THE NORTH BRIDGE AND SOUTH BRIDGE BOARDS

Warning! When connecting the north bridge and south bridge boards of the EPM-32, you must be sure that sockets JN5 and JN6 on the north bridge board mate perfectly with headers JS2 and JS3 of the south bridge board. Failure to connect the boards properly could cause serious damage and void the warranty.

See Connecting the North Bridge and South Bridge Boards on page 14.

Technical Support

If you are unable to solve a problem after reading this manual please visit the EPM-32 Product Support web page at http://www.VersaLogic.com/private/cheetahsupport.asp. If you have further questions, contact VersaLogic technical support at (503) 747-2261. VersaLogic technical support engineers are also available via e-mail at Support@VersaLogic.com.

EPM-32 Support Website

REPAIR SERVICE

If your product requires service, you must obtain a Returned Material Authorization (RMA) number by calling (503) 747-2261.

Please provide the following information:

- Your name, the name of your company, your phone number, and your e-mail address
- The name of a technician or engineer that can be contacted if any questions arise
- Quantity of items being returned
- The model and serial number (barcode) of each item
- A detailed description of the problem
- Steps you have taken to resolve or recreate the problem
- The return shipping address

Warranty Repair All parts and labor charges are covered, including return shipping charges for UPS Ground delivery to United States addresses.

Non-warranty Repair All non-warranty repairs are subject to diagnosis and labor charges, parts charges and return shipping fees. Please specify the shipping method you prefer and provide a purchase order number for invoicing the repair.

RMA Number Please mark the RMA number clearly on the outside of the box before returning.

Configuration and Setup

2

Initial Configuration

The following components are recommended for a typical development system.

- EPM-32 Two Board Set (CPU Module & I/O Module)
- 200-pin SODIMM DDR200, DDR266 or DDR333
- ATX Power Supply
- SVGA Video Monitor
- Keyboard and Mouse with PS2 Connector
- IDE Hard Drive
- IDE CD ROM Drive

The following VersaLogic cables are recommended. These cables are included in the development cable kit (CKR-CHEE) that ships with the EPM-32.

- CBR-1008 – ATX Adapter Cable
- CBR-1201 – Video Cable
- CBR-8001 – Standard I/O Breakout Cable
- CBR-4406 – IDE Data Cable
- CBR-4405 – 44-pin to 40-pin Adapter (one for each 3.5” drive)

Note: Non-RoHS-compliant versions of these cables are no longer available for purchase. Non-RoHS cable part numbers begin with the prefix CBL and have the same base numbers as their RoHS counterparts. If you own non-RoHS cables, they can be used with the EPM-32p or EPM-32t in non-RoHS applications only.

The VL-ENCL-5b enclosure provides a portable benchtop platform for system development. See the VL-ENCL-5 product page for information.

Basic Setup

The following steps outline the procedure for setting up a typical development system. The EPM-32 should be handled at an ESD workstation or while wearing a grounded antistatic wrist strap.

Before you begin, unpack the EPM-32 and accessories. Verify that you received all the items you ordered. Inspect the system visually for any damaged that may have occurred in shipping. Contact Support@VersaLogic.com immediately if any items are damaged or missing.

Gather all the peripheral devices you plan to attach to the EPM-32 and their interface and power cables.

It is recommended that you attach standoffs to the board to stabilize the board and make it easier to work with.

Figure 2 shows a typical start-up configuration (using RoHS compatible cables).

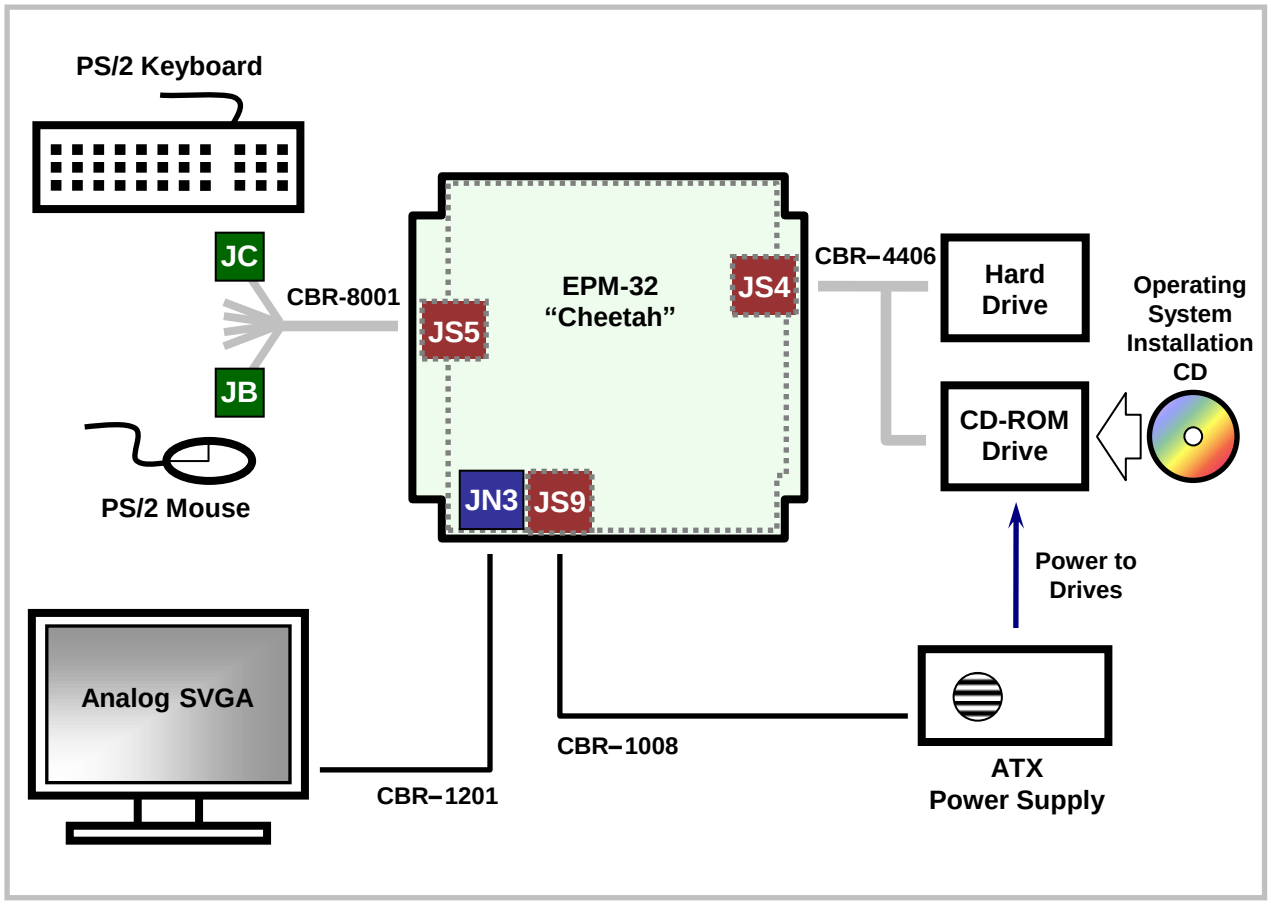


Figure 2. Typical Start-up Configuration

1. Install Memory

- Insert the DRAM module into socket SODIMM1 (see Figure 9)and latch into place.

2. Attach Power

- Plug the power adapter cable CBR-1008 into socket JS9. Attach the motherboard connector of the ATX power supply to the adapter.

3. Attach Cables and Peripherals

- Plug the video adapter cable CBR-1201 into socket JN3. Attach the video monitor interface cable to the video adapter.
- Plug the breakout cable CBR-8001 into socket JS5.
- Plug a PS/2 keyboard into connector JC of the breakout cable and the a PS/2 mouse into connector JB.
- Plug the hard drive data cable CBR-4406 into socket JS4. Attach a hard drive and CD-ROM drive to the connectors on the cable. If the hard drive is 3.5", use the 2mm to 0.1" adapter CBR-4405 to attach the IDE cable.
- Attach an ATX power cable to any 3.5" drive (hard drive or CD-ROM drive).
- Set the hard drive jumper for master device operation and the CD-ROM drive jumper for slave device operation.

4. Review Configuration

- Before you power up the system, double check all the connections. Make sure all cables are oriented correctly and that adequate power will be supplied to the EPM-32 and peripheral devices.

5. Power On

- Turn on the ATX power supply and the video monitor. If the system is correctly configured, a video signal should be present.

6. Change CMOS Setup Settings

- Enter CMOS Setup by pressing Delete during the early boot cycle.
- Select Basic Configuration and set or verify the following settings:

```
DRIVE ASSIGNMENT ORDER | Drive C: Ide 0/Pri Master

ATA DRV ASSIGNMENT | Ide 0: 3 = AUTOCONFIG, LBA
ATA DRV ASSIGNMENT | Ide 1: 5 = IDE CDROM

BOOT ORDER | Boot 1st: CDROM
BOOT ORDER | Boot 2nd: Drive C:
```

- Before saving the CMOS Setup settings, insert the Windows (or other OS) installation disk in the CD-ROM drive so it will be accessed when the system reboots.
- Press ESC and select the option to save the new parameters to CMOS RAM. The system will reboot.

7. Install Operating System

- Install the operating system according to the instructions provided by the OS manufacturer. (See Operating System Installation.)

  Note: If you intend to operate the EPM-32 under Windows XP or Windows XP Embedded, be sure to use Service Pack 2 (SP2) for the latest hardware support features.

CMOS Setup

See VersaLogic KnowledgeBase article VT1472 – EPM-32 CMOS Setup Reference for complete information on the CMOS configuration for the EMP-32.

Operating System Installation

The standard PC architecture used on the EPM-32 makes the installation and use of most of the standard x86 processor-based operating systems very simple. The operating systems listed on the VersaLogic OS Compatibility Chart use the standard installation procedures provided by the maker of the OS. Special optimized hardware drivers for a particular operating system, or a link to the drivers, are available at the EPM-32 Product Support web page at http://www.VersaLogic.com/private/cheetahsupport.asp.

Dimensions and Mounting

The EPM-32 complies with all PC/104-*Plus* standards. Dimensions are given below to help with pre-production planning and layout.

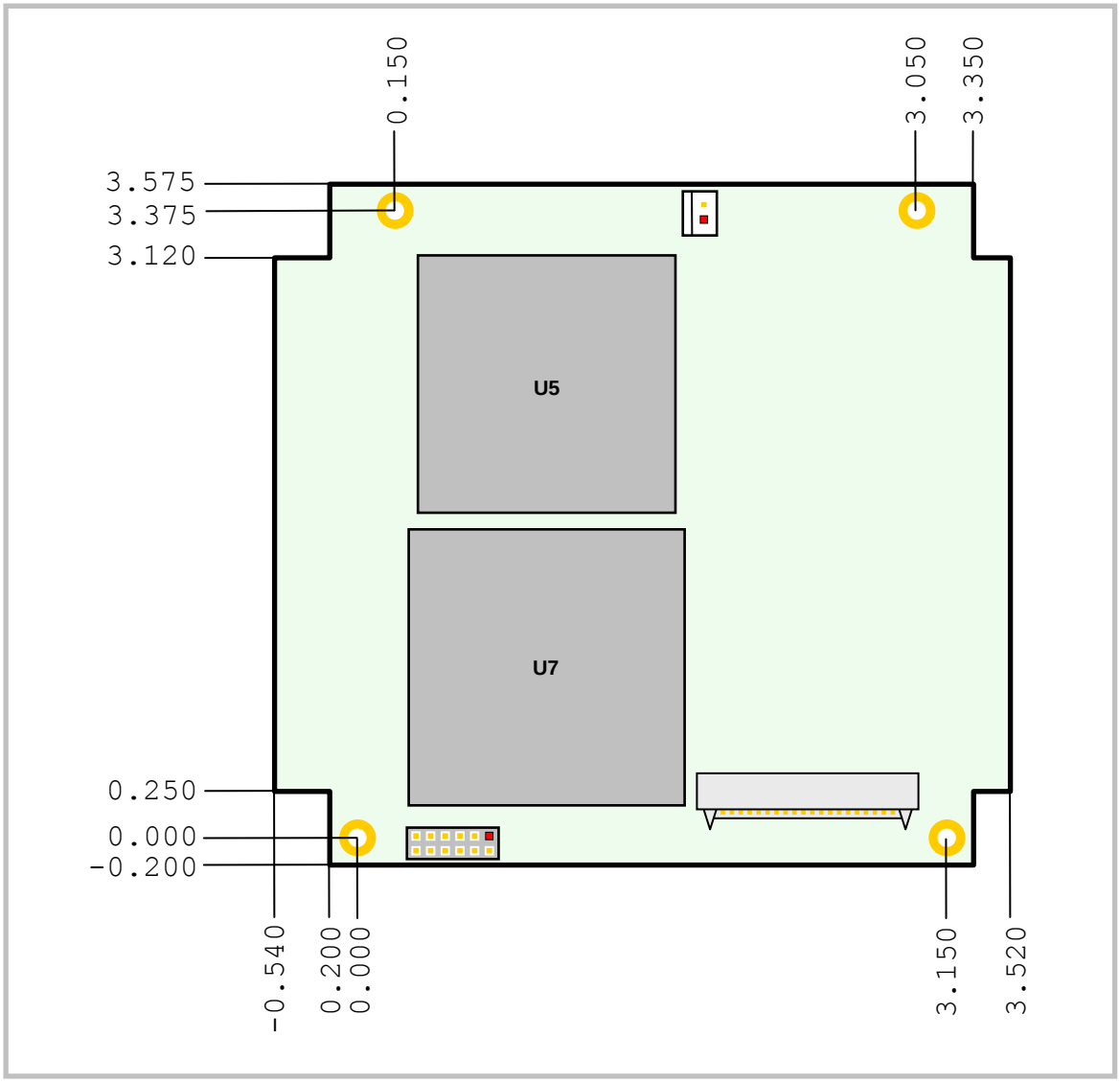


Figure 3. Dimensions and Mounting Holes
North Board – Top
(Not to scale. All dimensions in inches.)

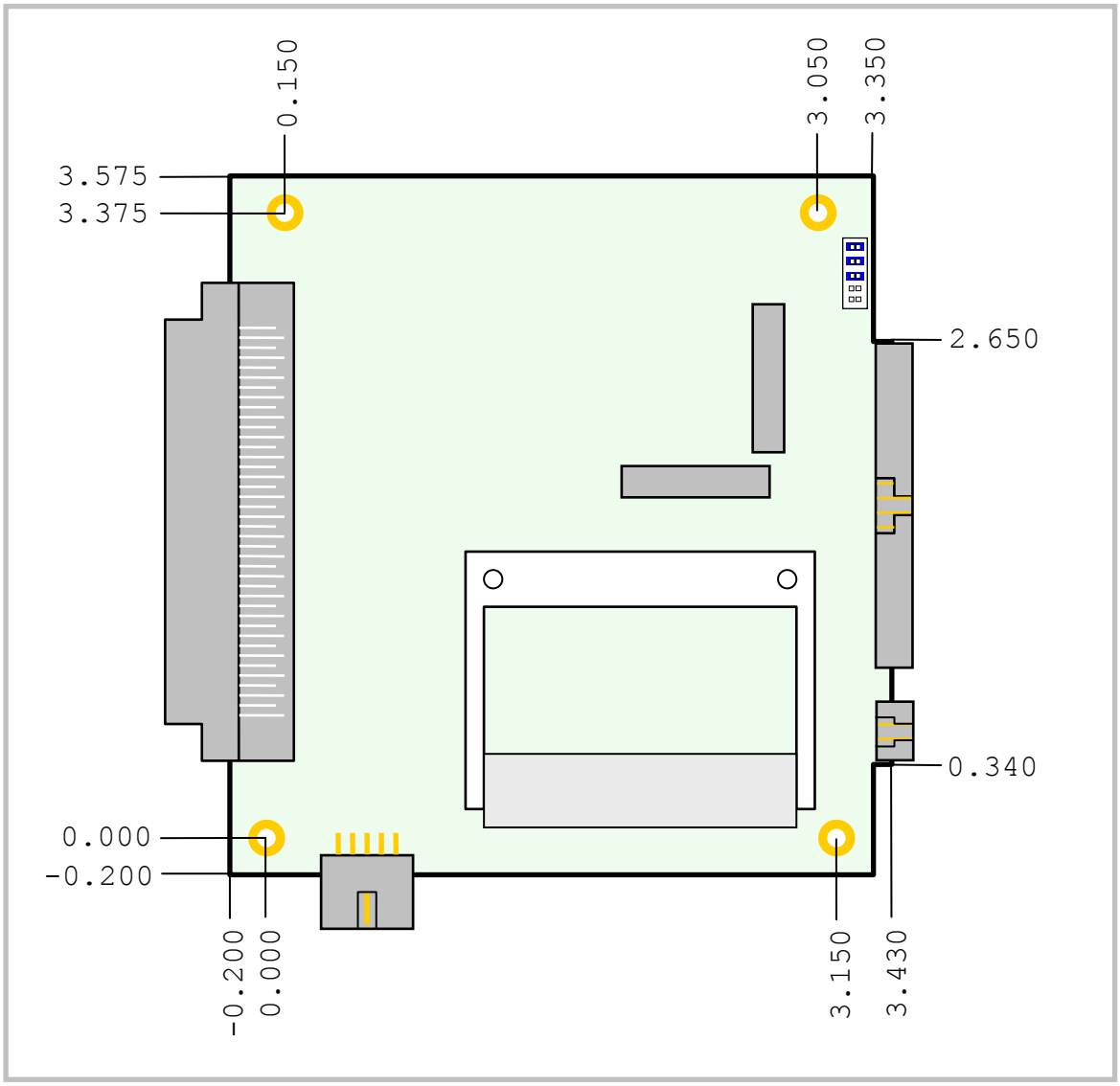


Figure 4. Dimensions and Mounting Holes
South Board – Top
(Not to scale. All dimensions in inches.)

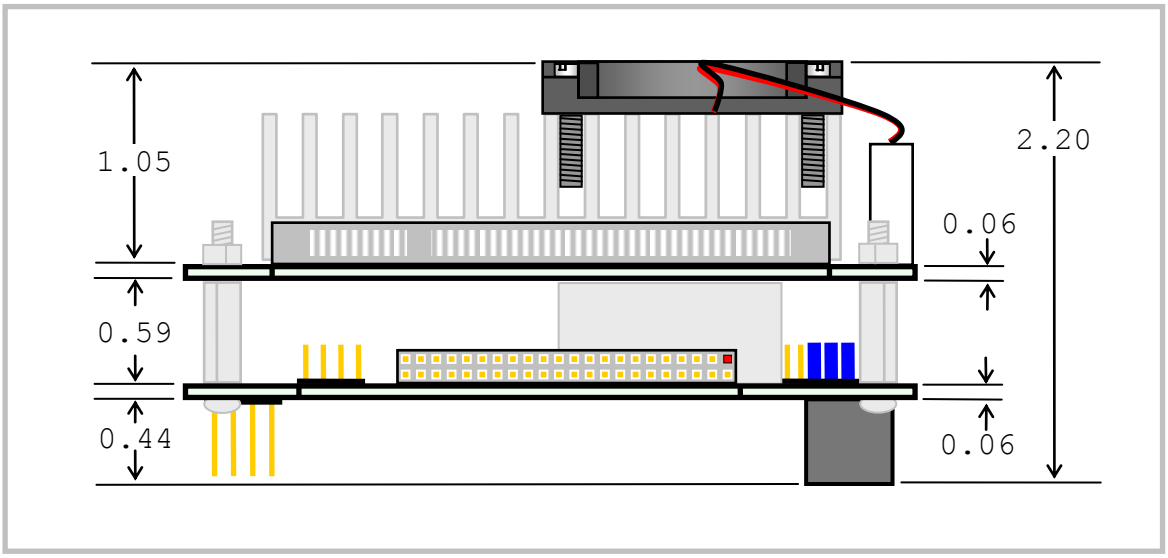


Figure 5. Height Dimensions

(Not to scale. All dimensions in inches.)

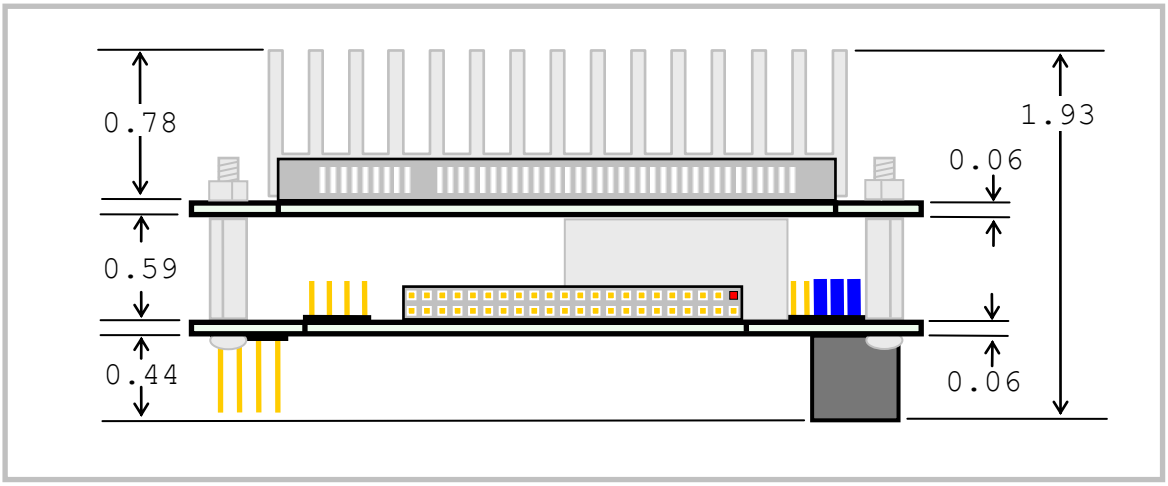


Figure 6. Height Dimensions – Fanless Model

HARDWARE ASSEMBLY

The EPM-32 consists of two boards that are mounted together with four 5mm x 15mm M3 threaded hex male/female standoffs (p/n VL-HDW-101) using the corner mounting holes. These standoffs are secured to the top circuit board using four pan head screws.

Caution: Extreme care must be taken not to damage components near the corner mounting holes when tightening standoffs with nut driver tools.

Additional PC/104-*Plus* or PC/104 cards can be attached to the bottom of the EPM-32 board set and secured with standoffs or 5mm nuts.

PC/104-*Plus* expansion modules can be secured directly to the underside of the EPM-32.

PC/104 expansion modules can be secured to the underside of the EPM-32; however, the 40-pin and 64-pin ISA pass-through connectors may need to be extended, and longer standoffs might need to be used to provide adequate clearance between the PCI connector and the components on the top side of the PC/104 expansion module.

The entire assembly can sit on a table top or it can be secured to a base plate. When bolting the unit down, make sure to secure all four standoffs to the mounting surface to prevent circuit board flexing. Refer to the drawing on page 10 for dimensional details.

An extractor tool is available (part number VL-HDW-201) to separate the modules from the stack.

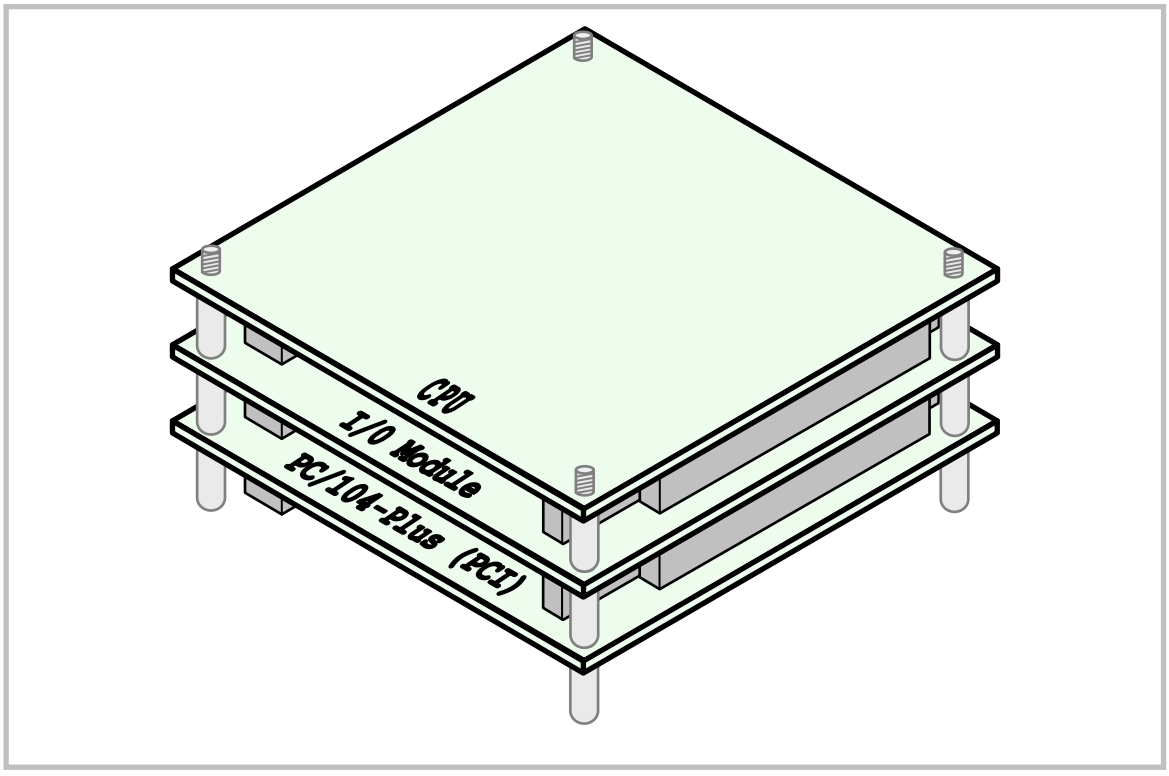


Figure 7. Stack Arrangement

CONNECTING THE NORTH BRIDGE AND SOUTH BRIDGE BOARDS

Warning! When connecting the north bridge and south bridge boards of the EPM-32, you must be sure that sockets JN5 and JN6 on the north bridge board mate perfectly with headers JS2 and JS3 of the south bridge board. Failure to connect the boards properly could cause serious damage and void the warranty.

To connect the north and south bridge boards of the EPM-32, follow this procedure:

1. Attach all four 5mm x 15mm standoffs to the top of the south bridge board using the provided screws.
2. Hold the boards so that sockets JN5 and JN6 are aligned with headers JS2 and JS3, and the standoffs are aligned with the holes of the north bridge board.
3. Lower the north bridge board over the standoffs while visually aligning sockets JN5 and JN6 with headers JS2 and JS3. Make sure the pins match the sockets perfectly before applying the pressure required to seat the connectors.
4. Secure standoffs to the north bridge board with the provided hex nuts.

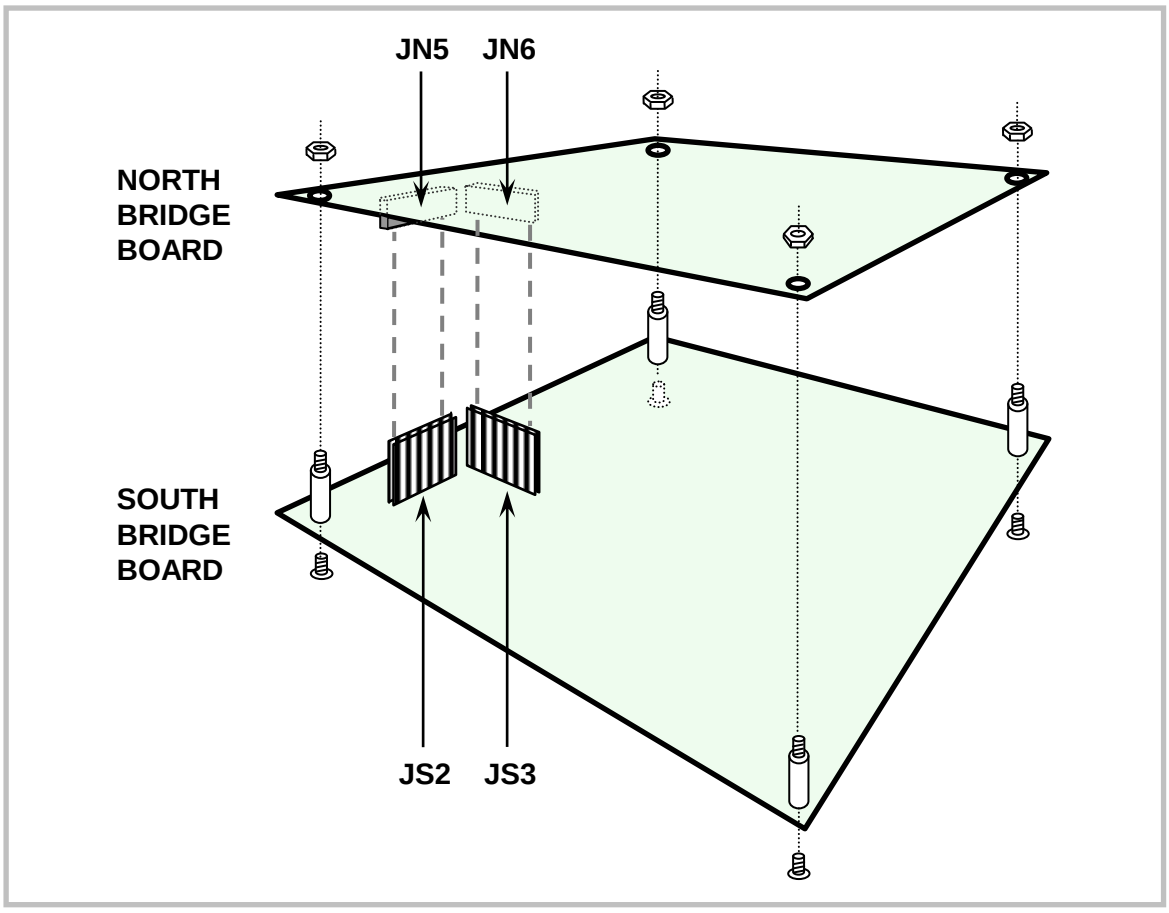


Figure 8. Connecting the North and South Bridge Boards

External Connectors

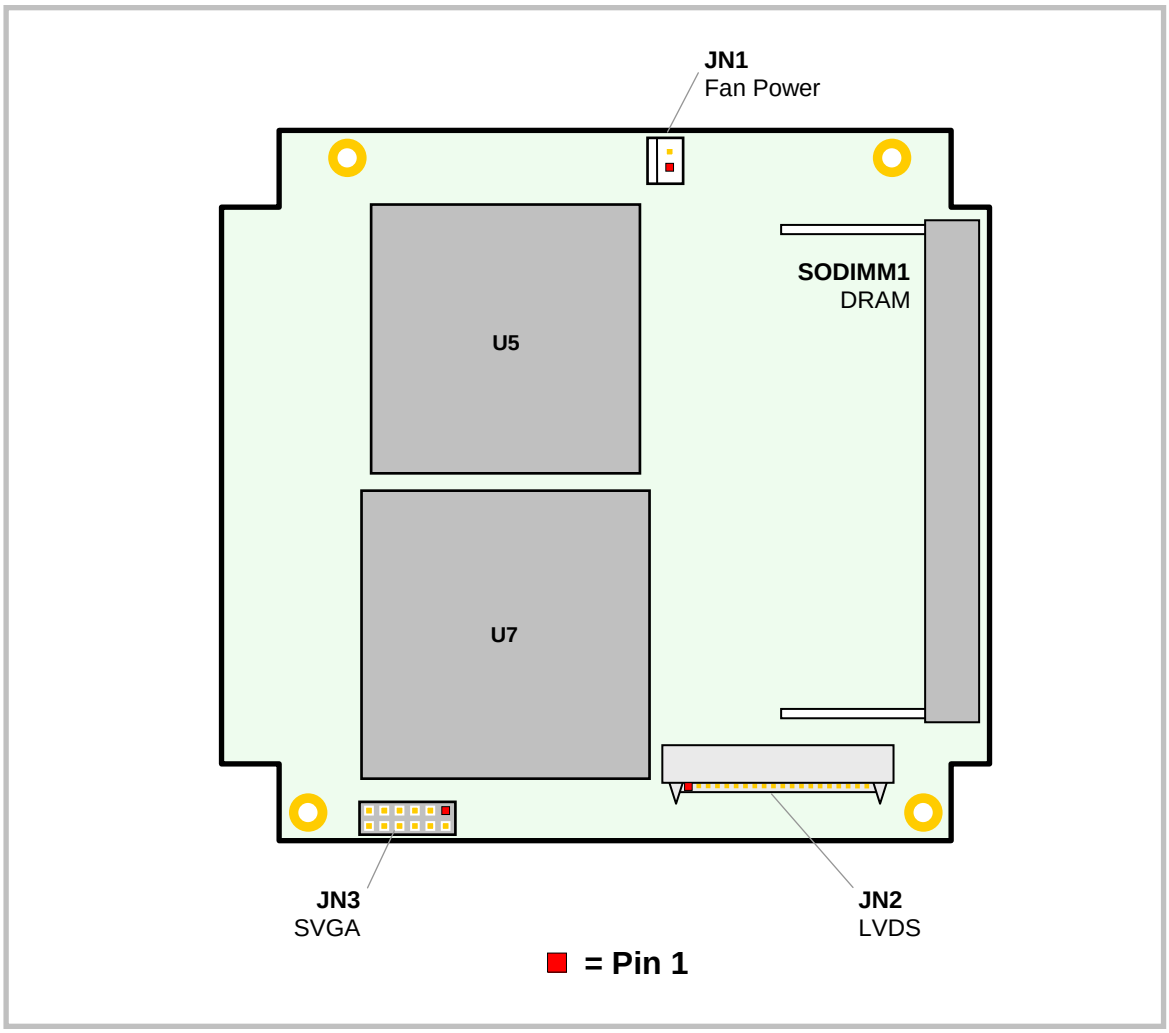


Figure 9. Connector Locations
North Bridge Board – Top
(Not to scale. All dimensions in inches.)

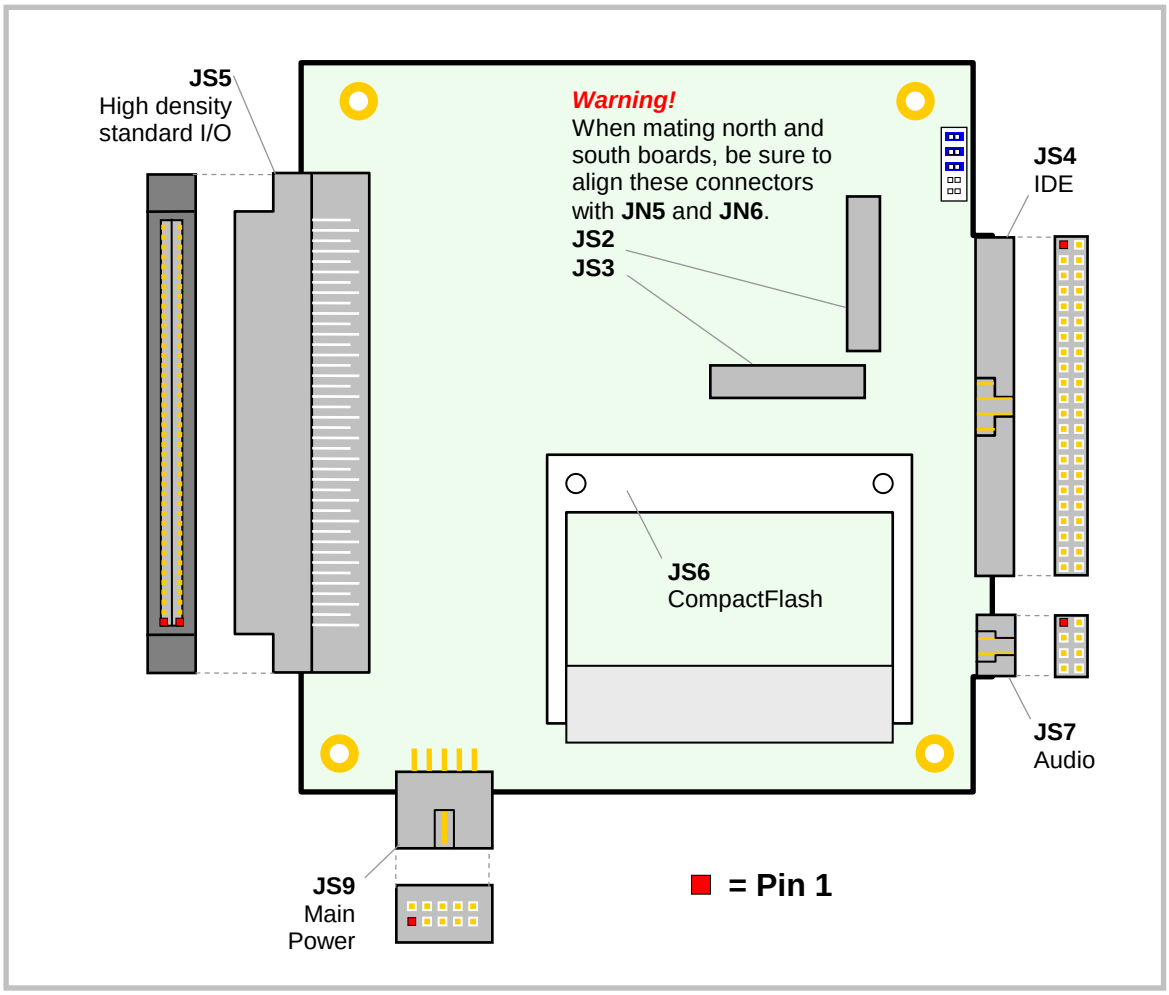


Figure 10. Connector Locations
South Bridge Board – Top
(Not to scale.)

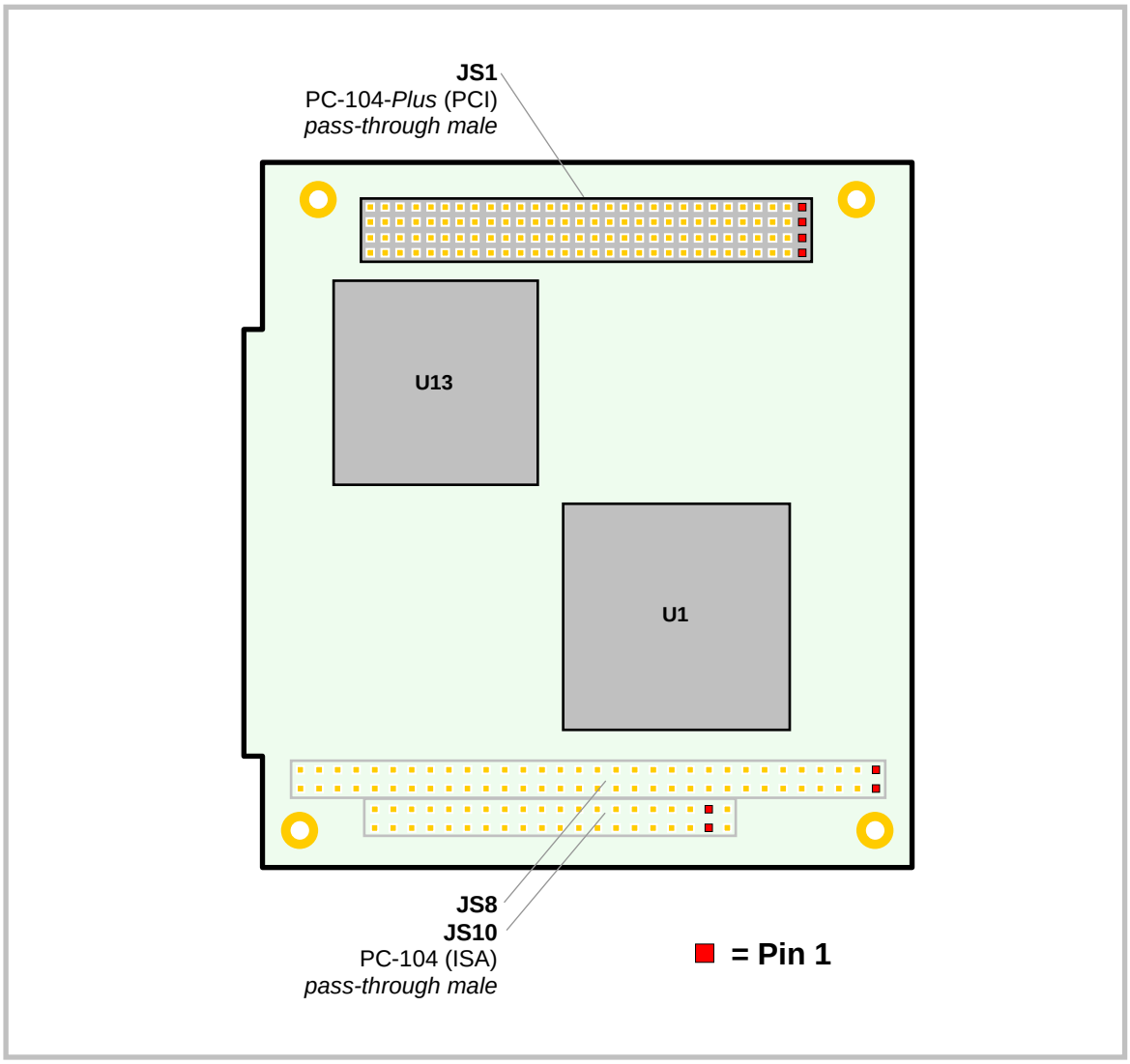


Figure 11. Connector Locations
South Bridge Board – Bottom
(Not to scale.)

CONNECTOR FUNCTIONS AND INTERFACE CABLES

The following table notes the function of each connector, as well as mating connectors and cables, and the page where a detailed pinout or further information is available.

Table 1: Connector Functions and Interface Cables

Connector	Function	Mating Connector	Transition Cable	Cable Description	[1]Pin 1 Location x Coord.	Y Coord.	Page
JN1	Fan Power Output (+5V)	Molex 22-01-3027 or Molex 22-01-2025	Provided with fan assembly	–	1.810	3.350	–
JN2	LVDS Flat Panel Output	Molex 51146-2000	CBR-2010 CBR-2011	20-pin EPM-32 to LVDS 18-bit TFT FPD	1.920	0.257	36
JN3	SVGA Video Output	FCI 89361-712LF or FCI 89947-712LF	CBR-1201	12" 2mm latching 12-pin socket to 15-pin D-sub SVGA connector	0.657	-0.036	35
JN4	Not used	–	–	–	1.223	-0.120	–
JN5	Board-to-board I/F	–	–	–	[2]2.800	2.150	–
JN6	Board-to-board I/F	–	–	–	[2]2.050	1.884	–
JS1	PC/104-*Plus* (PCI)	AMP 1375799-1	–	–	[3]0.450	3.139	42
JS2	Board-to-board I/F	–	–	–	[2]2.800	2.150	–
JS3	Board-to-board I/F	–	–	–	[2]2.050	1.884	–
JS4	IDE Hard Drive	FCI 89361-744LF or FCI 89947-744LF	CBR-4406	18" latching 44-pin IDE drive interface to two 44-pin 2mm IDE	3.235	2.552	26
JS5	Keyboard, Mouse, LPT1 (or Floppy), Speaker, USB1, USB2, COM1, COM2, Ethernet, IDE Data LED, Pushbutton Reset, Programmable LED	3M Robinson-Nugent P50E-080S-EA	CBR-8001	Breakout to standard PC device connectors	0.100	0.750	27
JS6	CompactFlash	Type I or Type II Compact Flash	–	–	1.289	1.356	33
JS7	Audio	FCI 89947-708LF or FCI 89361-708LF	CBR-0803	12" latching 8-pin 2mm to two 3.5mm stereo audio	3.237	0.633	40
JS8 JS10	PC/104 (ISA)	AMP 1375795-2	–	–	[3]0.050 [4]0.850	0.200 0.100	42
JS9	Main Power Input	Berg 69176-010 (Housing) +Berg 44715-000 (Pins) ‡	CBR-1008	12" ATX to EPM power cable	0.225	-0.050	21

1. The PCB Origin is the mounting hole to the lower left, as shown in Figures 1 and 2.
2. Mechanical pin closest to pin 1.
3. Pin A1.
4. Pin C0.

Note: Non-RoHS-compliant versions of VersaLogic cables for the EPM-32 are no longer available for purchase. Non-RoHS cable part numbers begin with the prefix CBL and have the same base numbers as their RoHS equivalents. If you own non-RoHS cables, they can be used with the RoHS-compliant versions of the EPM-32 in non-RoHS applications only.

Jumper Blocks

JUMPERS AS-SHIPPED CONFIGURATION.

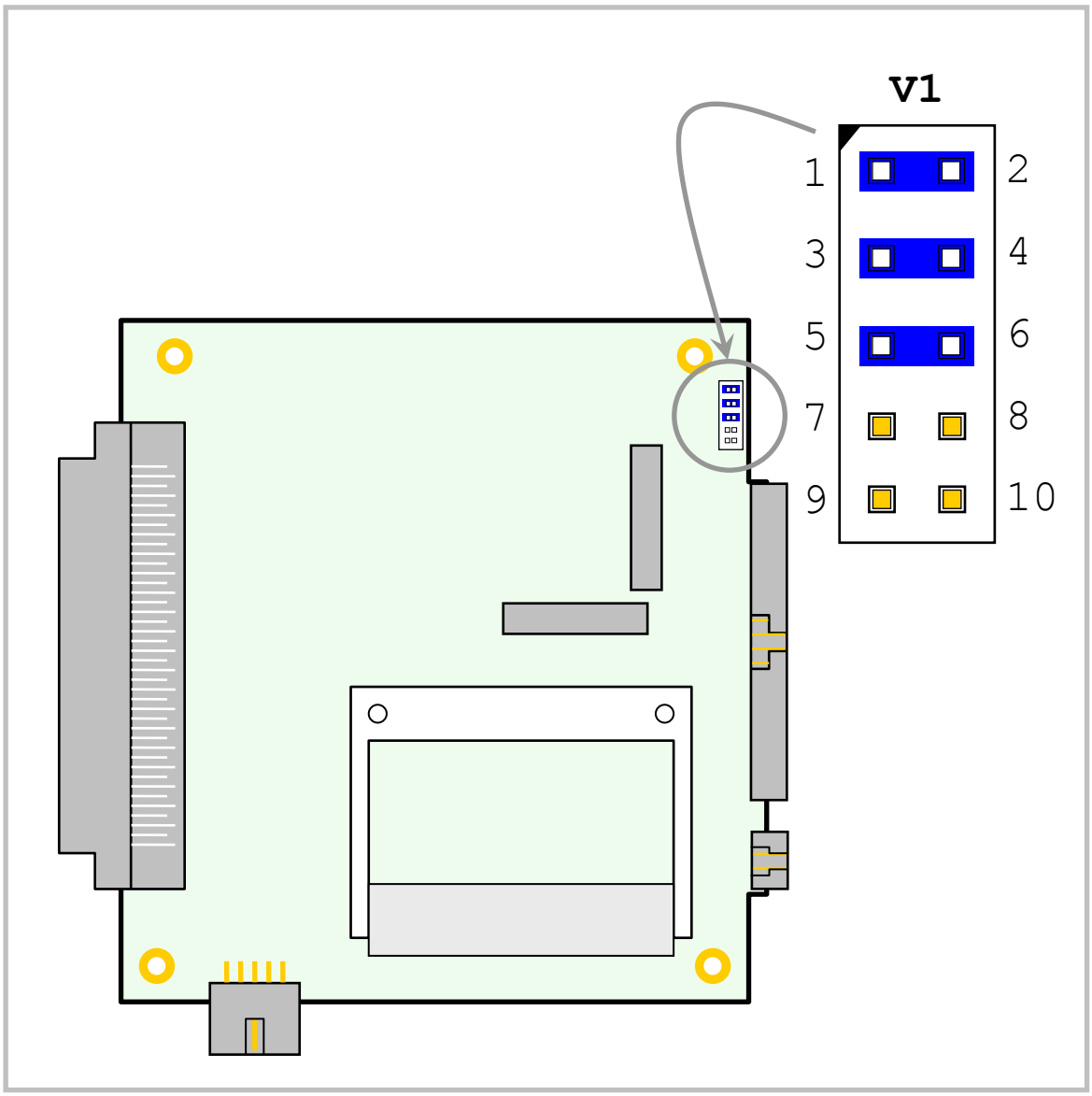


Figure 12. Jumper Block Location
South Bridge Board – Top

JUMPER SUMMARY

Table 2: Jumper Summary

Jumper Block	Description	As Shipped	Page
V1[1-2]	**System BIOS Selector** In — Runtime system BIOS selected Out — Master system BIOS selected. ***Note:*** *The Runtime System BIOS is field upgradeable using the BIOS upgrade utility. See www.VersaLogic.com/private/cheetahsupport.asp for further information.*	In	—
V1[3-4]	**Video BIOS Selector** In — Primary Video BIOS selected Out — Secondary Video BIOS selected ***Note:*** *The secondary Video BIOS is field-upgradeable using the BIOS upgrade utility. See www.VersaLogic.com/private/cheetahsupport.asp for further information*	In	35
V1[5-6]	**General Purpose Input 1** In — Bit D7 (GPI) of JSR register reads as 1 Out — Bit D7 (GPI) of JSR register reads as 0	In	49
V1[7-8]	**COM2 RS-422/485 Endpoint Termination** In — Endpoint Termination Enabled Out — Endpoint Termination Disabled	Out	29
V1[9-10]	**CMOS RAM and Real Time Clock Erase** In — Erase CMOS RAM and Real-Time Clock Out — Normal	Out	24

Power Supply

POWER CONNECTORS

Main power is applied to the EPM-32 through a 10-pin polarized connector. See page 15 for the JS9 power connector location.

Warning! To prevent severe and possibly irreparable damage to the system, it is critical that the power connectors are wired correctly. Make sure to use all +5VDC pins and all ground pins to prevent excess voltage drop. Some manufacturers include a pin-1 indicator on the crimp housing that corresponds to pin-10 of the pinout shown in Figure 13.

Table 3: JS9 Main Power Connector Pinout

JS9 Pin	Signal Name	Description
1	Ground	Ground
2	+5VDC	Power Input
3	Ground	Ground
4	+12VDC	Power Input
5	Ground	Ground
6	–12VDC	Power Input
7	+3.3VDC	Power Input
8	+5VDC	Power Input
9	Ground	Ground
10	+5VDC	Power Input

Figure 13 shows the VersaLogic standard pin numbering for this type of 10-pin power connector and the corresponding mating connector.

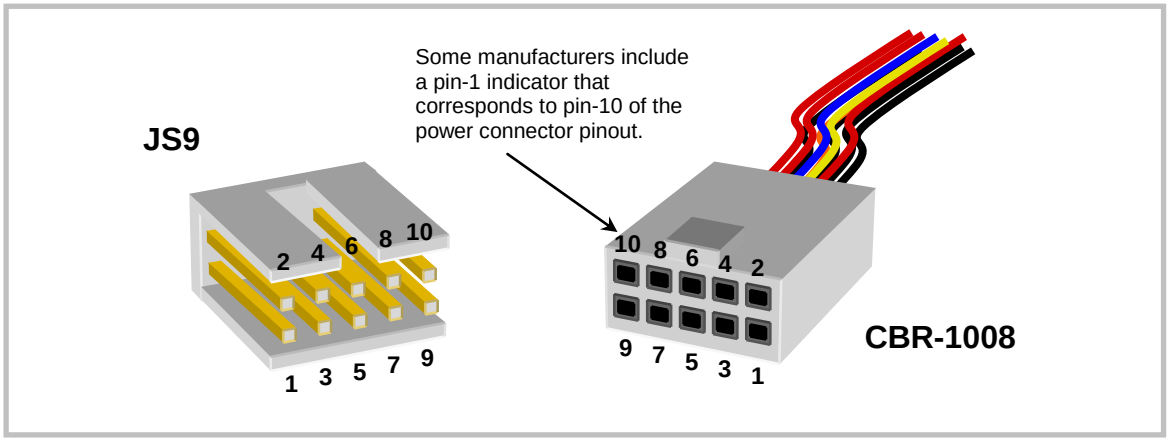


Figure 13. JS9 and CBR-1008 Pin Numbering

Note: The +3.3VDC, +12VDC and -12VDC inputs on the main power connector are only required for PC/104-*Plus* and PC/104 expansion modules that require the voltages.

POWER REQUIREMENTS

The EPM-32 requires only +5 volts (±5%) for proper operation. The voltage required for the RS-232 ports are generated with a DC/DC converter. A variable low-voltage supply circuit provides power to the CPU and other on-board devices.

The exact power requirement of the EPM-32 depends on several factors, including memory configuration, CPU speed, peripheral connections, type and number of expansion modules and attached devices. For example, PS/2 keyboards typically draw their power directly from the EPM-32, and driving long RS-232 lines at high speed can increase power demand.

POWER DELIVERY CONSIDERATIONS

Using a VersaLogic approved power supply (VL-PS200-ATX) and power cable (CBR-1008) will ensure high quality power delivery to the board. Customers who design their own power delivery methods should take into consideration the guidelines below to ensure good power connections.

Also, the specifications for typical operating current do not include any off-board power usage that may be fed through the EPM-32 power connector. Expansion boards and USB devices plugged into the board will source additional power through the EPM-32 power connector.

- Do not use wire smaller than 22 AWG. Use high quality UL 1007 compliant stranded wire.
- The length of the wire should not exceed 18".
- Avoid using any additional connectors in the power delivery system.
- The power and ground leads should be twisted together, or as close together as possible to reduce lead inductance.
- A separate conductor must be used for each of the power pins.
- All power input pins and all ground pins must be independently connected between the power source and the power connector.
- Use a high quality power supply that can supply a stable voltage while reacting to widely varying current draws.

LITHIUM BATTERY

Warning! To prevent shorting, premature failure or damage to the lithium battery, do not place the board on a conductive surface such as metal, black conductive foam or the outside surface of a metalized ESD protective pouch. The lithium battery may explode if mistreated. Do not recharge, disassemble or dispose of in fire. Dispose of used batteries promptly.

Normal battery voltage should be at least 2.5V. If the voltage drops below 2.5V, contact the factory for a replacement (part number T-HB3/0-1). The life expectancy under normal use is approximately seven years.

Note: The EPM-32 is designed to boot even with a dead or removed battery. See page 25 for further information.

CPU

CPU SPEED

The processor speed can be changed using CMOS Setup. The speed options range from 600 MHz to 1800 MHz. Reducing the CPU speed will decrease system power consumption and performance. Extended temperature versions of the board do not allow operation above 1000 MHz.

System RAM

Compatible Memory Modules

The EPM-32 accepts one 200-pin SODIMM memory module with the following characteristics:

- Size — Up to 1 GB
- Voltage — 2.5V
- Error Detection — Non-Parity
- Type — Unbuffered PC1600 (DDR200), PC2100 (DDR266) or PC2700 (DDR333)

CMOS RAM

Clearing CMOS RAM

A jumper may be installed into V1[9-10] to erase the contents of the CMOS RAM and the Real-Time Clock. The jumper should be installed when the EPM-32 is turned off, left installed for a minimum of three seconds and removed before powering on the EPM-32.

CMOS Setup Defaults

The EPM-32 permits users to modify the CMOS Setup defaults. This allows the system to boot up with user-defined settings from cleared or corrupted CMOS RAM, battery failure or battery-less operation. All CMOS setup defaults can be changed, except the time and date. The CMOS Setup defaults can be updated with the Flash BIOS Update (FBU) Utility, available from the General BIOS Information page.

If the CMOS Setup default settings make the system unbootable and prevent you from entering CMOS Setup, remove the System BIOS Selector jumper and reboot the system. The master system BIOS will allow the system to boot using its own DMOS Setup defaults.

Default CMOS RAM Setup Values

After the CMOS RAM is cleared, the system will load default CMOS RAM parameters the next time the board is powered on. The default CMOS RAM setup values will be used in order to boot the system whenever the main CMOS RAM values are blank, or when the system battery is dead or has been removed from the board.

SAVING CMOS SETUP PARAMETERS AS CUSTOM DEFAULTS

To save CMOS Setup parameters to custom defaults, you will need a DOS bootable floppy with the FBU utility on it.

1. Boot the EPM-32 and enter CMOS Setup by pressing Delete during the early boot cycle.
2. Change the CMOS parameters as desired and configure the floppy drive as the first boot device:

   ```
   Basic CMOS Configuration | BOOT ORDER | Boot 1st = Drive A:
   ```

3. Save the settings and exit CMOS Setup.
4. Reboot the system from the DOS boot floppy.
5. Run FBU and select Save CMOS contents. A file named CMOS.BIN is created and saved to the floppy.
6. Select the FBU option Load Custom CMOS defaults. A directory of the floppy is displayed.
7. Select the CMOS.BIN file and press the P key to program the new CMOS defaults.
8. Reboot the system from the hard disk. The custom CMOS parameters are now saved as defaults.

Real Time Clock

The I/O Controller Hub (ICH4) on the south bridge board contains a Motorola MC146818A-compatible real-time clock with 256 bytes of battery-backed RAM. The RTC operates on a 32.768 kHz crystal and a separate 3V lithium battery that provides up to seven years of protection. Under normal battery conditions, the clock maintains accurate timekeeping functions when the board is powered off.

SETTING THE CLOCK

The CMOS Setup utility (accessed by pressing the [DEL] key during a system boot) can be used to set the time/date of the real-time clock.

IDE Hard Drive / CD-ROM Interface

One IDE interface is available to connect up to two IDE devices, such as hard disks or CD-ROM drives. Connector JS4 is the IDE controller with a 44-pin connector. Use CMOS Setup to specify the drive parameters of the attached drives.

Note: The two devices connected to this interface are identified as IDE 0 and IDE 1 in CMOS Setup. The CompactFlash device operates on a different IDE channel and is identified as IDE 2. IDE 3 is not used in the EPM-32.

Cable length must be 18" or less to maintain proper signal integrity.

This interface supplies power to 2.5" IDE drives. If you are connecting a 3.5" drive to the interface (using the CBR-4405 44-pin to 40-pin IDE adapter), you must supply external power to the drive.

Table 4: JS4 IDE Hard Drive Connector Pinout

Pin	Signal Name	Function
1	Reset*	Reset signal from CPU
2	Ground	Ground
3	DD7	Data bus bit 7
4	DD8	Data bus bit 8
5	DD6	Data bus bit 6
6	DD9	Data bus bit 9
7	DD5	Data bus bit 5
8	DD10	Data bus bit 10
9	DD4	Data bus bit 4
10	DD11	Data bus bit 11
11	DD3	Data bus bit 3
12	DD12	Data bus bit 12
13	DD2	Data bus bit 2
14	DD13	Data bus bit 13
15	DD1	Data bus bit 1
16	DD14	Data bus bit 14
17	DD0	Data bus bit 0
18	DD15	Data bus bit 15
19	Ground	Ground
20	NC	Key
21	PDMARQ	DMA request
22	Ground	Ground

Pin	Signal Name	Function
23	DIOW	I/O write
24	Ground	Ground
25	DIOR	I/O read
26	Ground	Ground
27	IORDY	I/O ready
28	CSEL	Cable select
29	DMACK*	DMA acknowledge
30	Ground	Ground
31	INTRQ	Interrupt request
32	NC	No connection
33	DA1	Device address bit 1
34	CBLID*	Cable type identifier
35	DA0	Device address bit 0
36	DA2	Device address bit 2
37	CS1	Chip select 1
38	CS3	Chip select 3
39	DASP*	LED
40	Ground	Ground
41	Power	+5.0 V
42	Power	+5.0 V
43	Ground	Ground
44	NC	No connection

JS5 High-Density 80-Pin Connector

Connector JS5 provides interfaces for the following EPM-32 ports:

- Parallel (LPT or floppy)
- Serial (COM1 and COM2)
- PS/2 (keyboard and mouse)
- USB (two devices)
- Ethernet

The connector also provides interfaces to a programmable LED, IDE LED, reset button, and external speaker.

To connect devices to any of these ports, connect the 80-pin connector of the CBR-8001 transition cable to connector JS5 on the EPM-32, then plug the devices into the appropriate connector on the breakout cable.

Note: Optionally, you can manufacture a cable based on the pinout information provided for each interface.

Table 5 shows the pinout for the cable assembly.

Table 5: JS5 High-Density 80-Pin Connector Pinout

JS5 Pin	External Connector	Pin	Signal
A1	**LPT1**	1	Strobe
A2	JA	14	Auto feed
A3	DB-25F	2	Data bit 1
A4		15	Printer error
A5		3	Data bit 2
A6		16	Reset
A7		4	Data bit 3
A8		17	Select input
A9		5	Data bit 4
A10		18	Ground
A11		6	Data bit 5
A12		19	Ground
A13		7	Data bit 6
A14		20	Ground
A15		8	Data bit 7
A16		21	Ground
A17		9	Data bit 8
A18		22	Ground
A19		10	Acknowledge
A20		23	Ground
A21		11	Port Busy
A22		24	Ground
A23		12	Paper End
A24		25	Ground
A25		13	Select
A26	**MISC**	—	No Connect
A27		—	Programmable LED +
A28		—	Programmable LED –
A29		—	Speaker +
A30		—	Speaker –
A31		—	IDE Data LED –
A32		—	IDE Data LED +
A33	**MOUSE**	4	+5V (Protected)
A34	JB	1	Mouse Data
A35	6-pin	3	Ground
A36	Mini-DIN	5	Mouse Clock
A37	**KBD**	4	+5V (Protected)
A38	JC	1	Keyboard Data
A39	6-pin	3	Ground
A40	Mini-DIN	5	Keyboard Clock

JS5 Pin	External Connector	Pin	Signal
B1	**USB CH0**	1	+5V (Protected)
B2	**USB CH1**	6	Ground
B3	JD	2	Channel 0 Data –
B4	10-pin	7	Cable Shield
B5	0.1" Male	3	Channel 0 Data +
B6	Header	8	Channel 1 Data +
B7		4	Cable Shield
B8		9	Channel 1 Data –
B9		5	Ground
B10		10	+5V (Protected)
B11	**ETHERNET**	4	Isolated Ground
B12	JE	5	Isolated Ground
B13	8-pin	6	Receive Data –
B14	RJ-45	3	Receive Data +
B15	Jack	7	Isolated Ground
B16		8	Isolated Ground
B17		2	Transmit Data –
B18		1	Transmit Data +
B19	**PBRESET**	—	Pushbutton Reset
B20		—	Ground
B21	**COM1**	1	Data Carrier Detect
B22	JF	6	Data Set Ready
B23	DB-9M	2	Receive Data
B24		7	Request to Send
B25		3	Transmit Data
B26		8	Clear to Send
B27		4	Data Terminal Ready
B28		9	Ring Indicator
B29		5	Ground
B30		—	No Connect
B31	**COM2**	1	Data Carrier Detect
B32	JG	6	Data Set Ready
B33	DB-9M	2	Receive Data
B34		7	Request to Send
B35		3	Transmit Data
B36		8	Clear to Send
B37		4	Data Terminal Ready
B38		9	Ring Indicator
B39		5	Ground
B40		—	No Connect

The 5V power supplied to pins on this connector is protected by 1 Amp., self-resetting fuses.

Serial Ports

The EPM-32 features two on-board 16550-based serial channels located at standard PC I/O addresses. COM1 is an RS-232 (115.2K baud) serial port. The IRQ line is chosen in CMOS Setup.

COM2 can be operated in RS-232, RS-422 or RS-485 modes. Additional non-standard baud rates are also available (programmable in the normal baud registers) of up to 460k baud. The IRQ line is chosen in CMOS Setup.

Each COM port can be independently enabled or disabled in the CMOS setup screen.

These ports use IEC 61000-4-2-rated TVS components to help protect against ESD damage.

COM Port Configuration

There is no configuration jumper for COM1 since it only operates in RS-232 mode.

Use CMOS Setup to select between RS-232/RS-422/RS485 operating modes for COM2.

Jumper V1[7-8] is used to enable the RS-422/485 termination resistor for COM2. The termination resistor should be enabled for RS-422 and the RS-485 endpoint station. It should be disabled for RS-232 and the RS-485 intermediate station.

COM2 RS-485 Mode Line Driver Control

The TxD+/TxD– differential line driver can be turned on and off by manipulating the COMDIR bit in offset 0 of the Special Control Register. See page 47.

The following code example shows how to toggle the line driver for COM2 when the base address for the Board Control Registers (BCRs) is set to 1D0h.

```
MOV   DX,1D0H    ; POINT TO SPECIAL CONTROL REGISTER
IN    AL,DX      ; FETCH EXISTING VALUE
OR    AL,08H     ; SET BIT D3, COMDIR
OUT   DX,AL      ; WRITE MODIFIED VALUE
```

SERIAL PORT CONNECTORS

Connector JS5 provides interfaces to the COM1 and COM2 ports. See the *Connector Location Diagrams* on page 15 for connector and cable information, and the table on page 28 for JS5 pinout information.

The pinouts below apply to the DB9M connectors on the CBR-8001 breakout cable.

Table 6: COM1 Serial Port Pinout

COM1	
DB9 JF Pin	RS-232
1	DCD
2	RXD*
3	TXD*
4	DTR
5	Ground
6	DSR
7	RTS
8	CTS
9	RI

Table 7: COM2 Serial Port Pinout

COM2			
DB9 JG Pin	RS-232	RS-422	RS-485
1	DCD	—	—
2	RXD*	TxD+	—
3	TXD*	—	—
4	DTR	RxD–	TxD/RxD–
5	Ground	Ground	Ground
6	DSR	—	—
7	RTS	TxD–	—
8	CTS	Ground	Ground
9	RI	RxD+	TxD/RxD+

Parallel / Floppy Port

PARALLEL PORT OPERATION

The EPM-32 includes a standard bi-directional/EPP/ECP compatible LPT port that resides at the PC standard address of 378h. The port can be enabled or disabled and interrupt assignments can be made via CMOS Setup. The LPT mode is also set via CMOS Setup.

This port uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

Connector JS5 provides an interface to the LPT port. See the *Connector Location Diagrams* on page 15 for connector and cable information, and the table on page 28 for JS5 pinout information. The pinout below applies to the DB25F connector on the CBR-8001 breakout cable .

Table 8: JA LPT1 Parallel/Floppy Connector Pinout

CBR-8001 JA Pin	Centronics Signal	Floppy Signal	Signal Direction
1	Strobe	DS0*	Out
2	Data bit 1	INDEX*	In/Out
3	Data bit 2	TRK0*	In/Out
4	Data bit 3	WP*	In/Out
5	Data bit 4	RDATA*	In/Out
6	Data bit 5	DSKCHG	In/Out
7	Data bit 6	N.C.	In/Out
8	Data bit 7	MTR0*	In/Out
9	Data bit 8	N.C.	In/Out
10	Acknowledge	DS1*	In
11	Port Busy	MTR1*	In
12	Paper End	WDATA*	In
13	Select	WGATE*	In
14	Auto feed	RPM	Out
15	Printer error	HDSEL*	In
16	Reset	FDIR	Out
17	Select input	STEP*	Out
18	Ground	GND	—
19	Ground	GND	—
20	Ground	GND	—
21	Ground	GND	—
22	Ground	GND	—
23	Ground	GND	—
24	Ground	GND	—
25	Ground	GND	—

PARALLEL PORT FLOPPY DISK

The parallel port on the EPM-32 can be used as a floppy disk interface. Select “FDD” as the LPT mode in CMOS Setup and connect a floppy disk drive to the parallel connector on VL-CBR-8001 via the VL-CBR-2501 cable to use this feature.

Keyboard and Mouse

Standard PS/2 keyboard and mouse ports are available through connector JS5. These ports use IEC 61000-4-2-rated TVS components to help protect against ESD damage. See the *Connector Location Diagrams* on page 15 for connector and cable information, and the table on page 28 for JS5 pinout information.

The pinout below applies to the PS/2 connectors on the CBR-8001 breakout cable.

Table 9: PS/2 Mouse and Keyboard Connector Pinout

JB Pin	Signal	Description
1	MSDATA	Mouse Data
2	–	No Connection
3	GND	Ground
4	MKPWR	Protected +5V
5	MSCLK	Mouse Clock
6	–	No Connection
JC Pin	**Signal**	**Description**
1	KBDATA	Keyboard Data
2	–	No Connection
3	GND	Ground
4	MKPWR	Protected +5V
5	KBCLK	Keyboard Clock
6	–	No Connection

CompactFlash

Connector JS6 provides a socket for a Type I or Type II CompactFlash (CF) module. This IDE based interface operates on a separate channel than the IDE interface at connector JS4 (IDE 2 in CMOS Setup). The CF interface supports operation in DMA mode.

The following CF modules have been tested and qualified as bootable devices by VersaLogic. As an IDE device, there is no limitation to the capacity of CF module that can be used.

Table 10. Qualified Bootable CF Modules

Manufacturer	Density	Mfg Part Number
Hagiwara	1 GB	CF1-1GMDG(H00AA)
Hagiwara	512 MB	CF1-512MDG(H00AA)
Silicon Systems	256 MB	SSD-C25M-3012, -3500*
Silicon Systems	256 MB	SSD-C25MI-3012, -3500
Silicon Systems	1 GB	SSD-C01G-3012, -3500
Silicon Systems	2 GB	SSD-C02G-3012, -3500
Silicon Systems	2 GB	SSD-C02GI-3012, -3500
Silicon Systems	4 GB	SSD-C04GI-3012, -3500
Silicon Systems	512 MB	SSD-C51M-3012, -3500
Silicon Systems	512 MB	SSD-C51MI-3012, -3500

* Suffix of -3500 denotes RoHS-compliant module.

Programmable LED

Connector JS5 includes an output signal for a software controlled LED. Connect the cathode of the LED to JS5 pin A28; connect the anode to +5V. An on-board resistor limits the current to 15 mA when the circuit is turned on. A programmable LED is provided on the CBR-8001 breakout cable.

To turn the LED on and off, set or clear bit D7 in I/O port 1D0h (or 1E0h). When changing the register, make sure not to alter the value of the other bits.

The following code examples show how to turn the LED on and off. Refer to page 47 for further information.

LED On

```
MOV    DX,1D0H
IN     AL,DX
OR     AL,80H
OUT    DX,AL
```

LED Off

```
MOV    DX,1D0H
IN     AL,DX
AND    AL,7FH
OUT    DX,AL
```

Note: The LED is turned on by the BIOS during system startup. This causes the light to function as a "power on" indicator if it is not otherwise controlled by user code. The BIOS also flashes the LED in sync with “Beep Codes” when an error occurs.

External Speaker

A miniature 8 ohm speaker can be connected between JS5 pin A30 (Speaker -) and JS5 pin A29 (Speaker +). A speaker is provided on the CBR-8001 breakout cable.

Push-Button Reset

Connector JS5 includes an input for a push-button reset switch. Shorting JS5 pin B19 (Pushbutton Reset) to ground causes the EPM-32 to reboot.

This connector uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

A reset button is provided on the CBR-8001 breakout cable.

IDE LED

Connector JS5 includes an output signal for attaching an IDE Activity LED. Connect the cathode of the LED to JS5 pin A32, and connect the anode to +5V. An on-board resistor limits the current to 15 mA when the circuit is turned on. An IDE LED is provided on the CBR-8001 breakout cable.

Video Interface

An on-board video controller integrated into the chipset provides high performance video output for the EPM-32.

CONFIGURATION

The video interface uses PCI interrupt "INTA*". CMOS Setup is used to select the IRQ line routed to INTA*.

The EPM-32 uses shared memory architecture. This allows the video controller to use variable amounts of system DRAM for video RAM. The amount of RAM used for video is set in CMOS Setup with the Custom Configuration > Video Memory parameter. The default allocation is 8 MB. The maximum allocation is 32 MB.

The EPM-32 supports two types of video output, SVGA and LVDS Flat Panel Display. A CMOS setup option is used to select which output is enabled after POST.

VIDEO BIOS SELECTION

Jumper V1[3-4] can be removed to allow the system to boot off of the Secondary Video BIOS. Unlike the Primary Video BIOS, the Secondary Video BIOS can be reprogrammed in the field.

SVGA OUTPUT CONNECTOR

See the *Connector Location Diagram* on page 15 for the connector location. An adapter cable, part number VL-CBR-1201, is available to translate JN3 into a standard 15-pin D-Sub SVGA connector.

This connector uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

Table 11: JN3 Video Output Pinout

JN3 Pin	Signal Name	Function	Mini DB15 Pin
1	GND	Ground	6
2	CRED	Red video	1
3	GND	Ground	7
4	CGRN	Green video	2
5	GND	Ground	8
6	CBLU	Blue video	3
7	GND	Ground	5
8	CHSYNC	Horizontal Sync	13
9	GND	Ground	10
10	CVSYNC	Vertical Sync	14
11	NC	Not Connected	–
12	NC	Not Connected	–

LVDS Flat Panel Display Connector

The integrated LVDS Flat Panel Display in the EPM-32 is an ANSI/TIA/EIA-644-1995 specification-compliant interface. It can support up to 18 bits of RGB pixel data plus 3 bits of timing control (HSYNC/VSYNC/DE) on the 3 differential data output pairs. The LVDS clock frequency ranges from 25 MHz to 112 MHz.

CMOS Setup provides several options for standard LVDS Flat Panel types. If these options do not match the requirements of the panel you are attempting to use, contact Support@VersaLogic.com for a custom video BIOS.

The 3.3V power provided to pins 19 and 20 of JN2 is protected by a 1 Amp fuse.

See the *Connector Location Diagram* on page 15 for the connector location.

Table 12: JN2 LVDS Flat Panel Display Pinout

JN2 Pin	Signal Name	Function
1	GND	Ground
2	NC	Not Connected
3	LVDSA3	Diff. Data (+)
4	LVDSA3#	Diff. Data 3 (–)
5	GND	Ground
6	LVFSCLK0	Differential Clock (+)
7	LVDSCLK0#	Differential Clock (–)
8	GND	Ground
9	LVDSA2	Diff. Data 2 (+)
10	LVDSA2#	Diff. Data 2 (–)
11	GND	Ground
12	LVDSA1	Diff. Data 1 (+)
13	LVDSA1#	Diff. Data 1 (–)
14	GND	Ground
15	LVDSA0	Diff. Data 0 (+)
16	LVDSA0#	Diff. Data 0 (–)
17	GND	Ground
18	GND	Ground
19	+3.3V	Protected Power Supply
20	+3.3V	Protected Power Supply

COMPATIBLE LVDS PANEL DISPLAYS

The following list of flat panel displays are reported to work properly with the integrated graphics video controller chip used on the EPM-32:

Manufacture	Model Number	Panel Size	Resolution	Interface	Panel Technology
eVision Displays	xxx084S01 series	8.4”	800 x 600 18-bit	LVDS	TFT
au Optronix	B084SN01	8.4”	800 x 600 18-bit	LVDS	TFT
eVision Displays	xxx104S01 series	10.4”	800 x 600 18-bit	LVDS	TFT
au Optronix	B104SN01	10.4”	800 x 600 18-bit	LVDS	TFT
eVision Displays	xxx141X01 series	14.1”	1024 x 768 18-bit	LVDS	TFT

Ethernet Interface

The EPM-32 features one on-board Intel 82551ER Ethernet controller. Contact the factory for custom controller configurations. While this controller is not NE2000-compatible, it is widely supported. Drivers are readily available to support a variety of operating systems. See VersaLogic website for latest OS support.

BIOS CONFIGURATION

The Ethernet controller can be enabled or disabled in CMOS Setup. The Ethernet interface uses PCI interrupt "INTC#". CMOS Setup is used to select the IRQ line routed to each PCI interrupt line.

STATUS LED

The Ethernet controller provides a two-colored LED signal to provide an indication of the Ethernet status as follows:

Green LED (Link)

- ON — Active Ethernet cable plugged in
- OFF — Active cable not plugged in or cable not plugged into active hub

Yellow LED (Activity)

- ON — Activity detected on cable
- OFF — No Activity detected on cable

ETHERNET CONNECTOR

Connector JS5 includes an interface to the Ethernet controller. The 82551ER Ethernet controller autodetects 10BaseT/100Base-TX connectors. The Ethernet port uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

The CBR-8001 breakout cable provides an RJ-45 connector to make connections with Category 5 Ethernet cables.

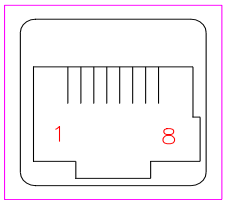


Table 13: RJ45 Ethernet Connector

JE Pin	Fast Ethernet Signal Name	Function
1	T+	Transmit Data +
2	T–	Transmit Data –
3	R+	Receive Data +
4	IGND	Isolated Ground
5	IGND	Isolated Ground
6	R–	Receive Data –
7	IGND	Isolated Ground
8	IGND	Isolated Ground

Audio

The audio interface on the EPM-32 is implemented using the Analog Devices AD1981B Audio Codec. This interface is AC ’97 2.3 compatible. Drivers are available for most Windows-based operating systems. To obtain the most current versions, consult the EPM-32 product support page at **www.VersaLogic.com/private/cheetahsupport.asp.**

JS7 provides the line-level stereo input and line-level stereo output connection points. The outputs will drive any standard-powered PC speaker set.

These connectors use IEC 61000-4-2-rated TVS components to help protect against ESD damage.

SOFTWARE CONFIGURATION

The audio interface uses PCI interrupt “INTB#”. CMOS Setup is used to select the IRQ line routed to INTB#.

The audio controller can be disabled within CMOS Setup.

Table 14: JS7 Audio Connector

JS7 Pin	Signal Name	Function
1	LINE_OUTR	Line-Out Right
2	Ground	Ground
3	LINE_OUTL	Line-Out Left
4	Ground	Ground
5	LINE_INR	Line-In Right
6	Ground	Ground
7	LINE_INL	Line-In Left
8	Ground	Ground

USB Interface

The USB interface on the EPM-32 is UHCI (Universal Host Controller Interface) and EHCI (Enhance Host Controller Interface) compatible, which provides a common industry software/hardware interface.

The USB controller can be enabled or disabled in CMOS Setup. The USB controller uses PCI interrupt "INTA#" and "INTD#". CMOS Setup is used to select the IRQ line routed to each PCI interrupt line.

This connector uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

There are two USB ports accessible on JS5. See the *Connector Location Diagrams* on page 15 for connector and cable information, and the table on page 28 for JS5 pinout information.

The pinout below applies to the USB connectors on the CBR-8001 breakout cable.

Table 15: JD USB 2.0 Interface Connector

JD Pin	Signal Name	Function
1	USBP0PWR	+5V (Protected)
2	USBP0–	Channel 0 Data –
3	USBP0+	Channel 0 Data +
4	GND	Cable Shield
5	GND	Ground
6	GND	Ground
7	GND	Cable Shield
8	USBP1+	Channel 1 Data +
9	USBP1–	Channel 1 Data –
10	USBP1PWR	+5V (Protected)

Warning! The 10-pin USB header on CBR-8001 is not numbered in the conventional manner for dual-row headers. Care must be taken to attach the USB adapter cables, as shown in Figure 14, to prevent voltage reversal.

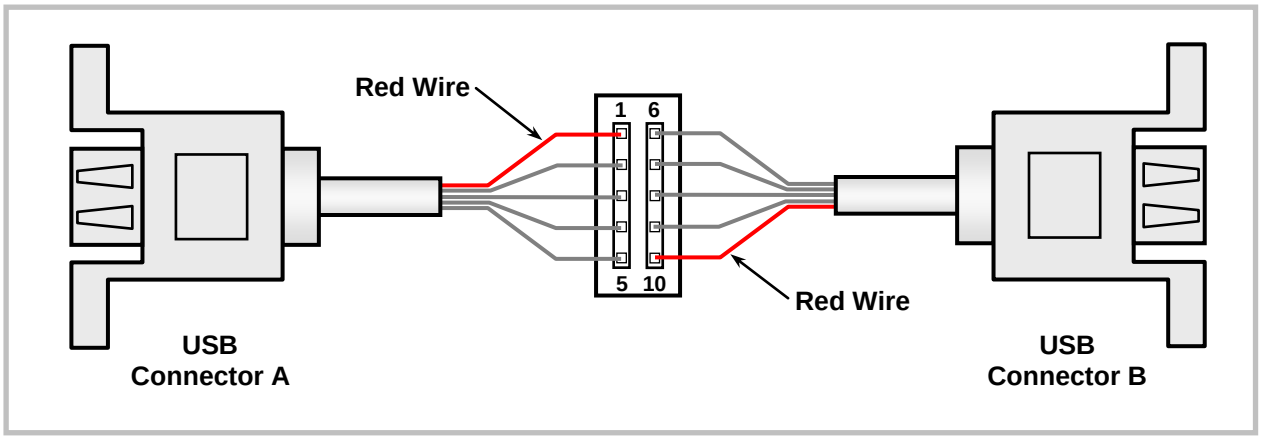


Figure 14. USB Header Pin Orientation

PC/104 Expansion Bus

The EPM-32 will accept up to four PC/104 and four PC/104-*Plus* expansion modules.

ARRANGING THE STACK

If PC/104-*Plus* modules are used, they go on the stack first (closest to the EPM-32 circuit board). The first module is called "slot 0," the next module is "slot 1," and the third module is "slot 2." Make sure to correctly configure the "slot position" jumpers on each PC/104-*Plus* module to match its physical position in the stack.

PC/104 modules are stacked below the PC/104-*Plus* modules; 16-bit modules first, followed by 8-bit PC/104 modules. Lastly, non-standard modules, which lack feed through connectors, should be assembled on the bottom of the stack.

I/O CONFIGURATION

PC/104 (ISA Bus) Modules

PC/104 I/O modules should be addressed in the 100h – 3FFh, address range. Care must be taken to avoid the I/O addresses shown in the *On-Board I/O Devices* table on page 45. These ports are used by on-board peripherals and video devices.

PC/104-Plus *(PCI Bus) Modules*

The BIOS automatically configures the I/O, memory and interrupt resources of PC/104-*Plus* modules. CMOS Setup may be used to disable modules or select IRQ assignment.

Watchdog Timer

A watchdog timer circuit is included on the EPM-32 to reset the CPU or issue an NMI if proper software execution fails or a hardware malfunction occurs.

ENABLING THE WATCHDOG

Bit D0 in I/O port 1D0h (or 1E0h) is used to enable or disable the watchdog from resetting the CPU on timer expiration. Bit D1 in I/O port 1D0h (or 1E0h) is used to enable or disable the watchdog from issuing a NMI on timer expiration. When changing the contents of the register, make sure not to alter the value of the other bits. The following procedure should be used when enabling the watchdog to prevent erroneous resets or NMI generation.

The following code example enables the watchdog reset:

```
        MOV   DX,1D2H  ;RESET THE WATCHDOG STATUS BIT
        IN    AL,DX
        OR    AL,04H
        OUT   DX,AL

LOOP:   MOV   DX,1D0H  ;LOOP WHILE BIT D2 (WDOG_STA) = 0
        IN    AL,DX
        AND   AL,04H
        JZ    LOOP

        MOV   DX,1D2H  ;RESET THE WATCHDOG STATUS BIT AGAIN
        IN    AL,DX
        OR    AL,04H
        OUT   DX,AL

        MOV   DX,1D0H  ;ENABLE THE WATCHDOG (RESET MODE)
        IN    AL,DX
        OR    AL,01H
        OUT   DX,AL
```

Note: The watchdog is disabled when the EPM-32 is powered on or reset.

DISABLING THE WATCHDOG

The watchdog may be disabled at any time by clearing the above mentioned bits; no special procedure is required.

REFRESHING THE WATCHDOG

If the watchdog timer is enabled, software must periodically refresh the watchdog timer at a rate faster than the timer is set to expire (1.0 sec minimum). Outputting a 5Ah to the Watchdog Timer Hold-Off Register at 1D1h (or 1E1h) resets the watchdog time-out period; see page 48 for additional information. There is no provision for selecting a different timeout period using software. The following code example refreshes the watchdog:

```
        MOV   DX,1D1H
        MOV   AL,5AH
        OUT   DX,AL
```

CPU Temperature Monitor

A thermometer circuit constantly monitors the die temperature of the CPU. This circuit can be used to detect over-temperature conditions which can result from fan or heat sink failure or excessive ambient temperatures.

The system can be configured to generate a Non-Maskable Interrupt (NMI) when the temperature exceeds the threshold.

The CMOS setup is used to set the temperature detection threshold. A status bit in the Special Control Register bit D5 if I/O port 1D0h (or 1E0h), can be read to determine if the die temperature is above the threshold.

Contact the factory for information on clearing the status bit or reading and writing to the thermometer circuit. See page 47 for additional information.

Memory and I/O Map

MEMORY MAP

The lower 1 MB memory map of the EPM-32 is arranged as shown in the following table.

Various blocks of memory space between C0000h and FFFFFh can be shadowed. The CMOS setup is used to enable or disable this feature.

Table 16: Memory Map

Start Address	End Address	Comment
E0000h	FFFFFh	System BIOS
D0000h	DFFFFh	PC/104
C0000h	CFFFFh	Video BIOS
A0000h	BFFFFh	Video RAM
00000h	9FFFFh	System RAM

I/O MAP

The following table lists the I/O devices in the EPM-32 I/O map. The I/O space range for the EPM-32 is 000h to 3FFh (10-bit decoding). User I/O devices should be added with care to avoid the devices already in the map as shown in the following table.

Table 17: On-Board I/O Devices

I/O Device	Standard I/O Addresses	Alternate * I/O Addresses
Super I/O	02Eh – 02Fh	
Secondary Hard Drive Controller	170h – 177h	
Special Control Register	1D0h	1E0h
Watchdog Hold-Off Register	1D1h	1E1h
Jumper and Status Register	1D2h	1E2h
Primary Hard Drive Controller	1F0h – 1F7h	
COM2 Serial Port	2F8h – 2FFh	
LPT1 Parallel Port	378h – 37Fh	
SVGA Video	3B0h – 3DFh	
Floppy Disk Controller	3F0h – 3F7h	
COM1 Serial Port	3F8h – 3FFh	

** User selectable via CMOS Setup*

Note: The I/O ports occupied by on-board devices are freed up when the device is disabled in the CMOS setup.

Interrupt Configuration

The EPM-32 has the standard complement of PC type interrupts. Ten non-shared interrupts are routed to the PC/104 bus, and up to four IRQ lines can be allocated to PCI devices. There are no interrupt configuration jumpers. All configurations are handled through the CMOS setup. If you need to use interrupt lines on the PC/104 bus, IRQ5, 9 or 10 are recommended.

Table 18: EPM-32 IRQ Settings.

● = default setting O = allowed setting

Source	IRQ															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Timer 0	●															
Keyboard		●														
Slave PIC			●													
COM1				O	●	O		O		O	O	O				
COM2				●	O	O		O		O	O	O				
Floppy							●									
LPT1*				O	O	O		●		O	O	O				
RTC									●							
Mouse													●			
Math Chip														●		
Pri. IDE															●	
Sec. IDE																●
ISA IRQ3				O												
ISA IRQ4					O											
ISA IRQ5						O										
ISA IRQ6							O									
ISA IRQ7								O								
ISA IRQ9										O						
ISA IRQ10											O					
ISA IRQ11												O				
ISA IRQ12													O			
ISA IRQ14															O	
ISA IRQ15																O
PCI INTA#				O	O	O		O		O	O	●				
PCI INTB#				O	O	O		O		O	O	●				
PCI INTC#				O	O	O		O		O	O	●				
PCI INTD#				O	O	O		O		O	O	●				

* When LPT1 is in floppy disk mode, the pins change function, the LPT device is no longer available, and the floppy disk controller uses IRQ 6.

Table 19: PCI Interrupt Settings

● = default setting O = allowed setting

Source	PCI Interrupt			
	INTA#	INTB#	INTC#	INTD#
Video	●			
Audio		●		
USB	●			
SMBus		●		
IDE			●	
USB				●
Ethernet			●	

Special Control Register

SCR (READ/WRITE) 1D0h (or 1E0h via CMOS Setup)

D7	D6	D5	D4	D3	D2	D1	D0
PLED	Reserved	OVERTEMP	HDOGNMI	COMDIR	WDOG_STA	WDOG_NMI	WDOG_RST

Table 20: Special Control Register Bit Assignments

Bit	Mnemonic	Description
D7	PLED	**Light Emitting Diode** — Controls the programmable LED on connector J4. PLED = 0 Turns LED off PLED = 1 Turns LED on
D6	Reserved	**Reserved** — This bit has no function.
D5	OVERTEMP	**Temperature Status —** Indicates CPU temperature. OVERTEMP = 0 CPU temperature is below value set in the CMOS setup OVERTEMP = 1 CPU temperature is above value set in the CMOS setup ***Note:*** *This bit is a read-only bit.*
D4	HDOGNMI	**Non-Maskable Interrupt Enable** — Controls the generation of NMIS whenever the CPU temperature sensor detects an over-temperature condition. HDOGNMI = 0 Disable HDOGNMI = 1 Enable
D3	COMDIR	**COM2 RS-485 Transmit Enable** — Enables the RS-485 transmitter. COMDIR = 0 Receive COMDIR = 1 Transmit
D2	WDOG_STA	**WDOG STATUS** — Indicates if the watchdog timer has expired. WDOG_STA = 0 Timer has not expired WDOG_STA = 1 Timer has expired ***Note:*** *Do not write to this bit.*
D1	WDOG_NMI	**Watchdog Non-Maskable Interrupt Enable** — Enables the generation of a NMI when the watchdog timer expires. WDOG_NMI = 0 Disables WDOG_NMI = 1 Enables
D0	WDOG_RST	**Watchdog Reset Enable** — Enables and disables the watchdog timer reset circuit. WDOG_RST = 0 Disables WDOG_RST = 1 Enables

Revision Indicator Register

REVIND (READ ONLY) 1D1h (or 1E1h via CMOS Setup)

D7	D6	D5	D4	D3	D2	D1	D0
PC4	PC3	PC2	PC1	PC0	REV2	REV1	REV0

This register is used to indicate the revision level of the EPM-32.

Bit	Mnemonic	Description
D7-D3	PC4-PC0	**Product Code** — These bits are hard-coded to represent the product type. The EPM-32 always reads as 11000. Other codes are reserved for future products. **PC4 PC3 PC2 PC1 PC0 Product Code** 1 1 0 1 0 EPM-32 ***Note:*** *These bits are read-only.*
D2-D0	REV2-REV0	**Revision Level** — These bits represent the EPM-32 circuit revision level. **REV2 REV1 REV0 Revision Level** 0 0 0 Initial product release, EPM-32c, p, v 1 0 0 EPM-32e, t ***Note:*** *These bits are read-only.*

Watchdog Timer Hold-Off Register

WDHOLD (WRITE ONLY) 1D1h (or 1E1h via CMOS Setup)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	1	0

A watchdog timer circuit is included on the EPM-32 board to reset the CPU and/or generate a NMI if proper software execution fails or a hardware malfunction occurs. The watchdog timer is controlled by the SCR and JSR.

If the watchdog timer is enabled, software must periodically refresh the watchdog timer at a rate faster than the timer is set to expire (1000 ms minimum). Writing 5Ah to WDHOLD resets the watchdog timeout period.

Jumper and Status Register

JSR (READ/WRITE) 1D2h (or 1E2h via CMOS Setup)

D7	D6	D5	D4	D3	D2	D1	D0
GPI	VB-SEL	SB-SEL	Reserved	Reserved	WDOG_CLR	Reserved	Reserved

Table 21: Jumper and Status Register Bit Assignments

Bit	Mnemonic	Description
D7	GPI	**General Purpose Input** — Indicates the status of jumper V1[5-6] . GPI = 0 Jumper Out GPI = 1 Jumper In ***Note:*** *This is a read-only bit.*
D6	VB-SEL	**Video BIOS Selection** — Indicates the status of jumper V1[3-4]. VB-SEL = 0 Jumper out, Secondary Video BIOS selected VB-SEL = 1 Jumper in, Primary Video BIOS selected ***Note:*** *This is a read-only bit.*
D5	SB-SEL	**System BIOS Selection** — Indicates the status of jumper V1[1-2]. SB-SEL = 0 Jumper out, Master System BIOS selected SB-SEL = 1 Jumper in, Run Time System BIOS selected ***Note:*** *This is a read-only bit.*
D4-D3	Reserved	**Reserved** — These bits have no function.
D2	WDOG_CLR	**Watchdog Clear** — Write a 1 to this bit to clear the WDOG_STA bit in the SCR register (1D0h).
D1-D0	Reserved	**Reserved** — These bits have no function.

Appendix A – References



PC Chipset *855GME Chipset*	Intel Corporation (http://developer.intel.com)
Ethernet Controller *Intel 82541ER* *Intel 82551ER*	Intel Corporation (http://developer.intel.com)
Video Controller	Extreme Graphics 2 chip set (http://developer.intel.com)
PC/104 Specification *PC/104 Resource Guide*	PC/104 Consortium (http://www.controlled.com/pc104)
PC/104-*Plus* Specification *PC/104 Resource Guide*	VersaLogic Corporation (http://www.VersaLogic.com)
CPU Chips *Pentium M® /Celeron M®*	Intel Corporation (http://developer.intel.com)
General PC Documentation *The Programmer's PC Sourcebook*	Microsoft Press (http://www.microsoft.com/learning/books/)
General PC Documentation *The Undocumented PC*	Powell's Books (http://www.powells.com)

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