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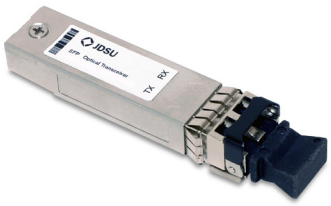
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Find the *VIAVI Solutions / JDSU PLRXPL-VE-SG4-62* at our website: *Click HERE*

RoHS-Compliant 4.25, 2.125, 1.063 Gbps 850 nm SFP Transceiver

PLRXPL-VE-SG4-62-x



Key Features

- Compliant with industry-wide physical and optical specifications
- RoHS-compliant
- Superior EMI performance
- Cost effective SFP solution
- Triple-rate FC performance
- Enables higher port densities
- Enables greater bandwidth
- Proven high reliability
- In-house precision alignment

Applications

- High-speed storage area networks
  - Switch and hub interconnect
  - Mass storage systems interconnect
  - Host adapter interconnect
- Computer cluster cross-connect
- Custom high-speed data pipes

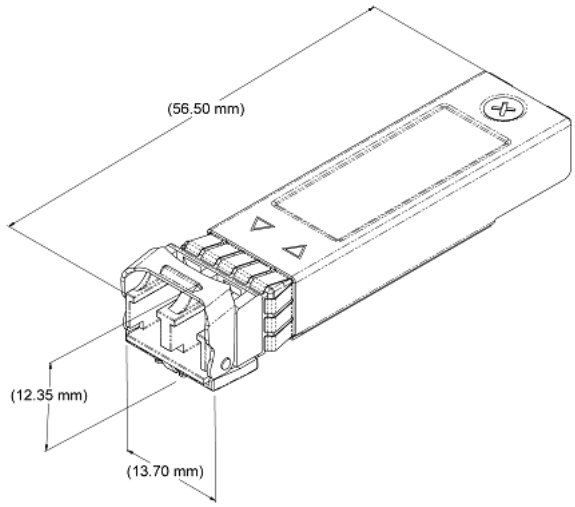
This RoHS-compliant multi-rate Small Form Factor Pluggable (SFP) transceiver provides superior performance for Fibre Channel applications, and is another in JDSU's family of products customized for high speed, short reach SAN, and intra-POP applications. The multi-rate feature enables its use in a wider range of system applications. It is fully compliant with FC-PI 100-M5/M6-SN-I, 200-M5/M6-SN-I, and 400-M5/M6-SN-I specifications. The rate select pin (pin 7) provides receiver bandwidth switching between 4.25G /2.125G and 2.125/1.0625G line rates for optimized link performance enabling hardware or software based rate-negotiation system architectures. JDUS's improved housing provides improved EMI performance for demanding 4GFC applications. This transceiver features a highly reliable 850 nm oxide vertical-cavity surface-emitting laser (VCSEL) coupled to a LC optical connector. Its small size allows for high-density board designs that, in turn, enable greater total aggregate bandwidth.

Highlights

- 4GFC, 2GFC, and 1GFC and 1GBE multiple rate performance enables flexible system design, and configuration, while maximizing bandwidth
- RoHS-compliant per Directive 2002/95/EC
- Enhanced digital diagnostic feature set allows real-time monitoring of transceiver performance and system stability.
- Bail mechanism enables superior ergonomics and functionality in all port configurations
- Extended voltage and extended temperature
- MSA-compliant small form factor footprint enables high port density and keeps overall system cost low
- Serial ID allows customer and vendor system specific information to be placed in transceiver
- All-metal housing provides superior EMI performance

PLRXPL-VE-SG4-62-x Features

- Utilizes a highly reliable, high-speed, 850nm, oxide VCSEL
- RoHS-compliant
- All-metal housing for superior EMI performance
- Hot pluggable
- Digital diagnostics, SFF-8472 rev 9.5 compliant
- Compliant with Fibre Channel 400-M5/M6-SN-I, 200-M5/M6-SN-I, and 100-M5/M6-SN-I
- Selectable 4G/2G/1G receiver bandwidth with rate select pin 7 or through digital diagnostics interface
- Low nominal power consumption (400 mW)
- -20°C to 85°C operating temperature range
- Single +3.3 V power supply
- ±10% extended operating voltage range
- Bit error rate < 1 x 10^{-12}
- OC Transmit disable, loss of signal and transmitter fault functions
- CDRH and IEC 60825-1 Class 1 laser eye safe
- FCC Class B compliant
- ESD Class 2 per MIL-STD 883 Method 3015
- UL-94 V-0 certified
- Internal AC coupling on both transmit and receive data signals



An eye-safe, cost effective serial transceiver, the PLRXPL-VE-SG4-62 features a small, low power, pluggable package that manufacturers can upgrade in the field, adding bandwidth incrementally. The robust mechanical design features a unique all-metal housing that provides superior EMI shielding.

Section 1 Functional Description

The PLRXPL-VE-SG4-62-x 850 nm VCSEL Gigabit Transceiver is designed to transmit and receive 8B/10B encoded serial optical data over 50/125 µm or 62.5/125 µm multimode optical fiber.

Transmitter

The transmitter converts 8B/10B encoded serial PECL or CML electrical data into serial optical data meeting the requirements of 100-M5/M6-SN-I, 200-M5/M6-SN-I, and 400-M5/M6-SN-I Fibre Channel specifications. Transmit data lines (TD+ & TD-) are internally AC coupled with 100 Ω differential termination.

An open collector compatible Transmit Disable (Tx_Dis) is provided. This pin is internally terminated with a 10 kΩ resistor to Vcc_T. A logic "1," or no connection on this pin will disable the laser from transmitting. A logic "0" on this pin provides normal operation.

The transmitter has an internal PIN monitor diode that is used to ensure constant optical power output across supply voltage and temperature variations.

An open collector compatible Transmit Fault (TFault) is provided. The Transmit Fault signal must be pulled high on the host board for proper operation. A logic "1" output from this pin indicates that a transmitter fault has occurred, or the part is not fully seated and the transmitter is disabled. A logic "0" on this pin indicates normal operation.

Receiver

The receiver converts 8B/10B encoded serial optical data into serial PECL/CML electrical data. Receive data lines (RD+ & RD-) are internally AC coupled with 100 Ω differential source impedance, and must be terminated with a 100 Ω differential load.

Rate select, pin 7, switches the receiver bandwith enabling superior performance at 4.25 Gbps, 2.125 Gbps, and 1.0625 Gbps line rates. With non rate-select part numbers or when rate-select is set "high" (4.25/2.125 Gbps mode) on rate-select part numbers, the receiver bandwidth is not compliant to the maximum receiver bandwidth specified under 100-M5/M6-SN-I.

Table 1 FC Compliance with Rate Select

Parameter	100-M5/M6-SN-I	200-M5/M6-SN-I	400-M5/M6-SN-I
High and -N part numbers	No[1]	Yes	Yes
Low	Yes	Yes	No

1. Not compliant with CD lasers

4

An open collector compatible Loss of Signal is provided. The LOS must be pulled high on the host board for proper operation. A logic "0" indicates that light has been detected at the input to the receiver (see Section 2.5 Optical characteristics, Loss of Signal Assert/Deassert Time on page 10). A logic "1" output indicates that insufficient light has been detected for proper operation.

Power supply filtering is recommended for both the transmitter and receiver. Filtering should be placed on the host assembly as close to the Vcc pins as possible for optimal performance.

Recommended "Application Schematics" are shown in Figure 2 on page 5.

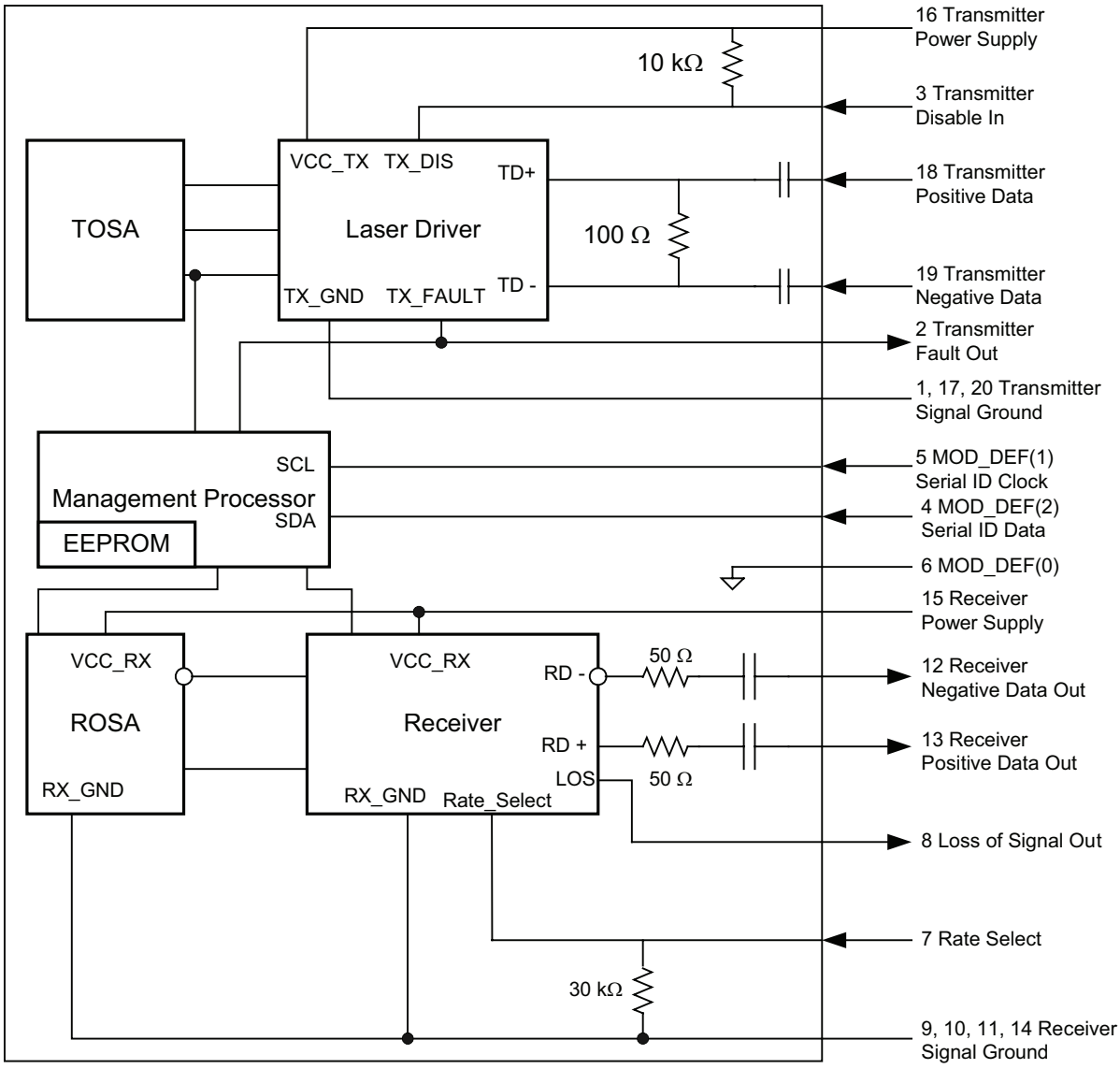
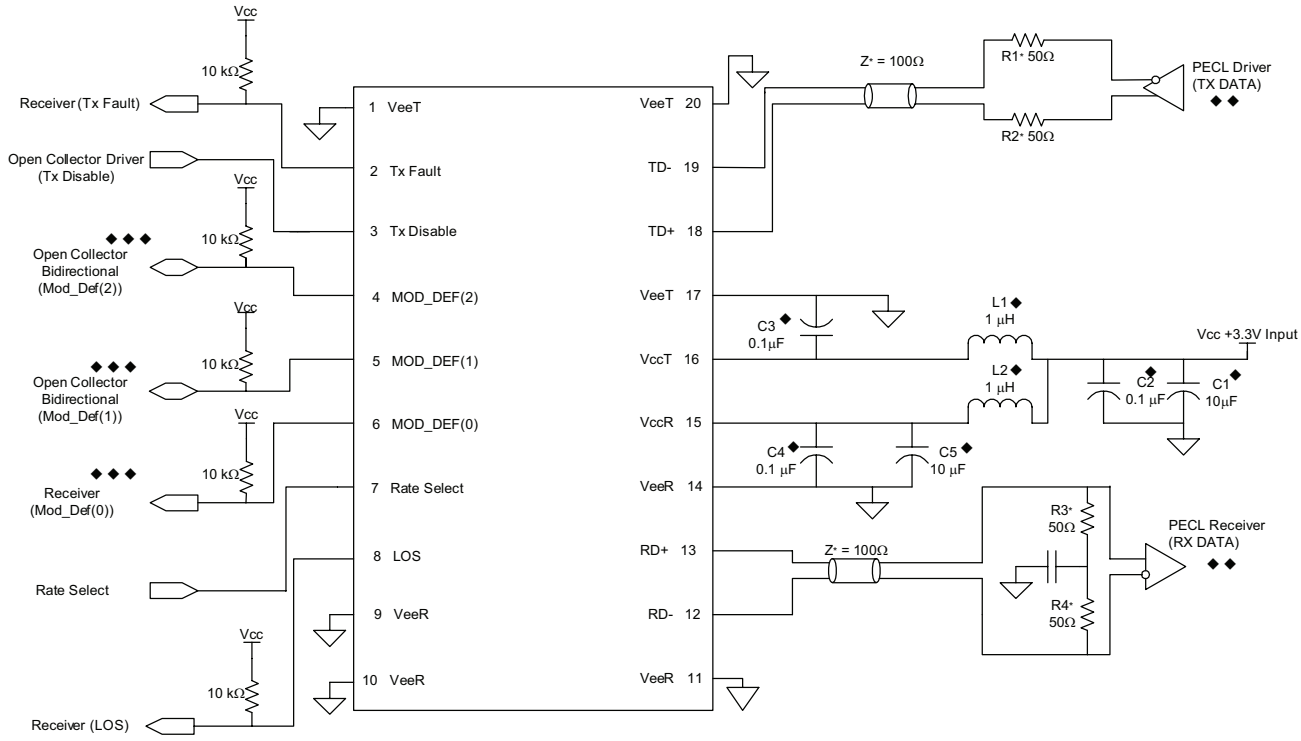


Figure 1 Block diagram

Section 2 Application Schematics

Recommended connections to the PLRXPL-VE-SG4-62-x transceiver are shown in Figure 2 below.



Notes

◆ Power supply filtering components should be placed as close to the V_{cc} pins of the host connector as possible for optimal performance.

◆◆ PECL driver and receiver will require biasing networks. Please consult application notes from suppliers of these components. CML I/O on the PHY are supported.

◆◆◆ MOD_DEF(2) and MOD_DEF(1) should be bi-directional open collector connections in order to implement serial ID (MOD_DEF[0,1,1]) PLRXPL-VE-S64-62-x transceiver.

◆◆◆◆ R1 and R2 may be included in the output of the PHY. Check application notes of the IC in use.

* Transmission lines should be 100 Ω differential traces. It is recommended that the termination resistor for the PECL Receiver (R3 + R4) be placed beyond the input pins of the PECL Receiver. Series Source Termination Resistors on the PECL Driver (R1+R2) should be placed as close to the driver output pins as possible

Figure 2 Recommended application schematic for the PLRXPL-VE-SG4-62-x transceiver

2.1 Technical data

Technical data related to the RoHS-Compliant 4.25 Gbps 850 nm SFP Transceivers includes:

- Section 2.2 Pin function definitions below
- Section 2.3 Absolute maximum ratings on page 8
- Section 2.4 Electrical characteristics on page 8
- Section 2.5 Optical characteristic on page 10
- Section 2.6 Link length on page 11
- Section 2.7 Regulatory compliance on page 12
- Section 2.8 PCB layout on page 13
- Section 2.9 Front panel opening on page 14
- Section 2.10 Module outline on page 14
- Section 2.11 Transceiver belly-to-belly mounting on page 15

2.2 Pin function definitions

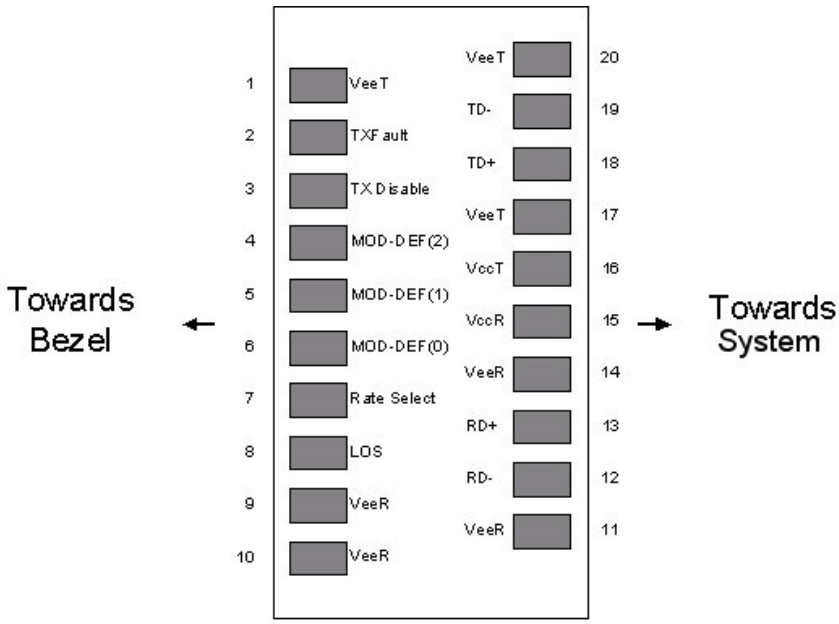


Figure 3 Transceiver pin descriptions

Table 2 Transceiver pin descriptions

Pin Number	Symbol	Name	Description
Receiver			
8	LOS	Loss of Signal Out (OC)	Sufficient optical signal for potential BER < $1x10^{-12}$ = Logic "0" Insufficient optical signal for potential BER < $1x10^{-12}$ = Logic "1" This pin is open collector compatible, and should be pulled up to Host Vcc with a 10 kΩ resistor.
9, 10, 11, 14	VeeR	Receiver Signal Ground	These pins should be connected to signal ground on the host board.
12	RD-	Receiver Negative DATA Out (PECL)	Light on = Logic "0" Output Receiver DATA output is internally AC coupled and series terminated with a 50 Ω resistor.
13	RD+	Receiver Positive DATA Out (PECL)	Light on = Logic "1" Output Receiver DATA output is internally AC coupled and series terminated with a 50 Ω resistor.
15	VccR	Receiver Power Supply	This pin should be connected to a filtered +3.3V power supply on the host board. See Application schematics on page 5 for filtering suggestions.
7	Rate	Rate Select (LVTTL)	This pin should be connected to the auto-negotiation rate select function Logic "1" and -N part numbers = 4.25Gbps/2.125Gbps Logic "0" = 2.125Gbps/1.25Gbps
Transmitter			
3	TX Disable	Transmitter Disable In (LVTTL)	Logic "1" Input (or no connection) = Laser off Logic "0" Input = Laser on This pin is internally pulled up to Vcc_T with a 10 kΩ resistor.
1, 17, 20	VeeT	Transmitter Signal Ground	These pins should be connected to signal ground on the host board.
2	TX Fault	Transmitter Fault Out (OC)	Logic "1" Output = Laser Fault (Laser off before t_fault) Logic "0" Output = Normal Operation This pin is open collector compatible, and should be pulled up to Host Vcc with a 10 kΩ resistor.
16	VccT	Transmitter Power Supply	This pin should be connected to a filtered +3.3V power supply on the host board. See Application schematics on page 5 for filtering suggestions.
18	TD+	Transmitter Positive DATA In (PECL)	Logic "1" Input = Light on Transmitter DATA inputs are internally AC coupled and terminated with a differential 100 Ω resistor.
19	TD-	Transmitter Negative DATA In (PECL)	Logic "0" Input = Light on Transmitter DATA inputs are internally AC coupled and terminated with a differential 100 Ω resistor.
Module Definition			
6, 5, 4	MOD_DEF(0:2)	Module Definition Identifiers	Serial ID with SFF 8472 Diagnostics (See section 3.1) Module Definition pins should be pulled up to Host Vcc with 10 kΩ resistors.

2.3 Absolute maximum ratings

Parameter	Symbol	Ratings	Unit
Storage temperature	T_{st}	-40 to +95	°C
Operating case temperature	T_c	-20 to +85	°C
Power supply voltage	V_{cc}	0 to +4.0	V_{P-P}
Transmitter differential input voltage	V_D	2.5	V
Relative humidity	RH	5 to 95	%

2.4 Electrical characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Supply voltage	V_{cc}	2.97	3.3	3.63	V	
Data rate		1.0	2.125	4.25	Gbps	BER < $1x10^{-12}$
Transmitter						
Supply current	I_{CCT}		40	70	mA	
Data input voltage swing	V_{TDp-p}	250	800	2200	mV_{p-p}	Differential, peak to peak
Data input rise/fall time		40		80	ps	20% - 80%, differential 4 GBd operation [3]
Data input rise/fall time		40		175	ps	20% - 80%, differential 2 GBd operation [3]
Data input rise/fall time		40		350	ps	20% - 80%, differential 1 GBd operation only [3]
Data input skew				20	ps	
Data input deterministic jitter	DJ			0.12	UI	±K28.5 pattern, δ_T, @ 1.062 Gbps [1, 5]
Data input deterministic jitter	DJ			0.14	UI	±K28.5 pattern, δ_T, @ 2.125 Gbps [1, 5]
Data input deterministic jitter	DJ			0.14	UI	±K28.5 pattern, δ_T, @ 4.25 Gbps [1, 5]
Data input total jitter	TJ			0.25	UI	2^7-1 pattern, δ_T, BER < $1x10^{-12}$, @ 1.062 Gbps [1, 5]
Data input total jitter	TJ			0.26	UI	2^7-1 pattern, δ_T, BER < $1x10^{-12}$, @ 2.125Gbps [1, 5]
Data input total jitter	TJ			0.26	UI	2^7-1 pattern, δ_T, BER < $1x10^{-12}$, @ 4.25 Gbps [1, 5]
Transmit disable voltage level	V_{IH} V_{IL}	V_{cc} -1.0 0		V_{cc} 0.8	V V	Laser output disabled after T_{TD} if input level is V_{IH}; laser output enabled after T_{TEN} if input level is V_{IL}
Transmit disable/enable assert time	T_{TD} T_{TEN}			10 1	µs ms	Laser output disabled after T_{TD} if input level is V_{IH}; laser output enabled after T_{TEN} if input level is V_{IL}
Transmit fault output voltage level	V_{OH} V_{OL}	V_{cc} -0.5 0		V_{cc} 0.5	V V	Transmit fault level is V_{OH} and Laser output disabled T_{Fault} after laser fault.
Transmit fault assert and reset times	T_{Fault} T_{Reset}	 10		100	µs µs	Transmitter fault is V_{OL} and Laser output restored T_{INI} after transmitter disable is asserted for T_{Reset}, then disabled.
Initialization time	T_{INI}			300	ms	After hot plug or Vcc ≥ 2.97V

2.4 Electrical characteristics (continued)

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Receiver						
Supply current	I_{CCR}		85	120	mA	
Data output voltage swing		600	720	1300	mV_{p-p}	R_{LOAD} = 100 Ω, differential
Data output rise/fall time			80	120	ps	20% - 80%, differential
Data output skew				40	ps	R_{LOAD} = 100 Ω, differential
Data output deterministic jitter	DJ			0.36	UI	±K28.5 pattern, δ_R, @ 1.062 Gbps [1,9]
Data output deterministic jitter	DJ			0.39	UI	±K28.5 pattern, δ_R, @ 2.125 Gbps [1,5]
Data output deterministic jitter	DJ			0.39	UI	±K28.5 pattern, δ_R, @ 4.25 Gbps [1,5]
Total jitter	TJ			0.61	UI	2^7-1 pattern, δ_R , BER < $1x10^{-12}$ @ 1.062 Gbps [1,5]
Total jitter	TJ			0.64	UI	2^7-1 pattern, δ_R , @ 2.125 Gbps [1,5]
Total jitter	TJ			0.64	UI	2^7-1 pattern, δ_R , @ 4.25 Gbps [1,5]
Loss of signal voltage level	V_{OH}	V_{cc} -0.5		V_{cc}	V	LOS output level V_{OL} T_{LOSD} after light input > LOSD [2]
	V_{OL}	0		0.5	V	LOS output level V_{OH} T_{LOSA} after light input < LOSA [2]
Loss of signal assert/deassert time	T_{LOSA}			100	µs	LOS output level V_{OL} T_{LOSD} after light input > LOSD [2]
	T_{LOSD}			100	µs	LOS output level V_{OH} T_{LOSA} after light input < LOSA [2]

δ

2.5 Optical characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Transmitter						
Wavelength	λ_p	840	850	860	nm	
RMS spectral width	$\Delta\lambda$		0.5	0.85	nm	
Average optical power	P_{AVG}	-9		-2.5	dBm	
Optical output rise/fall time	$t_{rise/fall}$			90	ps	20% - 80%
Optical modulation amplitude	OMA	250		1125	µW	
Deterministic jitter	DJ			0.21	UI	±K28.5 pattern, γ_T, @ 1.062 Gbps [1,5]
Deterministic jitter	DJ			0.26	UI	±K28.5 pattern, γ_T, @ 2.125 Gbps [1,5]
Deterministic jitter	DJ			0.26	UI	±K28.5 pattern, γ_T, @ 4.25 Gbps [1,5]
Total jitter	TJ			0.43	UI	2^7-1 pattern, γ_T, @ 1.062 Gbps [1,5]
Total jitter	TJ			0.44	UI	2^7-1 pattern, γ_T, @ 2.125 Gbps [1,5]
Total jitter	TJ			0.44	UI	2^7-1 pattern, γ_T, @ 4.25 Gbps [1,5]
Relative intensity noise	RIN		-125	-118	dB/Hz	12 dB reflection
Receiver						
Wavelength	λ	770	850	860	nm	
Maximum input power	Pm	0			dBm	
Sensitivity (OMA)	S_1		18	31	μW_{p-p}	1 Gbps operation, maximum is equivalent to -17dBm @9dB ER
	S_2		25	49	μW_{p-p}	2 Gbps operation
	S_4			61	μW_{p-p}	4 Gbps operation
Stressed Sensitivity (OMA) S_{S1}	ISI = 0.96dB	55			μW_{p-p}	1G operation
	ISI = 2.18dB	67			μW_{p-p}	1G operation
Stressed Sensitivity (OMA) S_{S2}	ISI = 1.26dB	96			μW_{p-p}	2G operation
	ISI = 2.03dB	109			μW_{p-p}	2G operation
Stressed Sensitivity (OMA) S_{S4}	ISI = 1.67dB	138			μW_{p-p}	4G operation
	ISI = 2.14dB	148			μW_{p-p}	4G operation
Loss of signal assert/deassert level	LOSD			-17	dBm	Chatter free operation
	LOSA	-30			dBm	Chatter free operation
Low frequency cutoff	F_C		0.2	0.3	MHz	-3 dB, P<-16 dBm

2.6 Link length

Data Rate / Standard	Fiber Type	Modal Bandwidth @ 850 nm (MHz*km)	Distance Range (m)	Notes
1.0625 GBd	62.5/125 µm MMF	200	2 to 300	6
Fibre Channel	50/125 µm MMF	500	2 to 500	6
100-M5-SN-I	50/125 µm MMF	900	2 to 630	6
100-M6-SN-I	50/125 µm MMF	1500	2 to 755	6
	50/125 µm MMF	2000	2 to 860	6
2.125 GBd	62.5/125 µm MMF	200	2 to 150	6
Fibre Channel	50/125 µm MMF	500	2 to 300	6
200-M5-SN-I,	50/125 µm MMF	900	2 to 350	6
200-M6-SN-I	50/125 µm MMF	1500	2 to 430	6
	50/125 µm MMF	2000	2 to 500	6
4.25 GBd	62.5/125 µm MMF	200	2 to 70	6
Fibre Channel	50/125 µm MMF	500	2 to 150	6
200-M5-SN-I,	50/125 µm MMF	900	2 to 175	6
200-M6-SN-I	50/125 µm MMF	1500	2 to 215	6
	50/125 µm MMF	2000	2 to 270	6

Specification notes

1. UI (Unit Interval): one UI is equal to one bit time. For example, 2.125 Gbits/s corresponds to a UI of 470.588ps.
2. For LOSA and LOSD definitions see Loss of Signal Assert/Deassert Level in Section 2.5 Optical characteristics on page 10.
3. When operating the transceiver at 1.0 - 1.3 Gbaud only, a slower input rise and fall time is acceptable. If it is planned to operate the module in the 1.0 - 4.25 Gbaud range, faster input rise and fall times are required.
4. Measured with stressed eye pattern as per FC-PI (Fibre Channel) using the worst case specifications.
5. All jitter measurements performed with worst case input jitter according to FC-PI.
6. Distances, shown in the "Link Length" table, are the distances specified in the Fibre Channel standards. "Link Length" distances are calculated for worst case fiber and transceiver characteristics based on the optical and electrical specifications shown in this document using techniques utilized in IEEE 802.3 (Gigabit Ethernet). In the nominal case, longer distances are achievable.

2.7 Regulatory compliance

The PLRXPL-VE-SG4-62-x complies with common ESD, EMI, Immunity, and Component recognition requirements and specification (see details in Table 3 on page 12).

The PLRXPL-VE-SG4-62-x is RoHS-compliant per Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

ESD, EMI, and Immunity are dependent on the overall system design. Information included herein is intended as a figure of merit for designers to use as a basis for design decisions.

Table 3 Regulatory compliance

Feature	Test Method	Performance
Component safety	UL 60950 UL94-V0 IEC 60950	UL File E209897 TUV Report/Certificate (CB scheme)
RoHS-compliant	Directive 2002/95/EC	Compliant per the Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment
Laser eye safety	U.S. 21CFR (J) 1040.10 EN 60825	CDRH compliant and Class 1 laser safety. TUV Certificate
Electromagnetic Compatibility (EMC)		
CE	EU Declaration of Conformity	Compliant with European EMC and Safety Standards
Electromagnetic emmissions	EMC Directive 89/336/EEC FCC CFR47 Part 15 IEC/CISPR 22 AS/NZS CISPR22 EN 55022 ICES-003, Issue 4 VCCI-03	Noise frequency range: 30 MHz to 12 GHz. Good system EMC design practice required to achieve Class B margins.
Electromagnetic immunity	EMC Directive 89/336/EEC IEC /CISPR/24 EN 55024	
ESD immunity	EN 61000-4-2	Exceeds requirements. Withstand discharges of; 8 kV contact, 15kV and 25kV Air
Radiated immunity	EN 61000-4-3	Exceeds requirements. Field strength of 10 V/m RMS, from 10 MHz to 1 GHz. No effect on transceiver performance is detectable between these limits.

2.8 PCB layout

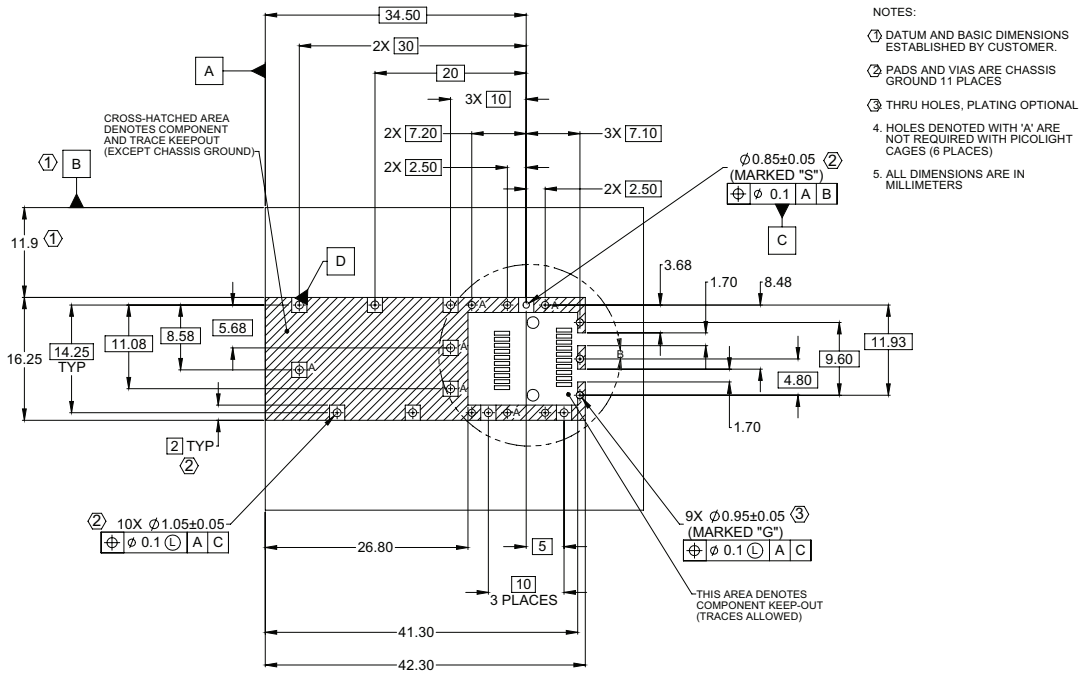


Figure 4 Board layout

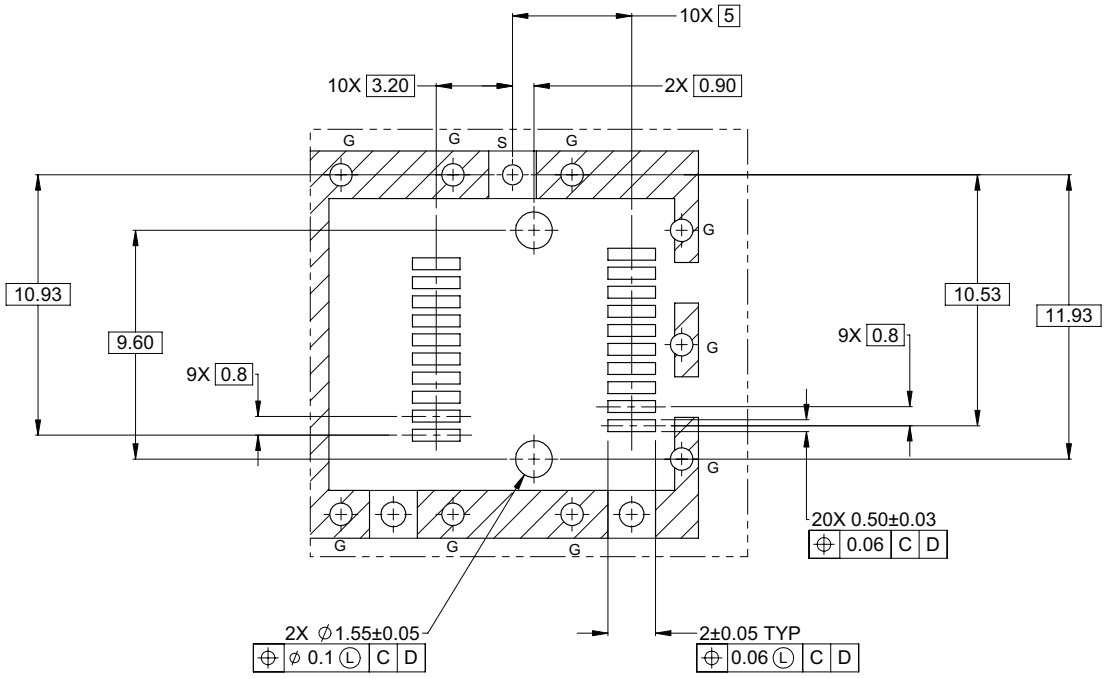
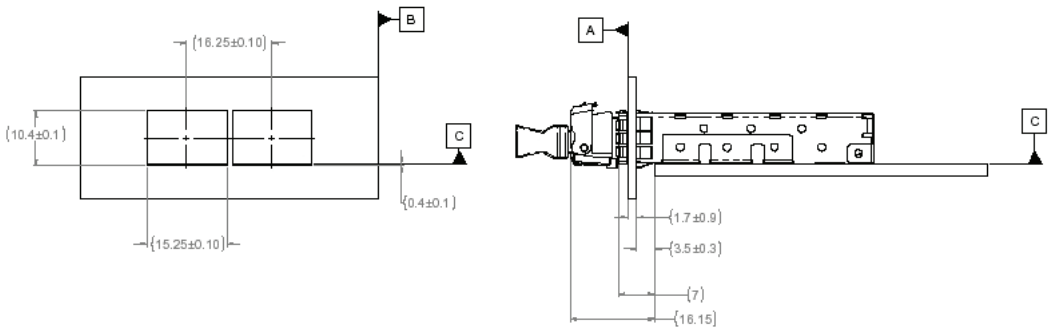


Figure 5 Detail layout

ALL DIMENSIONS ARE IN MILLIMETERS

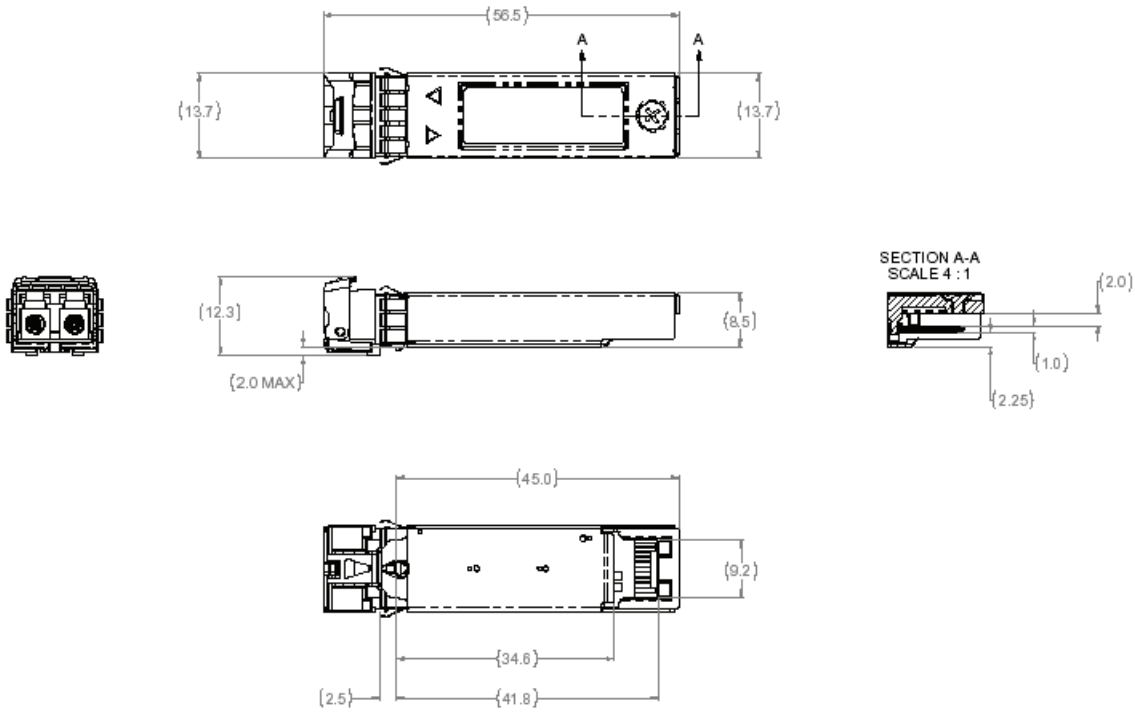
2.9 Front panel opening



All dimensions are in millimeters

Figure 6

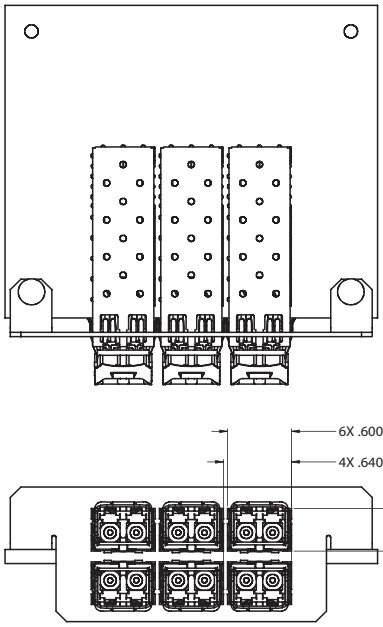
2.10 Module outline

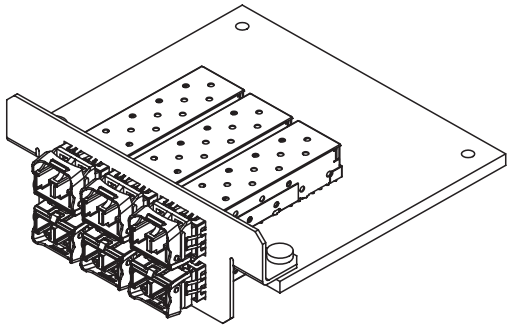


All dimensions are in millimeters

Figure 7

2.11 Transceiver belly-to-belly mounting





All dimensions in inches

Section 3 Related Information

Other information related to the RoHS-Compliant 4.25 Gbps 850 nm SFP Transceivers includes:

- Section 3.1 Digital Diagnostic Monitoring and Serial ID Operation below
- Section 3.2 Package and handling instructions on page 21
- Section 3.3 ESD Discharge (ESD) on page 21
- Section 3.4 Eye safety on page 21

3.1 Digital Diagnostic Monitoring and Serial ID Operation

The PLRXPL-VE-SG4-62-x is equipped with a 2-wire serial EEPROM that is used to store specific information about the type/identification of the transceiver as well as real-time digitized information relating to the transceiver's performance. See the Small Form Factor Commitee's document number SFF-8472 Rev 9.5, dated June 1, 2004 for memory/address organization of the identification and digital diagnostic data.

The enhanced digital diagnostics feature monitors five key transceiver parameters which are Internally Calibrated and should be read as absolute values and interpreted as follows;

Transceiver Temperature in degrees Celsius: Internally measured. Represented as a 16 bit signed two's complement value in increments of 1/256 degrees Celsius from -40 to +125°C with LSB equal to 1/256 degrees C. Accuracy is ± 3 degrees Celsius over the specified operating temperature and voltage range.

Vcc/Supply Voltage in Volts: Internally measured. Represented as a 16 bit unsigned integer with the voltage defined as the full 16 bit value(0-65535) with LSB equal to 100μV with a measurement range of 0 to +6.55V. Accuracy is ± 3% of nominal value over the specified operating temperature and voltage ranges.

TX Bias Current in μA: Represented as a 16 bit unsigned integer with current defined as the full 16 bit value(0-65535) with LSB equal to 2μA with a measurement range of 0 - 131μA. Accuracy is ± 10% of nominal value over the specified operating temperature and voltage ranges.

TX Output Power in mW: Represented as a 16 bit unsigned integer with the power defined as the full 16 bit value (0-65535) with LSB equal to 0.1μW. Accuracy is ± 2dB over the specified temperature and voltage ranges over the range of 100μW to 800μW(-10dBm to -1dBm). Data is not valid when transmitter is disabled.

RX Received Optical Power in mW: Represented as average power as a 16 bit unsigned integer with the power defined as the full 16 bit value(0-65535) with LSB equal to 0.1μW. Accuracy is ± 3dB over the specified temperature and voltage ranges over the power range of 30μW to 1000μW (-15dBm to 0dBm).

Reading the data

The information is accessed through the MOD_DEF(1), and MOD_DEF(2) connector pins of the module. The specification for this EEPROM (ATMEL AT-24CO1A family) contains all the timing and addressing information required for accessing the data.

The device address used to read the Serial ID data is 1010000X(A0h), and the address to read the diagnostic data is 1010001X(A2h). Any other device addresses will be ignored. Refer to Table 4, Table 5, and Table 6 for information regarding addresses and data field descriptions

MOD_DEF(0), pin 6 on the transceiver, is connected to Logic 0 (Ground) on the transceiver.

MOD_DEF(1), pin 5 on the transceiver, is connected to the SCL pin of the EEPROM.

MOD_DEF(2), pin 4 on the transceiver, is connected to the SDA pin of the EEPROM.

The EEPROM WP pin is internally tied to ground with no external access, allowing write access to the customer-writable field(bytes 128-247 of address 1010001X). Note: address bytes 0-127 are not write protected and may cause diagnostic malfunctions if written over.

Decoding the data

The information stored in the EEPROM including organization is defined in the Small Form-Factor document SFF-8472 draft rev 9.5, dated June 1, 2004.

Table 4 Data Field Descriptions

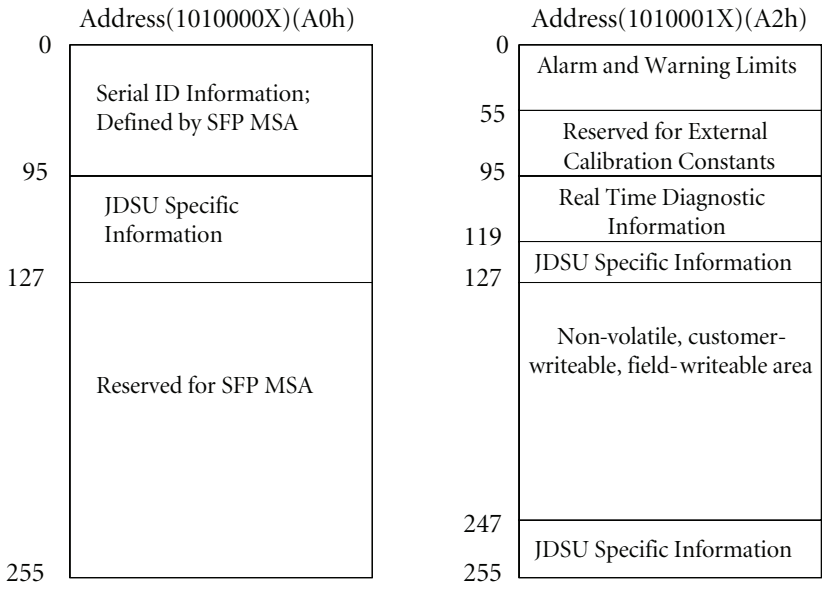


Table 5 Serial ID Data and Map

Memory Address	Value	Comments
Address (1010000X)(A0h)		
0	03	SFP Transceiver
1	04	SFP with Serial ID
2	07	LC Connector
3-10	0000000020400C15	850nm multimode, 100/200/400 FC, Intermediate Distance
11	01	8B10B encoding mechanism
12	2B	Nominal Bit rate of 4Gbps
13	00	Reserved
14	00	Single mode fiber not supported
15	00	Single mode fiber not supported
16	0F	150 meters of 50/125 µm fiber
17	07	70 meters of 62.5/125 µm fiber
18	00	Copper not supported
19	00	Reserved
20-35	JDSU	Vendor Name (ASCII)
36	00	Reserved
37-39	00019C	IEEE Company ID (ASCII)
40-55		Part Number (ASCII)
56-59		Rev of part number (ASCII)
60-61	0352	Wavelength of laser in nm; 850
62		Reserved
63		Check Code; Lower 8 bits of sum from byte 0 through 62
64	00	Reserved
65	3A	Rate Select, Tx_Disable, Tx Fault, Loss of Signal implemented; -62 part numbers
65	1A	Tx_Disable, Tx Fault, Loss of Signal implemented; 62-N part numbers
66	00	
67	00	
68-83		Serial Number (ASCII)
84-91		Date Code (ASCII)
92	68	Digital diagnostics monitoring implemented, interally calibrated, receiver power type is average
93	FO	Alarms & Warnings, TX_Fault and Rx_LOS monitoring implemented, TX_Disable Control & Monitoring. -62-N part number
	F8	Alarms & Warnings, TX_Fault and Rx_LOS monitoring implemented, TX_Disable Control & Monitoring, Rate Select. -62 part number
94	01	SFF-8472 Rev 9.4 compliant
95	64_94	Check Code; Lower 8 bits of sum from byte 64 through 94
96-127		JDSU specific EEPROM
128-255		Reserved

Table 6 Diagnostics Data Map

Memory Address	Value	Comments
Address (1010001X)(A2h)		
00-01	Temp High Alarm	MSB at low address
02-03	Temp Low Alarm	MSB at low address
04-05	Temp High Warning	MSB at low address
06-07	Temp Low Warning	MSB at low address
08-09	Voltage High Alarm	MSB at low address
10-11	Voltage Low Alarm	MSB at low address
12-13	Voltage High Warning	MSB at low address
14-15	Voltage Low Warning	MSB at low address
16-17	Bias High Alarm	MSB at low address
18-19	Bias Low Alarm	MSB at low address
20-21	Bias High Warning	MSB at low address
22-23	Bias Low Warning	MSB at low address
24-25	TX Power High Alarm	MSB at low address
26-27	TX Power Low Alarm	MSB at low address
28-29	TX Power High Warning	MSB at low address
30-31	Tx Power Low Warning	MSB at low address
32-33	RX Power High Alarm	MSB at low address
34-35	RX Power Low Alarm	MSB at low address
36-37	RX Power High Warning	MSB at low address
38-39	RX Power Low Warning	MSB at low address
40-55	Reserved	For future monitoring quantities
56-59	RP4	External Calibration Constant
60-63	RP3	External Calibration Constant
64-67	RP2	External Calibration Constant
68-71	RP1	External Calibration Constant
72-75	RP0	External Calibration Constant
76-77	Islope	External Calibration Constant
78-79	Ioffset	External Calibration Constant
80-81	TPslope	External Calibration Constant
82-83	TPoffset	External Calibration Constant
84-85	Tslope	External Calibration Constant
86-87	Toffset	External Calibration Constant
88-89	Vslope	External Calibration Constant
90-91	Voffset	External Calibration Constant
92-94	Reserved	Reserved
95	Checksum	Low order 8 bits of sum from 0-94
96	Temperature MSB	Internal temperature AD values
97	Temperature LSB	
98	Vcc MSB	Internally measured supply voltage AD values
99	Vcc LSB	
100	TX Bias MSB	TX Bias Current AD values

Table 6 Diagnostics Data Map (continued)

Memory Address	Value	Comments
Address (1010001X)(A2h)		
101	TX Bias LSB	
102	TX Power MSB	Measured TX output power AD values
103	TX Power LSB	
104	RX Power MSB	Measured RX input power AD values
105	RX Power LSB	
106	Reserved MSB	For 1st future definition of digitized analog input
107	Reserved LSB	
108	Reserved MSB	For 2nd future definition of digitized analog input
109	Reserved LSB	
110-7	Tx Disable State	Digital State of Tx Disable Pin
110-6	Soft Tx Disable Control	Writing "1" disables laser, this is OR'd with Tx_Disable pin
110-5	Reserved	
110-4	Rate Select State	Digital State of Rate Select Pin
110-3	Soft Rate Select Control	Writing "1" selects high bandwidth. This is OR'd with the hardware rate select pin.i
110-2	Tx Fault State	Digital State
110-1	LOS State	Digital State
110-0	Data Ready State	Digital State; "1" until trasnceiver is ready
111	Reserved	Reserved
112-119	Optional alarm & warning flag bits	Refer to SFF-8472 rev 9.5
120-127	Vendor specific	Vendor specific
128-247	User/Customer EEPROM	Field writeable EEPROM
248-255	Vendor specific	Vendor specific

* During Tx disable, Tx bias and Tx power will not be monitored.
Alarm and warning are latched. The flag registers are cleared when the system (Reads) AND (the alarm/warning condition no longer exists)

3.2 Package and handling instructions

Process plug
The PLRXPL-VE-SG4-62-x is supplied with a dust cover. This plug protects the transceiver's optics during standard manufacturing processes by preventing contamination from air borne particles.

Note: It is recommended that the dust cover remain in the transceiver whenever an optical fiber connector is not inserted.

Recommended cleaning and de-greasing chemicals
JDSU recommends the use of methyl, isopropyl and isobutyl alcohols for cleaning.

Do not use halogenated hydrocarbons (e.g. trichloroethane, ketones such as acetone, chloroform, ethyl acetate, MEK, methylene chloride, methylene dichloride, phenol, N-methylpyrolldone).

Flammability
The PLRXPL-VE-SG4-62-x housing is made of cast zinc and sheet metal.

3.3 ESD Discharge (ESD)

Handling
Normal ESD precautions are required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment utilizing standard grounded benches, floor mats, and wrist straps.

Test and operation
In most applications, the optical connector will protrude through the system chassis and be subjected to the same ESD environment as the system. Once properly installed in the system, this transceiver should meet and exceed common ESD testing practices and fulfill system ESD requirements.

Typical of optical transceivers, this module's receiver contains a highly sensitive optical detector and amplifier which may become temporarily saturated during an ESD strike. This could result in a short burst of bit errors. Such an event might require that the application re-acquire synchronization at the higher layers (e.g. Serializer/Deserializer chip).

3.4 Eye safety

The PLRXPL-VE-SG4-62-x is an international Class 1 laser product per IEC 60825-1:1993+A1:1997+A2:2001, and per CDRH 21 CFR 1040 Laser Safety Requirements. The PLRXPL-VE-SG4-62-x is an eye safe device when operated within the limits of this specification.

Operating this product in a manner inconsistent with intended usage and specification may result in hazardous radiation exposure.

Caution

Tampering with this laser based product or operating this product outside the limits of this specification may be considered an act of "manufacturing," and will require, under law, recertification of the modified product with the U.S. Food and Drug Administration (21 CFR 1040).

Ordering Information

For more information on this or other products and their availability, please contact your local JDSU account manager or JDSU directly at 1-800-498-JDSU (5378) in North America and +800-5378-JDSU worldwide or via e-mail at customer.service@jdsu.com.

Sample: PLRXPL-VE-SG4-62

Part Number	Temp. Range	Power Supply Tolerance	Rate Select	Digital Diagnostics
PLRXPL-VE-SG4-62	-20 to 85˚C	±10%	X	X
PLRXPL-VE-SG4-62-N	-20 to 85˚C	±10%		X

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