4001 Family of VMENIO Boards

The Antares 4001 VMEbus NTDS I/O board is a high speed intelligent NTDS I/O board for the VMEbus. The 4001 incorporates a mezzanine module that allows the base board to support many different I/O protocols. Currently available are:

- A (NTDS slow)
- B (NTDS fast)
- C (ANEW)
- D (NTDS Serial)
- E (NATO Low Level Serial)
- F (MIL-STD-1553B)
- H (high speed ANEW)

Support Software

Software is available in the form of Drivers, The ANAPI (parallel and serial) , The Basic End-Around-Test (parallel and serial) , and The V1553 Support Library for VxWorks (V1553).

Hardware Design

The VMENIO circuit board fits into one VMEbus 6U card slot incorporating both P1 and P2 connectors. The P2 bus is used for the A32:D32 bus specification, if desired. The NTDS I/O connections are made at the front of the board. The VMENIO board complies with the timing of VMEbus Specification Rev C.1.

Each board provides jumper plugs to allow the user to uniquely address the board as a slave anywhere in the 32-bit VMEbus address space. Thus multiple VMENIO boards are easily accommodated on the VMEbus. Decoding of non-priveleged address modifiers is jumper-selectable. The board implements a bus error timer for bus requests and for acknowledges after bus receipt. The standard VMEbus interrupt protocol is implemented, including a user-specified board ID response to the VMEbus IACK* signal. Any of the seven interrupt lines along with any of the four bus request/grant lines are jumper selectable on the board.

The NTDS interface provides 16-or 32-bit DMA data transfers under software control. The MIL-STD-1397 mode is also under software control to allow Category I (computer), Category II (intercomputer), or Category III (peripheral) operation. The four MIL-STD-1397 functions: External Interrupt, External Function, Output, and Input each have their own DMA control and instruction execution logic. The command address provides a fifth I/O chain.

Software Design

The software interface with the VMENIO board has been made as simple as possible and is functionally similar to the software interface for I/O in the AN/UYK-43 military computer. Each board is uniquely mapped into the VMEbus address space as two 32-bit words, denoted as hexadecimal addresses xxxxxxxY

and xxxxxxxY + 4 in Figure 1-1, where the "xx" portion of the address is jumper selectable for each VMENIO board. The "Y" value of the address, which can be either 0 or 8, is switch selectable from the card edge. The two 32-bit words which represent access to the VMENIO board are interpreted as shown below.

CPU Write To 4001

VMEbus Address	32 bit word
xxxxxxxY	Starting Address of I/O Instructions
xxxxxxxY+4	RESET Board (if data = nnnn0808)

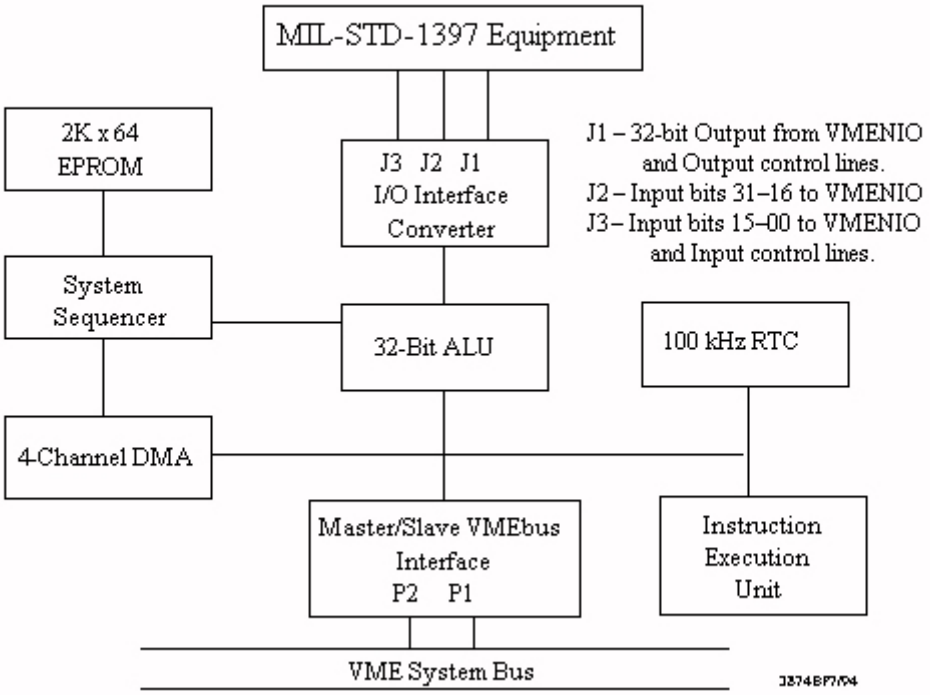
CPU Read from 4001

VMEbus Address	32 bit word	
xxxxxxxY	Interrupt Vector	Status Word
xxxxxxxY+4	Real Time Clock (100 kHz) Value	

The CPU writes a 32-bit value to the lower 32-bit address (xxxxxxxY) on the board, telling the VMENIO board where in memory to begin reading and executing I/O instructions. A write to the upper 32-bit address (xxxxxxxY + 4) with a value of 0x0808 RESETs the board by resetting all internal registers, setting the 10 MHz real-time clock to zero, clearing all pending interrupts and terminating all I/O activity. The RESET can be accomplished with either a long word write (0xnnnn0808) to address xxxxxxxY + 4 or a short word write (0x0808) to address xxxxxxxY + 6.

The CPU reads from the lower 32-bit address (xxxxxxxY) to obtain the normal board status and the local VMENIO board interrupt vector (not the VMEbus IACK* interrupt ID) following an IACK* sequence (refer to Figure 3-10). A read from the upper 32-bit address (xxxxxxxY + 4) supplies the value of the VMENIO board internal 32-bit, 100 kHz Real-Time Clock (LSB = 10 msec).

4001 Block Diagram



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