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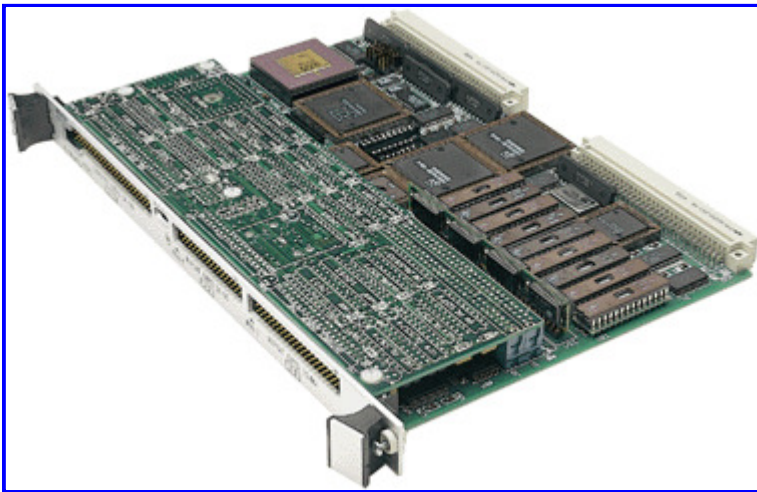
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Antares 4002 VMEbus NTDS I/O Board

4002 VMEbus NTDS I/O(VMENIO) Board



Click on an item in the 4002 VMENIO Board picture to see a description of that item.

Support Software

Software is available in the form of [Drivers](#), [The ANAPI](#), and [The Basic End-Around-Test](#).

About the 4002 VMENIO Board

The Antares 4002 VMENIO provides for high speed DMA transfers between the VMEbus and MIL-STD-1397 compatible I/O devices. The VMENIO board incorporates a [mezzanine module](#) system that allows the main board to support MIL-STD-1397 types A (NTDS slow), B (NTDS fast), C (ANEW), E (NATO low-level serial). The type D (serial), F (1553B), and H (high speed ANEW) interfaces are available in the Antares 4001 family only, at the present time.

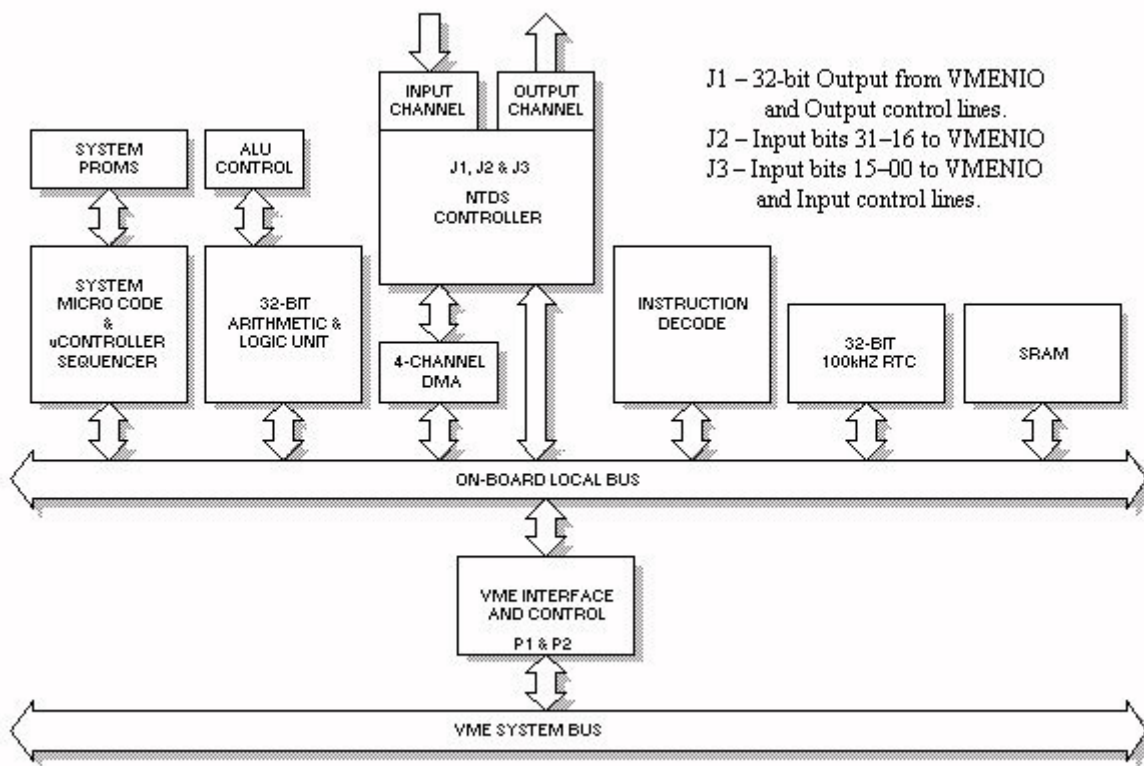
This capability allows direct connection of military computer equipment to the industry standard VMEbus for use in operational and support systems. The 4002 I/O main board is the newest product in the VMENIO 4000 family of boards. The addition of on-board shared memory and additional internal registers on the 4002 offers an expanded flexibility for the system designer.

SRAM

The on-board memory allows the user to store I/O instruction chains in the board's shared memory to provide increased instruction execution speed without accessing user memory (and the VMEbus). This feature provides the capability to execute sophisticated I/O chains where response times are critical. Software selectable memory offsets provide automatic adjustments for addresses of I/O chains and data buffers stored anywhere on the VMEbus including the VMENIO on-board memory.

The additional internal registers of the VMENIO 4002 allow the user to do "on-the-fly" processing of IB, OB, EF, and EI data in parallel (e.g., "running" 32-bit ones complement checksum on both input and output messages simultaneously).

Block Diagram



USER CONTROL

The 4002 board is programmable and operates similarly to the Navy's AN/UYK-43 computer I/O controller. The board can execute instructions out of any VMEbus memory. The instructions may be generated in a high level language such as Ada or C and are normally placed in memory at system load time. The VMEbus host processor initiates VMENIO operations with a single 32-bit store of the starting address of the first instruction in memory to be executed. No further host processor intervention is required. The I/O board continues to read and execute instructions from memory until an "end of chain" indication is encountered.

The VMENIO 4002 board provides on-board general purpose shared static memory in options of 64 Kbytes, 256 Kbytes, or 1 Mbyte. This memory may be mapped anywhere in the 32-bit (or 24-bit) address space of the VMEbus and provides a nominal 200 nanosecond access time. The memory is accessed automatically by the 4002 board processor when the board's programmed VMEbus address matches the mapped address. No

VMEbus cycles are used by the 4002 board processor when accessing on-board memory. This allows I/O instructions to reside on the board, reducing VMEbus cycles and speeding up execution times.

Transferring data buffers to and from the 4002 board shared memory is not recommended due to the "store and forward" delay inherent in having to move the data twice. However, this capability is available to the user if desired. Each VMENIO is uniquely mapped into the VMEbus address space as two 32-bit words. To control the VMENIO board, the user CPU writes to the command register on the board telling the board where in VMEbus memory to begin reading and executing I/O instructions. The user CPU reads the status register to obtain the normal board status and the local VMENIO board interrupt vector. A CPU read from the board's clock register supplies the value of the internal 32-bit, 100 KHz real-time clock. A CPU write of 0x808 to the reset register will reset the VMENIO board.

APPLICATIONS FLEXIBILITY

Entire NTDS I/O software protocols can be processed by the 4002 board without the intervention of a host computer. The instruction sequences are easy to design and write, and host CPU time dedicated to the I/O functions is minimal. The 4002 board parallel processing greatly enhances the throughput of I/O transactions; not just the data rate on the cable, but also the sequencing and verification processes of the software protocol. The 4002 board can sustain the full MIL-STD-1397 data rates of types A, B, C, D, E, and H while interfacing with external equipment. The board also supports the full-duplex requirement to transmit External Function words while an Output Buffer is active during operations in Intercomputer mode (Category II). The capability to send or receive forced External Function words (those sent without the use of the External Function Request/External Interrupt Enable signal) is supported on the 4002 boards. The board also allows the user to send forced Output words and Input/EI IDAs for special test or operational conditions.

PROGRAMMING

A powerful set of on-the-fly data processing codes are available to manipulate the incoming or outgoing data in real-time, at no expense to the host processor and very little overhead to the transfers. NTDS intercomputer software protocols typically require inconvenient instruction sequences for modern microprocessors. Such an inconvenience is calculating the checksum of 32-bit values using ones complement arithmetic.

To instruct the 4002 board processor to perform the ones complement checksum is a simple process; the actual calculation adds only 400 nanoseconds per transfer, considerably less than the time required using the host computer's instruction set. This user-selectable on-the-fly process allows the 4002 board user software to respond with positive or negative acknowledges to an incoming message within 15 microseconds of the completion of a buffer transfer, including verifying a checksum on all of the buffer data.

INSTALLATION

The VMENIO board is easily installed and integrated into the user environment through use of jumpers. The jumpers on the VMENIO board allow the user to select the following board parameters:

- Slave address
- Short (I/O) or standard (24/32 memory) slave
- Privileged-mode-only slave
- VMEbus master request level
- VMEbus master address size
- VMEbus master data word size

A six-position switch, accessible while the board is installed, contains address bits 08-03. Address bits 02-01 are used by the VMENIO board for decoding CPU requests. LEDs on the mezzanine module provide "buffer active" indicators.

SPECIFICATIONS

VMEbus Interface

DTB Master: A32/24:D32/16

Requestor: R(0-3) RWD

Bus Timer: BTO(102)

DTB Slave: A32/24/16:D32/16

Interrupter: I(1-7)DYN

NTDS INTERFACE

Data: 32-bit or 16-bit programmable for each of the four transfer operations. Functions: Four independent DMA buffers - Input, Output, External Function, and External Interrupt. Modes: Category I, II, and III are programmable.

All connections are via the [front panel](#).

ENVIRONMENT

+5 volts @ 5.1 amps.

-12 volts @ 0.3 amps.

Operating temperature: 0 to +50 C.

Storage temperature: -25 to +70 C.

Humidity: 0 to 95% non-condensing. Forced air cooling required.

Weight: 1.3 lbs (21 ounces).

Rugged version available.



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