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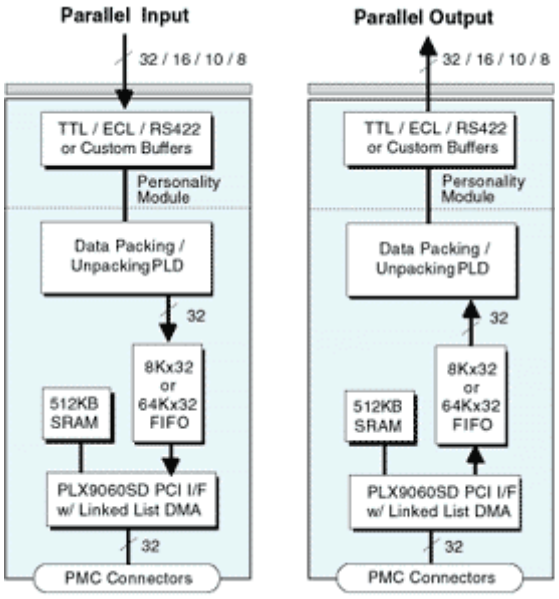
DPIO

FPDP Digital Parallel I/O PMC Module



Features

- **32-bit parallel data at up to100 MB/s**
- **FPDP (Front Panel Data Port) compatible**
- **Also in Positive ECL, RS422, LVDS or Custom versions**
- **Data packing of narrow samples**
- **8K or 32K FIFO depth**
- **Sync or Async ports with handshake**
- **Linked list DMA on PCI Input or Output versions**
- **VxWorks and Windows NT drivers**
- **PCI and CompactPCI supported with adapters**



BENEFITS

- **PMC implementation gives maximum flexibility for system integrators.**
- **Adaptable to custom interfaces.**
- **Packing capability conserves PCI bandwidth.**
- **Combine with other PMC and MIDAS to create "Digital I/O-to-Anything else" bridge.**

The DPIO is a PCI Mezzanine Card (PMC) designed for high-speed digital data acquisition or generation at data rates up to 75 Msamples/sec or 100 MBytes/sec. Typically, the module is used to bring huge amounts of raw sensor data between A/D or D/A converters and processors or memory/storage systems.

The DPIO is available with VxWorks SW support for VMETRO's MIDAS PMC I/O Subsystem for VMEbus & RACEway, as well as with Windows NT support for PC platforms (with module placed on a PCI adapter).

8K or 32K FIFO

The DPIO has a FIFO with 8K words or optionally 32K words. The FIFO contains three flags that indicates six possible states:

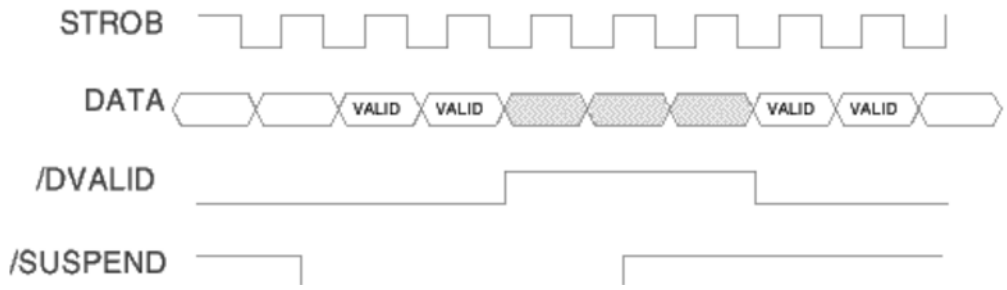
Empty / Almost Empty / Less Than Half Full / Greater Than Half Full / Almost Full / Full

The FIFO flags can be accessed via PCI for status readout.

FPDP COMPATIBLE

The -FI and -FO versions of the DPIO are fully compatible with the de facto standard FPDP (Front Panel Data Port). The FPDP is a 32-bit synchronous input/output parallel interface which is specified to operate at clock rates up to 20MHz with a TTL strobe and up to 40 MHz with PECL (Positive ECL) differential strobes.

The DPIO-FI and -FO will operate at up to 20 MHz at 32-bit with TTL strobe, up to 25 MHz at 32-bit with PECL strobes and up to 40 MHz at 16-bit with PECL strobes.



Example of FPDP signal timing with /DVALID and /SUSPEND signals to control data flow.

FLEXIBLE I/O STAGE

The DPIO PMC module is implemented with a very flexible I/O stage which can be factory-configured in a number of different ways. In order to accommodate different electrical interfaces, there is a front-end "personality module" which holds the connector and input buffers or line drivers that fit the application.

VMETRO offers standard versions compatible with FPDP (Front Panel Data Port), Positive ECL, LVDS and RS422 differential TTL. In addition, the customer may design his/her own front-end "personality module" to fit a specific requirement (see below).

32-bit standard FPDP
(-FI or -FO options)
Compatible with 3rd party A/D, D/A and DSPs.
- Up to 20 MHz @ 32-bits (80 MB/s) w/ TTL strobe.
- Up to 25 MHz @ 32-bits (100 MB/s) w/ PECL strobe.
- Up to 40 MHz @ 16-bits (80 MB/s) w/ PECL strobe.

32-bit RS422 Diff. TTL
(-DI or -DO options)
- Up to 10 MHz (40 MB/s)

10-bit 75 MHz / 16-bit 50 MHz
(-EI or -EO options)
- Positive ECL (PECL)

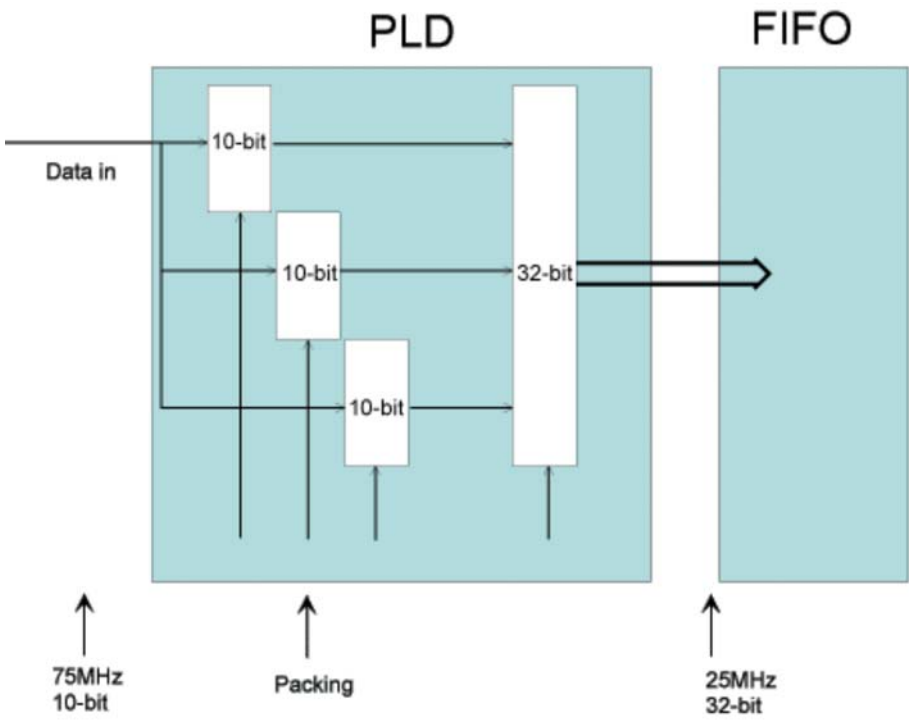
32-bit LVDS
(-LI or -LO options)
- Up to 25 MHz @ 32-bits (100 MB/s)
- Up to 49 MHz @ 16-bits (98 MB/s)

PACKING / UNPACKING CONSERVES PCI

Next to the front end personality module, there is a PLD device that offers various kinds of data packing/unpacking options. This allows data I/O widths to be of different sizes than the 32-bit FIFO word size, significantly reducing the load on the PCI bus. The packing options provided are 2x16-bit, 3x10-bit, 4x8-bit or 8x4-bit words packed in or unpacked from a 32-bit word. This provides a significant reduction in PCI load compared to sending one sample per PCI word.

The packing options are:

- **1x32-bit**
- **2x16-bit**
- **3x10-bit**
- **4x8-bit**
- **8x4-bit**



Example of 3:1 packing, placing three 10-bit words into a 32-bit word.

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