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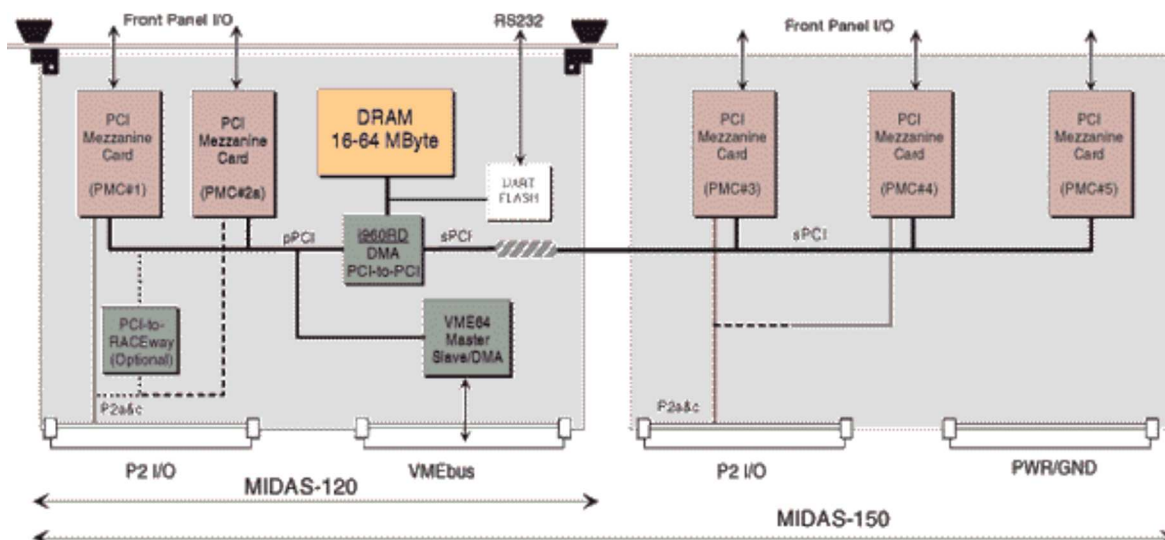
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MIDAS-100 Series

i960[®] RD PMC I/O Subsystem for VMEbus/RACEway



- i960[®] RD I/O processor with linked-list DMA-controllers and PCI-to-PCI bridge.
- Two independent PCI bus segments, each with >120MB/s sustained bandwidth.
- High-speed DRAM with 120MB/s sustained bandwidth. (16 - 64 MBytes.)
- PCI-to-RACEway interface with 120MB/s sustained bandwidth (optional).
- Holds 2-5 PMC modules, all accessible from VMEbus and RACEway.
- VME64 Master / Slave interface w/ DMA and Slot-1 controller (Universe[™] chip).
- Interrupts transferred between PMC modules and VMEbus / RACEway.
- Front-panel or P2 I/O from PMC modules.
- VxWorks[®] 5.3 Board Support Package

The MIDAS-100 series is a versatile PMC I/O Subsystem & Memory for VMEbus and/or RACEway, holding up to two or five PMC-PCI Mezzanine Cards. The board is designed for cost-effective integration of PCI I/O functions into a VME or RACEway system, where local memory and/or processing power are required.

i960[®] RD I/O Processor

A central element of the the MIDAS-100 series is the Intel [i960[®] RD](#) processor. This is a highly integrated device that contains not only a powerful RISC I/O processor, but a PCI-to-PCI bridge, memory controller and a flexible

DMA- controller with linked-list capability. The i960[®] RD has direct access to FLASH PROM (up to 2MBytes) and an RS232 UART in addition to the all PCI resources on the board, and of course the DRAM. This allows it to offload the host CPU by running dedicated I/O drivers for the PMC modules mounted on the board.

VxWorks[®] Support

A Board Support Package for VxWorks[®] 5.3 Real-time OS with drivers for selected PMC modules is available. For information on other operating systems, please contact VMETRO.

No Programming Necessary

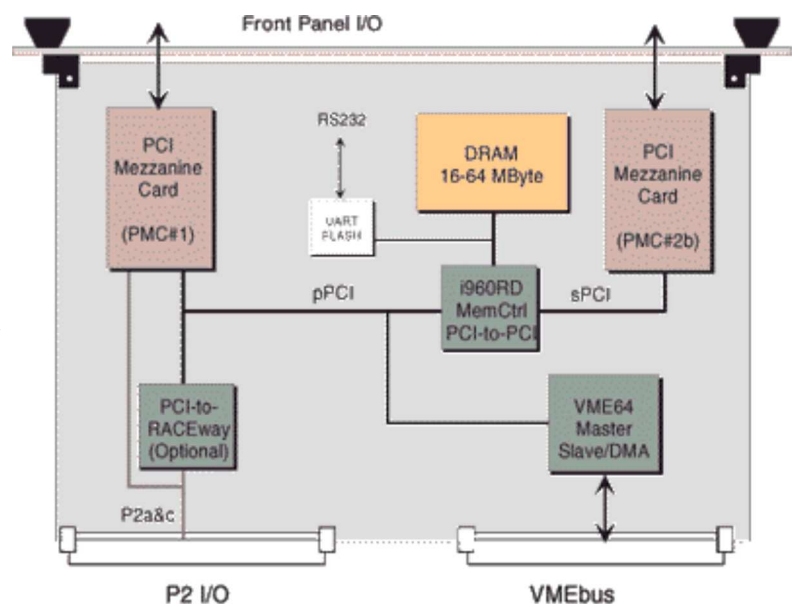
For applications that do not need the processing power of the i960[®] RD, but only the DRAM memory and/or DMA controller, the processor may rest idle during normal operation. This means that in such applications, the user does not need to program the i960[®] RD. The processor may run an embedded maintenance utility from FLASH for diagnostics and configuration through the serial port.

120 MB/s High-Speed DRAM

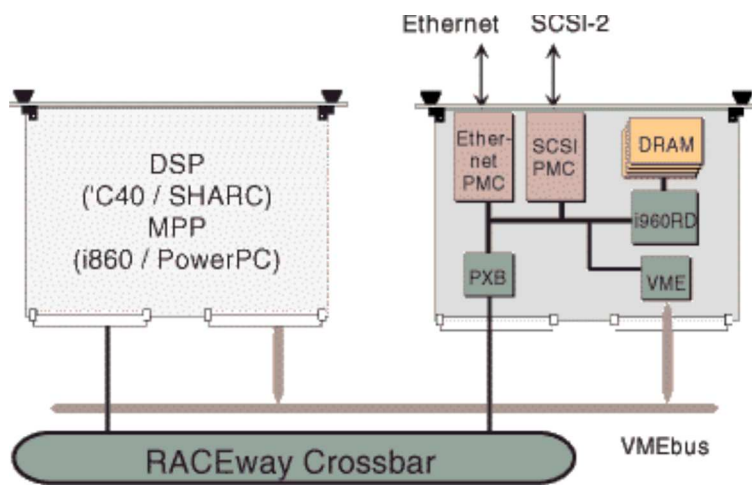
The DRAM is a high-speed memory that offers zero-wait-states within data bursts, with a sustained bandwidth of 120 MBytes/sec. It can be from 16 to 64 MBytes directly on the main board. (Larger memory options are studied.) The DRAM is accessible from both PCI busses, both with single cycles and with DMA. This means that devices on PCI, VMEbus and RACEway may access the DRAM directly as a regular slave memory.

MIDAS-120S: Symmetrical PMCs

In the standard version of the MIDAS-120 the two modules are located on the same primary PCI segment, see figure on previous page. However, in order to take advantage of the PCI-to-PCI bridge to have one PMC on each side of the i960[®] RD, a symmetrical arrangement of two PMC modules is offered (-S option, see figure above). This can be utilized to transfer data between PMC module #1 and VME / RACEway concurrently with transferring data between PMC #2b and the DRAM or i960 CPU.



MIDAS-120S Symmetrical PMC arrangement.



Application example: MIDAS-120R used as an intelligent I/O controller for RACEway and/or VMEbus.

The i960®RD runs the Ethernet and SCSI drivers under VxWorks®.

Ordering Information

Part nos.

M120 MIDAS-120, i960RD, 2 x PMC I/O Subsystem

M150 MIDAS-150, i960RD, 5 x PMC I/O Subsystem

Options

R RACEway Interface

S Symmetrical version of MIDAS-120

-xxD2 16, 32 or 64 MBytes of DRAM Memory.



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