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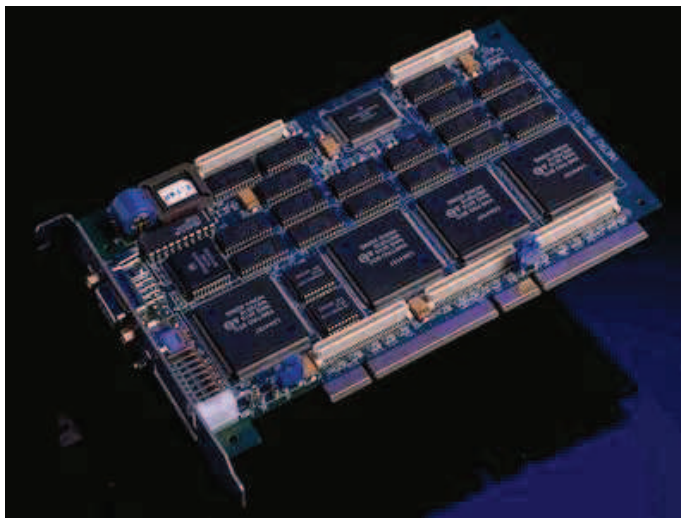
Find the *Curtiss-Wright / VMETRO PBT-315B* at our website: *Click HERE*

PBT-315 PCI Bus Analyzer

The ultimate tool in PCI test and debug

A LOGIC ANALYZER ON A CARD!

The **PBT-315 PCI Bus Analyzer** is a single-slot PCI short card that contains a complete logic analyzer for the PCI bus. The unit is able to monitor and trigger on all bus activity in 32-bit as well as **64-bit PCI** bus motherboards through a PCI expansion slot. This is a remarkable amount of functionality and performance in an extremely small package. See also the PBT-315 specification. Please contact us for more info. This page is an overview for fast sampling. Please study the detailed description. This PCI analyzer is also available in a PMC(PCI Mezzanine Card) version called the PBTM-315. For a free demodisk please send us an email to info@vmetro.com.



FEATURES:

- **Self-contained**
- **Non-intrusive**
- **Operated via RS232**
- **32 & 64-bits PCI**
- **Up to 33MHz**
- **128 channels**
- **32K/128K Trace Buffer**
- **Multi-level Triggering**
- **Statistics**

Detailed description PBT-315 Specifications

APPLICATIONS

As with VMETRO's widely known line of VMEbus Analyzers, the PBT-315 PCI Bus Analyzer is an indispensable tool for:

- **Hardware designers** of motherboards and expansion boards,
- **System integrators** putting together equipment from various vendors,
- **Software developers** involved in I/O-drivers, operating systems, etc.

PROTOCOL-SENSITIVE BUS SAMPLING

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One of the most fundamental properties of the PBT-315 is the protocol-sensitive sampling of bus cycles for state analysis. Unlike general-purpose logic analyzers, VMETRO bus analyzers know the bus protocol of the target bus to ensure that sampling takes place at the right moments. This gives a trace that includes all kinds of bus activity, like arbitration, interrupts, cache cycles etc., and it ensures that the bus is not sampled at unimportant times.

POWERFUL TRIGGER & STORE QUALIFIERS

To narrow in on the cycles of interest, the PBT-315 is equipped with powerful triggers and store qualifiers, based on four full-width word recognizers and a flexible 16 level sequencer. Each of the word recognizers offers powerful operators like RANGE, NOT and BINARY for address and data fields etc., and the user may specify signal values as hex, binary or mnemonics like "MemRd", "IOWri", etc. This eliminates the need for the user to remember the actual signal values for the different cycle types etc.

STATISTICS OF BUS TRAFFIC PATTERNS AND PERFORMANCE

Substantial amount of hardware is built into the PBT-315 to perform real-time statistics and performance measurements on PCI. Hardware event counters tied to the word recognizers provide powerful and responsive measurements of event occurrence and bus utilization. There are also trace based statistics, like the Bus Transfer Rate measurement.

EXPANDABLE

Although the PBT-315 offers substantial performance and functionality in itself, a family of powerful piggyback modules is planned. These will further enhance the capabilities of the analyzer while still occupying only a single slot. The planned modules include:

- **High-speed Timing Analyzer**
- **PCI Protocol Checker.**

Zero-Slot Adapter

No PCI slot to put the PCI Bus Analyzer in? VMETRO's Zero-Slot Adapter allows your analyzer to be plugged in as well as the PCI add-in card under test. See figure. This device is for use exclusively with the VMETRO PCI analyzer PBT-315. Contact VMETRO for more information.

ORDERING INFORMATION

-
- PBT-315B 32K/64-bit PCI Analyzer
- PBT-315C 128K/64-bit PCI Analyzer

Related Products

- BV-315-PC BusView for Windows: Graphical User-Interface for Windows on PC.
- PBTM-315 PMC-PCI Bus Analyzer
- PDRIVE PCI and PMC Bus Exerciser

Accessories

-
- 401-TER-232 Terminal Cable.
- 401-PC-232 PC Cable.
- 401-325-EPC External Power Cable.

 PBT-315 details

 PBT-315 Specifications

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APPLICATIONS
NON-INTRUSIVE AND STANDALONE
PLUG-AND-PLAY
STATE-OF-THE-ART TECHNOLOGY
EXPANDABLE
64-BIT PCI

POWERFUL TRIGGER & STORE QUALIFIERS
ADDRESS/DATA RANGE
SINGLE EVENT MODE
16-LEVEL SEQUENCER
TRIGGER OUTPUT
FIVE TRIGGER POSITIONS
PROTOCOL-SENSITIVE BUS SAMPLING
THREE SAMPLING MODES
SAMPLING OF SLOT-SPECIFIC OR USER-DEFINED SIGNALS
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STATISTICS OF PCI PERFORMANCE
EVENT COUNTING
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FORMATTED, FLEXIBLE TRACE DISPLAY
DEMULTIPLEXED ADDRESS / DATA
SEARCH & EXTRACT TRACE DATA
TIME TAG
LATENCY COUNTER
VERSATILE WAVEFORM DIAGRAMS
DUMP TRACE TO FILE
PRINT TRACE

EXTERNAL POWER SUPPLY PROVISION

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- **Hardware designers** of motherboards and expansion boards,
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- **Software developers** involved in I/O-drivers, operating systems, etc.

NON-INTRUSIVE AND STANDALONE

An important design feature of the PBT-315 is the totally **non-intrusive** and **standalone** operation as seen from the host computer to be analyzed. This is possible since the analyzer is equipped with its own processor, RS-232 serial port and all necessary firmware resident in Flash PROMs. The user may operate the analyzer from a PC running VMETRO's graphical user-interface **"BusView™"** for Microsoft® Windows™, from a standard ASCII terminal like VT100, or using a terminal emulator on a UNIX workstation.

PLUG-AND-PLAY

Being a full featured logic analyzer, but without the messy probes, cables or adapters associated with traditional instruments, the PBT-315 PCI Bus Analyzer offers **plug-and-play** installation for immediate bus traffic analysis. A standard

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screen/keyboard operating environment integrated with other tools such as compilers, debuggers and emulators, ensures optimum productivity in a busy development environment, essential in today's competitive marketplace where time-to-market is critical.

STATE-OF-THE-ART TECHNOLOGY

The PBT-315 is a state-of-the-art product based on the fourth generation of bus analyzers from VMETRO. Extensive use of high-speed gate array ASICs and double sided surface mount technology provides outstanding performance and functionality, for optimum test and debugging efficiency.

EXPANDABLE

Although the PBT-315 offers substantial performance and functionality in itself, a family of powerful piggyback modules is planned. These will further enhance the capabilities of the analyzer while still occupying only a single slot. The planned modules include:

- **High-speed Timing Analyzer**
- **PCI Bus Exerciser**
- **PCI Protocol Checker.**

64-BIT PCI

The high number of trace channels of the PBT-315 also facilitates sampling of 64-bit PCI data. This is possible by dynamically allocating the trace channels normally used for Address/Data demultiplexing to the extra 32-bit of data used for 64-bit data transfers.

POWERFUL TRIGGER & STORE QUALIFIERS

To narrow in on the cycles of interest, the PBT-315 is equipped with powerful triggers and store qualifiers, based on four full-width word recognizers and a flexible sequencer. Each of the word recognizers offers powerful operators like RANGE, NOT and BINARY for address and data fields etc., and the user may specify signal values as hex, binary or mnemonics like "MemRd", "IOWri", etc. This eliminates the need for the user to remember the actual signal values for the different cycle types etc.

ADDRESS/DATA RANGE

Each of the four word recognizers allows unrestricted address and data ranges, with both 'inside' and 'outside' possibilities. The address ranges can even be specified as 64-bits wide when capturing "dual address cycles".

SINGLE EVENT MODE

In many cases a simple trigger like "If Event X then Trigger" is sufficient. For this purpose, there is a default "Single Event Mode" which simply provides a trigger on the event pointed to in the Event Patterns window. When a more complex trigger is required, or a store or count qualifier is needed, the user may switch to the "Sequencer Mode".

16-LEVEL SEQUENCER

The PBT-315 provides an advanced 16-level Trigger Sequencer, with powerful operators like STORE, COUNT, DELAY and GOTO. The sequencer is shown in a separate window on the main status screen, and may be used to dynamically change sampling modes, define nested trigger conditions, or define the trigger position and store qualifiers etc.

TRIGGER OUTPUT

A Trigger Output signal is available on a pin header on the front panel. The TTL compatible signal has selectable polarity and mode, i.e. the signal may simply change logic level on trigger, or it may be selected to pulse when a trigger or a valid store condition occurs. The Trigger Output signal is useful to trigger external instruments, like a high speed oscilloscope, counters etc.

FIVE TRIGGER POSITIONS

For maximum flexibility, the trigger can be placed at five different positions in the trace buffer: Start, 25%, Middle, 75% and End of Trace.

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PROTOCOL-SENSITIVE BUS SAMPLING

One of the most fundamental properties of the PBT-315 is the protocol-sensitive sampling of bus cycles for state analysis. Unlike general-purpose logic analyzers, VMETRO bus analyzers know the bus protocol of the target bus to ensure that sampling takes place at the right moments. This gives a trace that includes all kinds of bus activity, like arbitration, interrupts, cache cycles etc., and it ensures that the bus is not sampled at unimportant times.

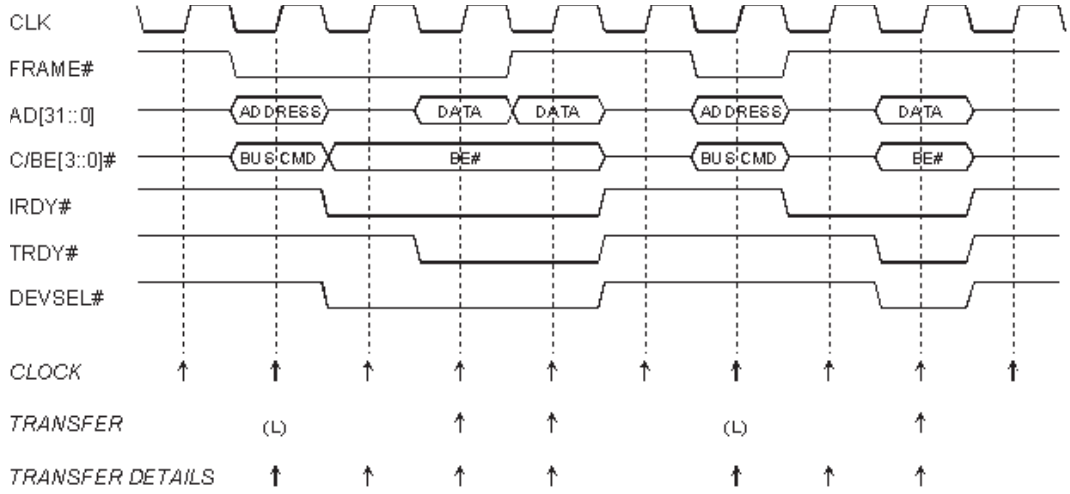
To overcome this, the PBT-315 has the capability to demultiplex Address/Data and COMMAND/BEx# into separate trace channels. This is possible since the PBT-315 has as many as 128 trace channels, a luxury found only on the most expensive logic analyzers.

This important feature not only simplifies readability of the trace, but allows powerful triggers and store qualifiers involving both address and data to be defined easily.

THREE SAMPLING MODES

When sampling the PCI bus, the PBT-315 stores 91 PCI signals, 8 external signals plus time tags and utility bits (128 bits total) into a 32K Trace Memory, optionally 128K. This is a vast amount of information, so in order to give the user the most suitable display for different applications, the PBT-315 can sample the activity of the PCI bus in three different ways:

CLK-synchronous sampling:	Stores one sample per each PCI CLK cycle. This captures all the details of how the PCI bus is exercised, clock-cycle by clock-cycle. This is useful to verify the behaviour of bus interface state machines etc.
TRANSFER-synchronous sampling:	As above, but stores one sample per each PCI CLK cycle only within a bus transaction, i.e. when the signals FRAME# or IRDY# are active. In this mode, all idle clock cycles are skipped, conserving space in the trace buffer.
TRANSFER- DETAILS sampling:	This mode is a subset of the TRANSFER- synchronous mode. Stores one sample per valid Data Phase. Each sample includes the Address which is latched from the address phase. This is the optimum way to analyze bus transactions as seen from a SW point of view (State Analysis).



SAMPLING OF SLOT-SPECIFIC OR USER-DEFINED SIGNALS

The PCI bus has certain slot-specific signals, such as the Request (REQx#) and Grant (GNTx#) signals used for arbitration. These signals can be brought to eight external inputs on the pin headers in the back panel. The external inputs, fully available in the trigger words, can also be used for any user-specific signals.

GRANT LATCHING

When the slot-specific GNTx# signals are connected as described above, a special latch may be activated to hold the value of the active grant during all data phases. The latched GNTx# value is available in the trace, triggers, store conditions and statistics.

STATISTICS OF BUS TRAFFIC PATTERNS AND PERFORMANCE

Substantial amount of hardware is built into the PBT-315 to perform real-time statistics and performance measurements on PCI. Hardware event counters tied to the word recognizers provide powerful and responsive measurements of event

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occurrence and bus utilization. There are also trace based statistics, like the Bus Transfer Rate measurement.

EVENT COUNTING	The Event Counting function, which is based on HW counters, provides a real-time count of the occurrence of four user-defined events. This very powerful function may for example be used to count the number of e.g. IACK cycles per second displayed as a function of time, or to investigate access patterns to the bus in multi-processor systems, etc.
BUS UTILIZATION	The Bus Utilization function provides a direct readout of the percentage of time the bus is occupied. This is ideal to determine whether the system bus has spare capacity to support another I/O-device or processor etc. This function, which is based on hardware counters and a pre-programmed usage of the word recognizers, provides an immediate response readout of how the bus is being used at any time.
BUS TRANSFER RATE	The Bus Transfer Rate function presents how much data is transferred over the bus, shown as MBytes/s and in Mtransfers/s. This can either be shown between selected lines directly in the trace buffer, to measure burst transfer rate, or as histograms that show the average transfer rate over a certain period of time. This function can be used to characterize a system, to verify if performance specifications have been fulfilled and to assist in system tuning.

FORMATTED, FLEXIBLE TRACE DISPLAY

The protocol-sensitive demultiplexed sampling scheme provides one trace line per data cycle, and the collected trace is presented in a formatted way with mnemonics for easy readability of the captured bus cycles. To optimize readability further, the user may freely rearrange the signal layout in the trace display. It is also possible to have multiple trace windows opened, to see various portions of the trace at the same time.

DEMULTIPLEXED ADDRESS / DATA

The PCI bus multiplexes Address and Data into a common 32-bit bus. In a similar way, the bus COMMAND signals are multiplexed with the data byte enables (BEx#). This saves system cost, since the number of pins on chips and connectors is reduced. However, it makes it more difficult to analyze the bus using a regular logic analyzer, since a given sample does not contain all information about a bus transfer.

SEARCH & EXTRACT TRACE DATA

Powerful Search and Extract functions are provided for easy location of particular samples in the trace memory. After a trace is collected, any combination of signals can be searched for in the trace buffer. It is also possible to qualify the displayed data with the search pattern, providing an extracted trace listing, with recalculated time tags, for rapid identification of the data of interest.

TIME TAG

The PBT-315 provides a high-resolution Time Tag for each sample in the trace list. The time tag may either show relative time between each sample, or absolute time from the trigger point.

LATENCY COUNTER

A second tag in the trace display shows the latency for each PCI transfer, which is defined as the number of wait states from FRAME# asserted to TRDY# asserted.

VERSATILE WAVEFORM DIAGRAMS

The easy-to-read waveform diagrams provide powerful zooming, cursors and navigation tools. To ease the search for cycles of interest, one may use an "edge-to-edge" scroll mode on a selected signal, as well as explicit jumps to given line numbers or to cursors.

DUMP TRACE TO FILE

Captured trace data may easily be dumped to a binary file on a PC and then loaded back later by means of Dump/Load commands. Partial traces may be loaded, and a packing algorithm reduces transfer time. Trace files may also be reviewed locally on the PC using BusView for Windows, or a DOS Simulator of the Terminal User-Interface.

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PRINT TRACE

A Print command allows a printout of the trace just as it is presented on the screen, either as waveforms or as an alphanumeric list with mnemonics and actual signal columns selected.

EXTERNAL POWER SUPPLY PROVISION

An important feature of the PBT-315 is the provision for an external power supply. This makes it possible to use the PBT-315 in systems with a marginal power supply.

 PBT-315 details

 PBT-315 Specifications

PCI Analysis Anomaly Timing Exerciser Products Support Applications HOME

SPECIFICATION

PBT-315 PCI Analyzer

 PBT-315 details  PBT-315 overview

Trace Memory:	32K x 128 bits (Model B) 128K x 128 bits (Model C)
Input channels:	91 PCI signals, plus 8 ext. inputs on pin header.
PCI clock requirements:	Max. 33MHz, min. 20MHz, Min. 5ns low or high pulse width. 1ms PLL lock time.
PCI signal levels:	5V or 3.3V
PCI loading:	Max. 10pF (One load + max 1.5"/3.8cm of trace length). Satisfies PCI specifications
PCI signals:	AD[31::0], AD[63::32], C/BE[3::0]#, C/BE[7::4]#, FRAME#, TRDY#, IRDY#, STOP#, DEVSEL#, PAR, PAR64, PERR#, SERR#, RST#, SDONE, SBO#, INTA#, INTB#, INTC#, INTD#, LOCK#, ACK64#, REQ64#. (Plus GNT3:0#, REQ3:0#, IDSEL via pin headers).
Trigger:	4 word recognizers covering all 91PCI signals and 8 Ext. inputs. RANGE & NOT operator on Address/Data.
Range:	Four A64/A32 address ranges, Four D32 data ranges. Inside/Outside.
Sequencer:	16 levels with If, Else, Elsif, Goto, Count, Delay, Trigger, Store, Sampling mode, Halt.
Trigger position:	0%, 25%, 50%, 75%, 100%
Occurrence counters:	Four 20-bits (in Sequencer).
Delay counters:	Three 20-bits (in Sequencer).
Event counters:	Four 20-bits (for Statistics).
Time Tag: Range:	30ns-2hrs15m@33MHz
Resolution:	30ns@33MHz
Latency Tag:	Counts latency (wait states) from FRAME# to TRDY# asserted. Max count: 128clks.
Trigger Output:	TTL level trigger output with programmable polarity, level or pulse. May pulse on each stored sample. Available on pin header on back panel.
External Inputs:	Eight TTL level inputs on pin header on back panel.
Processor:	MC68EC020 16,67 MHz512KByte RAM w/battery backup for Setup Storage. 512KByte Flash EPROM, Up to 512KByte UV EPROM.
Interfaces:	Two RS232C serial ports, both in one DB9 female connector. Baud rates: 1200-38400b/s, aut. adjusted.
Power supply requirements:	+5VDC +/-5% from PCI backplane or from ext. power supply via back panel inlet. Current: 1,3A typ. idle, 2,5A typ. sampling @ 33MHz. +12V, 0mA typ., 120mA max. when progr. FLASH only.
Dimensions:	174.6 x 106.7mm (Short card) One PCI slot.
Compatibility:	PCI Rev. 2.1
WARRANTY	All VMETRO analyzer products have one year warranty.

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 PBT-315 details  PBT-315 overview

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