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CompactPCI and PMC

Bus Analyzers, Exercisers & Protocol Checkers



VMETRO

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Introduction

The PMC and CompactPCI Analyzer product range from VMETRO offers unprecedented functionality and flexibility for debugging embedded applications. The PBTM-515 State Analyzer is common to both the PMC and CompactPCI solutions, and takes advantage of the reusability of HW, offering cost benefits to the user.

PMC

EXERBAT-M

Protocol Checker & Exerciser

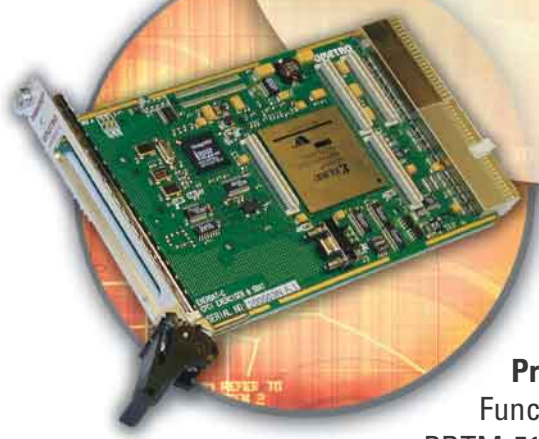
Companion board for the PBTM-515





PBTM-515

State Analyzer and Statistics module



CompactPCI

EXERBAT-C

Protocol Checker & Exerciser

Functions as a carrier board for the PBTM-515 in CompactPCI systems

PMC Solution

CompactPCI Solution

Solutions for PMC and CompactPCI

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PBTM-515

PMC State Analyzer



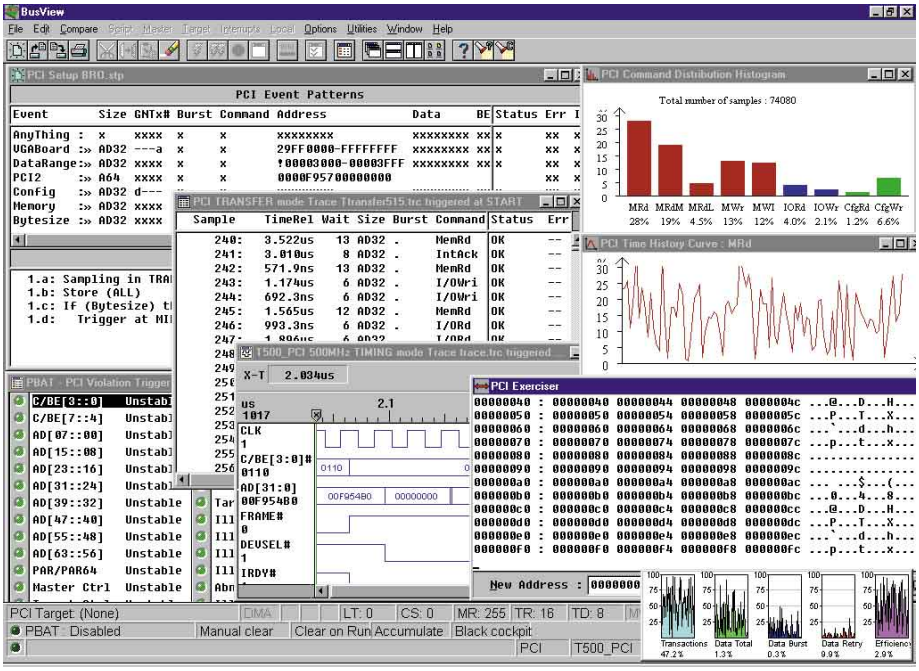
Features:

- 32 & 64-bit PCI Analysis
- Up to 66MHz
- 64K/256K Trace
- Multi -level Triggering
- Enhanced Statistics
- Self-contained
- Non-intrusive
- Operated via RS232 or USB
- PCI ver. 2.3 compliant
- PMC Exerciser & Protocol Checker with EXERBAT-M companion board
- Supports CompactPCI with EXERBAT- C
- Supports both 3.3V and 5V signalling

USB UNIVERSAL SERIAL BUS

PCI TRANSFER mode Trace Pcitrf4.trc triggered at START

Sample	TimeRel	Wait	Size	Burst	Command	Address	Data	Status	Err	INTx#
907:	1.800us	6	AD32	.	I/OWr	00000020	......0A	OK	--	----
908:	630ns	6	AD32	.	I/ORd	00000020	00	OK	--	----
909:	145.95us	11	AD32	.	MemRd	01FE0F08	01FD08E2	OK	--	----
910:	420ns	10	AD32	Start	MemRd	01FD08E0	01FD0982	OK	--	----
911:	30ns	.	AD32	B	MemRd	01FD08E4	01FD0940	OK	--	----
912:	420ns	10	AD32	Start	MemRd	01FD0940	01FD0940	OK	--	----
913:	30ns	.	AD32	B	MemRd	01FD0944	020007FF	OK	--	----
914:	30ns	.	AD32	B	MemRd	01FD0948	FFE080E1	OK	--	----
915:	30ns	.	AD32	B	MemRd	01FD094C	00000000	OK	--	----
916:	450ns	10	AD32	Start	MemRd	01FD0980	01FD0983	OK	--	----
917:	30ns	.	AD32	B	MemRd	01FD0984	01FD0960	OK	--	----
918:	420ns	10	AD32	Start	MemRd	01FD0960	01FD0960	OK	--	----
919:	30ns	.	AD32	B	MemRd	01FD0964	02000000	OK	--	----
920:	780ns	11	AD32	Start	MemRd	01FD0968	FFE080E1	OK	--	----
921:	30ns	.	AD32	B	MemRd	01FD096C	00000000	OK	--	----
922:	101.07us	8	AD32	.	IntAck	....	54	OK	--	----
923:	1.860us	6	AD32	.	I/OWr	00000021	....B8..	OK	--	----
924:	690ns	6	AD32	.	I/OWr	00000020	64	OK	--	----
925:	1.560us	8	AD32	.	I/ORd	000003FA	....	TdwodTr	--	----
926:	390ns	10	AD32	.	I/ORd	000003FA	....	TdwodTr	--	----
927:	300ns	6	AD32	.	I/ORd	000003FA	..C0....	OK	--	----
928:	750ns	8	AD32	.	I/ORd	000003FE	....	TdwodTr	--	----
929:	390ns	10	AD32	.	I/ORd	000003FE	....	TdwodTr	--	----
930:	390ns	10	AD32	.	I/ORd	000003FE	....	TdwodTr	--	----
931:	240ns	4	AD32	.	I/ORd	000003FE	..04....	OK	--	----
932:	990ns	8	AD32	.	I/ORd	000003FA	....	TdwodTr	--	----



STATE-OF-THE-ART IN PCI DEBUGGING

The PBTM-515 is designed to assist hardware, software and system validation engineers in developing, testing and validating 64-bit and 33/66 MHz PMC systems. Based on VMETRO's PBT-515 PCI Analyzer, the PBTM-515 offers unprecedented debugging capabilities in a PMC module. The PBTM-515 is a complete logic analyzer for PCI buses up to 64-bit wide and at clock speeds up to 66.7 MHz. The unit is operated through USB or RS232 from a PC running Windows and VMETRO's BusView™ graphical user interface, or via RS232 from an ASCII terminal or terminal emulator. As with all VMETRO analyzers, the unit may be powered from the target system or from an external power supply, and extensive on-line help is available.

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EXERBAT-M

Exerciser and Protocol Checker for PMC

(Companion board to be used with PBTM-515)

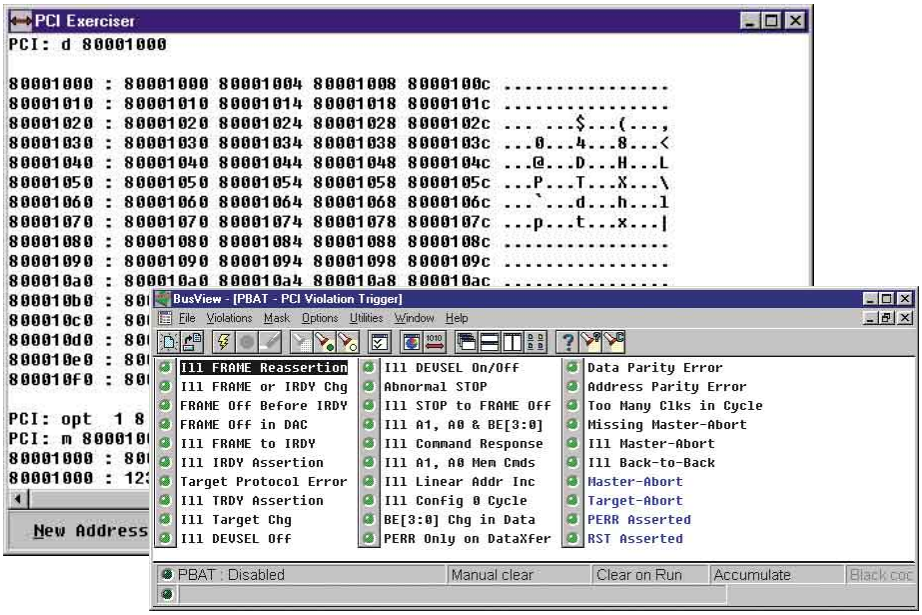


Features:

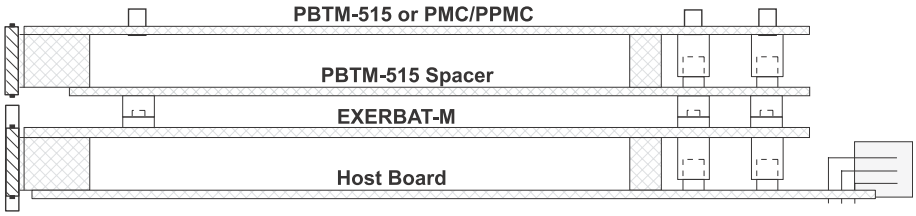
- PMC Exerciser & Protocol Checker
- Supports 64-bit and 32-bit PCI up to 66.7 MHz
- PCI 2.3 compliant
- Companion board for the PBTM-515 PMC/PCI Analyzer
- Supports both 3.3V and 5V signalling

Q: Why do I need the ability to run multiple functions simultaneously?

A: Because these functions (or tools) are best utilized when they are run together. For example, the state analyzer can capture a trace of bus traffic when the exerciser is scanning through config space.



The EXERBAT-M is a PMC module that contains a full-featured PCI Exerciser and Protocol Checker, designed to be used in combination with VMETRO's PBTM-515 PMC/PCI Analyzer. The combination of an EXERBAT-M and a PBTM-515 offers a complete Analyzer/ Exerciser/Protocol Checker for PMC. The user has full control of all sub-functions through a single user interface, with a choice of a Windows based GUI (BusView™) through USB or RS232, or with a built-in Terminal user-interface via RS232. The latter allows for operation also from UNIX/ Linux platforms using a Terminal Emulator.



Above: EXERBAT-M shown with PBTM-515 PMC/PCI Analyzer on top. Another PMC (target only) or PPMC (REQB#, GNTB#, IDSEL passed through) module may be installed on the EXERBAT-M.

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EXERBAT-C

Exerciser and Protocol Checker for CompactPCI & Carrier for PBTM-515

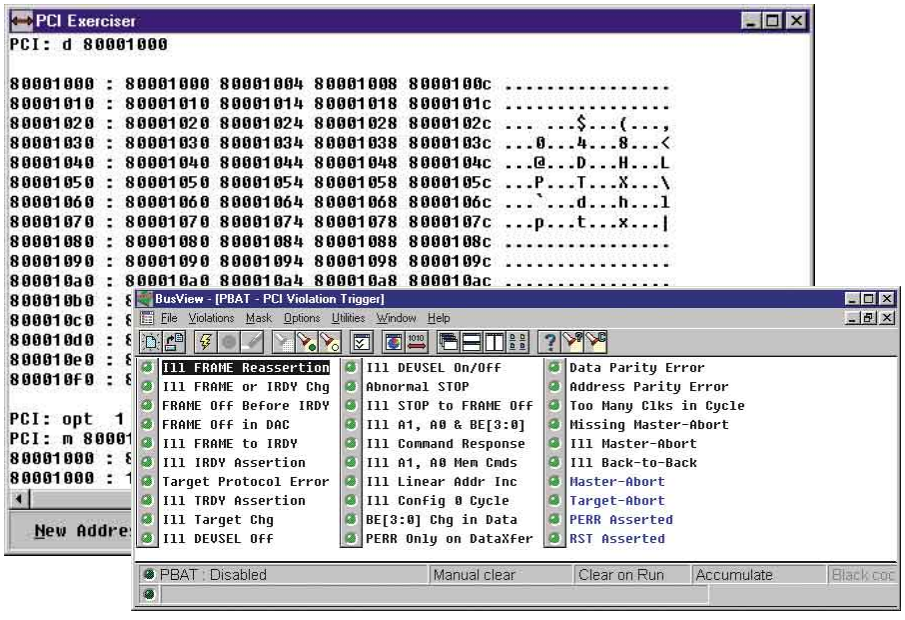


Features:

- CompactPCI Exerciser and Protocol Checker
- Carrier card for PBTM-515
- Supports 64-bit PCI
- Compliant with PCI 2.3
- Hot Swappable
- System Slot or Peripheral Slot capable
- Supports both 3.3V and 5V signalling

Q: Do I need a system slot controller installed in my CompactPCI system in order to debug my peripheral board?

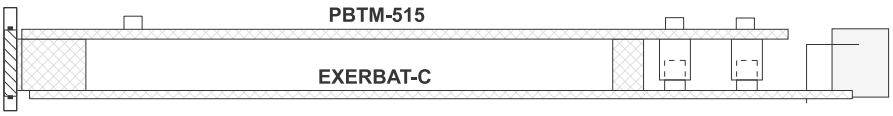
A: No, our CompactPCI solution includes full system slot functionality!



The EXERBAT-C is a PCI Exerciser & Protocol Checker implemented as a 3U CompactPCI card, with a provision for accepting the PBTM-515 PMC/PCI Analyzer. The combination of an EXERBAT-C and a PBTM-515 offers a complete Analyzer/Exerciser/Protocol Checker for CompactPCI in a single slot solution. The user has full control of all sub-functions through a single user interface, with a choice of a Windows based GUI (BusView™) through USB or RS232, or with a built-in Terminal user-interface via RS232. The latter allows for operation also from UNIX/Linux platforms using a Terminal Emulator.

The EXERBAT-C can function as a system controller, and generate a clock at 25, 33, 50 or 66MHz. The board is also fully hot swappable.

When acting as a System Slot Controller, the user can select which REQ#/GNT# signal pair to feed to the analyzer slot.



EXERBAT-C shown with PBTM-515 PMC Analyzer installed on top. The EXERBAT-C supports Hot Swap and is system slot capable (i.e. includes Arbiter). The whole assembly fits in one CompactPCI slot.

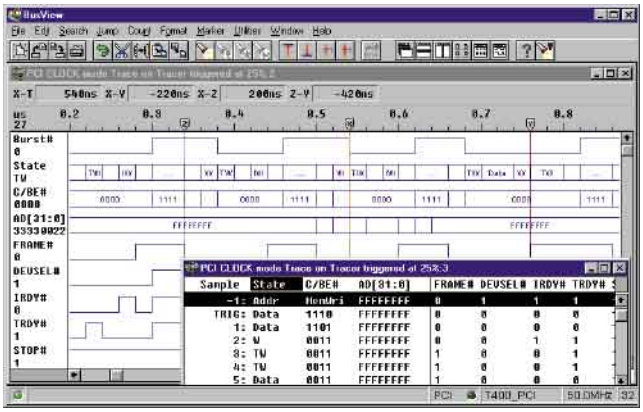
Q: Does your CompactPCI Analyzer support hot-swap?

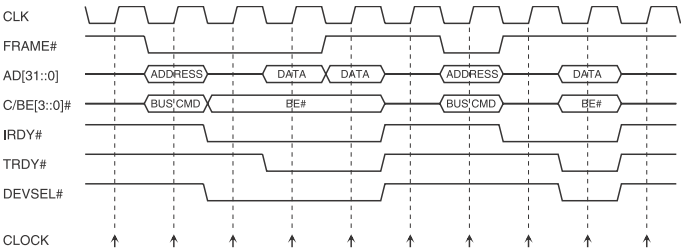
A: Yes, our CompactPCI solution supports hot-swap, meaning you can insert the Analyzer into a running system for debugging. In the world of telecommunications, shutting a system down is often not an option!

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When sampling the PCI bus, the State Analyzer captures 94 bus signals, 8 external signals plus internally generated time tags and utility bits (128 bits total) into a 64K Trace Memory, optionally 256K. This is a vast amount of information, so in order to give the user the most suitable display for different applications, the Analyzer offers three different ways to capture the bus activity:

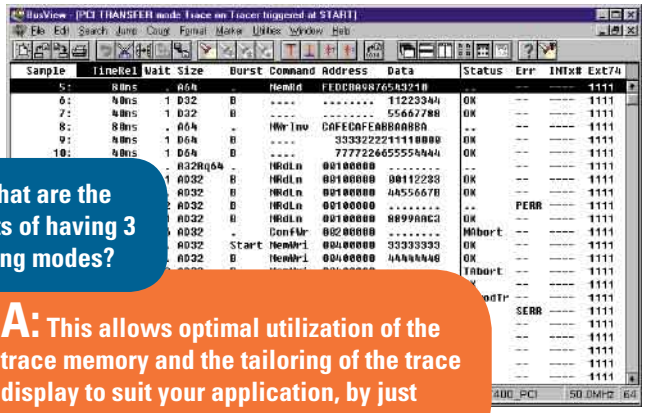
CLOCK sampling - For Hardware Analysis:





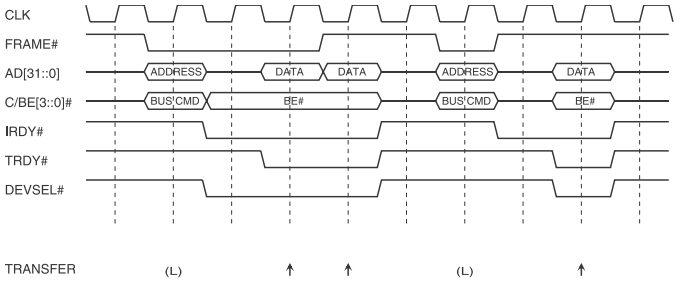
Stores one sample per PCI clock cycle. This captures all the details of how the PCI bus is exercised, clock-cycle by clock-cycle. This is useful to verify the behavior of hardware, such as bus interface state machines. In this mode, no demultiplexing takes place, all signals are captured straight from the bus and displayed as a list and/or as waveforms.

TRANSFER sampling - For Software Analysis:



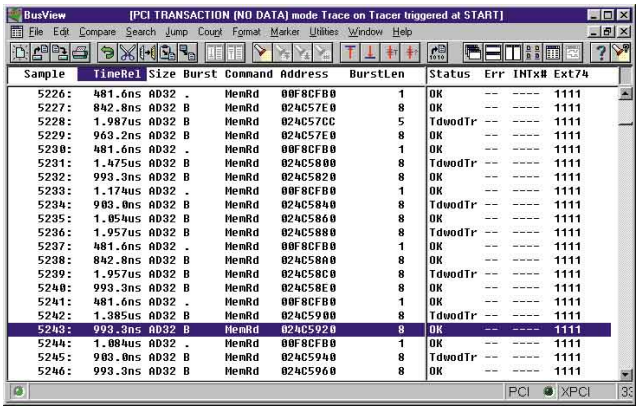
Q: What are the benefits of having 3 sampling modes?

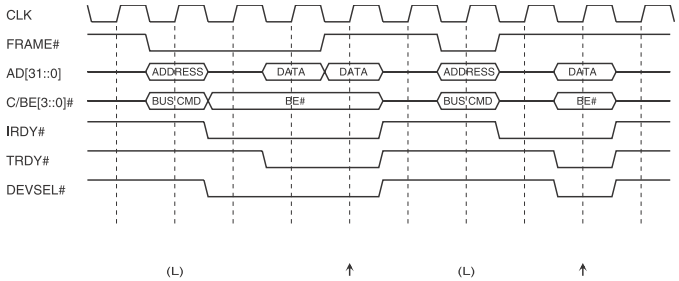
A: This allows optimal utilization of the trace memory and the tailoring of the trace display to suit your application, by just storing the details that interest you.



Stores one sample per valid Data Phase. For 32-bit transfers, each sample also includes the Address and Bus Command which is latched from the address phase (demultiplexing). Signals are grouped for easy interpretation of the bus activity. This is the optimum way to analyze bus transactions during Software development.

TRANSACTION sampling- For System Analysis:





Similar to Transfer Mode except that instead of displaying Data it displays the total Burst Length for each transaction. In this mode, a vast number of PCI transactions are stored in the trace buffer, producing trace that is optimal for system behavior analysis, validation and performance tuning.

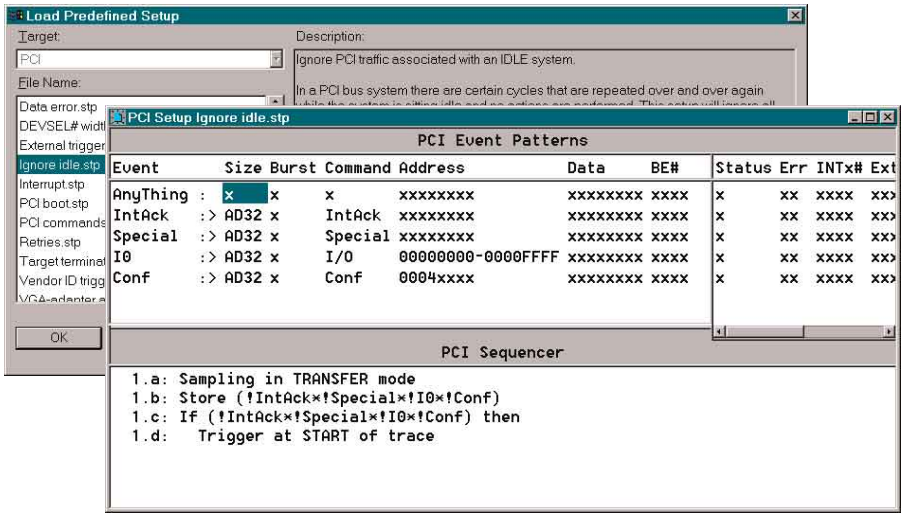
STATE ANALYZER WITH VARIOUS SAMPLING MODES

The State Analyzer of the PBTM-515 captures and displays 64-bit or 32-bit PCI bus activity up to 66.7 MHz with highly advanced (yet simple to use) triggering, filtering and counting capabilities. To provide optimum bus analysis for a given problem, the state analyzer offers a choice of three sampling modes.

The **CLOCK** sampling mode is a plain "clock-by-clock" sampling mode as found in any state analyzer. Augmented by address phase highlighting and command mnemonics, this is highly suitable for low-level hardware oriented analysis of the bus protocol as executed by bus interface state machines.

HIGH-LEVEL BUS SAMPLING

For software and system integration issues, debugging the PCI bus on a clock-by-clock basis is not productive, the user would have to spend time on understanding the bus protocol rather than investigating the actual problem. For this reason, analysis on a higher level is required, with focus on bus traffic rather than the bus protocol. Therefore, VMETRO offers in addition two unique higher level sampling modes, aimed at producing a more meaningful trace for software and system engineers. One such mode is called **TRANSFER Mode**, in which the analyzer hides details about the PCI bus protocol for the user, and avoids sampling during idle or wait states. This is done by means of protocol-sensitive bus sampling, de-multiplexing of address/data and Command/Byte enables (for 32-bit data transfers), internally generated utility signals for burst detection etc., and extensive use of mnemonics. This allows the user to focus explicitly on the essential Command, Address, Data and Status values, both in the trigger event specifiers and in the trace display. In addition, the user is given information about time from trigger, time between transactions and transfers, the latency or number of wait states per transaction and whether a transfer is part of a burst or at the start of a burst. The other higher level sampling mode is called **TRANSACTION Mode**. This is similar to Transfer Mode except that instead of displaying Data, it displays the total Burst Length for each transaction. In this mode, a vast number of PCI transactions are stored in the trace buffer, producing trace that is optimal for system behavior analysis, validation and performance tuning.



ADVANCED TRIGGER AND STORE CAPABILITIES

The PBTM-515 uses VMETRO's unique programming language-like trigger sequencer to specify triggers, store and count and delay qualifiers in an "If-then-else…" fashion. Together with the intuitive demultiplexed sampling method (which puts Command, Address, Data and Status as separate items also in the trigger event specifiers) and true inside/outside range specifiers on address and data fields, the user may easily create sophisticated triggers and store qualifiers without having to use multiple events to define trigger attributes of a single transfer. The user may store his own trigger setups, either in non-volatile memory on the analyzer or on files on the host PC. The analyzer also automatically maintains the current trigger and sequencer setting after power off/on cycling. In sum, all these features allow the user to solve his problem quickly, instead of spending hours trying to figure out how to set up and understand the analyzer.

DEMULTIPLEXED ADDRESS / DATA

The PCI bus multiplexes Address and Data into a common 32-bit or 64-bit bus. In a similar way, the bus COMMAND signals are multiplexed with the data byte enables (BEx#). This saves system cost, since the number of pins on chips and connectors is reduced. However, multiplexing makes it more difficult to analyze the bus using a regular logic analyzer, since a given sample does not contain all information about a bus transfer. To overcome this, the Analyzer has the capability to demultiplex Address/Data and COMMAND/BEx# into separate trace channels. This is possible since the Analyzer has 128 trace channels, a luxury found only on the most expensive logic analyzers. This important feature not only simplifies readability of the trace, but allows powerful triggers and store qualifiers involving both address and data to be defined easily.

SLOT-SPECIFIC OR USER-DEFINED SIGNALS

The PCI bus has certain slot-specific signals, such as the Request (REQx#) and Grant (GNTx#) signals used for arbitration. These signals can be brought in through eight external inputs on the pin headers on the front panel. The external inputs, fully available in the trigger words, can also be used for any user-specific signals.

GRANT LATCHING

When the slot-specific GNTx# signals are connected as described above, a special latch may be activated to hold the value of the active grant during all data phases. The latched GNTx# value is available in the trace, triggers, store conditions and statistics.

TIME & WAIT STATES TAGS

The Analyzer provides a high-resolution Time Tag for each sample in the trace list. The time tag may either show relative time between each sample or absolute time from the trigger point.

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A second tag in the trace display shows the latency for each PCI transfer, which is defined as the number of wait states from FRAME# asserted to TRDY# asserted.

BINARY DETAILS

Values for multi-bit fields like Address and Data are typically entered in hexadecimal format. But occasionally one may want to specify values of individual bits only, like setting bit 15 to 0 and/or bit 0 to 1, and so on. Called "Binary Details", this is another unique feature of VMETRO's bus analyzers.

ADDRESS/DATA RANGE

Each of the four word recognizers allows precise address and data ranges to be defined, with both 'inside' and 'outside' possibilities. This allows the user to trigger, store or count on accesses to a specific area, e.g. a particular data structure or a HW device. Note that the range can be specified with any arbitrary value down to the last digit, while most other analyzers only allow 2^n size ranges to be defined (by setting don't care in the LSBs).

16-LEVEL SEQUENCER

The Analyzer provides an advanced 16-level Trigger Sequencer with powerful operators like IF, ELSIF, ELSE, STORE, COUNT, DELAY and GOTO. The sequencer is shown in a separate window on the main status screen, and may be used to define nested trigger conditions, define store qualifiers, count and delays statements.

SINGLE EVENT MODE

In many cases a simple trigger like "If Event X then Trigger" is sufficient. For this purpose, there is a default "Single Event Mode" which simply provides a trigger on the event pointed to in the Event Patterns window. When a more complex trigger is required, or a store or count qualifier is needed, the user may switch to the "Sequencer Mode".

PREDEFINED SETUPS

To assist the novice user in defining trigger setups, and to provide a "short-cut" to a number of typical trigger scenarios. BusView offers a function called "Predefined Setups". This function programs the event patterns and sequencer with the appropriate values and commands for the selected task.

FIVE TRIGGER POSITIONS

For maximum flexibility, the trigger can be placed at five different positions in the trace buffer: Start, 25%, Middle, 75% and End of Trace.

TRIGGER OUTPUT

A Trigger Output signal is available on a pin header on the back panel. The TTL compatible signal has selectable polarity and mode, i.e. the signal may simply change logic level on trigger, or it may be selected to pulse when a trigger or a valid store condition occurs. The Trigger Output signal is useful for triggering external instruments like high speed oscilloscopes, counters, etc.

TRACE COMPARE

A powerful feature of the BusView software is the ability to compare the contents of the trace buffer with a trace stored on file on the host PC. This greatly simplifies error location, for example in cases where a system works fine under some circumstances but not under others. Or when one out of several presumably identical systems fails, one may use the Trace Compare function to rapidly spot differences between the failing and functioning systems (see figure at below).

DUMP TRACE TO FILE

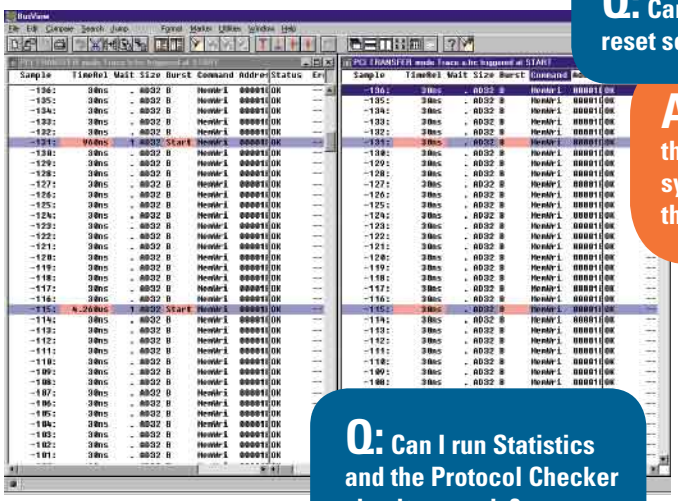
Captured trace data may easily be dumped to a binary or ASCII file on a PC and then loaded back later by means of Dump/Load commands. Partial traces may be loaded, and a packing algorithm reduces transfer time. Trace files may also be reviewed locally on the PC using BusView for Windows, or a DOS Simulator of the Terminal User-Interface.

SEARCH & EXTRACT TRACE DATA

Powerful Search and Extract functions are provided for easy location of particular samples in the trace memory. After a trace is collected, any combination of signals can be searched for in the trace buffer. It is also possible to qualify the displayed data with the search pattern, providing an extracted trace listing, with recalculated time tags, for rapid identification of data of interest.

VERSATILE WAVEFORM DIAGRAMS

When sampling in CLOCK mode the easy-to-read waveform diagrams provide powerful zooming, cursors and navigation tools. To ease the search for cycles of interest, one may use an "edge-to-edge" scroll mode on a selected signal, as well as explicit jumps to given line numbers or to cursors.



Q: Can I monitor a PCI reset sequence?

A: Yes, push and hold the Reset button in the system, start the Analyzer, then release the reset button.

Q: Can I run Statistics and the Protocol Checker simultaneously?

A: Yes, all VMETRO's analyzers have the ability to run all the functional modules independently. This means you can let the Analyzer look for violations to the protocol while you are debugging something else.

STATISTICS OF PCI BUS PERFORMANCE

The PBTM-515 comes with an extensive set of PCI bus statistics and performance measurement functions. Based on dedicated hardware counters, the analyzer offers real-time Bus Utilization and Efficiency statistics that can run at all times as an active window on the screen, in parallel with bus tracing or exercising. There is also real-time Event Occurrence statistics based on user-defined values in the trigger event recognizers. In addition, measurements of Bus Transfer Rate, Command Distribution and Burst Distribution are done by preprogrammed post-capture analysis of the data in the trace buffer. The user may save the displayed statistics data to an ASCII file, for later data importation into applications such as EXCEL for post processing and display.

NON-INTRUSIVE AND STANDALONE

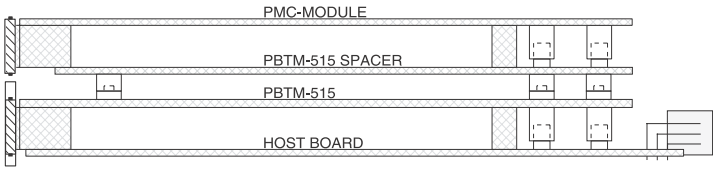
The PBTM-515 offers totally non-intrusive and standalone operation as seen from the host computer to be analyzed. This is possible since the analyzer is equipped with its own processor, communications ports (RS232/USB) and all necessary firmware resident in Flash PROMs. The user may operate the analyzer from a PC running VMETRO's graphical user-interface BusView™ for Windows™, from a standard ASCII terminal like VT100, or using a terminal emulator on a PC or UNIX workstation.

THREE ANALYZERS IN ONE

When used with appropriate adapters, the PBTM-515 can also be used for PCI and CompactPCI. This gives three analyzers in one as shown below.

STACKABLE TO CARRY PMC UNDER TEST

A unique design allows the PBTM-515 to carry another PMC module on top. This is a fundamental feature, allowing analysis of the PCI bus without having to remove a PMC module. The PMC P4 connector is also passed through, to accommodate PMC modules with rear I/O (e.g. to P2ac on VME boards).



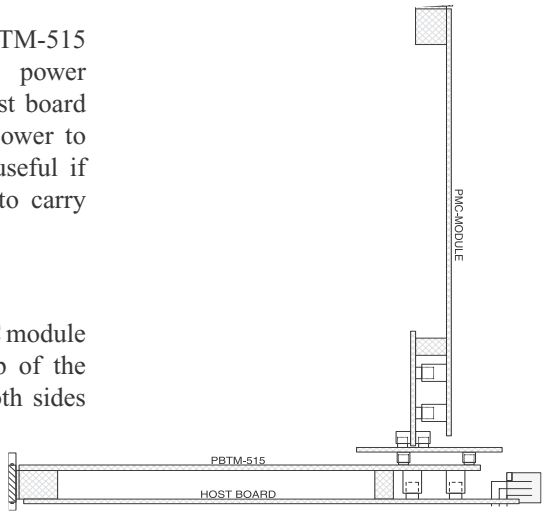
EXTERNAL POWER SUPPLY PROVISION

Another unique feature of the PBTM-515 is the provision for an external power supply. This may offload the host board from the burden of supplying power to the analyzer, and is especially useful if the stacking capability is used to carry another PMC module on top.

90º PMC TEST-ADAPTER

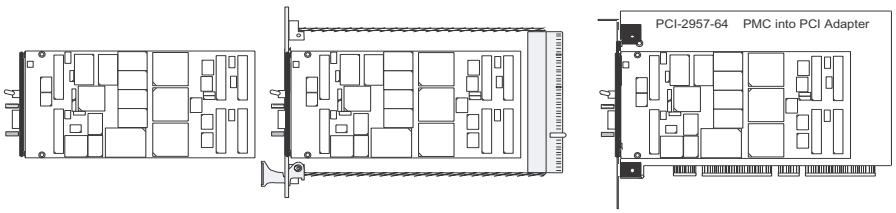
An optional adapter allows a PMC module to be put at a 90º angle on top of the PBTM-515, to give access to both sides of a PMC under test.

(Part # PBTM5-90-SPC).



APPLICATIONS

- Software developers involved in I/O-drivers, operating systems, etc.
- System integrators putting together equipment from various vendors.
- Hardware designers of interface chips, mother boards and expansion cards.



PMC
PBTM-515

CompactPCI
PBTM-515 with EXERBAT-C

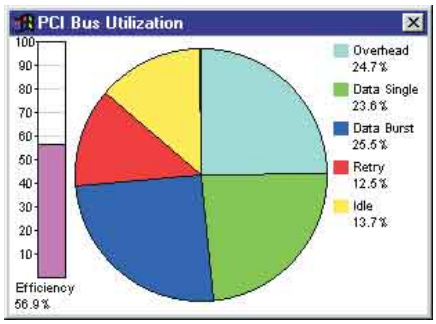
PCI
PBTM-515 with PCI-2957-64 (Clock speed above 33MHz not guaranteed with this adapter).

Q: Why do I need a spacer board on top of the PBTM-515 board?

A: The PBTM-515's low profile connectors prevent it from conflicting with a board in an adjacent VME/CPCI slot. Through a top spacer, the PBTM-515 can carry a PMC under test when an adjacent VME/CPCI slot is open.

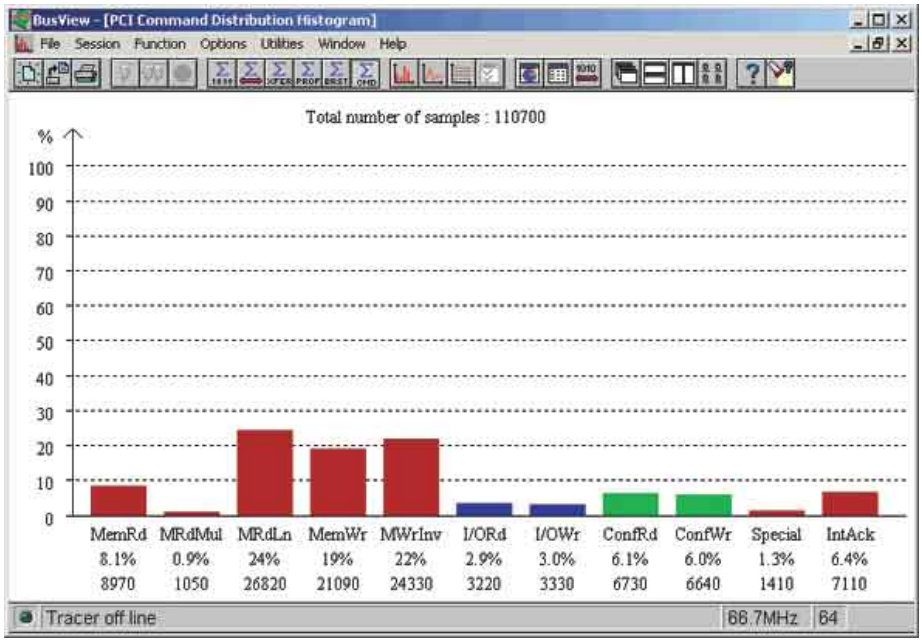
CONCURRENT STATISTICS

The PBTM-515 comes with an extensive set of PCI bus statistics and performance measurement functions. Based on dedicated hardware counters, the analyzer offers real-time Bus Utilization and Efficiency statistics that can run at all times as an active window on the screen, in parallel with bus tracing or exercising. There are also real-time Event Occurrence statistics based on user-defined values in the trigger event recognizers. In addition, measurements of Bus Transfer Rate, Command Distribution and Burst Distribution are done by preprogrammed post-capture analysis of the data in the trace buffer. The user may save the displayed statistics data to an ASCII file, for later data importation into applications such as EXCEL for post processing and display.



COMMAND DISTRIBUTION

The Command distribution statistics displays the relative distribution of the various PCI commands.

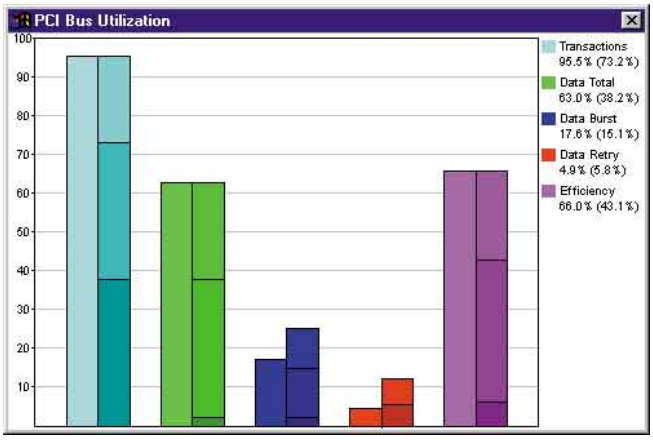


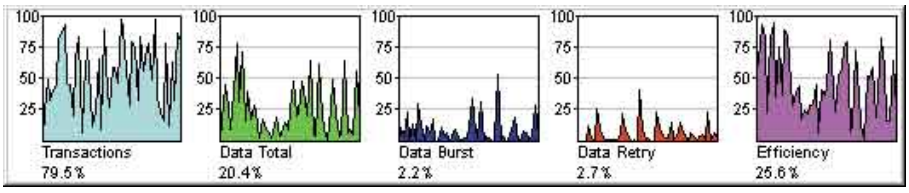
BUS UTILIZATION

The Bus Utilization function provides a direct readout of the percentage of time the bus is occupied. This is ideal for determining whether the system bus has spare capacity to support another I/O-device or processor etc. This function, which is based on hardware counters and a pre-programmed usage of the word recognizers, provides an immediate response readout of how the bus is being used at any time.

Q: Where can I find examples of advanced triggers?

A: The Predefined Setups menu provides a collection of advanced trigger scenarios.





Q: Why are background statistics important to me?

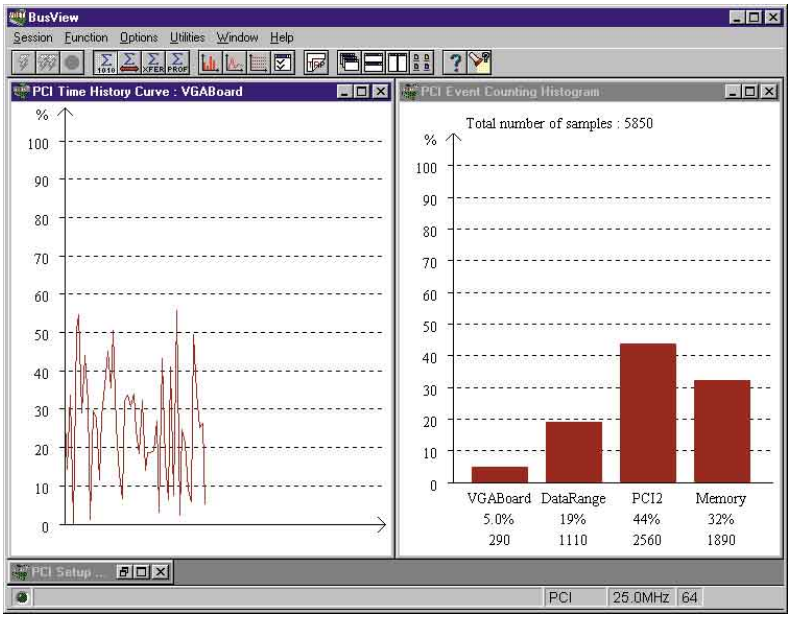
A: The ability to generate performance statistics while exercising the bus, means you can monitor performance metrics continuously while exercising the bus, or using other functions.

EVENT COUNTING

The Event Counting function, which is based on hardware counters, provides a real-time count of the occurrence of four user-defined events. This very powerful function may, for example, be used to count the number of IACK cycles per second displayed as a function of time, to count the number of Write or Read cycles, or to investigate access patterns to the bus in multi-processor systems, etc.

Q: Can I measure the amount of data my card generates as master?

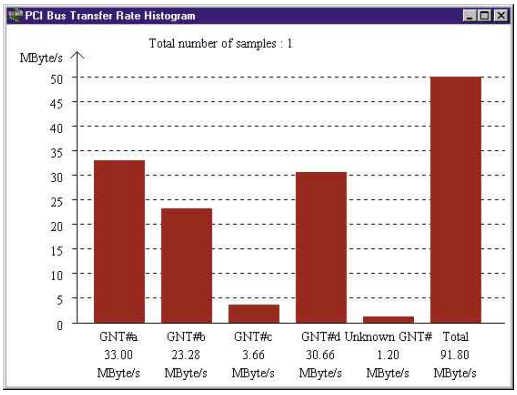
A: Yes, using an external probe connected to the GNT# signal, you can measure this and many other performance parameters.



BUS TRANSFER RATE

The Bus Transfer Rate function presents how much data is transferred over the bus, shown in MBytes/s or in MTransfers/s. This can either be shown between selected lines directly in the trace buffer, to measure burst transfer rate, or as histograms that show the average transfer rate over a certain period of time.

This function can be used to verify if system performance specifications have been fulfilled and to assist in system tuning.



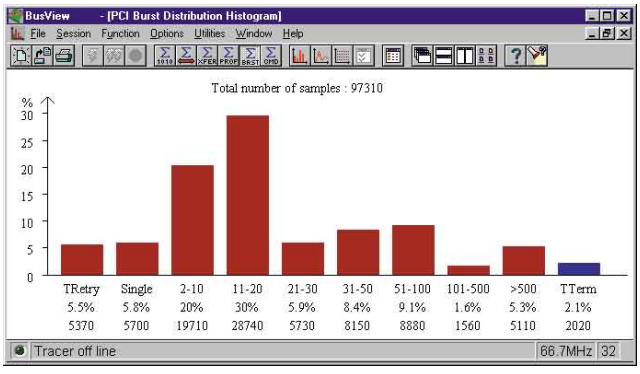
BUS PROFILE

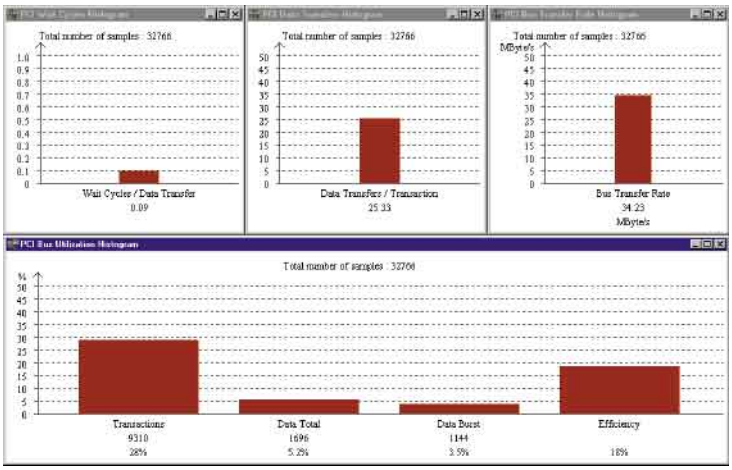
The bus profile function contains a number of different measurements, for characterization of a number of important parameters. These are:

- Number of Wait States per Data Transfer
- Number of Data Transfers per Transaction
- Bus Transfer Rate
- Bus Utilization, including Bus Rate and Bus Efficiency

BURST DISTRIBUTION

In order to optimize a system for a efficiency and/or performance, the burst length distribution statistics offers a detailed statistical overview of the burst length.





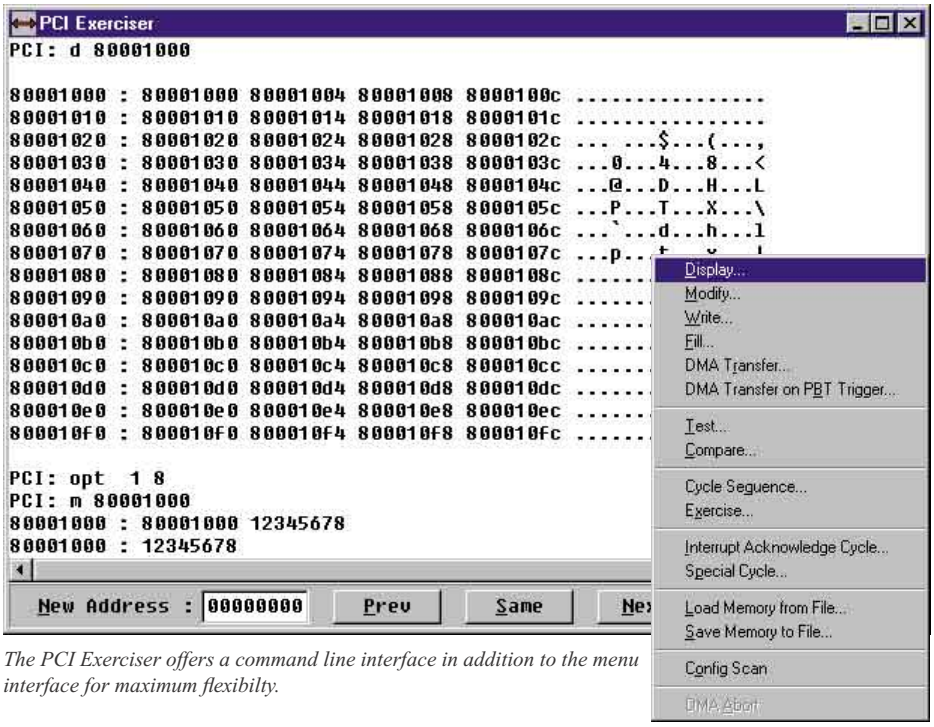
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Exerciser:

- Master, Target and Interrupter for 32-bit and 64-bit PCI up to 66.7MHz.
- Target at user defined address with 8 MB zero-wait-state burst memory.
- Built-in Script Recording and Playback capability.
- Memory Tests with walking ones/zeros, random patterns, etc.
- DMA transfers between Exerciser and target, or between two bus targets.
- Generate and handle interrupts.
- Supports Burst and Single cycles.
- Trigger analyzer if Memory Test fails.
- Start Exerciser on Analyzer Trigger
- Programmable burst length as Master
- Simultaneous Master & Target operation

APPLICATIONS:

- Test ASIC and FPGA designs under development.
- Emulate planned, but not yet available boards.
- Automated Tests during manufacturing.
- Insert Bus traffic load to analyze system performance effects.



The PCI Exerciser offers a command line interface in addition to the menu interface for maximum flexibilty.

64-BIT EXERCISER

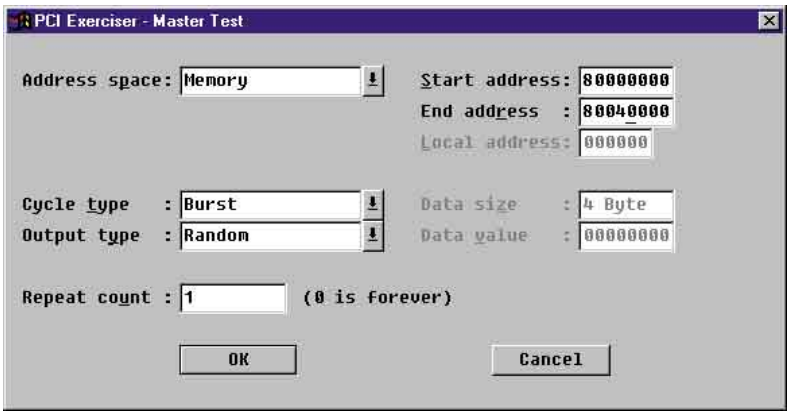
The EXERBAT-C and -M models feature an 64-bit Exerciser that functions as a Bus Master interface with DMA, a Target interface with 8MBytes of memory and an Interrupter. The exerciser supports 64-bit and 32-bit PCI up to 66.7 MHz. The exerciser is controlled via dialog boxes through the user-interface, or self-running with the built-in script recording and playback capability with programmable delay and loop functions.

SIMULTANEOUS EXERCISING & ANALYSIS

The Exerciser is a separate functional unit, which can start and run totally independently and concurrently with the analyzer. Similarly, the Target interface is another separate functional unit with 8MBytes of memory that can be accessed by other PCI agents at any time, with a base address specified by the user. The BIOS of the host system will not need to initialize the exerciser.

BUS MASTER WITH POWERFUL DMA

The Bus Master has two DMA engines, allowing the user to test transactions to several target devices concurrently. Normally, the DMA controllers transfer data between the local memory and PCI memory. However, a unique feature of the Exerciser is the ability to transfer data with DMA from one PCI device to another. Up to 8Mbytes of data can be transferred per DMA command, with peak burst data rates of 533MB/s.



Q: How do I create a test suite for my system?

A: The Exerciser script functionality allows you to create both automatic and interactive exerciser test suites

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MANIPULATE DATA IN PCI MEMORY

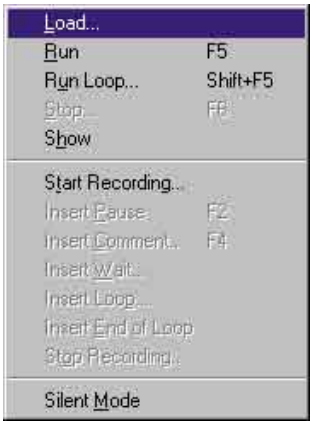
A comprehensive set of commands are available to the user to inspect, manipulate and test data in PCI and local memory. There are also commands to load, dump and compare data between PCI or local memory and files on the Windows host PC. Explicit memory test commands are also provided, using data patterns such as random or walking ones/ zeros. If an error is found, the exerciser can trigger the onboard state analyzer for immediate review of the failing cycle(s). The module may also generate interrupts, IntAck and Special Cycles on the PCI bus.

PLUG AND PLAY

The Exerciser is totally standalone and self-contained as seen from the PCI bus. This means that the BIOS of the host system will not need to configure the Exerciser. All parameters such as Target Address window/(BAR), etc. are set by software through user commands.

SCRIPT FUNCTION ALLOWS AUTOMATED TESTING

A built-in script engine allows test scripts to be created with a convenient record and playback function. Scripts are recorded by manually running through the various commands of the exerciser. Several scripts can be stored and retrieved for later use. Each script consists of sequences of bus cycles of any kind, with varying sizes, cycle types, etc. The script playback function can be set to run single, multiple or infinite playbacks, while the analyzer part of the product may perform bus monitoring in the background. This makes the Exerciser ideal for running automated tests during design verification or production test of PCI devices, adapters and motherboards.



Q: What is the benefit of the command line interface to the Exerciser in addition to the menu interface?

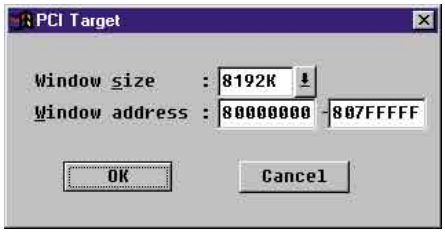
A: It gives you the functionality of an advanced debug monitor, making it very easy to generate PCI commands, set up DMAs etc.

EMULATE A BOARD UNDER DESIGN

In many cases a board intended for a specific system is not available. The Exerciser can emulate this card as a Target or as a Master. This way the software design can progress without waiting for the hardware. The Exerciser also contains a target interface that has its own address decoder for a user defined address window. This may respond to accesses from another module.

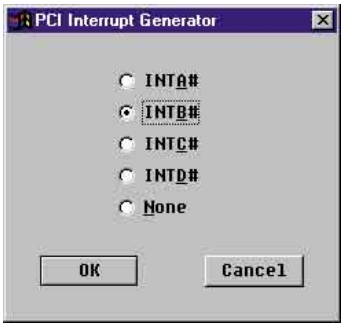
TARGET MEMORY

The module contains 8 MBytes of target memory that can be located anywhere in the PCI address map by a command in the user interface. Data can be written to and read from this memory as single cycles or as zero-wait-state burst cycles (after initial latency) for a peak bandwidth of 533MB/s.



GENERATE PCI INTERRUPTS

The Exerciser can generate any of the four PCI Interrupt lines INTA#, INTB#, INTC#, and INTD#. When an interrupt is generated, it can be turned off through the Exerciser user I/F, or it may remain asserted until another PCI device explicitly turns it off by writing to a certain address of the Exerciser Target. The status of the interrupts asserted by the Exerciser are indicated on the status line of BusView.



Q: Can I generate Type 0 (or 1) Config Cycles?

A: Yes, you can generate all PCI cycles using the Exerciser.

Partial List of available commands

- Display PCI memory in hex and ASCII.
- Modify PCI memory.
- Display Local user memory.
- Modify Local user memory.
- Fill PCI memory.
- Test PCI memory and IO space.
- Initiate DMA between local and PCI mapped memory.
- Map local user memory (as Target Memory) into PCI address space.
- Generate PCI interrupts.
- Sequence cycles.
- Exercise cycles.
- Change PCI access parameters.
- PCI Config Scan.

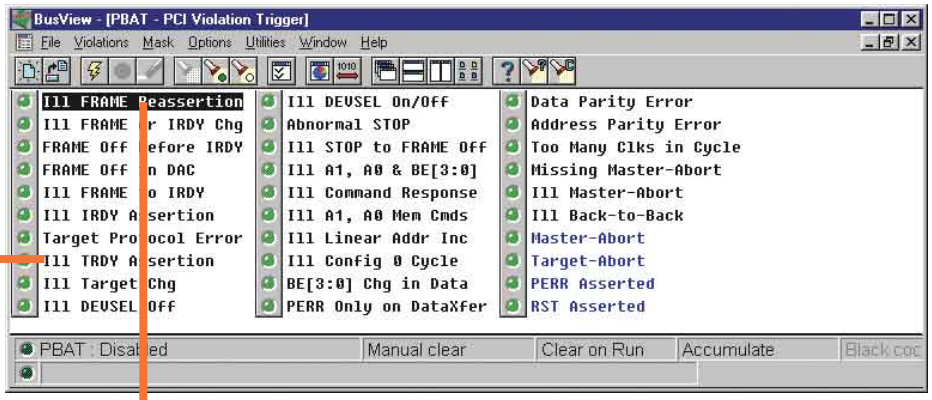
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Protocol Checker

- Continuously monitors the target bus for protocol violations of the PCI specification.
- Automatically detects 45 Protocol Violations and 4 warnings.
- Cross triggers to PBTM-515 for display of violations in waveform
- PCI 2.3 compliant.
- For detailed HW error analysis.

The EXERBAT features a built-in protocol checker for PCI. This versatile feature automatically detects up to 45 PCI protocol errors, helping the user to track down bus hardware errors without the need to understand the nature of the problem.

The protocol checker can run in the background when other analyzer functions are active. As an example, the state analyzer and bus utilization statistics can all be active at the same time while the protocol checker runs in the background, screening the bus for errors. If the protocol checker is used as the trigger source for the analyzer(s), the state analyzer will then provide a comprehensive picture of the bus activity around the point when an error was found. This helps the user to identify and correct the problem.

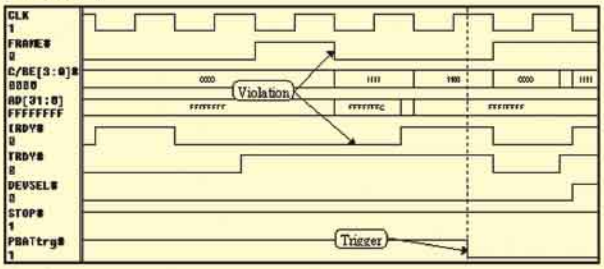


The Protocol Checker reports directly on the screen if protocol violations are detected in the system. Individual violations can be masked off in order to trigger on only one or a selected set of violations.

(Note: In the window below several entries cover multiple violations)

Illegal FRAME# Re-Assertion

Once **FRAME#** is de-asserted, it cannot be reasserted during the same transaction. A transaction is not finished until both **FRAME#** and **IRDY#** is de-asserted.



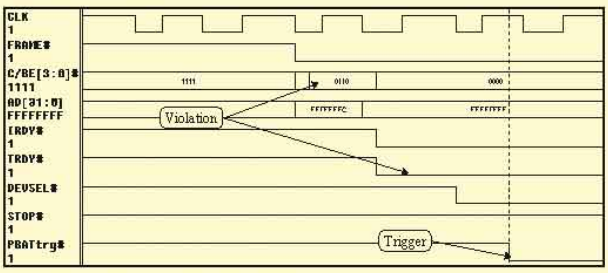
*Illegal **FRAME#** re-assertion*

PCI Spec. 2.1, page 245 - PCI Spec. 2.2, page 251
Rule 8b, and
PCI Spec. 2.1, page 40 - PCI Spec. 2.2, page 49
Section 3.3.3.1

A total of up to 45 PCI protocol violations (below) are automatically detected by the onboard protocol checker.

Illegal TRDY# Assertion

The first data phase on a Read transaction requires a turnaround cycle with **TRDY#** de-asserted.



***TRDY#** is asserted in a Turn-Around cycle*

PCI Spec. 2.1, page 36 - PCI Spec. 2.2, page 47
Section 3.3.1

When a violation is found, the user may pull up a detailed explanation of it in the On-line Help system. This includes reference to the affected rules in the PCI specifications. See yellow boxes.

Q: Can I trigger an external oscilloscope when the Protocol Checker finds a violation?

A: Yes, the Protocol Checker can easily generate an external trigger, both as a level change and as pulses.

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SPECIFICATIONS & ORDERING INFORMATION

PBTM-515

PCI bus:	32/64-bit, up to 66.7MHz
Trace Memory:	64K x 128 bits (Model B) 256K x 128 bits (Model C)
Input channels:	94 PCI signals, plus 8 ext. inputs on pin header.
PCI clock requirements:	Max. 66.7MHz, min. 10MHz, Min. 3.75ns low or high pulse width. 10ms PLL lock time.
PCI signal levels:	5V or 3.3V
PCI signals:	AD[31::0], AD[63::32], C/BE[3::0]#, C/BE[7::4]#, FRAME#, TRDY#, IRDY#, STOP#, DEVSEL#, PAR, PAR64, PERR#, SERR#, RST#, SDONE, SBO#, INTA#, INTB#, INTC#, INTD#, LOCK#, ACK64#, REQ64#, REQ#, GNT#, IDSEL, (Plus GNT3:0#, REQ3:0#, IDSEL via pin headers).
Trigger:	4 word recognizers covering all 94 PCI signals and 8 Ext. inputs. RANGE & NOT operator on Address/Data.
Range:	Four A32 address ranges, Four D32 data ranges. Inside/Outside.
Sequencer:	16 levels with If, Else, Elsif, Goto, Count, Delay, Trigger, Store, Sampling mode, Halt.
Trigger position:	0%, 25%, 50%, 75%, 100%
Occurrence counters:	Four 20-bits (in Sequencer).
Delay counters:	Three 20-bits (in Sequencer).
Event counters:	Five 20-bits (for Statistics), one can run at all times.
Time Tag:	Range: 30ns-9min@33MHz,15ns-4min30sec@66MHz. Resolution: 30ns@33MHz, 15ns@66MHz.
Latency Tag:	Counts latency (wait states) from FRAME# to TRDY# asserted. Max count: 64clks.
Trigger Output:	TTL level trigger output with programmable polarity, level or pulse. May pulse on each stored sample. Available on pin header in bezel.
External Inputs:	Eight TTL level inputs on pin header in bezel.
Compliant to:	IEEE 1386.1, PCI Rev. 2.3
PCI loading:	Max 10pF
Interfaces:	One RS232C serial port, 1200-38400b/s, aut. adjusted. (Cable included). One USB port, 12 Mb/s.
Power supply requirements :	+5VDC +/-5% from PCI host or from ext. power supply via bezel inlet. 1.3A typ. idle, 2.25A sampling @ 33MHz. 2.9A Sampling @ 66MHz. +12V, 0mA typ., 15mA max. when progr. FLASH only. (Optional external power supply available. Part# 401-EPSU)
Dimensions:	74.0 x 149.0mm (Single-wide PMC card)

EXERBAT-M

PMC bus:	32/64 bit, up to 66.7MHz
Master:	Zero-wait-states, 533MB/s peak burst rate, 3 DMA controllers
Target:	8MBytes memory, 533MB/s peak burst rate
Protocol Checker:	45 Protocol Violations
Interfaces:	RS232, USB connection via PBTM-515
Power Supply Requirements:	typ 1.0A @ 5V (EXERBAT-M only) typ 3.9A @ 5V (EXERBAT-M and PBTM-515)
Dimensions:	74mm by 149mm (Single wide PMC card)
Compliant to:	IEEE 1386.1, PCI Rev. 2.3

EXERBAT-C

CompactPCI bus:	32/64 bit, up to 66.7MHz
Master:	Zero-wait-states, 533MB/s peak burst rate, 3 DMA controllers
Target:	8MBytes memory, 533MB/s peak burst rate
Protocol Checker:	45 Protocol Violations
Interfaces:	RS232, USB connection via PBTM-515
Power Supply Requirements:	typ 0.7A @ 3.3V, typ 0.5A @ 5V (EXERBAT-C only) typ 0.7A @ 3.3V, typ 3.4A @ 5V (EXERBAT-C and PBTM-515)
Dimensions:	3U (100mm by 160 mm)
Compliant to:	CompactPCI Rev. 2.1, PCI 2.3

ORDERING INFORMATION

PBTM-515B	64K 64-bit 66 MHz PCI Analyzer
PBTM-515C	256K 64-bit 66 MHz PCI Analyzer
EXERBAT-M	Exerciser & Protocol Checker for PMC
EXERBAT-C	Exerciser & Protocol Checker for CompactPCI

Packages:

PBTM-515z-XM	Analyzer, Protocol Checker & Exerciser for PMC.
PBTM-515z-XC	Analyzer, Protocol Checker & Exerciser for CompactPCI.
PBTM-515Bz-XMC	Analyzer, Protocol Checker & Exerciser for PMC & Compact PCI.

(Replace z with B for 64K Trace and C for 256K Trace)

BusView software is included with all PBTM-515 models and packages. (Supports Windows™ 95*, 98, NT4.0 (*95 version 4.00.950b or later), 2000, Me and XP).

Note: The EXERBAT-M/C can be used standalone (without the PBTM-515), as an Exerciser only. The Protocol Checker capabilities are only available when used together with a PBTM-515 operated with BusView for Windows.

WARRANTY

All VMETRO analyzer products have one year warranty.

Specifications subject to change without notice. V1.2002.

BusView is a trademark of VMETRO, Inc., USA. Windows is a trademark of Microsoft Corp. USA.

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