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VBT-325
VMEbus Analyzer



VMEbus

VSB

SCSI

UserP2

VXI

VMETRO
www.vmetro.com

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VBT-325

VBT-325C VMEbus & VSB/SCSI/P2 Analyzer
VBT-325B VMEbus Analyzer



THE INDISPENSIBLE TOOL FOR VMEbus DEVELOPMENT

The VBT-325 is a state-of-the-art VMEbus Analyzer, proven in labs throughout the world to be the de facto reference tool kit for VMEbus system developers. The unit offers state and timing analysis with powerful triggering, as well as statistics of bus performance for timing.

TWO MODELS

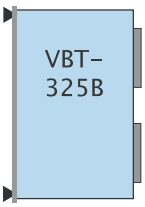
The VBT-325 is available in two models, the VBT-325B and ´C. The VBT-325B is a high-performance VMEbus analyzer only, while the VBT-325C offers two independent analyzers, one for VME and one for a P2 bus such as VSB, SCSI or a user-defined bus. VBT-325C can also be used for VXI analysis by means of an adapter (VXE-35C).

OPTIONAL PIGGYBACK MODULES

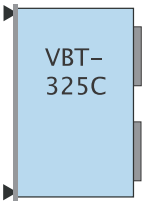
For additional performance or functionality, a family of piggyback modules is available, like 200MHz timing analyzer, anomaly trigger, bus masters and slave, extended trace buffers, and pattern generator. (Please refer to separate catalogue for details).

OPERATES FROM WINDOWS OR TERMINAL

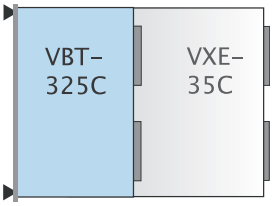
The VBT-325 is operated through RS232 from a Windows PC running the BusView™ GUI (see page 12), or from a terminal such as VT100. A terminal emulator also allows operation from e.g. a UNIX environment.



VME



VME
P2
VSB/SCSI/USER

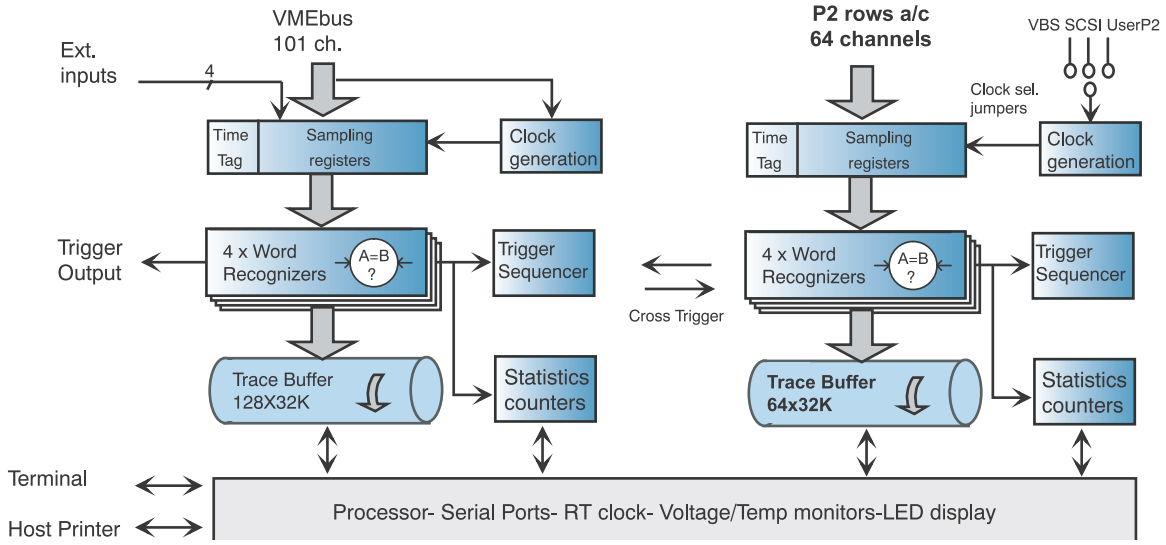


VXI

VBT-325 SPECIFICATION HIGHLIGHTS

- **101 VME signals sampled**
- **64 P2 signals sampled (VBT-325C only)**
- **4 external inputs and one trigger output**
- **32K Samples Trace Buffer (up to 1M samples optional)**
- **Up to 25MHz State Analysis**
- **50MHz Timing Analysis (200MHz optional)**
- **4 Trigger Words (8 opt.), each w/ Address & Data Ranges**
- **16 Levels Trigger Sequencer w/ If, Count, Delay, Go to, Store etc.**
- **20ns Trigger Sensitivity (5ns opt.)**
- **Built-in Voltage Monitor**
- **Optional Temperature Probe**

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The VBT-325C consists of two dedicated analyzers, one for VME and one for P2, configurable for VSB, SCSI or user-defined P2 buses with jumpers. The VBT-325B is a VMEbus Analyzer only.

APPLICATIONS

SW Analysis

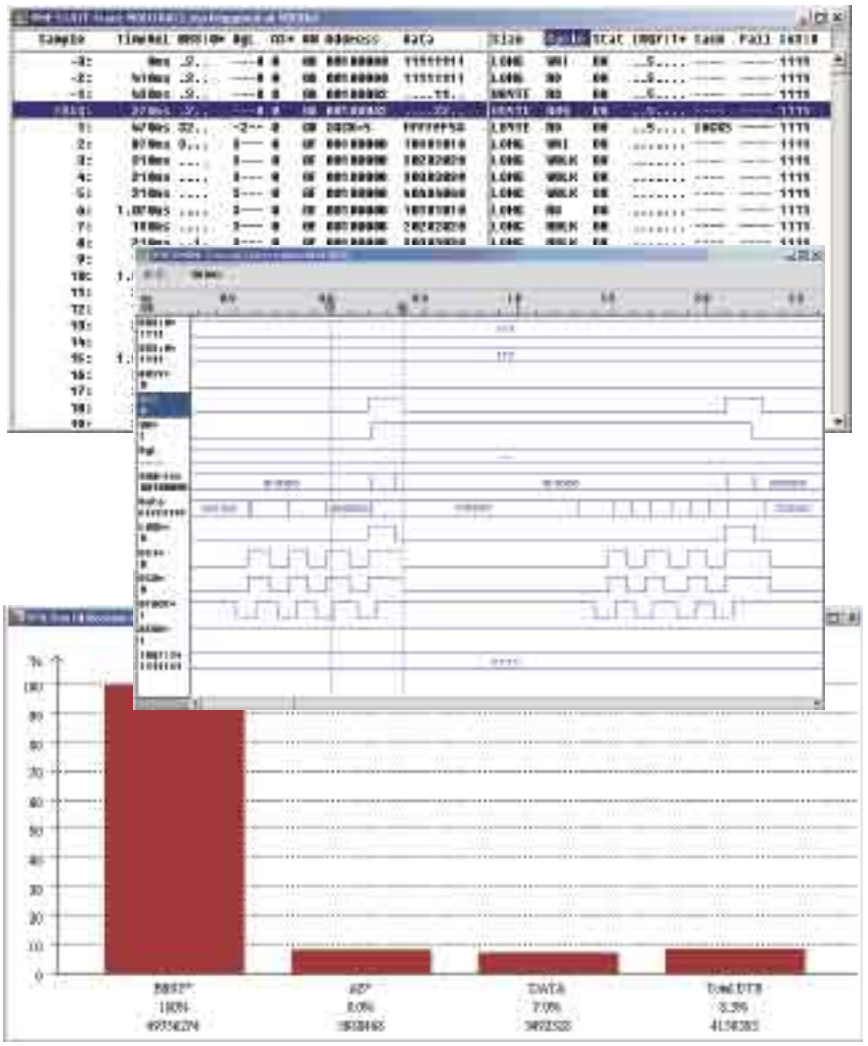
- Board Configuration
- Device Drivers
- Interrupt Systems
- Real-Time Kernels
- Multiprocessors
- State Trace Listing

HW Analysis

- Bus Timing
- Board Incompatibilities
- Protocol Violations
- Margin Testing
- Intermittent Failures
- Timing Waveforms

System Analysis

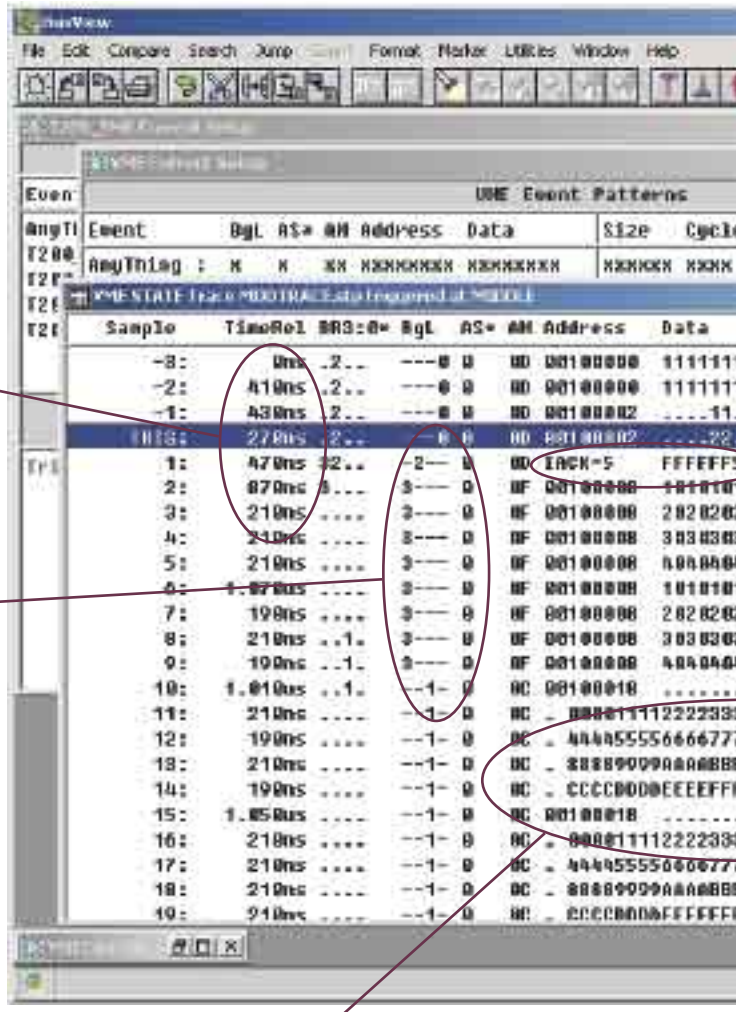
- Bus Traffic Patterns
- Event Statistics
- Performance Measurements
- Bus Utilization
- System Tuning
- Statistics Histograms



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STATE ANALYSIS

Monitor bus activity cycle-by-cycle



PROTOCOL-SENSITIVE STATE SAMPLING

One of the most fundamental features of the VBT-325 is the protocol-sensitive sampling of bus cycles for state analysis. Unlike other logic analyzers, VMETRO bus analyzers know the bus protocol of VMEbus, as well as VSB, SCSI and VXI, and derive sampling clocks from the bus cycles at the right moments. This gives a complete trace of all kinds of bus activity, including arbitration, interrupts, block cycles, RMW etc.



POWERFUL TRIGGER AND STORE QUALIFIERS

To narrow in on just the cycles of interest, the VBT-325 is equipped with powerful triggers and store qualifiers, based on four full-width word recognizers and a flexible sequencer. There are separate sets of word recognizers and sequencers for the VME and P2 part, allowing cross-triggering both ways. Each of the word recognizers offer powerful operators like RANGE, NOT and BINARY for address and data fields etc., and the user may specify signal values as hex, binary or by mnemonics like WRITE, LWORD etc. This eliminates the need for the user to remember the actual signal values for the different cycle types etc.

NOT OPERATOR

An important feature is the ability to specify a NOT operator, to allow constructs like: Trigger on

DATA *not equal* VALUE

ADDRESS/DATA RANGE

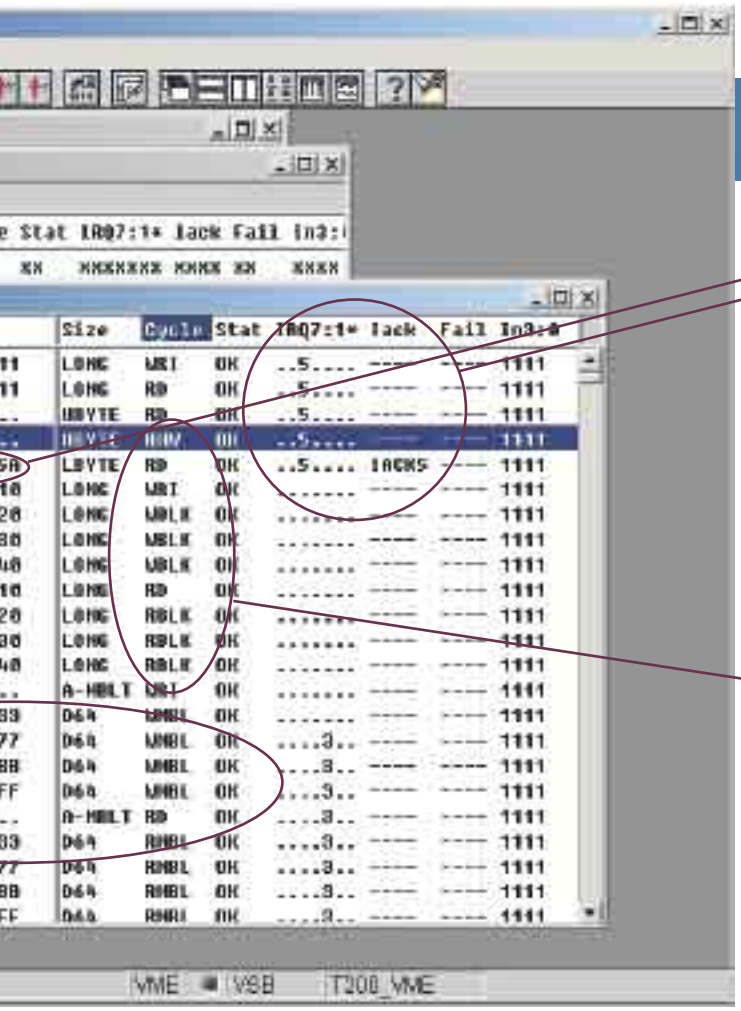
Each of the four word recognizers allows unrestricted address and data ranges, with both 'inside' and 'outside' possibilities. The address ranges can even be specified as 64-bits wide to comply with VME rev.D.

SINGLE EVENT MODE

In many cases a simple trigger like "If Event X then Trigger" is sufficient. For this purpose, there is a default "Single Event Mode" which simply gives a trigger on the event pointed to in the Event Patterns window. When a more complex trigger is required, or a store or count qualifier is needed, the user may switch to the "Sequencer Mode".

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SW ANALYSIS



Interrupts
The flow of Interrupt Requests and Interrupt Acknowledge cycles can easily be read out from the trace list.

Mnemonics
are used for Transfer Size, Cycle Type and Status to maximize readability. The formatting supports all VMEbus transactions incl. VME64, IACK and RMW cycles.

16-LEVEL SEQUENCER

The VBT-325 provides an advanced 16-level Trigger Sequencer, with powerful operators like STORE, COUNT, DELAY and GOTO. The sequencer is shown in a separate window on the main status screen, and may be used to dynamically change sampling mode, define nested trigger conditions, or define the trigger position and store qualifiers etc.

TIME TAG

During state sampling, the VBT-325 measures the elapsed time between bus cycles, and this is displayed as a "Time Tag" for each sample in a separate column in the state trace list. The time tag may either show relative time between each sample, or absolute time from the trigger point. A resolution of 20ns is provided, with a range of 40ns up to 1,5 hour. (The time tag is also used to calculate Bus Transfer Rates in the Statistics and Count functions.)

BUS GRANT SAMPLING

The Bus Grants on VMEbus (BG3-0IN/OUT*) are valid only for a short time when BBSY* is asserted. In order to provide information about the bus grants during state analysis, the VBT-325 contains a unique circuit to sample and latch the Bus Grants when valid, and display this information together with the address, data etc. in the trace. This is essential information when testing multi-master systems.

FORMATTED, FLEXIBLE TRACE DISPLAY

The protocol-sensitive state sampling method provides one trace line per bus cycle, and the collected trace is presented in a formatted way with mnemonics for easy readability of the captured bus cycles. To optimize readability further, the user may freely rearrange the signal layout in the trace display. It is also possible to have multiple trace windows opened, to see various portions of the trace at the same time.

SEARCH & EXTRACT TRACE DATA

Powerful Search and Extract functions are provided for easy location of particular samples in the trace memory. After a trace is collected, any combination of the signals in the trace can be searched for. It is also possible to qualify the displayed data with the search pattern, giving an extracted trace listing, with recalculated time tags, for rapid identification of the data of interest.

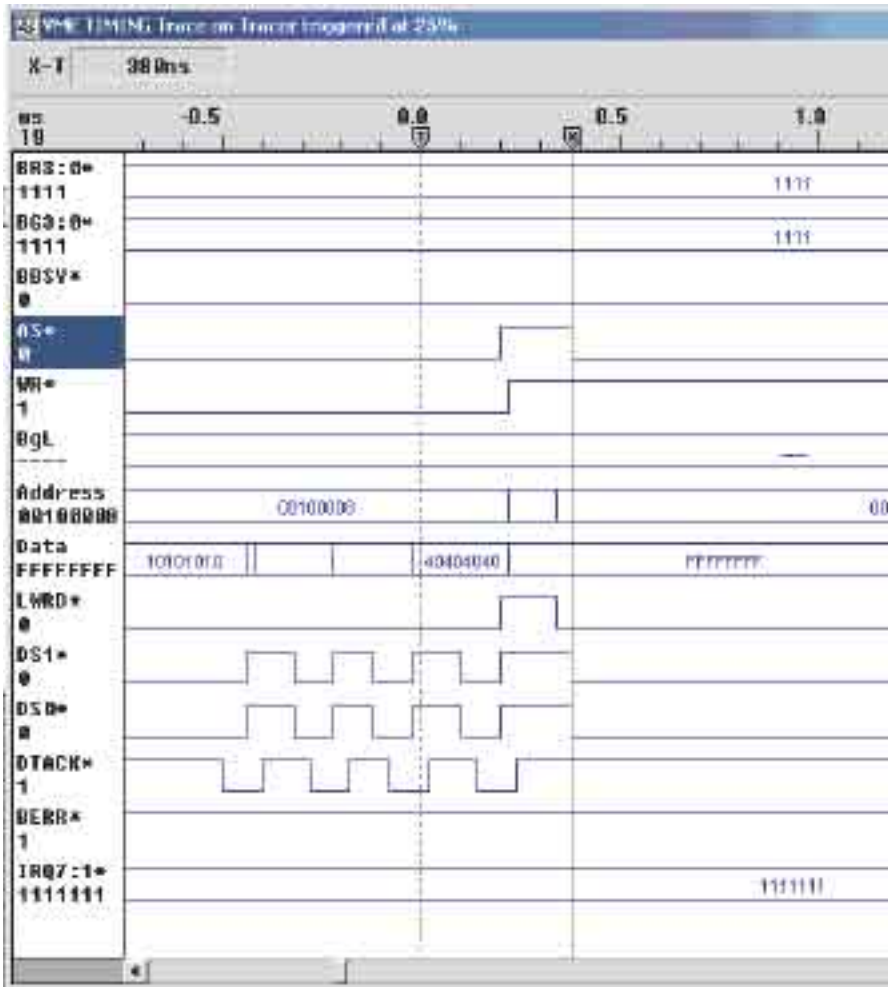
CROSS-TRIGGERING

Since the two analyzer parts of the VBT-325 are completely independent, cross-trigger signals are provided in both directions between the two parts. It is also possible to run state (synchronous) sampling in the VME part and timing (asynchronous) sampling on P2 or vice versa.

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TIMING ANALYSIS

Monitor bus cycle details



TIMING ANALYSIS

To reveal details of bus timing, measure access times etc., the VBT-325 provides timing analysis up to 50MHz with full-speed trigger on all VME and P2 signals. The sampling clock may also be selected to slower rates down to 0.1MHz independently on VME and P2, useful to analyze events of long duration, like timeouts and power-up/down signals like SYSRESET* and SYSFAIL*. For more demanding analysis of bus timing problems, 200 MHz Timing Analysis on all bus signals in parallel is available with the TIMBAT-PB optional piggyback module. This module also offers automatic detection of VMEbus anomalies. (See inserts and also separate catalogue).

FULL-SPEED TRIGGERING

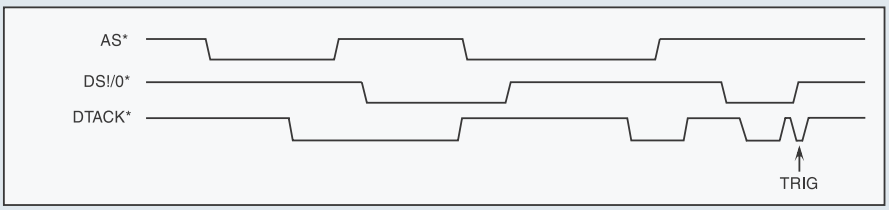
The same powerful triggering mechanisms as used for state analysis apply also to timing sampling with the VBT-325. The four full-width word recognizers can be used individually, or in a sequence as defined in the Trigger Sequencer. The VBT-325 word recognizers and sequencer are fast enough to react on events as short as the fastest sample period, i.e. 20ns at 50MHz. (Similarly, the 200MHz option with TIMBAT-PB offers a trigger speed of 5ns).

STORE QUALIFIERS

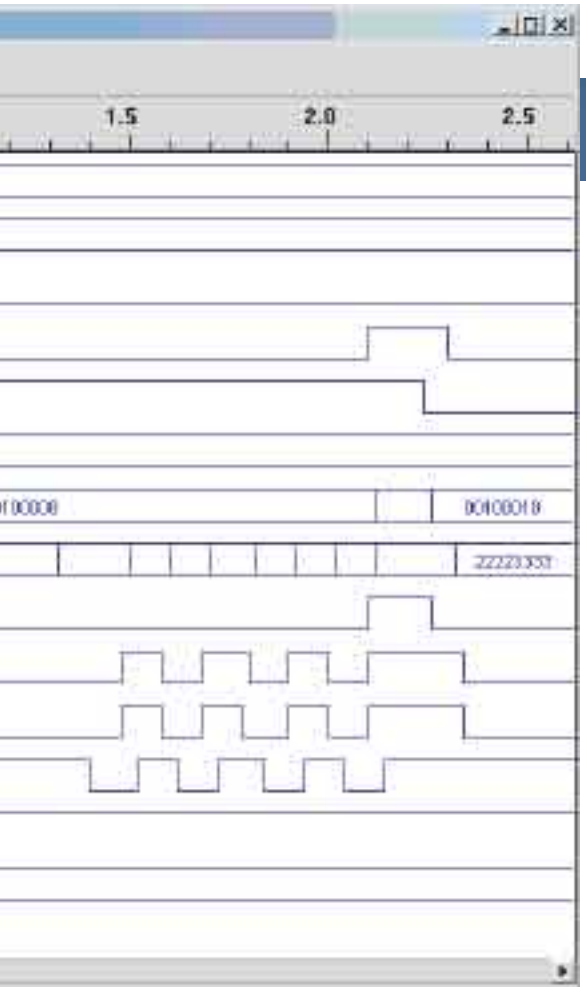
Like in state sampling mode, store qualifiers can also be used in timing mode. For example, this allows only cycles belonging to a certain Bus Grant level on VMEbus to be stored (using the latched Bus Grant, "BgL", as qualifier), thus avoiding consuming space in the trace buffer for cycle of no interest.

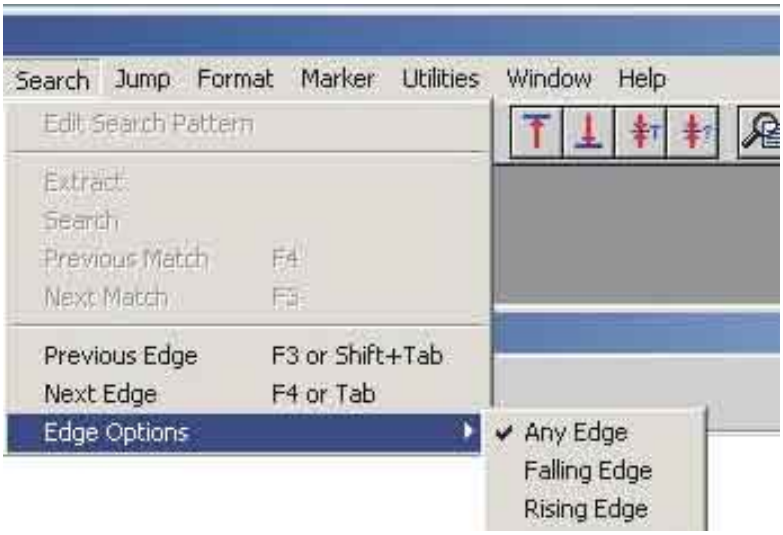
200 MHz Timing

The TIMBAT-PB is a piggyback module that offers 200 MHz Timing Analysis on all VMEbus address, data and control signals. This module allows full-speed triggering on all channels, with a "duration filter" that gives a trigger only if the specified pattern is valid for >/< a given time, useful to reveal glitches (e.g. DTACK* < 10 ns), excessive access times (e.g. DS1/0* > 500 ns), etc.



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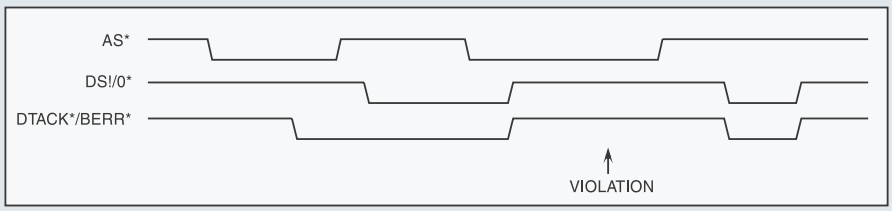


VERSATILE WAVEFORM DIAGRAMS

The easy-to-read waveform diagrams provide powerful zooming, cursors and navigation tools. To ease the search for cycles of interest, one may use an "edge-to-edge" scroll mode on a selected signal, as well as explicit jumps to given line numbers or to cursors. The address and data are always shown on top of the waveform window together with readout of delta-time between cursors to measure time between events.

Anomaly Trigger

The VBAT64-PB and TIMBAT-PB are piggyback modules that contain a VMEbus Anomaly Trigger which automatically screens the VMEbus for violations of the bus protocol. Rule-based parallel trigger elements continuously and simultaneously report bus timing violations like illegal cycle termination, address not stable, bus granted to two masters etc., giving explicit error messages on the screen and by a trigger signal to the VBT-325.

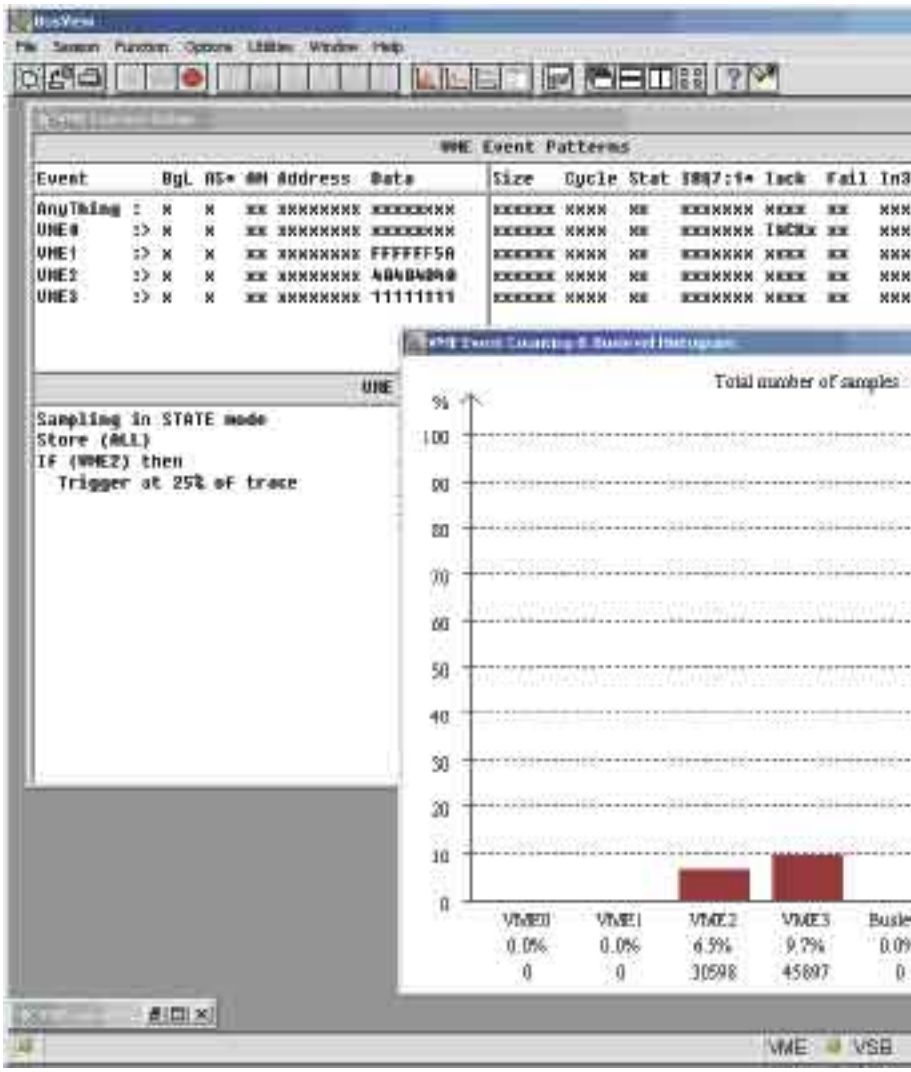


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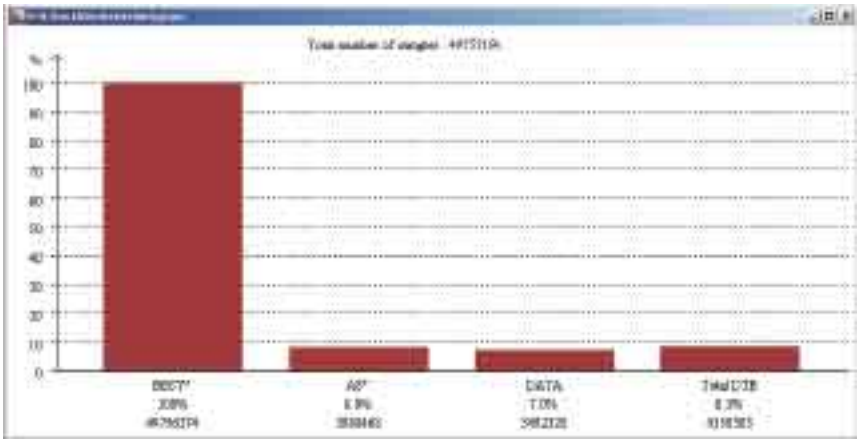
STATISTICS

Bus behaviour shown as histograms

Substantial amount of hardware is built into the VBT-325 to perform real-time statistics and performance measurements on VMEbus and P2 buses like VSB and SCSI. Hardware event counters tied to the word recognizers, complemented with separate counters that count cycles on each of the Bus Levels on VME, allow powerful and responsive measurements of event occurrence, bus level usage and bus utilization. There is also trace based statistics, performing post-processing on a series of traces, as for the Bus Transfer Rate measurement.



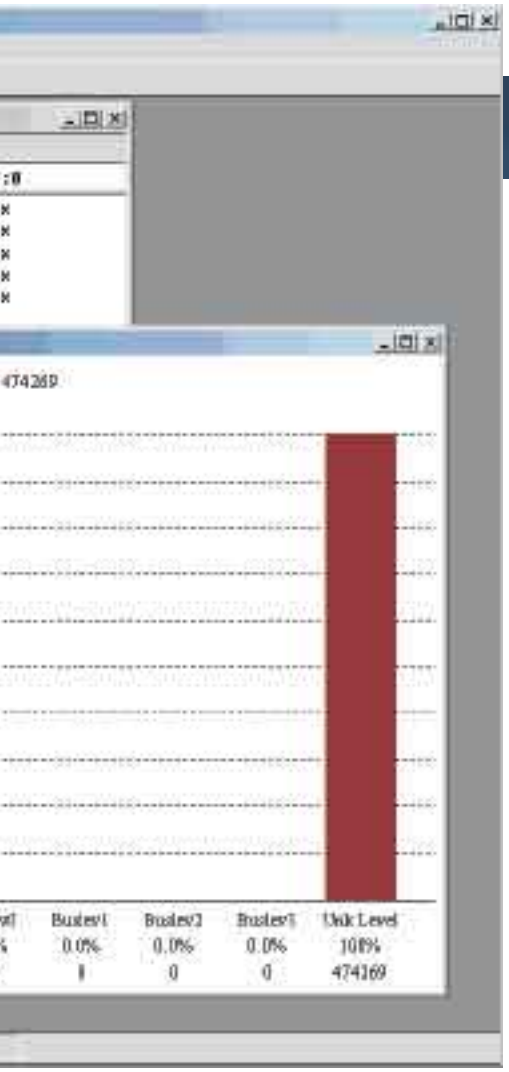


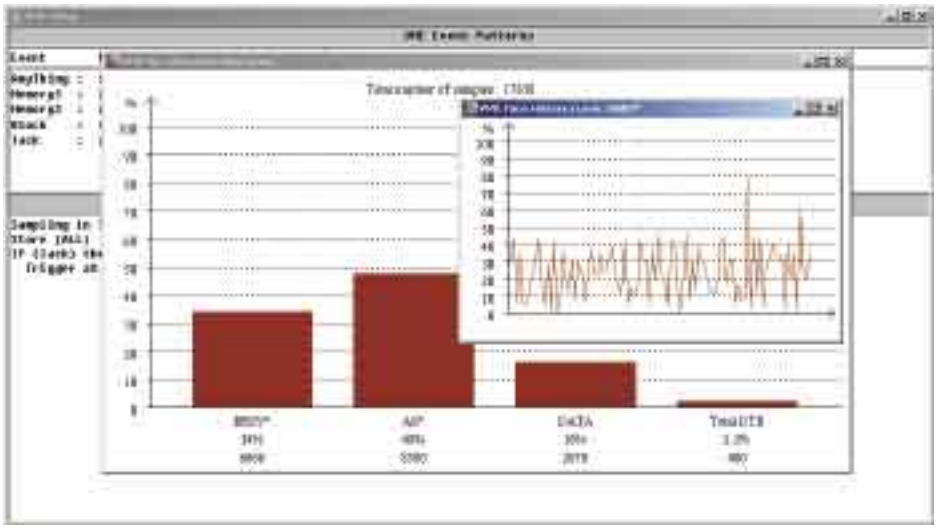


POWERFUL DISPLAY OPTIONS

The statistics histograms can be presented with a number of display options, like bar markers to indicate min./max./average values, different maximum scale readings, as well as a Time History Diagram to show variance over time. Also, the histogram update rate can be chosen to a specific count number (e.g. update every 1M samples) or at a given time (e.g. update every 2 sec).

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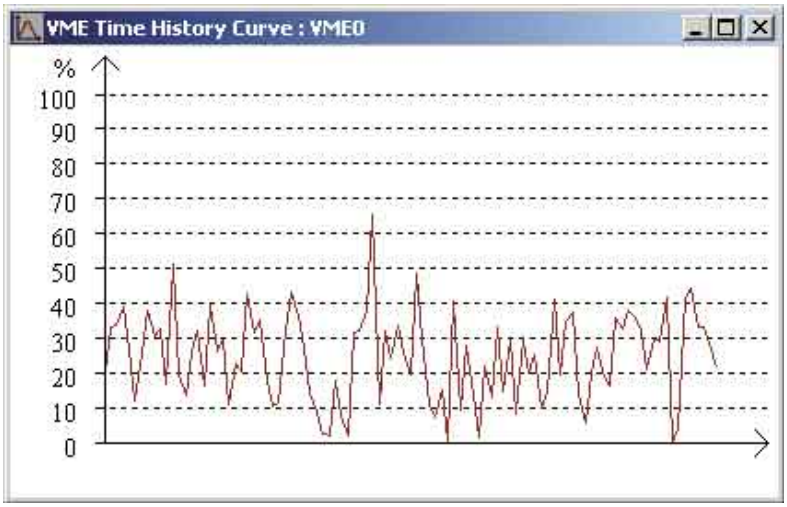


EVENT AND BUS LEVEL COUNTING

Based on HW counters, the Event and Bus Level Counting function provides a real-time count of the occurrence of four user-defined events, as well as the distribution of cycles over the four VMEbus Bus Levels. This very powerful function may for example be used to count the number of e.g. IACK cycles per second displayed as a function of time, or to ensure fair access to the bus in multi-processor systems, etc.

BUS UTILIZATION

The Bus Utilization function provides a direct readout of the percentage of time when the bus is occupied. This is ideal to determine whether the system bus is overloaded, if it has spare capacity to support another processor etc. Separate readings are provided for bus ownership ("BUSY"), addressing and data transfer, as well as the sum in time when either of the three is active. Based on the hardware counters, asynchronous sampling and a pre-programmed usage of the word recognizers, this function gives an immediate response readout of how the bus is being used at any time.



The Time History Diagram displays the statistics readings as a function of time, as shown in the example above.

BUS TRANSFER RATE

Based on trace post-processing of the time tag and transfer size stored with each sample, the Bus Transfer Rate function presents how much data is transferred over the bus, shown as MBytes/s and in Mtransfers/s. This is either shown between selected lines directly in the trace buffer (e.g. a specific DMA transfer), or as histograms that also show the transfer rate on the four VME bus levels. This function can be used to characterize a system, to verify if performance specifications have been fulfilled and to assist in system tuning.

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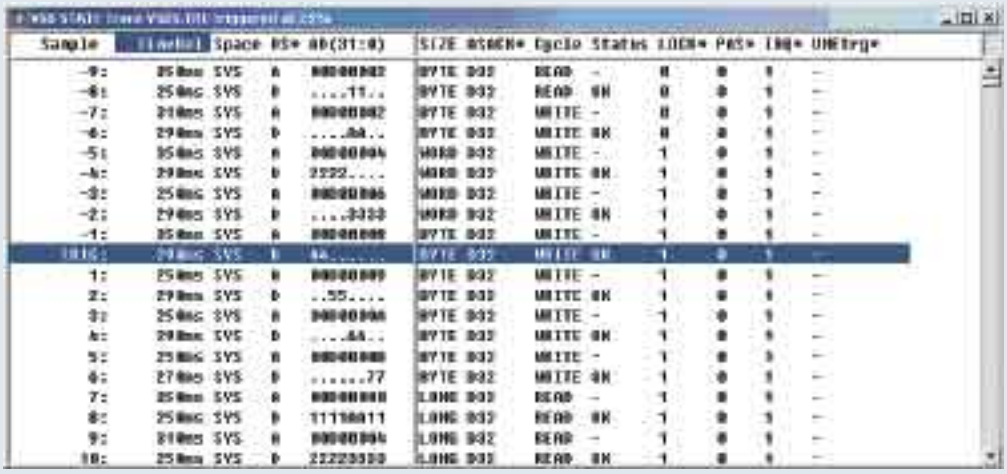
VMEbus

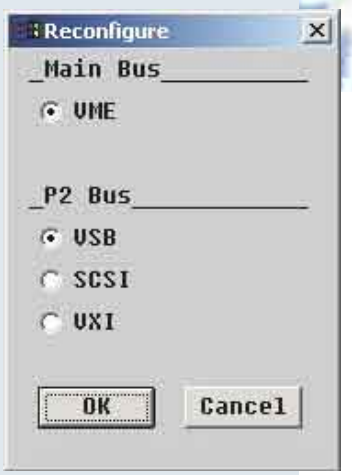
VMEbus is the workhorse industry-standard bus for embedded systems, and as a consequence, analysis of VMEbus systems is the most important application the VBT-325 analyzer. Inheriting the expertise gained from VMETRO's three previous generations of VMEbus analyzers and incorporating wishes and suggestions from customers over 10 years, the VBT-325 offers VME analysis capabilities superior to any other analyzer available.

The flexible architecture of the VBT-325 allows analysis of various P2 buses in addition to VMEbus. Simple jumper reconfiguration selects actual P2 bus.

VSB

Many VME systems take advantage of the "VME Subsystem Bus" - VSB - on the P2 connector to increase available bandwidth in the system. The twin architecture of the VBT-325C allows powerful state, timing and statistics measurements for VSB at the same time as VME analysis is performed, using a separate set of HW resources.





SCSI

The P2-part of VBT-325C may perform timing or state analysis of SCSI or SCSI-2 bus. A single-ended SCSI-bus can be attached directly to the back of the slot where the VBT-325 is installed, using a standard 50-lead flat cable on P2 a/c rows 8-32. This supports an 8-bits SCSI/SCSI-2 directly, while a 16-bits SCSI-2 requires an adapter board that is installed between the cable and the P2 plug.

The SCSI trace screen shows commands, messages etc. in a decoded form with mnemonics. Also waveform diagrams may be provided, particularly useful if timing sampling is employed. Statistics like event counting based on 20-bit hardware event counters is also supported for SCSI/SCSI-2.



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USER P2

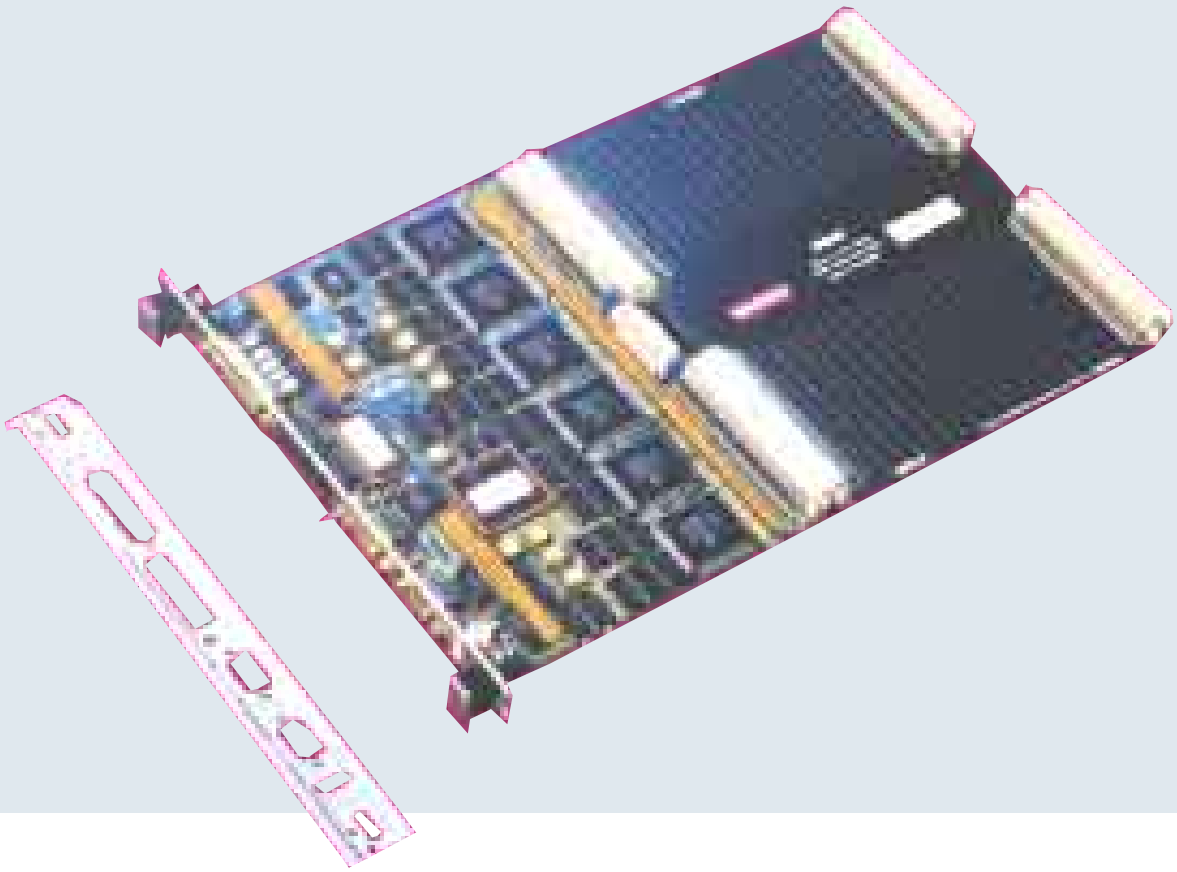
The 64 user-definable pins on the a- and c-row on the P2 connector of VME boards are in many applications used for custom I/O or proprietary local buses. To provide convenient analysis of such buses, the VBT-325C allows the user to define freely his/her own P2 bus definition, by assigning signal and bus names to any P2ac signal or signal group. For state analysis, the user may supply a sampling clock to a separate onboard socket.

VXI

The VBT-325C can be used as a VXI analyzer in C-size VXI systems by means of the VXE-35C VXI Adapter, allowing simultaneous analysis of VME and TTL signals on P2 in VXI systems. The VXE-35C handles the necessary form-factor adaptation, daisy-chaining of the LBUS signals between rows a and c on P2, as well as the necessary isolation of non-TTL signals on P2ac.

VXE-35C Features

- **Supports LBUS11:0 (TTL level) and TTLTRG7:0* in P2 analyzer of VBT-325C.**
- **State analysis of P2 VXI signals possible with user-supplied sampling clock.**
- **Provides continuity from LBUSA11:0 to LBUSC11:0.**
- **Isolates ECLTRG1/0, CLK10+/-, SUMBUS and all power supply pins on P2 to prevent damage of VBT-325C TTL inputs.**
- **Provides 825W pulldown resistor on MODID for module detection.**
- **Supplied with VXI front panel for the VBT-325C, with mechanical lockout keys to prevent installation in non-TTL slots.**



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USER INTERFACE

The VBT-325 is equipped with a powerful user-interface in onboard FLASH PROMs, to run with character-based terminals like VT100 etc., or PCs/workstations with a terminal emulator. As an option, a true Windows-based Graphical User-Interface is available, see BusView description below.
Whether run from a terminal, PC/WS with terminal emulator or from Windows, the user will find similar windows, command bars, pull-down menus and dialog boxes. To speed up operation for experienced users, single-letter accelerator commands are always available in the menus and dialog boxes.

PRINT TRACE

A Print command allows printout of the trace just as it is presented on the screen, either as waveforms or as an alphanumeric list with mnemonics and actual signal columns selected. An ASCII printer attached to the RS232 “Host” port may be used, or, if running under Windows, the default Windows printer may be used.

DUMP TRACE TO FILE

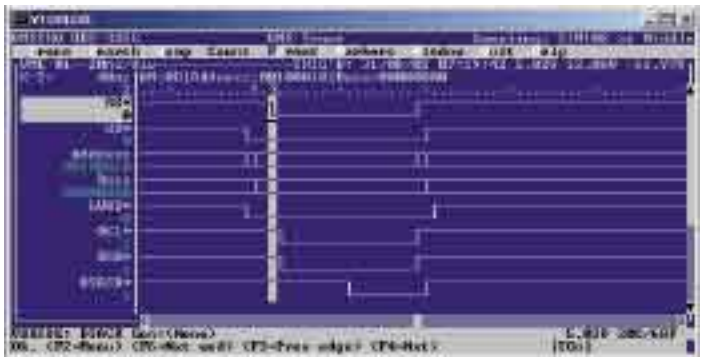
Captured trace data may easily be dumped to a binary file on a PC and loaded back later by means of Dump/Load commands. Partial traces may be loaded, and a packing algorithm reduces transfer time. Trace files may also be reviewed locally on the PC using the “Simulator”.

TRACE REVIEW USING SIMULATOR

In order to review trace files that have been dumped to a file on a PC, a “Simulator” of the user-interface is delivered with each VBT-325. The Simulator runs under DOS, and is a true replica of the user-interface of the VBT-325.







BusView™

Graphical User-Interface for PCs & Windows™

BusView is an optional Windows-based graphical user-interface for the VBT-325 Analyzer, bringing together the user-friendliness and flexibility of Windows with the unmatched analysis efficiency of the VBT-325. BusView offers high-resolution graphics, user-friendly mouse operation, multi-windowing and immediate file storage capabilities for trace data and setups, taking full advantage of the PC and the Windows platform.

- Runs under Windows 95, NT, 3.X.
- File storage of setups and trace data.
- Transparent access to host/target processor on other serial line in a separate window.
- Harmonized with the terminal version of VBT-325 user-interface, allows users to switch easily between PC and terminals.

BusView is a trade mark of VMETRO, Inc., USA.
Windows is a trade mark of Microsoft Corporation, USA.

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UTILITIES

TEMPERATURE PROBE INPUT

For measuring ambient temperature in various locations in the system, for example to locate areas with insufficient cooling, an optional temperature sensor with 1m/3ft cable can be connected to a mini-coax input on the front panel. The readout may either be presented on the screen, or on the front panel display.

VOLTAGE MONITORS

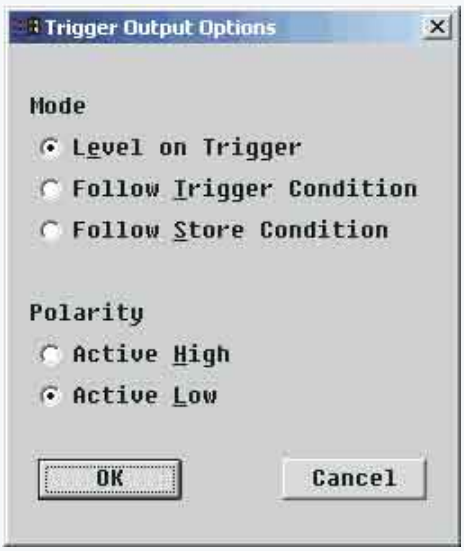
The VBT-325 is equipped with voltage monitors for the +5V and the +/-12V supplies, for presentation in on the screen, or on the front panel display. The voltages are also sampled at trigger time, together with temperature and time-of-day, and this information is stored as a tag with the captured trace. This may reveal errors caused by temporarily illegal voltages or temperature.

EXTERNAL POWER SUPPLY PROVISION

An important feature of the VBT-325 is the provision for an external power supply. This not only makes it possible to use the VBT-325 in systems with a marginal power supply, but it allows a complete monitoring of the power-up sequence of VMEbus systems.

TRIGGER OUTPUT

A Trigger Output signal is available on a mini-coax outlet on the front panel. The TTL compatible signal has selectable polarity and mode, i.e. the signal may simply change logic level on trigger, or it may be selected to pulse when a trigger or a valid store condition occurs. The Trigger Output signal is useful to trigger external instruments, like high speed oscilloscopes, counters etc.



FOUR EXTERNAL INPUTS

There are four external input signals available via mini-coax connectors on the front panel. These are included in the trace as well as in the four word recognizers, so that any of these signals can take part in the trigger, count or store qualifiers.

LED DISPLAY

The alphanumeric LED display on the front panel presents various status information like trigger status, voltage, temperature or bus violations found by a Bus Anomaly Trigger on a piggyback module etc.

RS232 SERIAL PORTS

There are two RS232 serial port for connection to a terminal or PC and to a printer or a host. For example, if the second serial port is connected to a CPU board in the VME system, the “Transparent mode” allows the VBT-325 to be operated from a terminal already connected to the CPU. In this way there is no need for a separate terminal or PC for the VBT-325. Baud rates from 1200 to 19200 are supported.

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PIGGYBACKS



Although the VBT-325 offers substantial performance and functionality in itself, a family of powerful piggyback modules is available to further enhance the capabilities of the analyzer. By selecting the proper piggyback module, this allows the user to tailor his/her VBT-325 to offer the best solution for the application, whether it is for HW or SW analysis.

PIGGYBACK CARRIER

Some applications may benefit from using more than one piggyback module at a time. For this purpose, VMETRO offers the "VMETRO Piggyback Carrier" - VPC-MkII. The VPC-MkII is a 6U VME board with its own 68EC020 processor, serial ports and onboard firmware, and is designed to hold one piggyback module, just as the VBT-325. When used together with a VBT-325, both modules can be operated from the same terminal or PC by using the "transparent mode" between the two serial ports of the VBT-325.

COMBINE PIGGYBACKS FOR THE ULTIMATE TEST CAPABILITIES

As an example of an extremely powerful 2-slot solution, a VBT-325 with a TIMBAT-PB and a VPC-MkII with a VDRIVE will offer all the following features in parallel:

- **VME State analysis**
- **P2 State or Timing analysis**
- **200MHz VME Timing analysis**
- **VME Anomaly detection**
- **VMEbus Exerciser (Master/Slave)**

Anomaly Trigger

- Detect violations of the VMEbus protocol
- Reveal design errors in bus interface
- Find cause of board incompatibilities
- Trigger without knowing what to look for

Master-Slave-System Controller

- Patch or or inspect bus memory locations, registers etc.
- Test bus devices with all possible cycle types
- Generate and respond to interrupts
- Emulate planned but not yet available boards

Extended Trace Buffer

- Track events long before system crash
- Post-mortem analysis
- Data logging and documentation
- Software verification tasks

VBAT64-PB

TIMBAT-PB

VDRIVE-PB

XMEM325-PB

VPC-MkII

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SPECIFICATIONS

VBT-325C VMEbus & VSB/SCSI/P2 Analyzer

Trace Memory:	32K x 128 bits (VME part) 32K x 64 bits (P2 part) Trace depth expandable to 256K-512K-1M with XMEM325-PB piggyback module.
Input channels:	101 VME signals, 4 ext. inputs on mini-coax, 23 utility bits, plus 64 P2a/c signals, jumper selectable for VSB, SCSI or user-defined P2 bus, plus cross-trigger VME<->P2.
VMEbus signals:	A31-01, D31-00, DS1*, DS0*, AS*, LWORD*, DTACK*, BERR*, WRITE*, AM5-0, IRQ7-1*, IACK*, IACKIN, IACKOUT*, BBSY*, BR3-0*, BG3-0IN/OUT*, BCLR*, RETRY*, ACFAIL*, SYSFAIL*, SYSRES*, SYSCLK. (BG3-0IN/OUT* also clocked separately, encoded and stored as Bus Level. RMW and BLOCK w/ VME64 internally generated.)
VSB signals:	AD31-0, WR*, DS*, SPACE1-0, SIZE1-0, LOCK*, IRQ*, CACHE*, ASACK1-0*, ACK*, PAS*, ERR*, BREQ*, BUSY*, BGIN/OUT*. (BLOCK int. generated.)
SCSI signals:	Single-ended: DB7-0 (P2a15-8a), I/O* (P2a32), REQ*, (P2a31), RST* (P2a27), ACK* (P2a26), BSY* (P2a25), MSG* (P2a28), C/D* (P2a30), ATN* (P2a23). Differential and/or SCSI-2 Wide supported with P2 plug-on adapter.
User P2 signals:	All 64 signals on P2 rows a & c.
Async. Sampling:	50, 25, 6.25, 1.56, 0.78, 0.39, 0.2 or 0.1 MHz onboard asynchro nous clock, indep. selectable for VME and VSB/SCSI/P2. 200MHz optional with TIMBAT-PB.
Sync. Sampling:	Max 25MHz for VMEbus, VSB, SCSI and P2. Max. 50MHz with ext. supplied sampling clocks
VME sampling:	Bus Grants: Falling edge of BBSY*. Hold time: 1,5ns typ. (3ns max.). Setup time: <0ns All other signals: Non-SSBLT : Falling edge of DTACK* or BERR* conditioned with DS1* or DS0* low. SSBLT Read: Falling and rising edge of DTACK*. SSBLT Write: Addr: Falling edge of DTACK*, Data: Falling and rising edge of DS0*. Hold time: 10ns typ. (18ns max.) Setup time: <0ns
VSB sampling:	Bus Grant (Parallel arb.): Rising edge of AC. Address: Falling edge of ASACK1/0*. Data: Falling edge of ACK* or ERR*. Hold time: 10ns typ. (18ns max.) Setup time: <0ns
SCSI sampling:	Ident: Rising edge of BSY*. Data: Falling edge of ACK*. Hold time: 10ns typ. (18ns max.) Setup time: <0ns
P2 sampling:	Rising edge of user-supplied clock (on pin socket). Hold time: 10ns typ. (18ns max.) Setup time: <0ns
Trigger:	Four full-width word recognizers, separate for VME and P2 part, each with cross trigger signal, feeds Sequencer, see below. NOT operator on signal groups.
Trigger sensitivity:	20ns @ 50MHz.
Range:	Four A64/A32 address ranges, Four D32 data ranges on VME part. Four A/D32 ranges on P2 part.
Sequencer:	16 levels with If, Else, Elsif, Goto, Count, Delay, Trigger, Store, Sampling mode, Halt.
Trigger position:	0%, 25%, 50%, 75%, 100% of Trace
Occurrence counters:	Four 20-bits occurrence counters, separate for VME and P2 part, for use with Sequencer.
Delay counters:	Three 20-bits delay counters (40ns-0.33s), separate for VME and P2 part, for use with Sequencer.
Event counters:	Four 20-bit event counters, sepa rate for VME and P2 part, for use with Statistics.
VME Bus Level counters:	Four 20-bit VME Bus Level counters, for use with Statistics.
Total samples counter:	One 20-bit total samples counter, separate for VME and P2 part, for use with Statistics.
Time Tag:	Range: 40ns-1,5hrs. Resolution: 20ns (synchronized) Displayed as relative time between samples or absolute time from trigger point in each trace line, separate time tags for VME and P2 part.
Trigger Output:	TTL level trigger output with programmable polarity, level or pulse. May pulse on each stored sample. Available on mini-coax on front panel.
External Inputs:	Four TTL level inputs on mini-coax on front panel. One input may be used as input for ext. temp. probe.
Voltage sensors:	+5V: Range: 4.50-5.50V. Resolution: 10mV +/-12V: Range: +/-11.0-13.0V. Resolution: 10mV
Temperature sensor:	With external probe, 1m/3ft cable. Range: 0-80C (32-176F) Resolution: 1C
Processor:	MC68EC020 16,67 MHz RAM w/battery backup for setup storage. Flash EPROM with user interface SW. Time-of-Day clock, calendar.
Interfaces:	Two RS232C serial ports with DB9 female connectors. Baud rates: 1200-38400b/s. Automatically adjusted. Bits per character, parity mode, stop-bits selectable.
Power supply requirements :	+5VDC +/-5% from VME back plane or from ext. power supply via front panel inlet. Current consumption: Idle : 2,8A typ. Sampling: 3,7A typ. @ 6MHz, VME only. 4,8A typ. @ 50MHz, VME only. 5,4A typ. @ 50MHz, VME and P2. +/-12V from VME backplane. Current consumption: 10mA typ. (+12V/120mA max., when programming Flash EPROMs only).
Dimensions:	160x233,4mm (6U), One slot.
Compatibility:	VMEbus Rev.D 1992. VSB Rev.C 1986.
VBT-325B:	VMEbus Analyzer As VBT-325C, but without VSB/ SCSI/ P2 support.

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ORDERING INFORMATION

VBT-325B	High Performance VMEbus Analyzer.*
VBT-325C	High Performance VMEbus and P2 Analyzer.*

(Includes one 401-PC-232 PC cable and one 401-325-10BN1 trigger cable)*

Related Products

BV-325-PC	BusView for Windows Graphical User-Interface for Windows™ on PC.
VXE-35C	VXI Extender Board.

Piggyback Modules: See separate catalogue.

Accessories

401-TER-232	Terminal Cable.
401-TM-232	Transparent Mode Cable.
401-325-EPC	External Power Cable.
401-325-IOBN5	4xInput/Trigger Output BNC Coax Cable.
401-325-ETS-1	Environment Temperature Sensor.
401-325-ALL	VBT-325 Cable Package (All five entries above).
401-325-IOBN1	1xInput/Trigger Output BNC Coax Cable.
401-SCSI-VSC3	SCSI P2 Ext. Cable.
401-325-STA	VPC-MkII Trigger Cable.

WARRANTY

All VMETRO products have one year warranty.

Specifications subject to change without notice.
V2.2000

BusView is a trademark of VMETRO, Inc., USA.
Windows is a trademark of Microsoft Corp., USA.

Please refer to separate catalogue for details about the Piggyback Modules!

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