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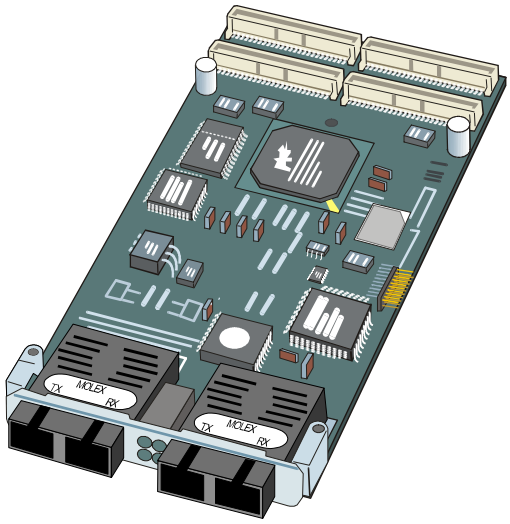
Find the *Curtiss-Wright / VMETRO VMFC-2230-CF* at our website: *Click HERE*

# User's Guide

# VMFC-2100/2230/2250

## Fibre Channel I/O Module

Rev. 1.3 - Valid for VMFC-2100 & VMFC-2230/50 PMC & PCI versions




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# Contents


**General Information** 6

This document ..... 6
Conventions used in this document ..... 6
Related Documents ..... 7

**Product Overview** 8

VMFC-2100/22x0 ..... 8
Block Diagram ..... 8
Key features VMFC-2100, VMFC-2230 and VMFC-2250 ..... 9
Protocol Engine ..... 9
OmniPort integrated hub Interconnection ..... 9
PCI interface ..... 12

**Installation** 13

Board Precautions ..... 13
Unpacking ..... 13
Installation of PMC VMFC-2100/22x0 Module ..... 13
Assembly Procedure ..... 14
Configuration Switch & Jumpers ..... 15

**Front Panel Indicators** 16

**Fibre Channel cable connection** 16

**Front Panels** 18

Board Layouts ..... 19

**VMFC-2100/22x0 Specifications** 21

**Appendix I: Laser Safety** 23

Laser Safety Information and laser specifications ..... 23

**Appendix II: Fibre Channel cables available from VMETRO** 25

**Appendix III: Copper connector information** 27

**Appendix IV: ISP2100A Data Sheet** 29

**Appendix V: ISP2200 Data Sheet** 31

**Appendix VI:** 33

List of Tables ..... 33
List of Figures ..... 33





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# General Information

## This document

This document has been prepared to help the customer get started with the VMFC-2100 or VMFC-22x0 Fibre Channel module. The following models are covered by this document:

| | |
|---|---|
| VMFC-2100/22x0-DC: | Fibre Channel PMC module with a dual copper HSSDC interface and integrated hub. |
| VMFC-2100/22x0-CF: | Fibre Channel PMC module with single fiber-optic and single HSSDC copper interface and integrated hub. |
| VMFC-2100/22x0-DF: | Fibre Channel PMC module with dual fiber-optic interface and integrated hub. |
| . | |
| VMFC-2100P/22x0P-xx: | Fibre Channel PCI module for PC installation. |

## Conventions used in this document

The following section describes conventions used in this document.

| *Symbols* | *Meaning:* |
|---|---|
|   | The STOP symbol indicates a section of critical importance. Overlooking this information may cause damage to the VMFC-xx00 and/or other equipment. |
|  | Indicates important, but not crucial, information. Still, you should take notice if you want to use all capabilities built into your VMFC-xx00. |



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## Related Documents

This document does not include detailed information about the following:

- Fibre Channel Standard
- PCI Local Bus Specification V2.2

Since this document is only written as a guide to the installation and operation of the VMFC-xx00, there are only small references to the above specifications. If more information is required, refer to the following:

| Producer | Document |
|---|---|
| VMETRO | - FC-AL SCSI Driver Reference Guide<br>Contact VMETRO for more information |
| PCI Special Interest Group | - PCI Local Bus Specification Revision 2.2<br>Available from http://www.pcisig.com/ |
| Fibre Channel Association | - Information on Fibre Channel standards<br>- FC information book: Connection to the Future<br>Available from http://www.fibrechannel.com |



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# Product Overview

## VMFC-2100/22x0

The VMFC-2100/22x0 is a Fibre Channel PMC module specifically designed to maximize throughput while minimizing transfer latency and host processor overhead in embedded real-time applications. In addition to mainstream Fibre Channel applications such as disk storage, this interface is particularly well suited to applications where low latency communications and high-sustained throughput are essential. This includes areas such as multi-processor communications (telecom & radar signal processor), sensor I/O (radar, sonar & image processing), and ultra-high performance computer networks (digital broadcasting & subsystems data links).

## Block Diagram

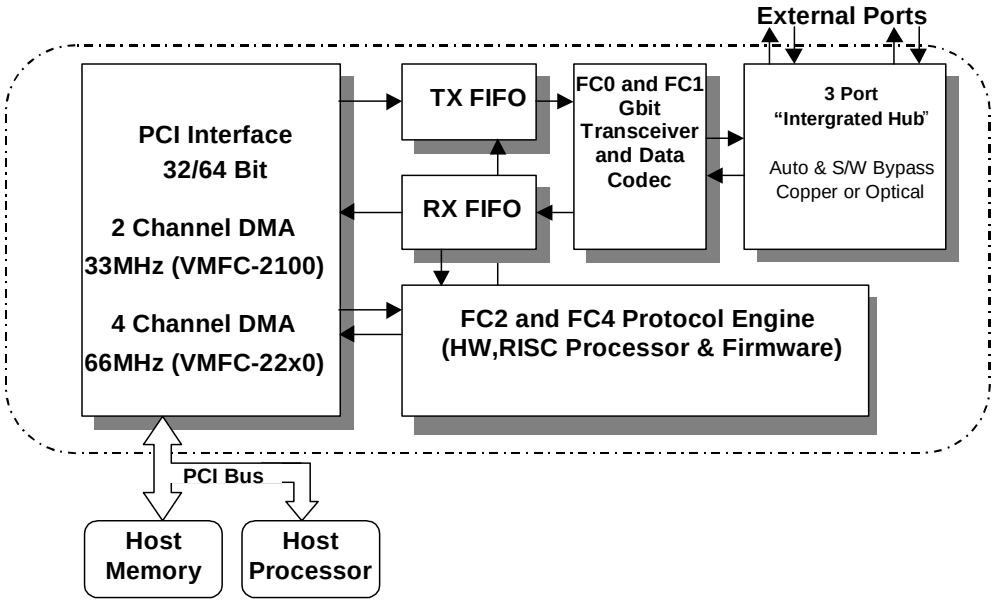



*Figure 1: VMFC-2100/22x0 Block Diagram*



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## Key features VMFC-2100, VMFC-2230 and VMFC-2250

| **VMFC-2230, VMFC-2250** | **VMFC-2100** |
|---|---|
| QLOGIC ISP-2200 RISC Processor | QLOGIC ISP-2100 RISC Processor |
| 200 MB/s Full duplex (2 x 100 MB/s) | 100 MB/s Half duplex (1 x 100 MB/s) |
| 64bit 66Mhz PCI | 64bit 33MHZ PCI |
| Improved Remote DMA | |
| Latency reduced by 30 to 50% | |
| Broadcast (2250 only) | |
| Public loop and direct fabric logon | |
| VMFC-2100 direct replacement | |
| External receive FIFO (2250 only) | |

## Protocol Engine

The Protocol Engine incorporated into the VMFC-2100/22x0 consists of the QLogic ISP-2x00 with associated application firmware. The QLogic ISP-2x00 is the highest performance single chip Fibre Channel controller, making use of an integrated RISC processor to reduce host processor utilization by offloading the Fibre Channel protocol processing. The firmware is downloaded by the host processor at start-up, and can be changed to provide field upgrades and to support field upgrades.

## OmniPort integrated hub Interconnection

The integrated hub capabilities of the Patent pending OmniPort Fibre Channel I/O port allows for simple cascading of multiple Fibre Channel devices. Standard duplex HSSDC copper and SC Duplex fiber optic cabling is supported. Three modes of operation include integrated hub, redundant point to point and redundant arbitrated loop (JBOD connection).

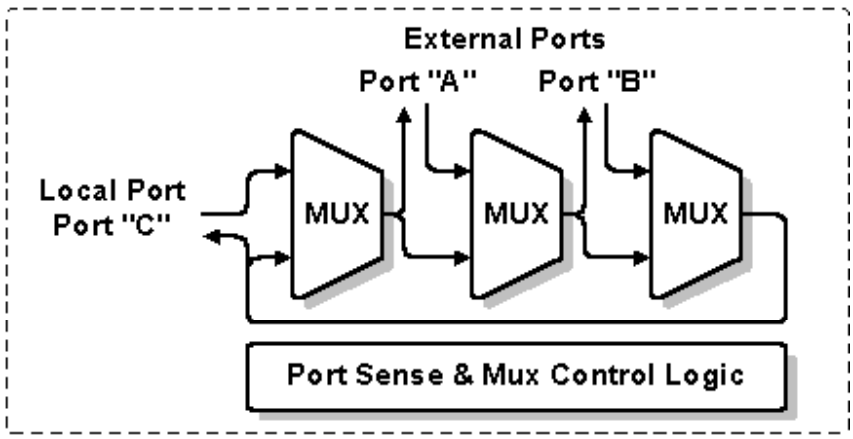


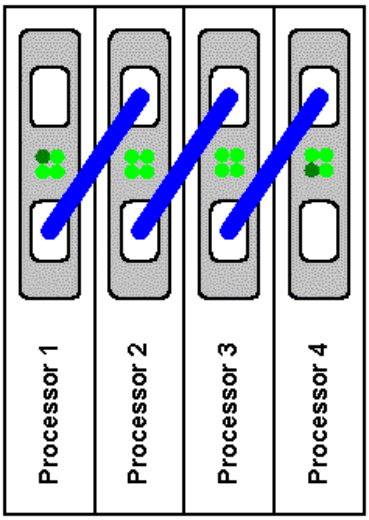

*Figure 2: Intergrated Hub block diagram*



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## Mode 1: Integrated Hub

The OmniPort automatically extends the loop as more devices are added. It does not matter which of the two ports are used.



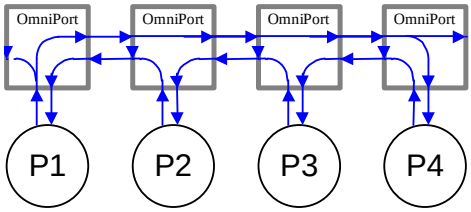




*Figure 3: Integrated Hub functional diagram*

*Figure 4: Integrated Hub connection.*

## Interprocessor and Shared Disk - Automatic Hub

The OmniPort automatically extends the loop as more devices are added. It does not matter which of the two ports are used.

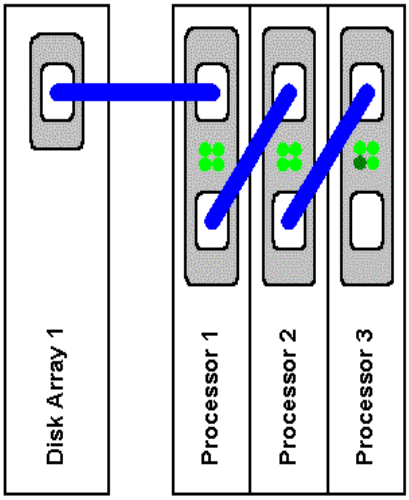



*Figure 5: Automatic Hub connection*

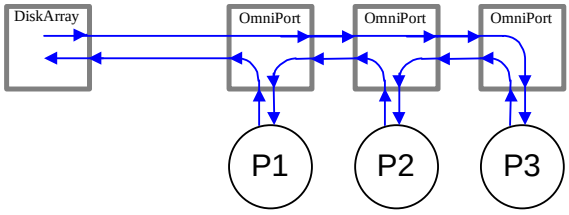



*Figure 6: Integrated Hub functional diagram*



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## Single Failure Redundant Hub

This mode significantly increases the reliability of the loop. Any single failure will still allow the loop to operate normally. The ports must be connected from port 1 to port 2 of the next device as shown in Fig. 4.

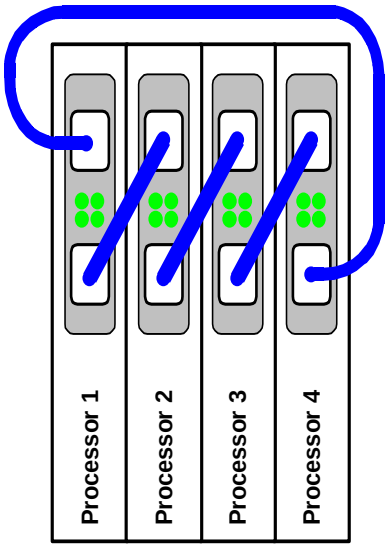



*Figure 7: Redundant Hub*

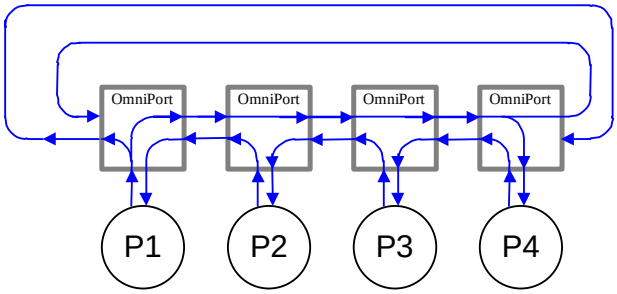



*Figure 8: Redundant Hub Functional diagram*

## Mode 2: Redundant Point to Point Connection

The OmniPort supports a redundant channel mode where two host adapters can be redundantly connected. The OmniPort always stays on port 1 unless the loop on port 1 has failed, in which case it will switch to port 2. It will switch back to port 1 as soon as the loop on port 1 is operational. The redundant (standby loop) is looped back to the disk array. TX data is present on both ports.

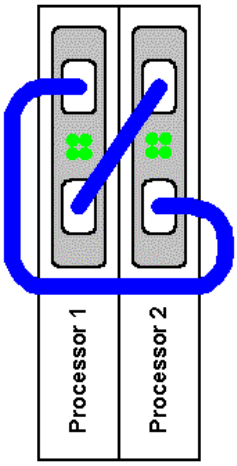



*Figure 9: Redundant point to point connection*

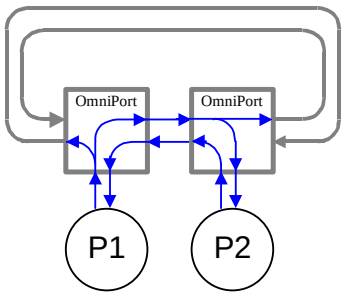


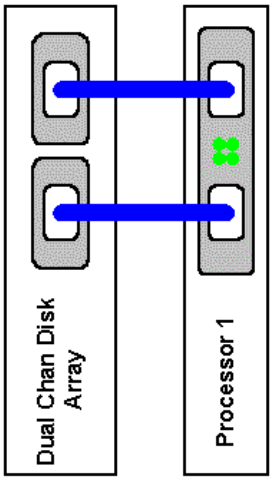

*Figure 10: Redundant point to point functional diagram*



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### *Mode 3:Redundant Arbitrated Loop (JBOD connection)*

When connected to a redundant Disk array, the OmniPort automatically switches to the redundant loop when the current loop fails. The redundant (standby loop) is looped back to the disk array. The OmniPort will park on the last known good loop and only switch upon failure detection.



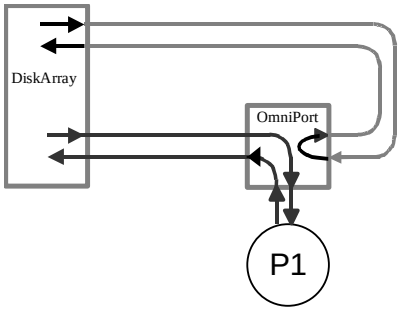




*Figure 11: Redundant Arbitrated Loop functional diagram*

*Figure 12: Redundant Arbitrated Loop connection*

## PCI interface

The VMFC-2100/22x0 is designed to interface directly to a PCI local bus and operate as a 32 or 64-bit DMA master, which is backward compatible to 32-bit operation. The PCI host bus interface is compliant with PCI Local Bus Specification revision 2.1. Further information can be found in the PCI Local Bus Specification Rev 2.2 and in Appendix IV: ISP2100A Data Sheet or Appendix V: ISP2200 Data Sheet .



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# Installation

## Board Precautions




- The VMFC-2100/22x0 circuit board is sensitive to static electricity and can be damaged by a static discharge. Always wear a grounded anti-static wrist strap and use grounded, static protected work surfaces when touching the circuit board and its components.

- When the board is not installed, always keep in the static-protective envelope.

## Unpacking

All precautions described above must be taken when unpacking the VMFC-2100 /22x0 from its shipping container. Verify that no damage has occurred in the shipment. Refer to packing list and verify that all items are present.

## Installation of PMC VMFC-2100/22x0 Module

This procedure explains how to mount the VMFC-2100/22x0 on to a VMETRO PowerMIDAS (not ruggedized version). Although mounting is to a MIDAS card, the procedure is quite generic and could be helpful when mounting to other PMC carriers.




Note:

- Be extremely careful when inserting screws to secure PMC modules. Touching component leads or the printed circuit board itself, with a screwdriver may cause permanent damage to the board.

- Do not install the VMFC-2100/22x0 while power is applied



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# Assembly Procedure

## PMC version

The MIDAS and other PMC carrier boards are usually shipped with two PMC filler panels mounted in the front panel. They act as EMC shielding in unused PMC positions. Before installing a PMC module, the filler panel(s) must be removed. This is done by pushing them out from the backside of the front panel.

Four screws must be used to secure each PMC on the PMC carrier board.

The VMFC-2100/22x0 comes with two pre-installed 10 x 2.5mm spacers for mounting onto the PMC carrier PCB. If they have been removed, replace them before continuing the installation.

**STEP#1:** **Mount VMFC-2100/22x0 module(s) on the PMC carrier board.**

**See** Figure 13

- Place the PMC carrier board on a smooth static protected work surface.
- Install VMFC-2100/22x0 module #1 in a vacant position on the PMC carrier board by first aligning the front-panel into the PMC carrier front-panel slot and then firmly seating the back of the VMFC-2100/22x0 into the PMC carrier connectors.
- Install VMFC-2100/22x0 module #2 in the other vacant PMC carrier position as described above (if required)
- Double check to ensure that all PMC connectors is well mated.

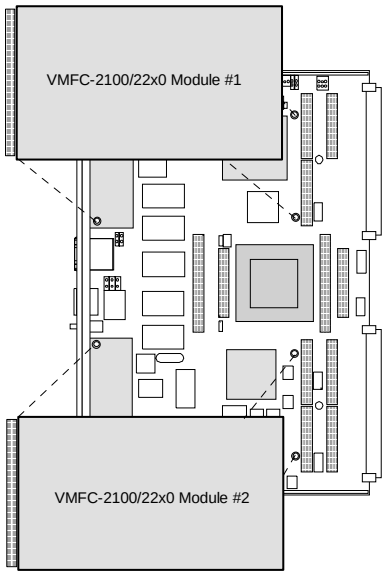



*Figure 13: Steps 1: Mount VMFC-2100/22x0 module(s) on the PowerMIDAS PMC carrier board.*



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**STEP#2: Mount and fasten screws to the back of the PMC carrier board.**

- Secure PMC modules with screws on the bottom side of the PMC carrier board.
- The VMFC-2100/22x0 is now ready for operation.

### PCI version

The PCI version of the VMFC-2100/22x0 requires a standard personal computer PCI slot. For Windows NT driver installation instructions, refer to other documentation accompanying this product.

# Configuration Switch & Jumpers

There are no user adjustable switches or jumpers on the VMFC-2100/22x0.



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# Front Panel Indicators

There are four LED indicators on the front panel of the Host Adapter assigned as follows:

**AUT** – The OmniPort is configured for automatic operation. (Default)

**LCL** – The Host Adapter Fibre Channel controller is active.

**P1** – Valid Fibre Channel signaling is detected on external port 1.

**P2** – Valid Fibre Channel signaling is detected on external port 2.

# Fibre Channel cable connection

## *VMFC-2100-DF*

The simplest connection possible with the VMFC-2100/22x0 is the point to point connection. For this type of connection 2, VMFC-2100/22x0's can be connected or a VMFC-2100/22x0 can be used in conjunction with another Fibre channel device to form a point to point communications link.

Molex recommends that the minimum Fibre Channel optical-fiber cable length is 2 meters. Cable lengths shorter than this can saturate the optical receiver under some circumstances.

### *Single point to point connection.*

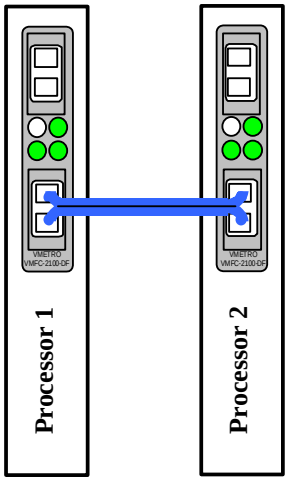



*Figure 14: Single point to point connection*



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## *Multi node loop connection*

When using VMFC-2100/22x0-DF in a loop topology, the standard dual Fibre channel cable must have its connectors separated in-order to allow connection between the nodes. As most Fibre Channel optical-cables come as a receiver/transmitter pair, the separation must be done manually. The procedure for separation of the dual “SC” connector varies from manufacture to manufacture and is therefore not covered in detail in this manual.

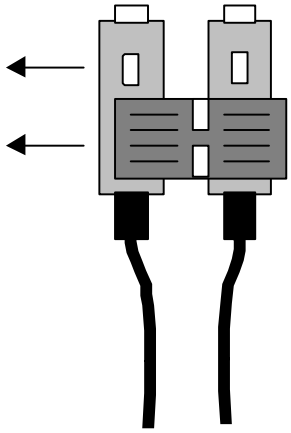


*Figure 15: Separating Fibre Channel SC cables from retainer*

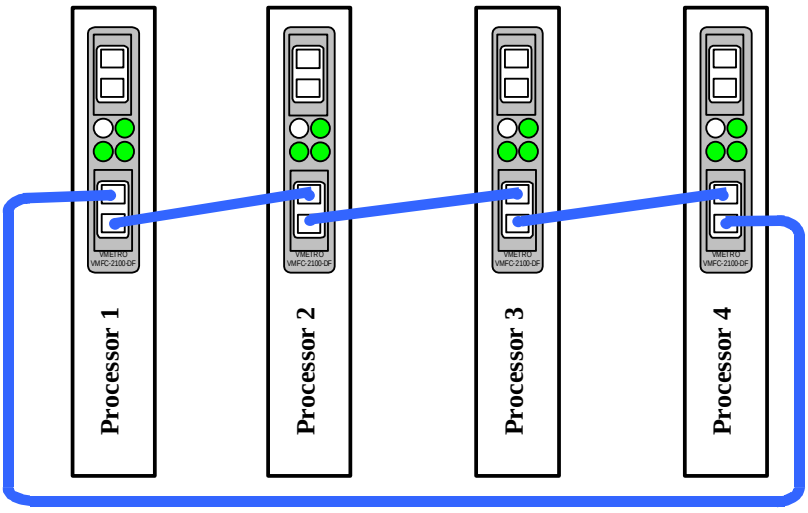



*Figure 16: Multi node loop connection using the VMFC-2100-F*



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# Front Panels

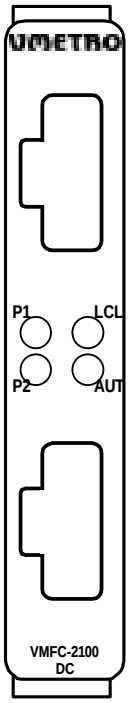



*Figure 17: PMC & PCI Dual Copper*

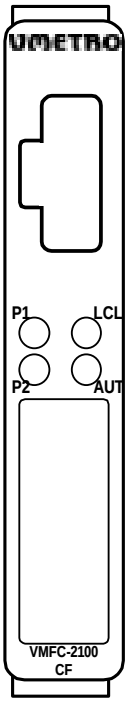



*Figure 18: PMC & PCI Combo*

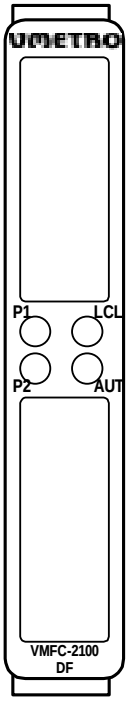
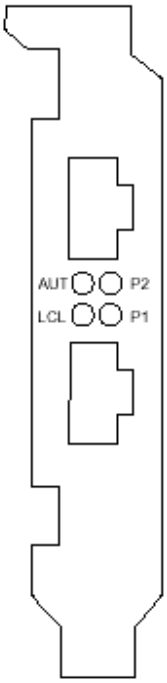
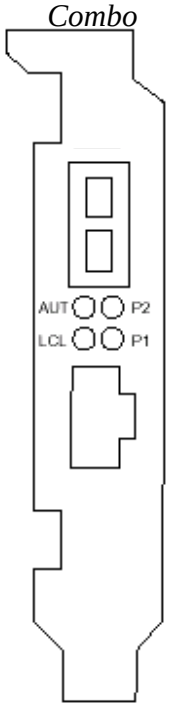
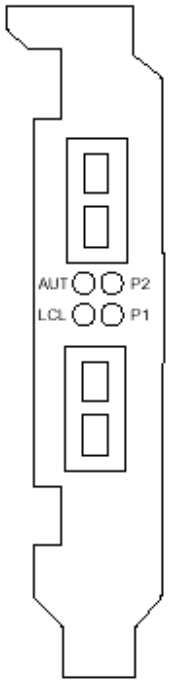



*Figure 19: PMC & PCI Dual Fiber*






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# Board Layouts

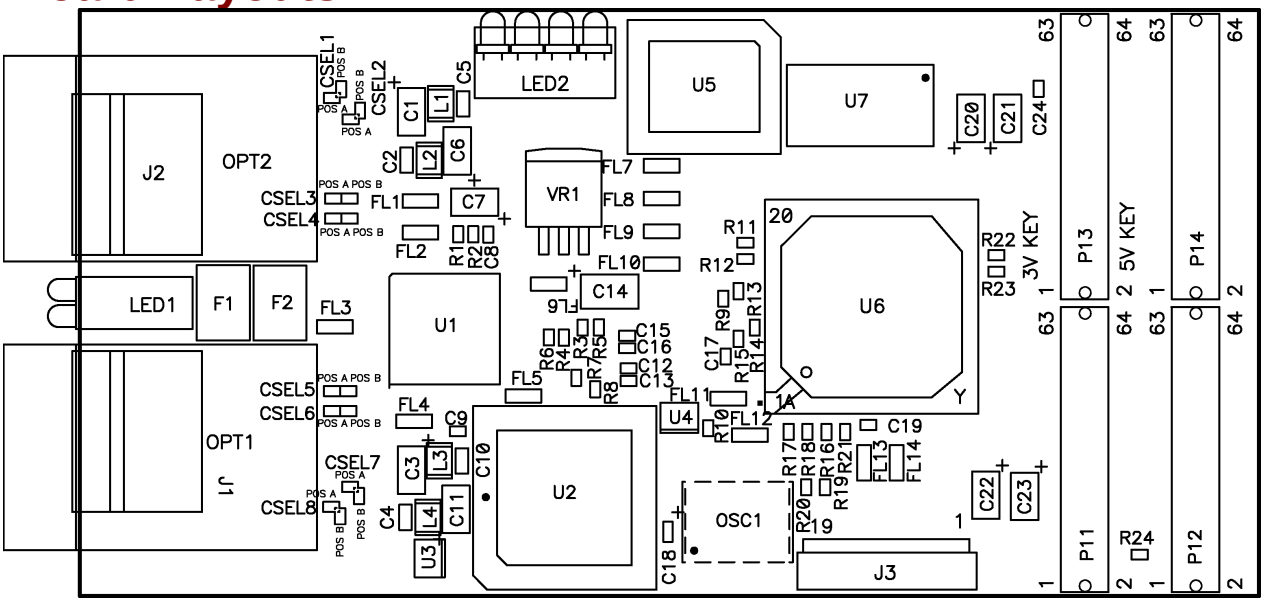



*Figure 20: VMFC-2100 PMC Board layout*

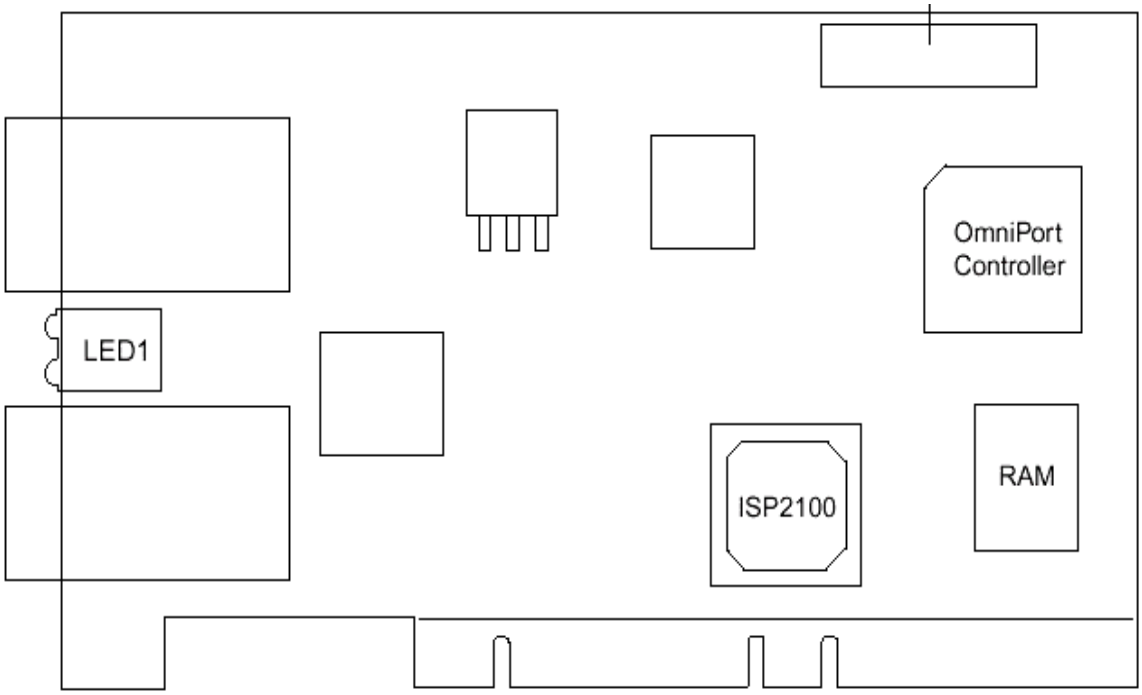



*Figure 21: VMFC-2100 PCI Board layout*



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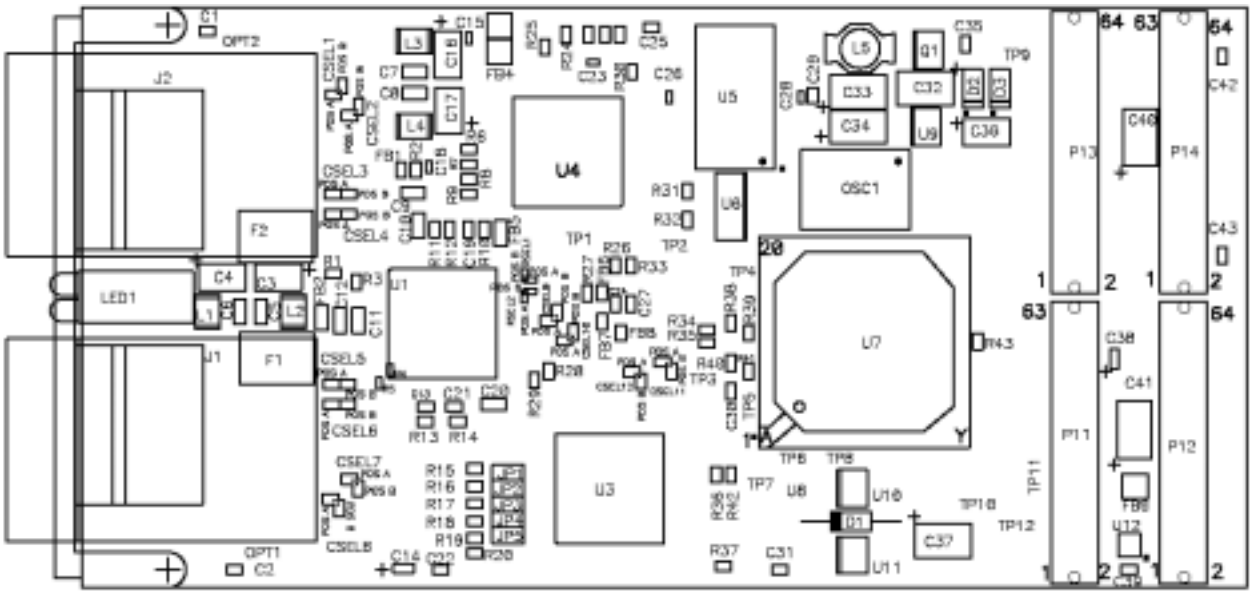



*Figure 22: VMFC-2250 PMC Board layout*



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# VMFC-2100/22x0 Specifications

| | |
|---|---|
| Fibre Channel | FC-AL-2 rev 6.4 |
| | FC-PH |
| | SCSI_FCP |
| | FC-FLA rev 2.7 |
| | FC-PLDA rev 2.1 |
| | FC-TAPE rev 1.13 |
| PMC, PMC Host Bus | PCI Local Bus revision 2.2 |
| | PMC IEEE P1386.1 (PMC version only) |
| | CMC IEEE P1386 (PMC version only) |
| Operating Temperature | 0 to 50 C (Forced air cooling, exit air temp.)<br>Extended temperature versions also available |
| Storage Temperature | -40 to +70 °C |
| Operating Humidity | 5% to 95% non-condensing |
| Storage Humidity | 5% to 95% non-condensing |
| Power | +5 Vdc @ 1.3 amps max Dual Copper |
| | +5 Vdc @ 1.2 amps max Single Copper |
| | +5 Vdc @ 1.5 amps max Single Fiber |
| | +5 Vdc @ 1.7 amps max Dual Fiber |
| Weight | 100gm (Dual Copper PMC) |

*Table 1: Specifications*

*VMETRO reserves the right, without notice, to make changes in product design and specifications.*



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# Appendix I: Laser Safety

## Laser Safety Information and laser specifications

**Operation and Maintenance Operation and Maintenance**

This optoelectronic transceiver is a Class 1 Laser Product, which complies with 21 CFR 1040.10 and 1040.11 and with IEC825-1. This product is to be used only under the conditions described in this document. No maintenance or service of the product may be performed. To avoid possible exposure to hazardous laser radiation, do not open or alter the sealed housing of the product.

### *Radiation Specifications*

The specifications of this optoelectronic transceiver are shown in Table 2

| | |
|---|---|
| Wavelength | 770 nm to 810 nm |
| Maximum radiant power (CDRH) | 12.5 μW |
| Radiant power (IEC) | < 300 μW |
| Beam divergence | (9 ± 1)° (FWHM)<br>(15 ± 1)° (FWHM) |
| Pulse duration (DC-coupled) | DC - 670 ps |
| Pulse duration (AC-coupled) | 10 ns - 670 ps |

*Table 2: Radiation Specifications*

This optoelectronic transceiver contains a Class IIIb diode laser, which emits invisible laser radiation in the range 770 nm to 810 nm. Light from the diode laser is attenuated so the optoelectronic transceiver conforms to Class I standards. To avoid possible exposure to hazardous laser radiation, do not open the sealed housing of the product. The specifications of the diode laser are shown in Table 3.

| | |
|---|---|
| Wavelength | 770 nm to 810 nm |
| Total radiant power | 3 mW |
| Beam divergence | (11 ± 4)° (FWHM)<br>(37 ± 9)° (FWHM) |
| Pulse duration (DC-coupled) | DC - 670 ps |
| Pulse duration (AC-coupled) | 10 ns - 670 ps |

*Table 3: Laser diode specifications*



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## Radiation apertures

Invisible laser radiation is emitted from the locations shown in Figure 23.

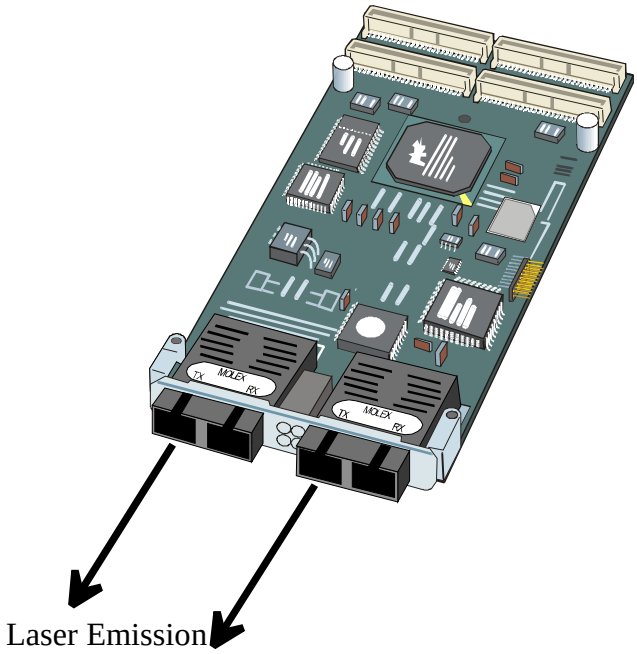



*Figure 23: Laser apertures*

## Control and Adjustments

This opto-electronic transceiver contains no controls that can be adjusted by the user. No maintenance or service of the product may be performed by the user.

Caution: Use of controls, adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

## Caution statement

Caution: The use of optical instruments with this product will increase eye hazard.



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# Appendix II: Fibre Channel cables available from VMETRO

As standard, VMFC-2100/22x0 is shipped from VMETRO without cables. The following cables can be ordered directly from VMETRO.

| Part Number: | Part description: |
|---|---|
| FCC-HH-005 | 0.5 meter Fibre Channel HSSDC Copper Cable |
| FCC-HH-03 | 3 meter Fibre Channel HSSDC Copper Cable |
| FCC-HH-05 | 5 meter Fibre Channel HSSDC Copper Cable |
| FCC-HH-10 | 10 meter Fibre Channel HSSDC Copper Cable |
| FCC-HH-20 | 20 meter Fibre Channel HSSDC Copper Cable |
| FCC-HH-20 | 20 meter Fibre Channel HSSDC Copper Cable |
| | |
| FCC-HD-03 | 3 meter Fibre Channel HSSDC to DB9 Plug, Copper Cable |
| FCC-HD-05 | 5 meter Fibre Channel HSSDC to DB9 Plug, Copper Cable |
| FCC-HD-10 | 10 meter Fibre Channel HSSDC to DB9 Plug, Copper Cable |
| FCC-HD-20 | 20 meter Fibre Channel HSSDC to DB9 Plug, Copper Cable |
| | |
| FCC-FF-01 | 1 meter Fibre Channel Fiber Optic Cable, Dual SC to Dual SC |
| FCC-FF-03 | 3 meter Fibre Channel Fiber Optic Cable, Dual SC to Dual SC |
| FCC-FF-05 | 5 meter Fibre Channel Fiber Optic Cable, Dual SC to Dual SC |
| FCC-FF-10 | 10 meter Fibre Channel Fiber Optic Cable, Dual SC to Dual SC |
| FCC-FF-20 | 20 meter Fibre Channel Fiber Optic Cable, Dual SC to Dual SC |
| | |
| FCC-DD-03 | 3 meter Fibre Channel DB9 Plug to DB9 Plug, Copper Cable |
| FCC-DD-05 | 5 meter Fibre Channel DB9 Plug to DB9 Plug, Copper Cable |
| FCC-DD-10 | 10 meter Fibre Channel DB9 Plug to DB9 Plug, Copper Cable |
| FCC-DD-20 | 20 meter Fibre Channel DB9 Plug to DB9 Plug, Copper Cable |
| | |
| FCC-HAD-005 | 0.5 meter 8pin HSSDA to DB9 Receptacle Adapter |

*Table 4: Fibre Channel Cables available from VMETRO*

For other cable lengths contact VMETRO.



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# Appendix III: Copper connector information

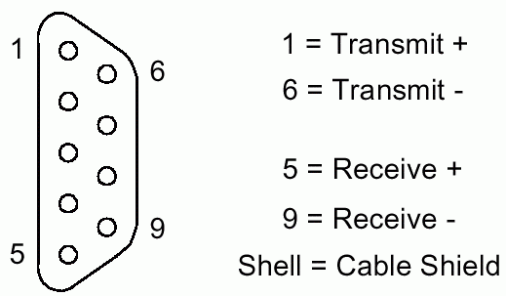



*Figure 24: DB9 Style Fibrechannel connector wiring.*

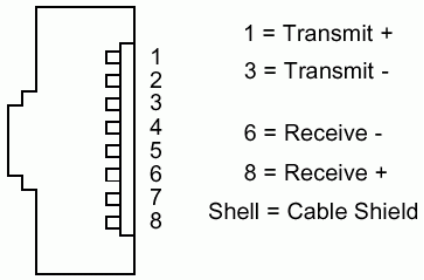



*Figure 25: HSSDC style Fibrechannel connector wiring.*

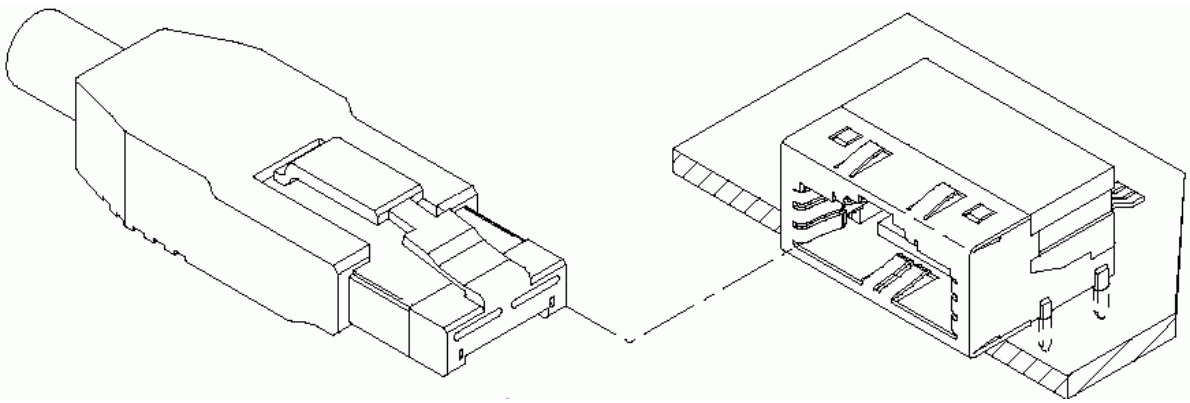


*Figure 26: HSSDC connector.*



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# Appendix IV: ISP2100A Data Sheet



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QLogic Corporation

# ISP2100A Intelligent Fibre Channel Processors

## Data Sheet

## Features

- Available in two versions:
  - 66-MHz, 64-bit PCI host bus interface
  - 33-MHz, 64-bit PCI host bus interface
- Compliance with *PCI Local Bus Specification* revision 2.1
- Compliance with ANSI SCSI standard X3.131-1994
- Supports all Fibre Channel topologies and classes of service
- Compliance with *Fibre Channel Arbitrated Loop (FC-AL) Direct Disk Attach Profile* and *Fibre Channel Public Loop (FC-PL) Fabric Loop Attach Profile*, class 2 and class 3 service
- Compliance with *PCI Bus Power Management Interface Specification* Revision 1.0 (PC97)
- Supports 100 Mbytes/sec sustained Fibre Channel data transfer rate
- Initiator or target mode
- Onboard RISC processor to execute operations at the I/O control-block (IOCB) level from the host memory
- Onboard gigabit serial transceivers
- Supports external transceivers with a 10-bit interface
- Supports PCI dual-address cycle (64-bit addressing) and cache commands
- No host intervention required to execute SCSI operations from start to finish
- Simultaneous, multiple logical threads
- Full duplex frame buffer architecture
- Supports JTAG boundary scan

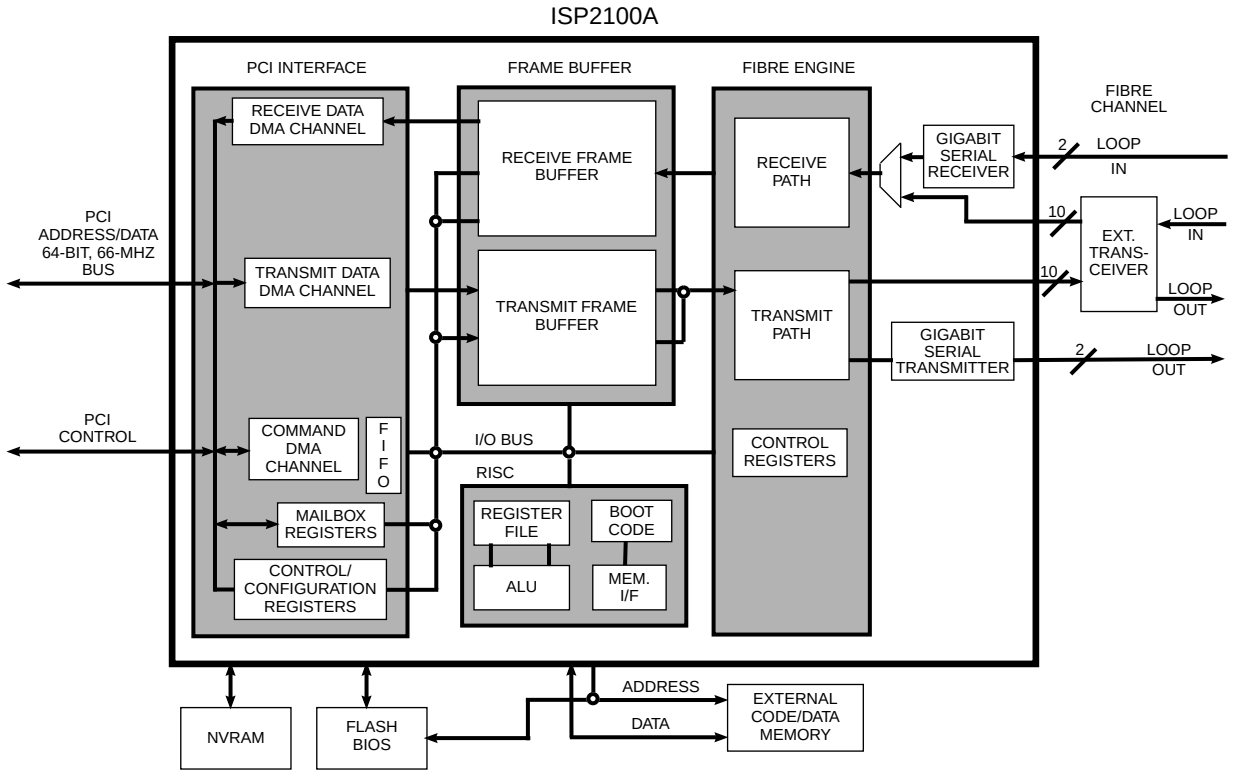



***Figure 1. ISP2100A Block Diagram***



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# Product Description

The ISP2100A is a single-chip, highly integrated, bus master, FC-AL processor that targets SCSI applications. This chip connects the PCI bus to a Fibre Channel loop and contains an onboard RISC processor. The ISP2100A is pin compatible with the ISP2100. Like the ISP2100, the ISP2100A is a fully autonomous device, capable of managing multiple I/O operations and associated data transfers from start to finish without host intervention.

The ISP2100A provides power management support in accordance with the *PCI Bus Power Management Interface Specification*. The ISP2100A block diagram is illustrated in figure 1.

## ISP Initiator and Target Firmware

The ISP2100A firmware implements a multitasking host adapter that provides the host system with complete SCSI command and data transport capabilities, thus freeing the host system from the demands of the SCSI Fibre Channel protocol (FCP). The firmware provides two interfaces to the host system: the command interface and the Fibre Channel transport interface. The single-threaded command interface facilitates debugging, configuration, and recovering errors. The multithreaded transport interface maximizes use of the Fibre Channel and host buses.

The ISP2100A can switch between initiator and target modes.

## Software Drivers

The ISP2100A supports a host software interface similar to the ISP1020/1040 family. Existing 1020/1040 software drivers are easily modified to support the ISP2100A.

BIOS firmware is available for the ISP2100A. Software drivers are available for the following operating systems:

- AIX
- $I_2O$
- DOS/Windows
- Novell NetWare
- OS/2
- SCO UNIX
- UnixWare
- Windows 95; x86 and Alpha systems
- Windows NT; x86 and Alpha systems
- Solaris; x86 and SPARC systems

# Subsystem Organization

To maximize I/O throughput and improve host and loop utilization, the ISP2100A incorporates a high-speed, proprietary RISC processor; a Fibre Channel protocol manager (FPM); integrated frame buffer memory; and a host bus, three-channel, bus master DMA controller. The FPM and host bus DMA controller operate independently and concurrently under the control of the onboard RISC processor for maximum system performance.

The complete I/O subsystem solution using the ISP2100A and associated supporting memory devices is shown in figure 2.

# Interfaces

The ISP2100A interfaces consist of the FC-AL interface, PCI bus interface, RISC interface, flash BIOS interface, and NVRAM control. Pins that support these interfaces and other chip operations are shown in figure 3.

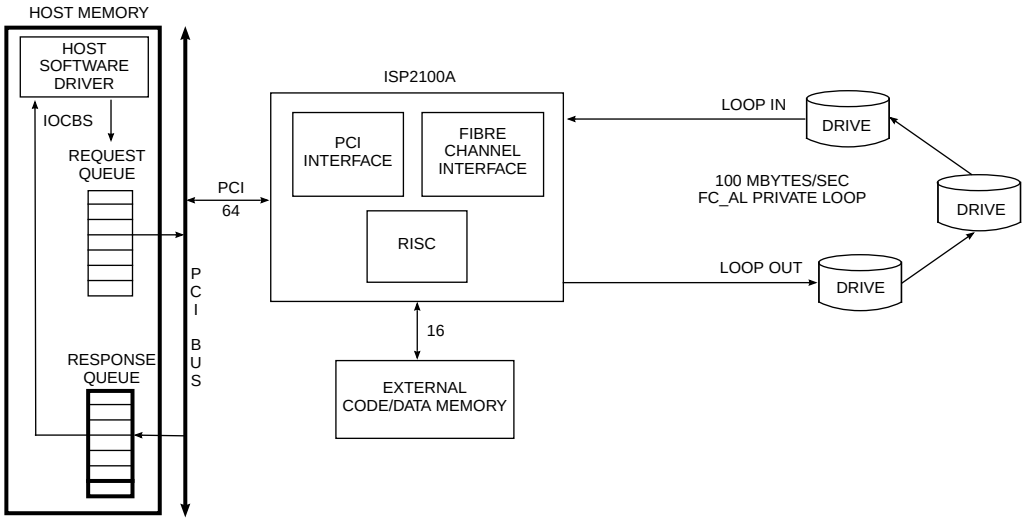



***Figure 2. I/O Subsystem Design Using the ISP2100A***



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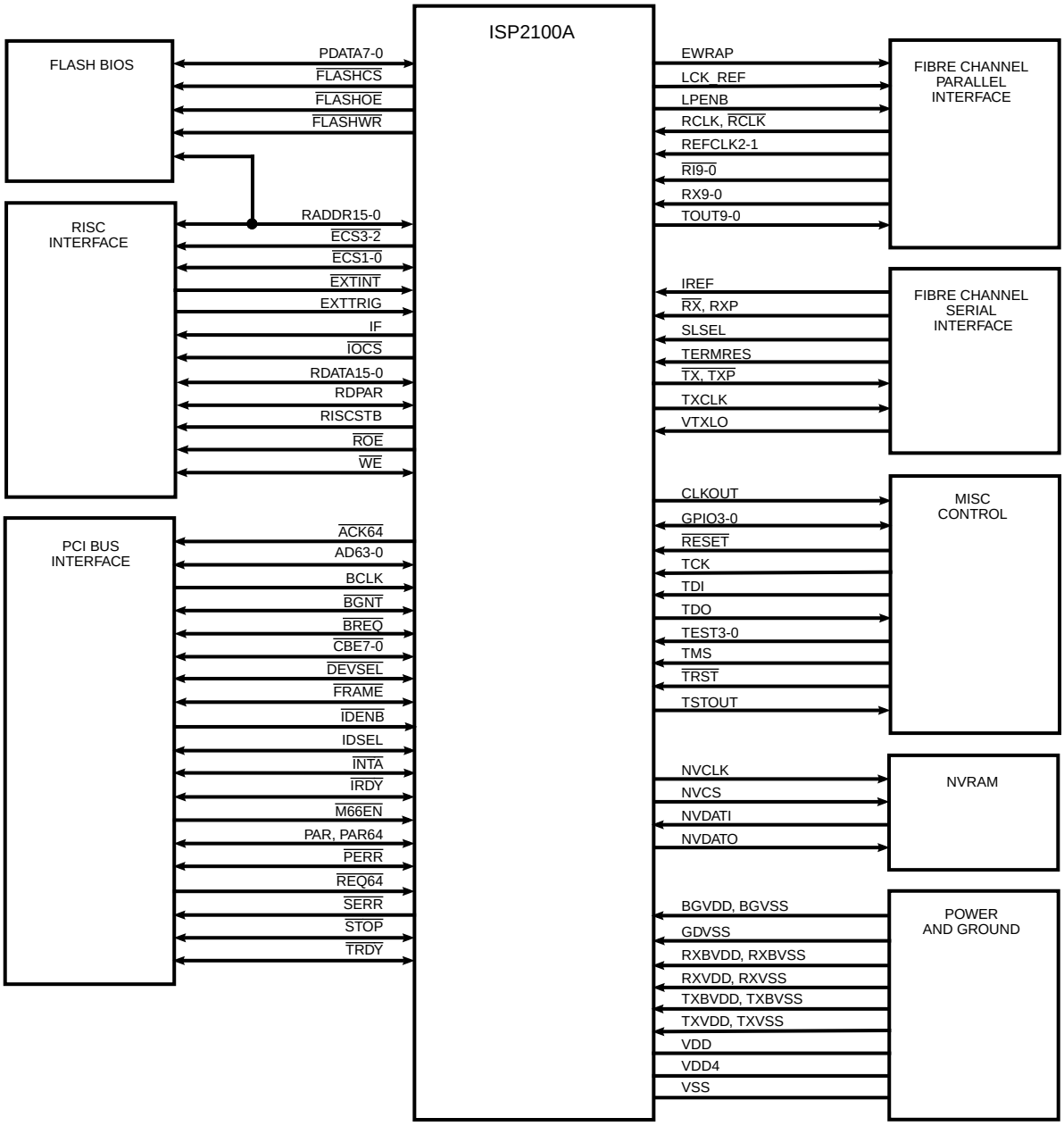



***Figure 3. ISP2100A Functional Signal Grouping***

## Fibre Channel Interface

The ISP2100A provides on-board gigabit transceivers for direct connection to the Fibre Channel loop on copper media. A standard 10-bit interface is also provided to connect to external transceivers, if desired.

## Fibre Channel Protocol Manager

The ISP2100A FPM supports the following:

- Support for one Fibre Channel loop
- 100 Mbytes/sec sustained data transfer rate
- 10-bit interface to external transceivers
- Gigabit serial interface
- Integrated frame buffer that supports up to 2-KB frame payload

The FPM includes an 8B/10B encoder and decoder, an elasticity buffer for clock skew management, and an FC-AL state machine. The FPM transmits and receives at the full Fibre Channel rate of 106.25 Mbytes/sec. The on-chip frame buffer includes separate areas for received data and transmit data, as well as areas for managing special frames such as command and response. The FPM receive



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path validates and routes frames received from the Fibre Channel to the appropriate area in the frame buffer. The transmit path transmits frames from the frame buffer to the Fibre Channel. The FPM automatically handles frame delimiters and frame control.

## PCI Interface

The ISP2100A PCI interface supports the following:

- 33-MHz or 66-MHz, 64-bit, intelligent bus master interface for fetching IOCBs and data transfers
- 64-bit host memory addressing (dual address cycle)
- Backward compatible to 32-bit PCI
- Three-channel DMA controller
- 16-bit slave mode for communication with host
- Pipelined DMA registers for efficient scatter/gather operations
- 32-bit DMA transfer counter for I/O transfer length of up to four gigabytes
- Support for PCI cache commands
- Support for flash BIOS PROM
- Support for subsystem ID
- 3.3V and 5.0V tolerant PCI I/O buffers

The ISP2100A is designed to interface directly to the PCI bus and operate as a 64-bit, DMA bus master, which is backward compatible to 32-bit operation. This function is accomplished through a PCI bus interface unit (PBIU) containing an onboard DMA controller. The PBIU generates and samples PCI control signals, generates host memory addresses, and facilitates the transfer of data between host memory and the onboard frame buffer. It also allows the host to access the ISP2100A internal registers and communicate with the onboard RISC processor.

The ISP2100A supports the minimum power management capabilities specified in revision 1.0 of the *PCI Bus Power Management Interface Specification*, which defines power states D0-D3, where D0 provides maximum power consumption and D3 provides minimal power consumption. The D1 and D2 power states provide intermediate power consumption. The D3 power state is entered by either software (D3 *hot*) or by physically removing power (D3 *cold*). Hot and cold refer to the presence or absence of VCC, respectively.

The ISP2100A supports power states D0, D3 hot, and D3 cold.

The ISP2100A onboard DMA controller consists of three independent DMA channels that initiate transactions on the PCI bus and transfer data between the host memory and frame buffer. The command DMA channel is used mainly by the RISC processor for small transfers, such as fetching commands from and writing status information to the host memory over the PCI bus. The two data DMA channels, one for transmit and one for receive, transfer data between the FC-AL and the PCI bus, allowing for fast context switching.

The PBIU internally arbitrates between the two data DMA channels and the command DMA channel and alternately services them. Each DMA channel has a set of DMA registers that are programmed for transfers by the RISC processor.

## RISC Processor

The ISP2100A RISC processor supports the following:

- Execution of multiple I/O control blocks from the host memory
- Reduced host intervention and interrupt overhead
- One interrupt or less per I/O operation

One of the major features of the ISP2100A is its ability to handle complete I/O transactions from start to finish with no intervention from the host. This high level of integration is accomplished with an onboard RISC processor. The ISP2100A RISC processor controls the chip interfaces; executes simultaneous, multiple IOCBs; and maintains the required thread information for each transfer.

# Packaging

The ISP2100A is available in a 256-pin ball grid array (BGA) package.

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Alpha is a trademark of Digital Equipment Corporation.
DOS, OS/2, Windows NT, and Windows 95 are trademarks or registered trademarks of Microsoft Corp.
Novell and NetWare are registered trademarks of Novell, Inc.
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# Appendix V: ISP2200 Data Sheet



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QLogic Corporation

# ISP2200A/33 and ISP2200A/66 Intelligent Fibre Channel Processors

## Data Sheet

## Features

- Available in two speed grades (collectively referred to as *ISP2200A*):
  - 66-MHz, 64-bit PCI host bus interface (ISP2200A/66)
  - 33-MHz, 64-bit PCI host bus interface (ISP2200A/33)
- Compliance with *PCI Local Bus Specification* revision 2.2
- Supports full-duplex communications in all Fibre Channel topologies
- Compliance with ANSI SCSI standards for class 2 and class 3 service:
  - *Fibre Channel Arbitrated Loop (FC-AL-2*) working draft, rev 6.4, August 28, 1998
  - *Fibre Channel Fabric Loop Attachment (FC-FLA)* working draft, rev 2.7, August 12, 1997
  - *Fibre Channel Private Loop SCSI Direct Attach (FC-PLDA)* working draft, rev 2.1, September 22, 1997
  - *Fibre Channel Tape (FC-TAPE)* profile, T11/98-124vD, rev 1.13, February 3, 1999
- Supports Fibre Channel protocol SCSI (FCP-SCSI) and Fibre Channel IP protocols
- Compliance with *PCI Bus Power Management Interface Specification* Revision 1.0 (PC98)
- Supports up to 200 Mbytes/sec sustained Fibre Channel data transfer rate
- Supports SCSI initiator, initiator/target, and target modes
- Onboard, enhanced RISC processor
- Onboard gigabit serial transceivers
- Supports PCI dual-address cycle and cache commands
- No host intervention required to execute complete SCSI and IP operations
- Supports multi-ID aliasing in target mode
- Supports external frame buffering for performance scalability over long distances

## Product Description

The ISP2200A is a single-chip, highly integrated, bus master, Fibre Channel processor that targets storage, clustering, and networking applications. This chip connects the PCI bus to a Fibre Channel loop or to a point-to-point Fibre Channel port.

The ISP2200A/33 is pin compatible with the ISP2100A/33. The ISP2200A/66 is pin compatible with the ISP2100A/66.

The ISP2200A is a fully autonomous device, capable of managing multiple I/O operations and associated data transfers from start to finish without host intervention.

The ISP2200A provides power management support in accordance with the *PCI Bus Power Management Interface Specification*. The ISP2200A block diagram is illustrated in figure 1.

### ISP Initiator/Target SCSI and IP Firmware

The ISP2200A firmware implements a multitasking host adapter that provides the host system with IP communications and complete SCSI command and data transport capabilities, thus freeing the host system from the simultaneous execution of SCSI and IP traffic. The firmware provides two interfaces to the host system: the command interface and the Fibre Channel transport interface. The single-threaded command interface facilitates debugging, configuration, and recovering errors. The multithreaded transport interface maximizes use of the Fibre Channel and host buses.

The ISP2200A can operate simultaneously in SCSI initiator and target modes, and supports SCSI and IP protocols concurrently.

### Software Drivers

The ISP2200A supports a host software interface similar to the QLogic parallel SCSI and FC-AL processor family. Existing ISP2100A software drivers for all major operating systems are easily modified to support the ISP2200A. The ISP2200A also supports FCP-SCSI and IP software drivers for most major operating systems.



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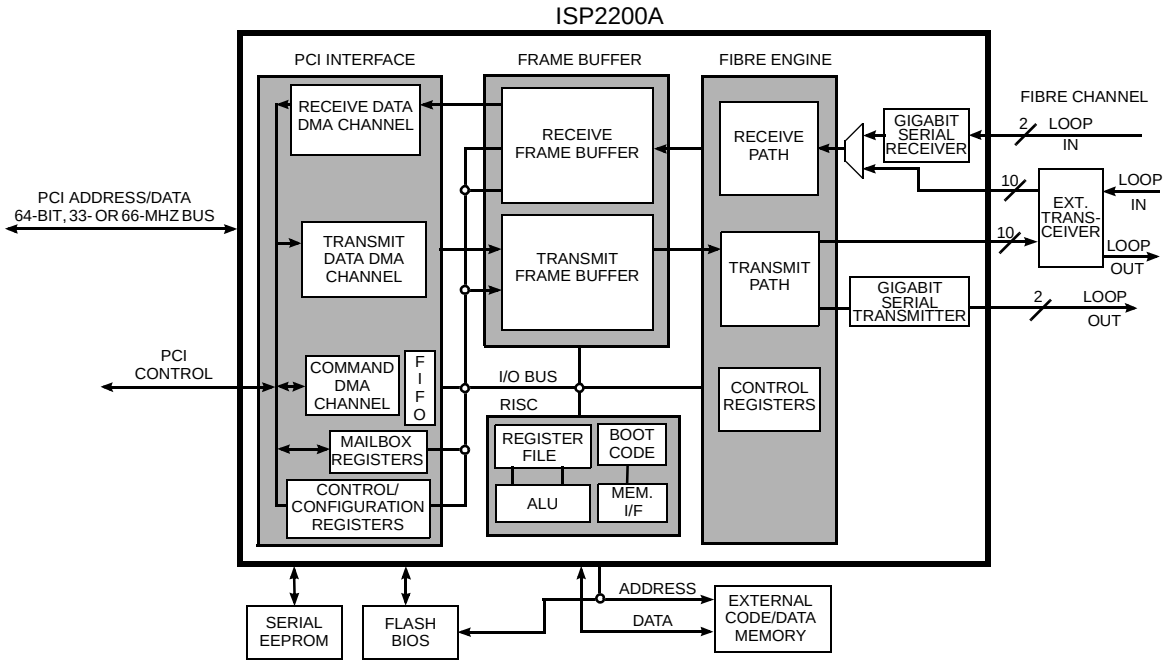



***Figure 1. ISP2200A Block Diagram***

## Subsystem Organization

To maximize I/O throughput and improve host and Fibre Channel utilization, the ISP2200A incorporates a high-speed, proprietary RISC processor; a Fibre Channel protocol manager (FPM); integrated frame buffer memory; and a host bus, three-channel, bus master DMA controller. The FPM and host bus DMA controller operate independently and concurrently under the control of the onboard RISC processor for maximum system performance.

The complete I/O subsystem solution using the ISP2200A and directly connected hard drives is shown in figure 2.

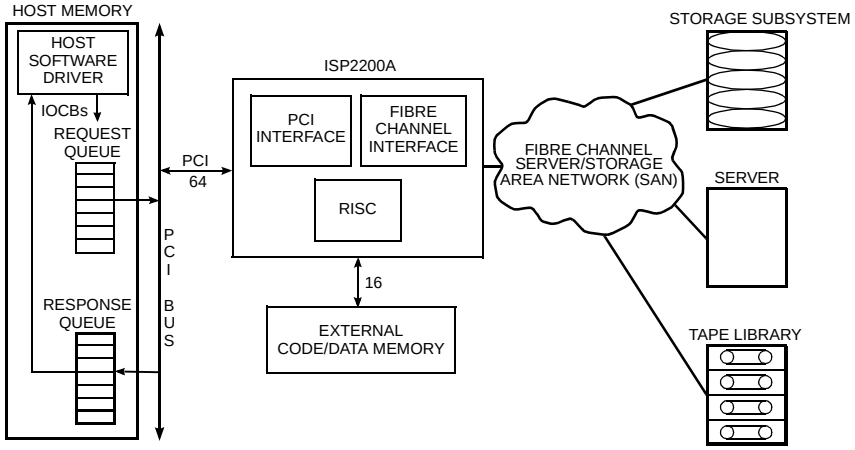



***Figure 2. I/O Subsystem Design Using the ISP2200A***

## Interfaces

The ISP2200A interfaces consist of the FC-AL interface, PCI bus interface, RISC interface, flash BIOS interface, and NVRAM control. Pins that support these interfaces and other chip operations are shown in figure 3.



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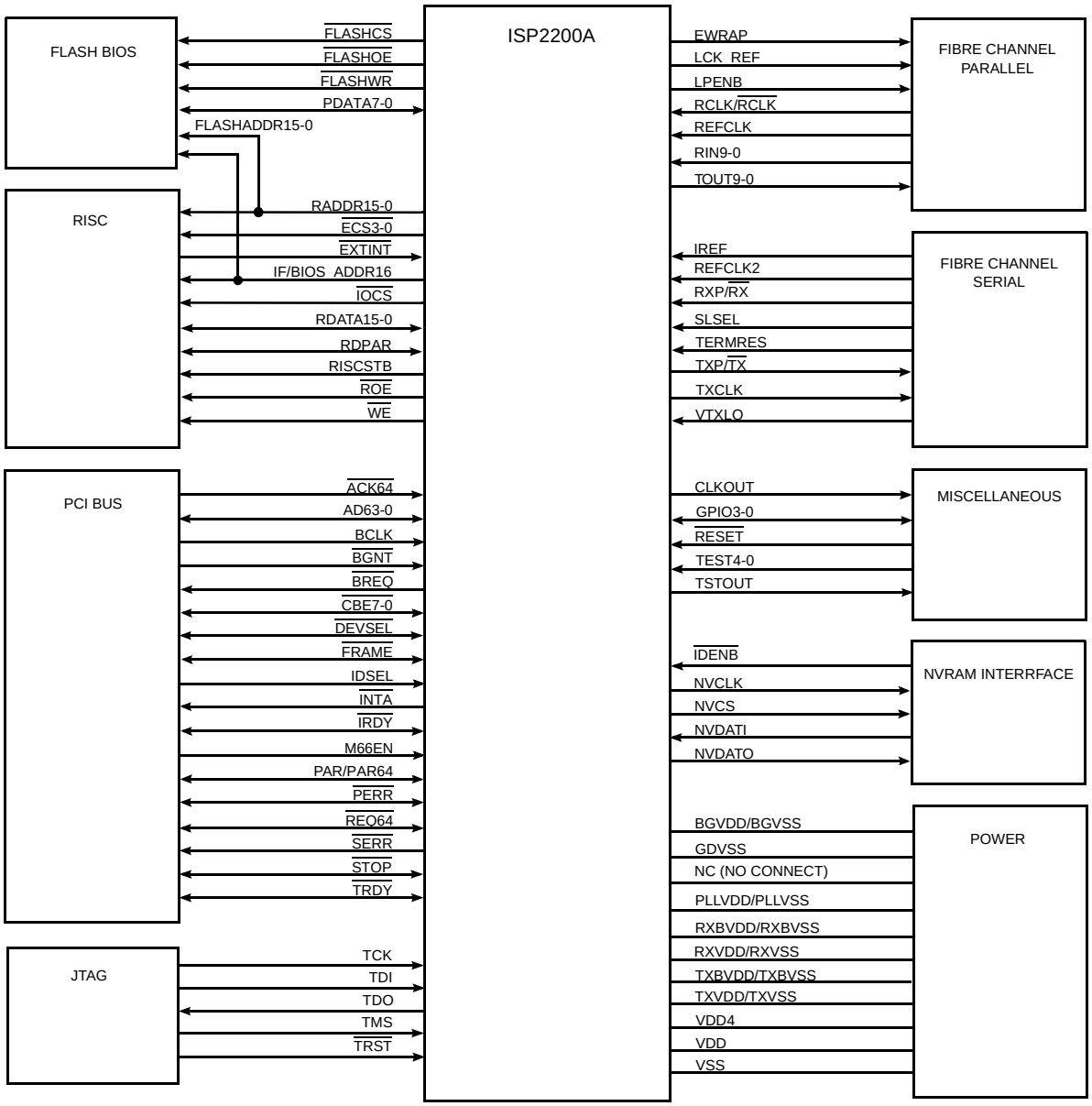



***Figure 3. ISP2200A Functional Signal Grouping***

## Fibre Channel Interface

The ISP2200A provides onboard gigabit transceivers for direct connection to the Fibre Channel ports on copper media. A standard 10-bit interface is also provided to connect to external transceivers, if desired.

## Fibre Channel Protocol Manager

The ISP2200A FPM supports the following:

- Support for one Fibre Channel port
- Gigabit serial interface
- Full-duplex data transfer rate up to 200 Mbytes/sec
- 10-bit interface to external transceivers
- Integrated frame buffer that supports up to 2112-byte frame payload
- 8b/10b encoder and decoder with clock skew management
- Support for an external buffer

The FPM transmits and receives at the full Fibre Channel rate of 106.25 Mbytes/sec. The on-chip frame buffer includes separate areas for received data and transmit data, as well as areas for managing special frames such as command and response. The FPM receive path validates and routes frames received from the Fibre Channel to the appropriate area in the frame buffer.



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The transmit path transmits frames from the frame buffer to the Fibre Channel. The FPM automatically handles frame delimiters and frame control.

The external buffer supports additional receive buffering for 10-km optical Fibre Channel links to eliminate dead time and allow a remote transmitter to send frames continuously. Enough initial buffer credit can then be issued by the ISP2200A to keep a remote transmitter busy until it sees an R_RDY return.

## PCI Interface

The ISP2200A PCI interface supports the following:

- 33-MHz (ISP2200A/33) or 66-MHz (ISP2200A/66), 64-bit, intelligent bus master interface
- 64-bit host memory addressing (dual address cycle)
- Backward compatible to 32-bit PCI
- Three-channel DMA controller
- 16-bit slave mode for communication with host
- Pipelined DMA registers for efficient scatter/gather operations
- 32-bit DMA transfer counter for I/O transfer length of up to four gigabytes
- Support for PCI cache commands
- Support for flash BIOS PROM
- Support for subsystem ID
- 3.3V and 5.0V tolerant PCI I/O buffers

The ISP2200A is designed to interface directly to the PCI bus and operate as a 64-bit DMA bus master. This function is accomplished through a PCI bus interface unit (PBIU) containing an onboard DMA controller. The PBIU generates and samples PCI control signals, generates host memory addresses, and facilitates the transfer of data between host memory and the onboard frame buffer. It also allows the host to access the ISP2200A internal registers and communicate with the onboard RISC processor.

The ISP2200A supports the minimum power management capabilities specified in revision 1.0 of the *PCI Bus Power Management Interface Specification*, which defines power states D0-D3, where D0 provides maximum power consumption and D3 provides minimal power consumption. The D3 power state is entered by either software (D3 *hot*) or by physically removing power (D3 *cold*). Hot and cold refer to the presence or absence of VCC, respectively.

The ISP2200A supports power states D0, D3 hot, and D3 cold.

The ISP2200A onboard DMA controller consists of three independent DMA channels that initiate transactions on the PCI bus and transfer data between the host memory and frame buffer. The command DMA channel is used mainly by the RISC processor for small transfers, such as fetching commands from and writing status information to the host memory over the PCI bus. The two data DMA channels, one for transmit and one for receive, transfer data between the FC-AL and the PCI bus, allowing for fast context switching.

The PBIU internally arbitrates between the two data DMA channels and the command DMA channel and alternately services them. Each DMA channel has a set of DMA registers that are programmed for transfers by the RISC processor.

## RISC Processor

The ISP2200A RISC processor supports the following:

- Execution of multiple I/O control blocks from the host memory
- Reduced host intervention and interrupt overhead
- One interrupt or less per I/O operation

One of the major features of the ISP2200A is its ability to handle complete I/O transactions from start to finish with no intervention from the host. This high level of integration is accomplished with the onboard RISC processor. The ISP2200A RISC processor controls the chip interfaces; executes simultaneous, multiple IOCBs; and maintains the required thread information for each transfer.

# Packaging

The ISP2200A/33 and the ISP2200A/66 are available in a 256-pin ball grid array (BGA) package. The ISP2200A/33 is pin compatible with the ISP2100A/33. The ISP2200A/66 is pin compatible with the ISP2100A/66.

Specifications are subject to change without notice.

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# Appendix VI:

## List of Tables

Table 1: Specifications ..... 21
Table 2: Radiation Specifications ..... 23
Table 3: Laser diode specifications ..... 23
Table 4: Fibre Channel Cables available from VMETRO ..... 25

## List of Figures

Figure 1: VMFC-2100/22x0 Block Diagram ..... 8
Figure 2: Intergrated Hub block diagram ..... 9
Figure 3: Integrated Hub functional diagram ..... 10
Figure 4: Integrated Hub connection. ..... 10
Figure 5: Automatic Hub connection ..... 10
Figure 6: Integrated Hub functional diagram ..... 10
Figure 7: Redundant Hub ..... 11
Figure 8: Redundant Hub ..... 11
Figure 9: Redundant point to point connection ..... 11
Figure 10: Redundant point to point functional diagram ..... 11
Figure 11: Redundant Arbitrated Loop functional diagram ..... 12
Figure 12: Redundant Arbitrated Loop connection ..... 12
Figure 13: Steps 1: Mount VMFC-2100/22x0 module(s) on the PowerMIDAS PMC carrier board. ..... 14
Figure 14: Single point to point connection ..... 16
Figure 15: Separating Fibre Channel SC cables from retainer ..... 17
Figure 16: Multi node loop connection using the VMFC-2100-F ..... 17
Figure 20: VMFC-2100 PMC Board layout ..... 19
Figure 21: VMFC-2100 PCI Board layout ..... 19
Figure 22: VMFC-2250 PMC Board layout ..... 20
Figure 23: Laser apertures ..... 24
Figure 24: DB9 Style Fibrechannel connector wiring. ..... 27
Figure 25: HSSDC style Fibrechannel connector wiring. ..... 27
Figure 26: HSSDC connector. ..... 27



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