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# VMIVME-7765

## Dual Pentium III Processor - VMEbus SBC

## Product Manual

A GE Fanuc Company

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500-007765-000 Rev. C

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# Overview

## Introduction

VMIC's VMIVME-7765 is a full-featured Dual Pentium III processor computer in a dual slot, passively cooled, Eurocard form factor that utilizes the advanced technology of Serverworks LE chipset running at a front-side bus rate of 133 MHz. The VMIVME-7765 is compliant with the VME Specification Rev. C.1 and features a PCI-to-VME bridge, allowing the board to function in multi-CPU systems.

The VMIVME-7765 provides features typically found on desktop systems, such as:

- Up to 2GB PC133 SDRAM
- PCI based SVGA support with 4 Mbytes video DRAM
- Built-in dual 10/100 Mbit Ethernet
- IDE drive support
- Floppy drive support
- Two RS232 serial ports
- Dual USB ports
- Real-Time clock/calendar
- Front panel reset switch
- Miniature speaker
- Keyboard/Mouse port
- Two Ultra 160 SCSI channels
- 64 Bit, 66MHz PMC site
- Compact Flash (Type I or II)
- One parallel port



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The LE chipset allows the VMIVME-7765 to provide enhanced features such as 133MHz front-side bus support and ATA-100 IDE support. The VMIVME-7765 is capable of executing many of today's desktop operating systems such as Microsoft's Windows NT 4.0, Windows 2000 and a wide variety of Linux-based operating systems. The standard features of the VMIVME-7765 are described in Chapter 2 of this manual.

The VMIVME-7765 provides features useful to embedded applications, such as:

- Remote Ethernet booting
- Up to 192 Mbytes of bootable compact flash (optional)
- Four general-purpose programmable timers (two 16-bit and two 32-bit)
- Software-selectable Watchdog Timer with reset

Additionally, the VMIVME-7765 offers a 64 Bit, 66 MHz PMC expansion site with front-panel access. The embedded features of the VMIVME-7765 are described in Chapter 3 of this manual.

The VMIVME-7765 is suitable for use in a variety of applications, such as: telecommunications, simulation, instrumentation, industrial control, process control and monitoring, factory automation, automated test systems, data acquisition systems and anywhere that the highest performance dual processor in a dual VME slot is desired.



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# Serverworks LE Chipset

The VMIVME-7765 incorporates the Serverworks chipset technology LE Server Set. This chipset allows for increased system performance by separating many high-bandwidth I/O accesses (like IDE or USB devices) from PCI accesses, relieving bottlenecks on the high speed PCI bus. Furthermore, the LE chipset brings new levels of integration to motherboard chipsets and provides additional features (like ATA-100 support) over other chipsets.



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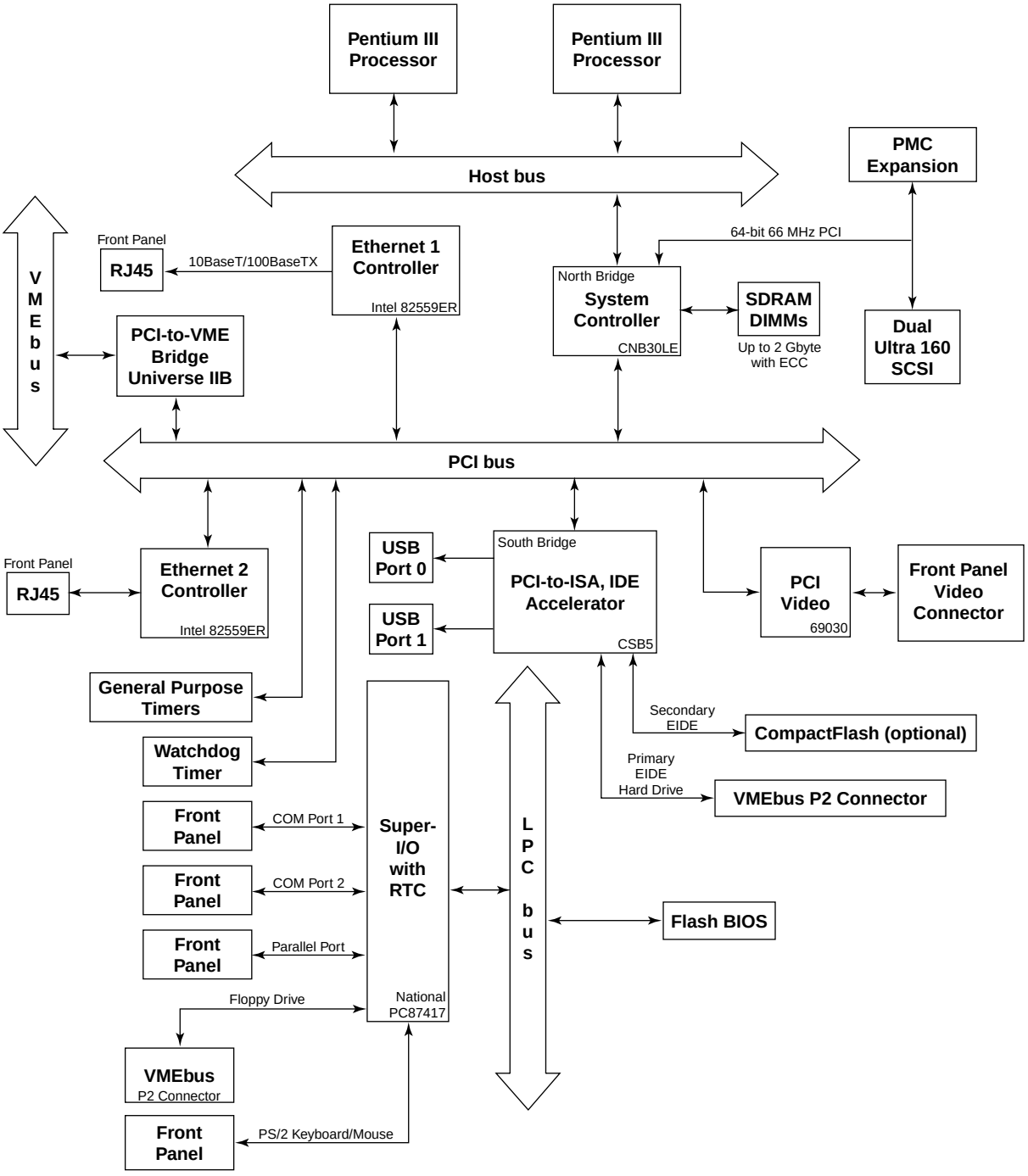



**Figure 1** VMIVME-7765 Block Diagram



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## Organization of the Manual

This manual is composed of the following chapters and appendices:

***Chapter 1 - Installation and Setup*** describes unpacking, inspection, hardware jumper settings, connector definitions, installation, system setup and operation of the VMIVME-7765.

***Chapter 2 - Standard Features*** describes the unit design in terms of the standard PC memory and I/O maps, along with the standard interrupt architecture.

***Chapter 3 - Embedded PC/RTOS Features*** describes the unit features that are beyond standard functions.

***Chapter 4 - Maintenance*** provides information relative to the care and maintenance of the unit.

***Appendix A - Connector Pinouts*** illustrates and defines the connectors included in the unit's I/O ports.

***Appendix B - System Driver Software*** provides details for installing drivers under Windows NT and Windows 2000.

***Appendix C - Phoenix BIOS*** describes the menus and options associated with the Phoenix (system) BIOS.

***Appendix D - LANWorks BIOS*** describes the menus and options associated with the LANWorks BIOS.

***Appendix E - SCSI BIOS*** describes general information about the SDMS SCSI BIOS and Configuration Utility version 4.19.00.

***Appendix F - Sample C Software*** provides example code to use with the VMIVME-7765.



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# References

***Pentium III Processor with 512Kb L2 Cache at 1.13GHz to 1.26GHz***
August 2001, Order Number 249657-002

***Pentium III Processor for the PGA370 Socket at 500MHz to 1.0GHz***
August 2000, Order Number 245264-006

***PCI Local Bus Specification, Rev. 2.1***
PCI Special Interest Group
P.O. Box 14070
Portland, OR 97214
(800) 433-5177 (U.S.)
(503) 797-4207 (International)
(503) 234-6762 (FAX)

***PC87417 Super I/O***

National Semiconductor
2900 Semiconductor Dr.
P.O. Box 58090
Santa Clara, CA 95052-8090
(800) 272-9959
(800) 737-7018 (FAX)

***LSI SYM53C1010 Dual SCSI Controller***
LSI Logic Corp.
1551 McCauthy Blvd.
Milpitas, CA 95035
(866) 574-5741

***CMC Specification, P1386/Draft 2.0 from:***
IEEE Standards Department
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445 Hoes Lanes, P.O. Box 1331
Piscataway, NJ 08855-1331, USA

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***VMISFT-9420 IOWorks Access User's Guide***
Doc. No. 520-009420-910
VMIC
12090 South Memorial Pkwy.
Huntsville, AL 35803-3308
(800) 322-3616
www.vmic.com



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### *VMIC's Tundra Universe II Based VMEbus Interface*

Doc. No. 500-000211-000
VMIC
12090 South Memorial Pkwy.
Huntsville, AL 35803-3308
(800) 322-3616
www.vmic.com

For a detailed description and specification of the VME bus, please refer to:

### *VMEbus Specification Rev. C. and the VMEbus Handbook*

VMEbus International Trade Assoc. (VITA)
7825 East Gelding Dr.
Suite 104
Scottsdale, AZ 85260
(602) 951-8866
(602) 951-0720 (FAX)
www.vita.com

The following is useful information related to remote Ethernet booting of the VMIVME-7765:

### *Microsoft Windows NT Server Resource Kit*

Microsoft Corporation
ISBN: 1-57231-344-7
www.microsoft.com



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# Safety Summary

The following general safety precautions must be observed during all phases of the operation, service and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture and intended use of this product.

VMIC assumes no liability for the customer's failure to comply with these requirements.

## Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

## Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

## Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

## Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person capable of rendering first aid and resuscitation is present.

## Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VMIC for service and repair to ensure that safety features are maintained.

## Dangerous Procedure Warnings

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

**WARNING:** Dangerous voltages, capable of causing death, are present in this system. Use extreme caution when handling, testing and adjusting.



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## Warnings, Cautions and Notes

**STOP** informs the operator that a practice or procedure should not be performed. Actions could result in injury or death to personnel, or could result in damage to or destruction of part or all of the system.

**WARNING** denotes a hazard. It calls attention to a procedure, practice or condition, which, if not correctly performed or adhered to, could result in injury or death to personnel.

**CAUTION** denotes a hazard. It calls attention to an operating procedure, practice or condition, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

**NOTE** denotes important information. It calls attention to a procedure, practice or condition which is essential to highlight.



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## Notation and Terminology

This product bridges the traditionally divergent worlds of Intel-based PC's and Motorola-based VMEbus controllers; therefore, some confusion over "conventional" notation and terminology may exist. Every effort has been made to make this manual consistent by adhering to conventions typical for the Motorola/VMEbus world; nevertheless, users in both camps should review the following notes:

- Hexadecimal numbers are listed Motorola-style, prefixed with a dollar sign: $F79, for example. By contrast, this same number would be signified 0F79H according to the Intel convention, or 0xF79 by many programmers. Less common are forms such as $F79_h$ or the mathematician's $F79_{16}$.
- An 8-bit quantity is termed a "byte," a 16-bit quantity is termed a "word," and a 32-bit quantity is termed a "longword." The Intel convention is similar, although their 32-bit quantity is more often called a "doubleword."
- Motorola programmers should note that Intel processors have an I/O bus that is completely independent from the memory bus. Every effort has been made in the manual to clarify this by referring to registers and logical entities in I/O space by prefixing I/O addresses as such. Thus, a register at "I/O $140" is not the same as a register at "$140," since the latter is on the memory bus while the former is on the I/O bus.
- Intel programmers should note that addresses are listed in this manual using a linear, "flat-memory" model rather than the old segment:offset model associated with Intel Real Mode programming. Thus, a ROM chip at a segment:offset address of C000:0 will be listed in this manual as being at address $C0000. For reference, here are some quick conversion formulas:

Segment:Offset to Linear Address

Linear Address = (Segment × 16) + Offset

Linear Address to Segment:Offset

Segment = ((Linear Address ÷ 65536) – *remainder*) × 4096

Offset = *remainder* × 65536

Where *remainder* = the fractional part of (Linear Address ÷ 65536)

Note that there are many possible segment:offset addresses for a single location. The formula above will provide a unique segment:offset address by forcing the segment to an even 64 Kbyte boundary, for example, $C000, $E000, etc. When using this formula, make sure to round the offset calculation properly!



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CHAPTER 1

# Installation and Setup

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## Introduction

This chapter describes the hardware jumper settings, connector descriptions, installation, system setup and operation of the VMIVME-7765.

## Unpacking Procedures

Any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC Customer Service along with a request for advice concerning the disposition of the damaged item(s).

**CAUTION:** Some of the components assembled on VMIC's products may be sensitive to electrostatic discharge and damage may occur on boards that are subjected to a high energy electrostatic field. When the board is placed on a bench for configuring, etc., it is suggested that conductive material be inserted under the board to provide a conductive shunt. Unused boards should be stored in the same protective boxes in which they were shipped.



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## Hardware Setup

The VMIVME-7765 is factory populated with user-specified options as part of the VMIVME-7765 ordering information. The CPU speed, RAM size and flash memory size are not user-upgradable. To change CPU speeds or RAM / Flash size, contact customer service to receive a Return Material Authorization (RMA).

VMIC Customer Service is available at: 1-800-240-7782.

Or E-mail us at customer.service@vmic.com

The VMIVME-7765 is tested for system operation and shipped with factory-installed header jumpers. The physical location of the jumpers and connectors for the single board CPU are illustrated in Figure 1-1 on page 29. The definitions of the CPU board jumpers and connectors are included in Table 1-1 through Table 1-4.

**CAUTION:** All jumpers marked *User Configurable* in the following tables may be changed or modified by the user. All jumpers marked factory configured should not be modified by the user.

**Care must be taken when making jumper modifications to ensure against improper settings or connections. Improper settings may result in damage to the unit.**

Modifying any jumper not marked “User Configurable” will void the Warranty and may damage the unit. The default jumper condition of the VMIVME-7765 is expressed in Table 1-1 through Table 1-4 with **bold text** in the table cells.



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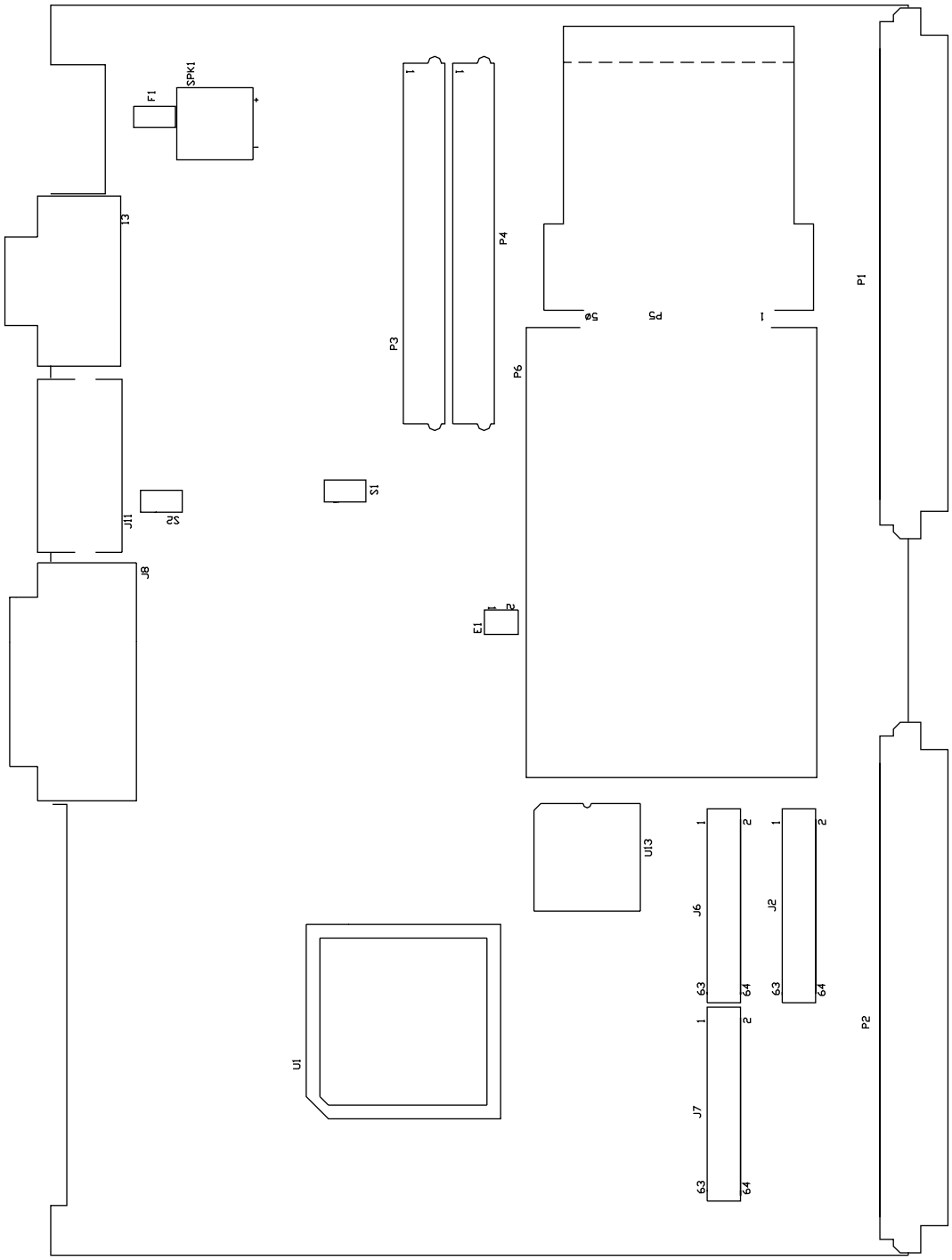



**Figure 1-1** VMIVME-7765 (Top Board) Jumper Locations



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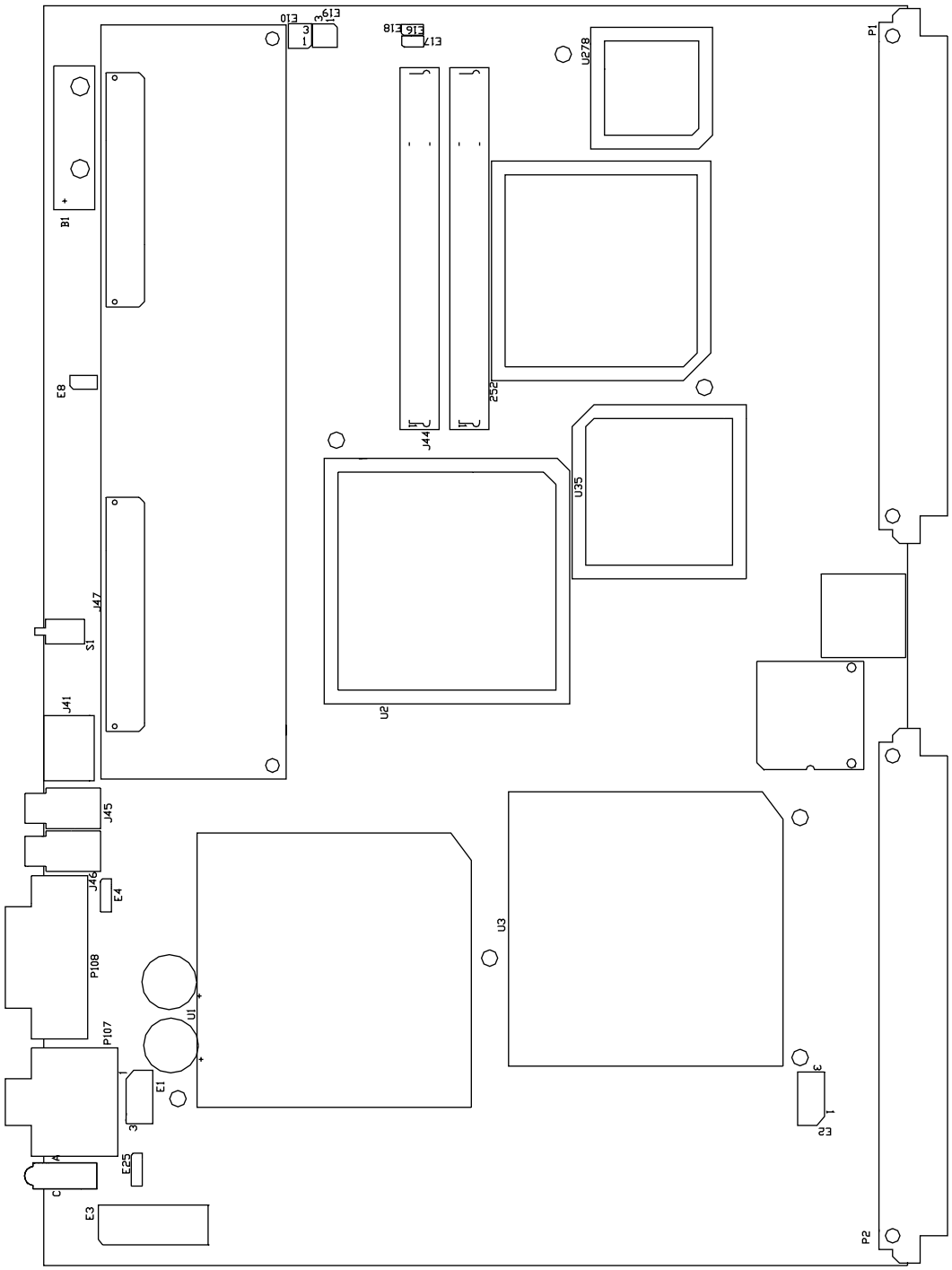



**Figure 1-2** VMIVME-7765 (Bottom Board) Jumper Locations



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**Table 1-1** CPU Board Connectors

| Connector (Main Board) | Function |
|---|---|
| E1, E2 | Fan |
| E4, E8, E17, E25 | Factory Reserved (all jumpers open)<br>Do Not Use |
| E10, E19 | VME Jumpers |
| E18 | CMOS Clear |
| J2, J6, J7 | PMC Slot 1 |
| J8 | Dual SCSI |
| J11 | Ethernet 1 & 2 |
| J13 | Video |
| J41 | Mouse/Keyboard |
| J45, J46 | Dual USB |
| P1, P2 | VME |
| P2 | IDE (PRI), Floppy |
| P107 | COM 1, COM 2 |
| P108 | Parallel Port |

**NOTE:** The BIOS has the capability (not currently enabled) of password protecting casual access to the unit's CMOS set-up screens. The Password Clear jumper allows the user to clear the password in the case of a forgotten password.

To clear the CMOS password:

1. Turn off power to the unit.
2. Remove the jumper from E18.
3. Power up the unit.
4. Power down the unit and replace the jumper on E18.

When power is reapplied to the unit, the CMOS password will be cleared.

**Table 1-2** CMOS Clear (**User Configurable**) - Jumper (E18)

| Select | Jumper Position |
|---|---|
| **Normal** | **Short** |
| Clear CMOS/Password | Open |



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**Table 1-3** VME Jumper (**User Configurable**) - Jumper (E10)

| Select | Jumper Position |
|---|---|
| **Map UNIV2 to I/O Space** | **1-3** |
| **Enable SYSFAIL Generation** | **2-4** |

**Table 1-4** VME Jumper (**User Configurable**) - Jumper (E19)

| Select | Jumper Position |
|---|---|
| **Enable VME SYSRESET Driver** | **1-3** |
| **Enable SYSRESET Receiver** | **2-4** |



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# Installation

The VMIVME-7765 conforms to the VMEbus physical specification for a dual slot 6U dual Eurocard (dual height). It can be plugged directly into any standard chassis accepting this type of board.

**CAUTION:** Do not install or remove the board while power is applied.

The following steps describe the VMIC recommended method for VMIVME-7765 installation and power-up:

1. Make sure power to the equipment is off.
2. Choose chassis slot. The VMIVME-7765 ***must*** be attached to a dual P1/P2 VMEbus backplane. Both slots must have populated P1/P2 connectors to provide the necessary power pins.

   If the VMIVME-7765 is to be the VMEbus system controller, choose the first two VMEbus slots. If a different board is the VMEbus system controller, choose any two adjacent slots **except** slots one and two. The VMIVME-7765 does not require jumpers for enabling/disabling the system controller function.

**The VMIVME-7765 requires forced air cooling** Air flow requirement as measured at output side of heatsink is to be greater than 450LFM.

It is advisable to install blank panels over any exposed VMEbus slots. This will allow for better air flow over the VMIVME-7765.

Insert the VMIVME-7765 into the chosen VMEbus chassis slots. While ensuring that the board is properly aligned and oriented in the supporting board guides, slide the board smoothly forward against the mating connector until firmly seated. As this is a two slot product, special attention must be given to ensure that all four VME connectors are properly seated, and the provided mounting screws are installed.

3. Connect all needed peripherals to the front panel. Each connector is clearly labeled on the front panel, and detailed pinouts are in Appendix A. Minimally, a keyboard and a monitor are required if the user has not previously configured the system.
4. Apply power to the system. Several messages are displayed on the screen, including names, versions and copyright dates for the various BIOS modules on the VMIVME-7765.
5. The VMIVME-7765 features a Flash Disk resident on the board. Refer to Chapter 3 for set up details.
6. If an IDE drive is installed, the BIOS Setup program must be run to configure the



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drive types. See Appendix C to properly configure the system.

7. If a drive is present, install the operating system according to the manufacturer's instructions.

See Appendix B for instructions on installing VMIVME-7765 peripheral driver software during operating system installation.

## BIOS Setup

The VMIVME-7765 has an on-board BIOS Setup program that controls many configuration options. These options are saved in a special non-volatile, battery-backed memory chip and are collectively referred to as the board's 'CMOS Configuration'. The CMOS configuration controls many details concerning the behavior of the hardware from the moment power is applied.

The VMIVME-7765 is shipped from the factory with hard drive type configuration set to AUTO in the CMOS.

Details of the VMIVME-7765 BIOS setup program are included in Appendix C.

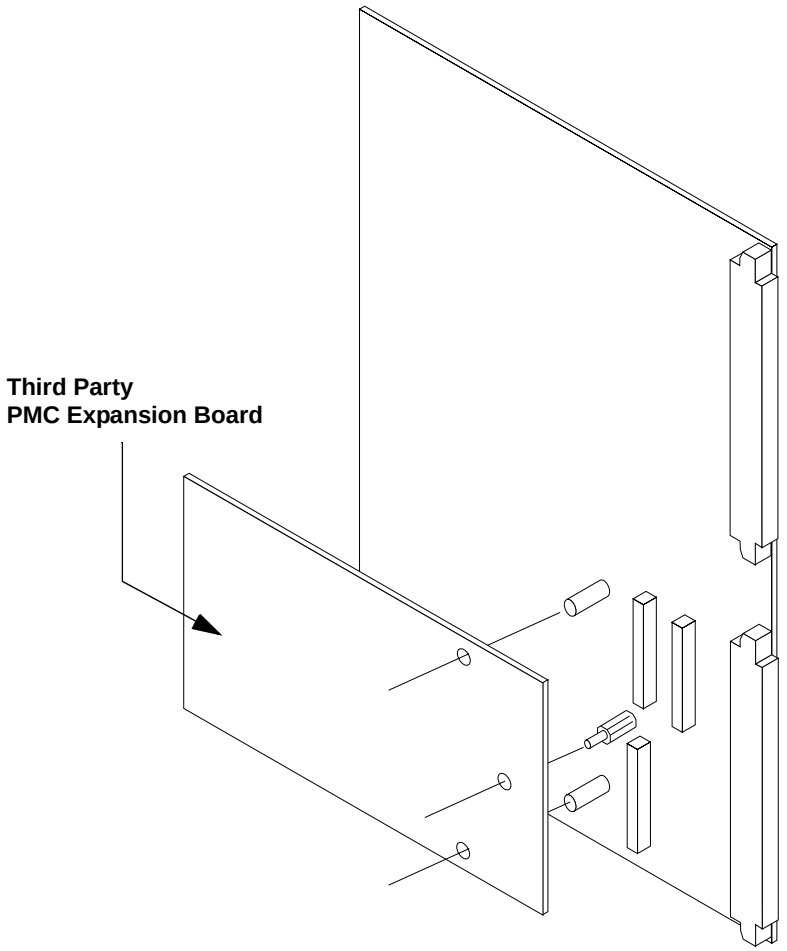



**Figure 1-3** Installing a PMC Card on the VMIVME-7765



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## Front/Rear Panel Connectors

The VMIVME-7765 provides front-panel access to the PMC expansion site, the VGA connector, both 10/100 Ethernet connectors, the manual reset switch, COM 1 and 2, dual USB, parallel port, the dual Ultra 160 SCSI and the status LEDs. A drawing of the VMIVME-7765 front-panel is shown in Figure 1-4. The front-panel connectors and indicators are labeled as follows:

- ENET 1 — 10/100 Mbit Ethernet connector
- ENET 2 — 10/100 Mbit Ethernet connector
- SVGA — SVGA video connector
- Parallel — Parallel port
- RST — Manual reset switch
- COM 1:2 — Two COM ports
- M/K — Dual mouse/keyboard connector
- USB 1:2 — Dual USB connector
- PMC — PMC site
- BPAS — Status LEDs
- Ultra 160 SCSI A&B — Two Ultra 160 SCSI channels

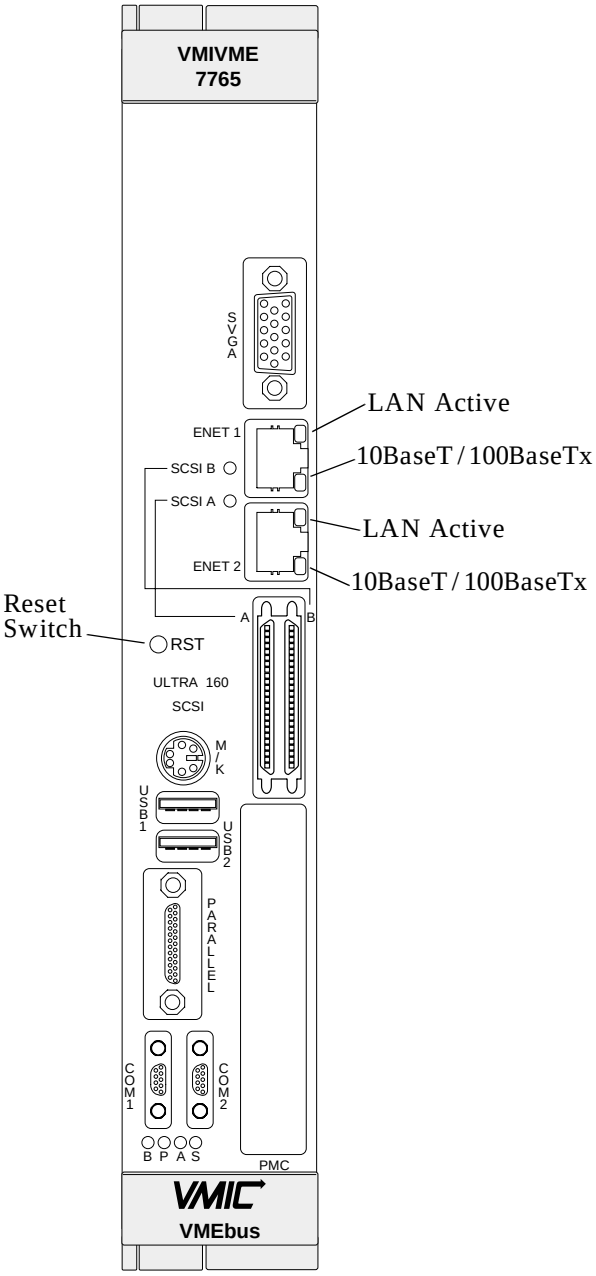
The VMIVME-7765 provides rear I/O support for a Primary IDE drive and a floppy drive. These signals are accessed by the use of a rear-panel transition board such as the VMIACC-0562, which terminates into industry standard connectors.

The front panel connectors, including connector pinouts and orientation, for the VMIVME-7765 are defined in Appendix A. Rear panel connections are defined in the appropiate rear panel transition utility board Installation Guide. See the VMIVME-7765 product specification for compatible rear panel transistion utility boards offered by VMIC.



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## LED Definition




| | |
|---|---|
| Reset Switch | *Reset* - Allows the system to be reset from the front panel. |
| LED B | *Boot Done* - Lights during Power up Self Test (POST). Off when CPU has passed POST. |
| LED P | *Power* - Indicates when +5v power is applied to the board, (Green LED). |
| LED A | *IDE "Activity" Indicator* - Indicates when IDE activity is occurring, (Yellow LED). |
| LED S | *Sysfail* - Any VME 'SYSFAILS' will be indicated by this LED. |
| LAN1 Active | Indicates the Ethernet is active, (Yellow LED). |
| LAN1 10/100BaseTx | Indicates whether 10BaseT or 100BaseTx mode. Yellow LED indicates 10BaseT, and Green LED indicates 100BaseTx. |
| LAN2 Active | Indicates the Ethernet is active, (Yellow LED). |
| LAN2 10/100BaseTx | Indicates whether 10BaseT or 100BaseTx mode. Yellow LED indicates 10BaseT, and Green LED indicates 100BaseTx. |

**Figure 1-4** Front Panel LED Positions



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CHAPTER
2

# Standard Features

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## Introduction

The VMIVME-7765 is a dual Intel Pentium III, processor-based SBC that is compatible with modern industry standard desktop systems. The VMIVME-7765 therefore retains industry standard memory and I/O maps along with a standard interrupt architecture. The integrated peripherals described in this section (such as serial ports, USB ports, IDE drives, floppy drives, video controller, Ethernet controller and Ultra 160 SCSI controllers) are all memory mapped the same as similarly equipped desktop systems, ensuring compatibility with modern operating systems.

The following sections describe the standard features of the VMIVME-7765.



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## CPU Sockets

The VMIVME-7765 CPU sockets are factory populated with a high-speed Pentium III processor. The CPU speed and RAM / flash size are user specified as part of the VMIVME-7765 ordering information.

To change CPU speeds, RAM size or flash size contact customer service to receive a Return Material Authorization (RMA).

VMIC Customer Service is available at: 1-800-240-7782.

## Physical Memory

The VMIVME-7765 provides Synchronous DRAM (SDRAM) as on-board system memory. Memory can be accessed as bytes, words or longwords.

The VMIVME-7765 accepts surface mount SDRAM modules with ECC for a maximum capacity of 2 Gbytes. The on-board DRAM is accessible from the VMEbus through the PCI-to-VME bridge and is addressable by the local processor, as well as the VMEbus slave interface by another VMEbus master. Caution must be used when sharing memory between the local processor and the VMEbus to prevent a VMEbus master from overwriting the local processor's operating system.

**NOTE:** When using the Configure utility of VMIC's IOWorks Access with Windows NT 4.0 to configure RAM, do not request more than 25 percent of the physical RAM. Exceeding the 25 percent limit may result in a known Windows NT bug that causes unpredictable behavior during the Windows NT boot sequence, and requires the use of an emergency repair disk to restore the computer. The bug is present in Windows NT 4.0 service pack level 3. It is recommended that an emergency repair disk be kept up-to-date and easily accessible.

**NOTE:** Memory capacity may be extended as parts become available.



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# Memory and Port Maps

## Memory Map - Tundra Universe II-Based PCI-to-VMEbus Bridge

The memory map for the Tundra Universe II-based interface VMIVME-7765 is shown in Table 2-1. All systems share this same memory map, although a VMIVME-7765 with less than the full 256 Mbyte of SDRAM does not fill the entire space reserved for On-Board Extended Memory.

**Table 2-1** VMIVME-7765, Universe II-Based Interface Memory Address Map

| MODE | MEMORY ADDRESS RANGE | SIZE | DESCRIPTION |
|---|---|---|---|
| PROTECTED MODE | $FFFF 0000 - $FFFF FFFF | 64 Kbyte | ROM BIOS Image |
| | $0400 0000 - $FFFE FFFF | 1.9 Gbyte | Unused * |
| | $0010 0000 - $0FFF FFFF | 2 Gbyte | Reserved for ** On-Board Extended Memory (not filled on all systems) |
| REAL MODE | $E0000 - $FFFFF | 128 Kbyte | Reserved for BIOS Area |
| | $D8018 - $DFFFF | 32 Kbyte | |
| | $D8016 - $D8017 | 2 bytes | |
| | $D8014 - $D8015 | 2 bytes | |
| | $D8010 - $D8013 | 2 bytes | |
| | $D800E - $D800F | 2 bytes | |
| | $D8000 - $D800D | 14 bytes | |
| | $C8000 - $D7FFF | 64 Kbyte | |
| | $C0000 - $C7FFF | 32 Kbyte | |
| | $A0000 - $BFFFF | 128 Kbyte | |
| | $00000 - $9FFFF | 640 Kbyte | |

* This space can be used to set up protected mode PCI-to-VMEbus windows (also referred to as PCI slave images). BIOS will also map on-board PCI based video DRAM, Timers and Watchdog Timers in this area.

** This space can be allocated as shared memory (for example, between the Pentium processor-based CPU and VMEbus Master). Note that if a PMC board is loaded, the expansion BIOS may be placed in this area.



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# I/O Port Map

Like a desktop system, the VMIVME-7765 includes special input/output instructions that access I/O peripherals residing in I/O addressing space (separate and distinct from memory addressing space). Locations in I/O address space are referred to as *ports*. When the CPU decodes and executes an I/O instruction, it produces a 16-bit I/O address on lines A00 to A15 and identifies the I/O cycle with the M/I/O control line. Thus, the CPU includes an independent 64 Kbyte I/O address space, which is accessible as bytes, words or longwords.

Standard hardware circuitry reserves only 1,024 byte of I/O addressing space from I/O $000 to $3FF for peripherals. All standard PC I/O peripherals, such as serial and parallel ports, hard and floppy drive controllers, video system, real-time clock, system timers and interrupt controllers are addressed in this region of I/O space. The BIOS initializes and configures all these registers properly; adjusting these I/O ports directly is not normally necessary.

The assigned and user-available I/O addresses are summarized in the I/O Address Map, Table 2-2.

**Table 2-2** VMIVME-7765 I/O Address Map

| I/O ADDRESS RANGE | SIZE IN BYTES | HW DEVICE | PC/AT FUNCTION |
|---|---|---|---|
| $000 - $00F | 16 | | DMA Controller 1<br>(Intel 8237A Compatible) |
| $010 - $01F | 16 | | Reserved |
| $020 - $021 | 2 | | Master Interrupt Controller<br>(Intel 8259A Compatible) |
| $022 - $03F | 30 | | Reserved |
| $040 - $043 | 4 | | Programmable Timer<br>(Intel 8254 Compatible) |
| $044 - $05F | 30 | | Reserved |
| $060 - $064 | 5 | | Keyboard, Speaker, System Configuration<br>(Intel 8042 Compatible) |
| $065 - $06F | 11 | | Reserved |
| $070 - $071 | 2 | | Real-Time Clock |
| $072 - $07F | 14 | | Reserved |
| $080 - $08F | 16 | | DMA Page Registers |
| $090 - $091 | 2 | | Reserved |
| $092 | 1 | | Alt. Gate A20/Fast Reset Register |
| $093 - $09F | 11 | | Reserved |



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**Table 2-2** VMIVME-7765 I/O Address Map (Continued)

| I/O ADDRESS RANGE | SIZE IN BYTES | HW DEVICE | PC/AT FUNCTION |
|---|---|---|---|
| $0A0 - $0A1 | 2 | | Slave Interrupt Controller (Intel 8259A Compatible) |
| $0A2 - $0BF | 30 | | Reserved |
| $0C0 - $0DF | 32 | | DMA Controller 2 (Intel 8237A Compatible) |
| $0E0 - $16F | 142 | | Reserved |
| $170 - $177 | 8 | ICH2 | Secondary Hard Disk Controller |
| $178 - $1EF | 120 | | User I/O |
| $1F0 - $1F7 | 8 | ICH2 | Primary Hard Disk Controller |
| $1F8 - $277 | 128 | | User I/O |
| $278 - $27F | 8 | I/O Chip* | LPT2 Parallel I/O* |
| $280 - $2E7 | 104 | | Reserved |
| $2E8 - $2EE | 7 | UART* | COM4 Serial I/O* |
| $2EF - $2F7 | 9 | | User I/O |
| $2F8 - $2FE | 7 | Super-I/O Chip | COM2 Serial I/O (16550 Compatible) |
| $2FF - $36F | 113 | | Reserved |
| $370 - $377 | 8 | Super-I/O Chip | Secondary Floppy Disk Controller |
| $378 - $37F | 8 | Super-I/O Chip* | LPT1 Parallel I/O* |
| $380 - $3E7 | 108 | | Reserved |
| $3E8 - $3EE | 7 | UART* | COM3 Serial I/O* |
| $3F0 - $3F7 | 8 | Super-I/O Chip | Primary Floppy Disk Controller |
| $3F8 - $3FE | 7 | Super-I/O Chip | COM1 Serial I/O (16550 Compatible) |
| $3FF - $4FF | 256 | | Reserved |
| $500 - CFF | 2048 | | Reserved |

** While these I/O ports are reserved for the listed functions, they are not implemented on the VMIVME-7765. They are listed here to make the user aware of the standard PC usage of these ports.*



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# Interrupts

## System Interrupts

In addition to an I/O port address, an I/O device has a separate hardware interrupt line assignment. Assigned to each interrupt line is a corresponding interrupt vector in the 256-vector interrupt table at $00000 to $003FF in memory. The 16 maskable interrupts and the single Non-Maskable Interrupt (NMI) are listed in Table 2-3 along with their functions. Table 2-4 on page 43 details the vectors in the interrupt vector table. The interrupt number in HEX and decimal are also defined for real and protected mode in Table 2-4 on page 43.

The interrupt hardware implementation on the VMIVME-7765 is standard for computers built around the PC architecture, which evolved from the IBM PC/XT. In the IBM PC/XT computers, only eight interrupt request lines exist, numbered from IRQ0 to IRQ7 at the PIC. The IBM PC/AT computer added eight more IRQx lines, numbered IRQ8 to IRQ15, by cascading a second slave PIC into the original master PIC. IRQ2 at the master PIC was committed as the cascade input from the slave PIC. This architecture is represented in Figure 2-1 on page 47.

To maintain backward compatibility with PC/XT systems, IBM chose to use the new IRQ9 input on the slave PIC to operate as the old IRQ2 interrupt line on the PC/XT Expansion Bus. Thus, in AT systems, the IRQ9 interrupt line connects to the old IRQ2 pin (pin B4) on the AT Expansion Bus (or ISA bus).

**Table 2-3** PC Hardware Interrupt Line Assignments

| IRQ | AT FUNCTION | COMMENTS |
|---|---|---|
| NMI | Parity Errors<br>(Must be enabled in BIOS Setup) | Used by VMIVME-7765 PCIbus Interface |
| 0 | System Timer | Set by BIOS Setup |
| 1 | Keyboard | Set by BIOS Setup |
| 2 | Duplexed to IRQ9 | |
| 3 | COM2 | |
| 4 | COM1 | |
| 5 | Not Assigned | Determined by BIOS |
| 6 | Floppy Controller | |
| 7 | Parallel Port | |
| 8 | Real-Time Clock | |
| 9 | Not Assigned | Determined by BIOS |
| 10 | Not Assigned | Determined by BIOS |
| 11 | Not Assigned | Determined by BIOS |



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**Table 2-3** PC Hardware Interrupt Line Assignments (Continued)

| IRQ | AT FUNCTION | COMMENTS |
|---|---|---|
| 12 | Mouse | |
| 13 | Math Coprocessor | |
| 14 | Primary IDE | Routed to P2 Only* |
| 15 | Secondary IDE | CF Type I/II |

**Determined by BIOS if no IDE devices are present*

**Table 2-4** PC Interrupt Vector Table

| INTERRUPT NO. | | IRQ LINE | REAL MODE | PROTECTED MODE |
|---|---|---|---|---|
| HEX | DEC | | | |
| 00 | 0 | | Divide Error | Same as Real Mode |
| 01 | 1 | | Debug Single Step | Same as Real Mode |
| 02 | 2 | NMI | Memory Parity Error, VME Interrupts | Same as Real Mode (Must be enabled in BIOS Setup) |
| 03 | 3 | | Debug Breakpoint | Same as Real Mode |
| 04 | 4 | | ALU Overflow | Same as Real Mode |
| 05 | 5 | | Print Screen | Array Bounds Check |
| 06 | 6 | | | Invalid OpCode |
| 07 | 7 | | | Device Not Available |
| 08 | 8 | IRQ0 | Timer Tick | Double Exception Detected |
| 09 | 9 | IRQ1 | Keyboard Input | Coprocessor Segment Overrun |
| 0A | 10 | IRQ2 | BIOS Reserved | Invalid Task State Segment |
| 0B | 11 | IRQ3 | COM2 Serial I/O | Segment Not Present |
| 0C | 12 | IRQ4 | COM1 Serial I/O | Stack Segment Overrun |
| 0D | 13 | IRQ5 | Unassigned | Unassigned |
| 0E | 14 | IRQ6 | Floppy Disk Controller | Page Fault |
| 0F | 15 | IRQ7 | Unassigned | Unassigned |
| 10 | 16 | | BIOS Video I/O | Coprocessor Error |
| 11 | 17 | | System Configuration Check | Same as Real Mode |
| 12 | 18 | | Memory Size Check | Same as Real Mode |



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**Table 2-4** PC Interrupt Vector Table (Continued)

| INTERRUPT NO. | | IRQ LINE | REAL MODE | PROTECTED MODE |
|---|---|---|---|---|
| HEX | DEC | | | |
| 13 | 19 | | XT Floppy / Hard Drive | Same as Real Mode |
| 14 | 20 | | BIOS Comm I / O | Same as Real Mode |
| 15 | 21 | | BIOS Cassette Tape I / O | Same as Real Mode |
| 16 | 22 | | BIOS Keyboard I / O | Same as Real Mode |
| 17 | 23 | | BIOS Printer I / O | Same as Real Mode |
| 18 | 24 | | ROM BASIC Entry Point | Same as Real Mode |
| 19 | 25 | | Bootstrap Loader | Same as Real Mode |
| 1A | 26 | | Time of Day | Same as Real Mode |
| 1B | 27 | | Control / Break Handler | Same as Real Mode |
| 1C | 28 | | Timer Control | Same as Real Mode |
| 1D | 29 | | Video Parameter Table Pntr | Same as Real Mode |
| 1E | 30 | | Floppy Parm Table Pntr | Same as Real Mode |
| 1F | 31 | | Video Graphics Table Pntr | Same as Real Mode |
| 20 | 32 | | DOS Terminate Program | Same as Real Mode |
| 21 | 33 | | DOS Function Entry Point | Same as Real Mode |
| 22 | 34 | | DOS Terminate Handler | Same as Real Mode |
| 23 | 35 | | DOS Control / Break Handler | Same as Real Mode |
| 24 | 36 | | DOS Critical Error Handler | Same as Real Mode |
| 25 | 37 | | DOS Absolute Disk Read | Same as Real Mode |
| 26 | 38 | | DOS Absolute Disk Write | Same as Real Mode |
| 27 | 39 | | DOS Program Terminate, Stay Resident | Same as Real Mode |
| 28 | 40 | | DOS Keyboard Idle Loop | Same as Real Mode |
| 29 | 41 | | DOS CON Dev. Raw Output | Same as Real Mode |
| 2A | 42 | | DOS 3.x+ Network Comm | Same as Real Mode |
| 2B | 43 | | DOS Internal Use | Same as Real Mode |
| 2C | 44 | | DOS Internal Use | Same as Real Mode |
| 2D | 45 | | DOS Internal Use | Same as Real Mode |
| 2E | 46 | | DOS Internal Use | Same as Real Mode |
| 2F | 47 | | DOS Print Spooler Driver | Same as Real Mode |
| 30-60 | 48-96 | | Reserved by DOS | Same as Real Mode |



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**Table 2-4** PC Interrupt Vector Table (Continued)

| INTERRUPT NO. | | IRQ LINE | REAL MODE | PROTECTED MODE |
|---|---|---|---|---|
| HEX | DEC | | | |
| 61-66 | 97-102 | | User Available | Same as Real Mode |
| 67-6F | 103-111 | | Reserved by DOS | Same as Real Mode |
| 70 | 112 | IRQ8 | Real Time Clock | |
| 71 | 113 | IRQ9 | Redirect to IRQ2 | |
| 72 | 114 | IRQ10 | Not Assigned | |
| 73 | 115 | IRQ11 | Not Assigned | |
| 74 | 116 | IRQ12 | Mouse | |
| 75 | 117 | IRQ13 | Math Coprocessor | |
| 76 | 118 | IRQ14 | Primary IDE | |
| 77 | 119 | IRQ15 | Secondary IDE | |
| 78-7F | 120-127 | | Reserved by DOS | Same as Real Mode |
| 80-F0 | 128-240 | | Reserved for BASIC | Same as Real Mode |
| F1-FF | 241-255 | | Reserved by DOS | Same as Real Mode |

## PCI Interrupts

Interrupts on Peripheral Component Interconnect (PCI) Local Bus are optional and defined as “level sensitive,” asserted low (negative true), using open drain output drivers. The assertion and de-assertion of an interrupt line, INTx#, is asynchronous to CLK. A device asserts its INTx# line when requesting attention from its device driver. Once the INTx# signal is asserted, it remains asserted until the device driver clears the pending request. When the request is cleared, the device de-asserts its INTx# signal.

PCI defines one interrupt line for a single function device and up to four interrupt lines for a multifunction device or connector. For a single function device, only INTA# may be used while the other three interrupt lines have no meaning. Figure 2-1 on page 47 depicts the VMIVME-7765 interrupt logic pertaining to VME operations and the PMC site.

Any function on a multifunction device can be connected to any of the INTx# lines. The Interrupt Pin register defines which INTx# line the function uses to request an interrupt. If a device implements a single INTx# line, it is called INTA#; if it implements two lines, they are called INTA# and INTB#; and so forth. For a multifunction device, all functions may use the same INTx# line, or each may have its own (up to a maximum of four functions), or any combination thereof. A single function can never generate an interrupt request on more than one INTx# line.



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The slave PIC accepts the VME interrupts through lines that are defined by the BIOS. The BIOS defines which interrupt line to utilize depending on which system requires the use of the line.

## PCI Device Interrupt Map

The PCI bus-based external devices include the PMC sites, Ethernet controller and the PCI-to-VME bridge. The default BIOS maps these external devices to the PCI Interrupt Request (PIRQx) lines of the CSB5. This mapping is illustrated in Figure 2-1 on page 47 and is defined in Table 2-5.

The device PCI interrupt lines (INT0 through INT7) that are present on each device *cannot* be modified.

**Table 2-5** PCI Device Interrupt Mapping by the BIOS

| DEVICE | COMPONENT | PCI Bus | VENDOR ID | DEVICE ID | CPU ADDRESS MAP ID SELECT | PCI IRQ | Arbitration Request Line |
|---|---|---|---|---|---|---|---|
| PCI-to-VME Bridge | Tundra Universe IIB | 0 | 0x10E3 | 0x0000 | AD19 | INT0 | REQ0 |
| Timer / Watchdog FPGA | VMIC Proprietary | 0 | 0x114A | 0x0005 | AD20 | INT3 | N / A |
| PMC | N / A | 1 | N / A | N / A | AD31 | INT4-7 | REQ0 |
| Ethernet Controller 1 | Intel 82559ER | 0 | 0x8086 | 0x1209 | AD21 | INT1 | REQ1 |
| PCI Host Bridge | CNB30LE | 0 | 0x1166 | 0x0009 | N / A | N / A | N / A |
| VGA Controller | Chips&Technology 69030 | 0 | 0x102C | 0x0DC0 | AD23 | N / A | N / A |
| PCI-LPC Bridge | CSB5 | 0 | 0x1166 | 0x0230 | N / A | N / A | N / A |
| Secondary Host Bridge | CNB30LE | 0 | 0x1166 | 0x0009 Function 1 | N / A | N / A | N / A |
| USB Controller | CSB5 | 0 | 0x1166 | 0x0220 | N / A | N / A | N / A |
| South Bridge | CSB5 | 0 | 0x1166 | 0x0201 | N / A | N / A | N / A |
| Ethernet Controller 2 | Intel 82559ER | 0 | 0x8086 | 0x1209 | AD22 | INT2 | REQ2 |
| PCI-to-IDE Bridge | CSB5 | 0 | 0x1166 | 0x0212 | N / A | N / A | N / A |
| SCSI Controller A | LSI 53C1010 | 1 | 0x1000 | 0x0021 | AD29 | INT5 | REQ1 |
| SCSI Controller B | LSI 53C1010 | 1 | 0x1000 | 0x0021 | AD29 | INT6 | REQ1 |



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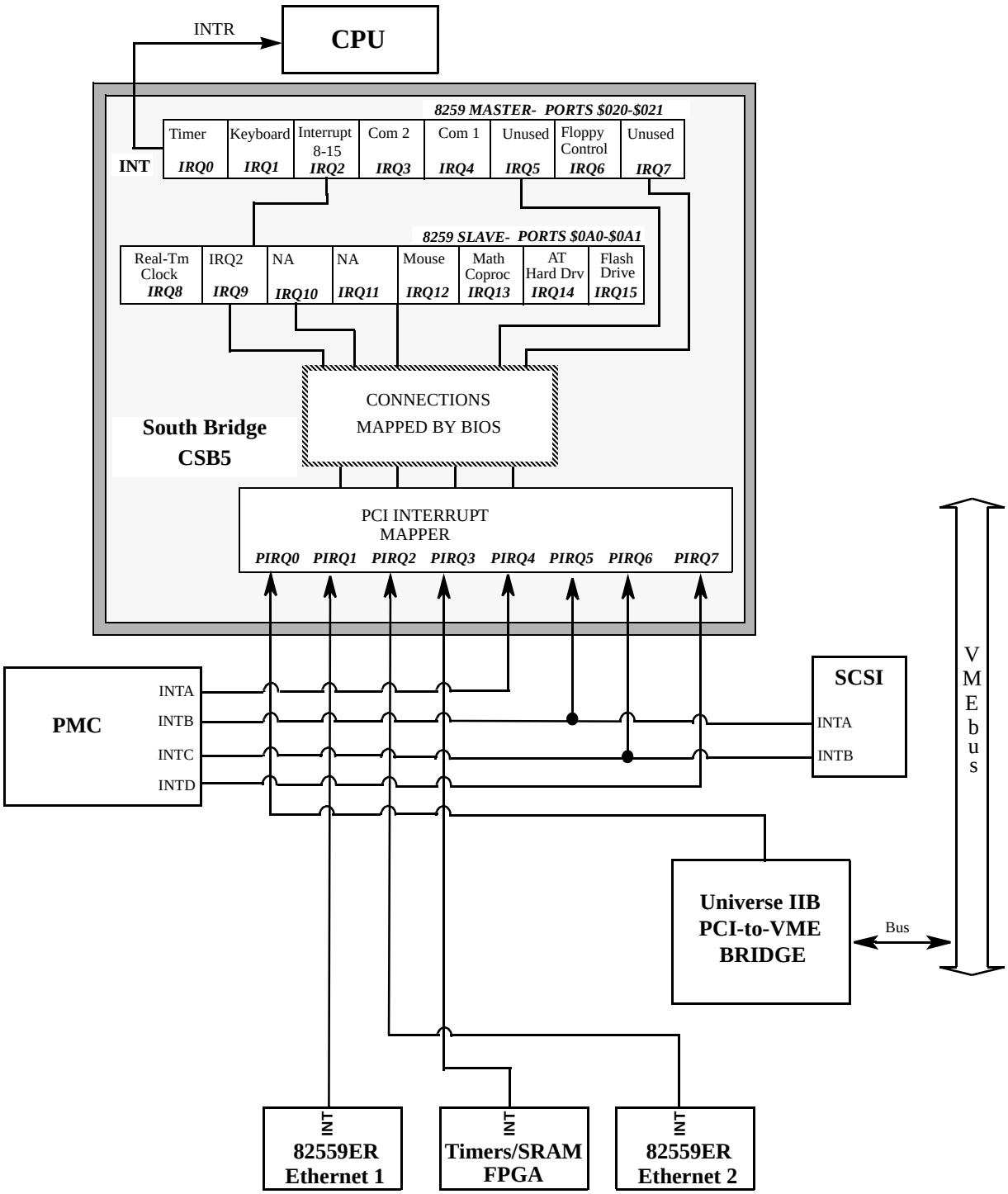



**Figure 2-1** Connections for the PC Interrupt Logic Controller



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The PCI-to-VME Bridge has the capability of generating a Non-Maskable Interrupt (NMI) via the PCI SERR# line. Table 2-6 describes the register bits that are used by the NMI. The SERR interrupt is routed through logic back to the NMI input line on the CPU. The CPU reads the NMI Status Control register to determine the NMI source (bits set to 1). After the NMI interrupt routine processes the interrupt, software clears the NMI status bits by setting the corresponding enable / disable bit to 1. The NMI Enable and Real-Time Clock register can mask the NMI signal and disable / enable all NMI sources.

**Table 2-6** NMI Register Bit Descriptions

| | |
|---|---|
| **Status Control Register (I/O Address $061, Read/Write, Read Only)** | |
| **Bit 7** | SERR# NMI Source Status (Read Only) - This bit is set to 1 if a system board agent detects a system board error. It then asserts the PCI SERR# line. To reset the interrupt, set Bit 2 to 0 and then set it to 1. When writing to port $061, Bit 7 must be 0. |
| **Bit 2** | PCI SERR# Enable (Read / Write) - 1 = Clear and Disable, 0 = Enable |
| **Enable and Real-Time Clock Address Register (I/O Address $070, Write Only)** | |
| **Bit 7** | NMI Enable - 1 = Disable, 0 = Enable |
| **Enable PCI SERR for NMI (I/O Address $C14)** | |
| **Bit 6** | 0 = Enable PCI SERR to generate NMI<br>1 = Disable |



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# I/O APIC Interrupts

While the standard ISA Compatible interrupt controller (located in the OSB4) is intended for use in a uni-processor system, the I/O Advanced Programmable Interrupt Controller (IOAPIC) can be used in either a uni-processor or multi-processor system. The IOAPIC provides multi-processor interrupt management and incorporates both static and dynamic symmetric interrupt distribution across all processors. In systems with multiple I/O subsystems, each subsystem can have its own set of interrupts.

In a multi-processor system, the IOAPIC's dedicated interrupt bus can reduce interrupt latency over the standard interrupt controller (i.e., the latency associated with the propagation of the interrupt acknowledge cycle across multiple buses using the standard interrupt controller approach). Interrupts can be controlled by the standard ISA Compatible interrupt controller in the OSB4, the IOAPIC unit or mixed mode where both the standard ISA Compatible Interrupt Controller and IOAPIC are used. The selection of which controller responds to an interrupt is determined by how the interrupt controllers are programmed. Note that it is the programmer's responsibility to make sure that the same interrupt input signal is not handled by both interrupt controllers.

At the system level, APIC consists of two parts; one residing in the I/O subsystem (called the IOAPIC) and the other in the CPU (called the Local APIC). The local APIC and the IOAPIC communicate over a dedicated APIC bus. The IOAPIC bus interface consists of two bi-directional data signals (APIC[1:0]) and a clock input (APICCLK).

The CPU's Local APIC Unit contains the necessary intelligence to determine whether or not its processor should accept interrupts broadcast on the APIC bus. The Local Unit provides local pending of interrupts, nesting and masking of interrupts, and handles all interactions with its local processor (e.g., the INT/INTA/EOI protocol). The Local Unit further provides inter-processor interrupts and a timer to its local processor. The register level interface of a processor to its local APIC is identical for every processor.

The IOAPIC Unit consists of a set of interrupt input signals, a 16-entry Interrupt Redirection Table, programmable registers, and a message unit for sending and receiving APIC messages over the APIC bus. I/O devices inject interrupts into the system by asserting one of the interrupt lines to the IOAPIC. The IOAPIC selects the corresponding entry in the Redirection Table and uses the information in that entry to format an interrupt request message. Each entry in the Redirection Table can be individually programmed to indicate edge/level sensitive interrupt signals, the interrupt vector and priority, the destination processor, and how the processor is selected (statically or dynamically). The information in the table is used to transmit a message to other APIC units (via the APIC bus).



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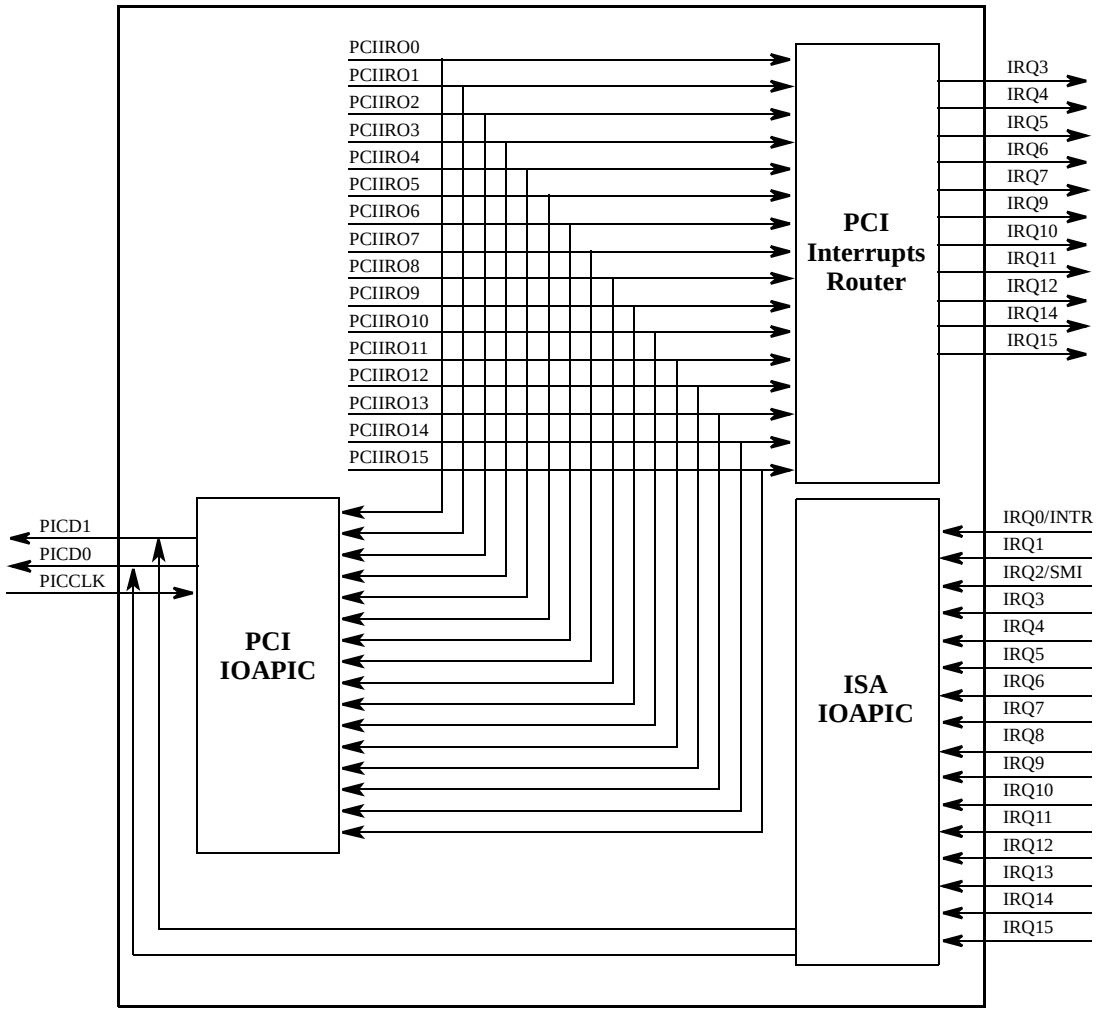



**Figure 2-2** Extended APIC Configuration



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## Integrated Peripherals

The VMIVME-7765 incorporates a National Semiconductor Super I/O (SIO) chip. The SIO located on the main board provides the VMIVME-7765 with a standard floppy drive controller, two 16550 UART-compatible serial ports, keyboard and mouse ports and general purpose I/O for system monitoring functions. Both serial port signals are available from the front panel. The floppy signals are available via the VME backplane connectors and can be accessed with the appropriate transition utility board (VMIACC-0562). A parallel port is provided via the front panel.

The IDE interface is provided by the CSB5 South Bridge chip. The IDE interface supports two channels known as the primary and secondary channels. The secondary channel is routed on-board to a compact flash socket. The primary channel is routed out the VME backplane and is supported by a VMIVME-7452 Hard Drive card, along with a VMIVME-7455 CD ROM card. The VMIACC-0562 transition utility board, also available from VMIC, terminates into a standard 40-pin header. This channel can support two drives, a master and slave. The IDE interface on the VMIVME-7765 supports ATA-33, ATA-66 and ATA-100 drives and automatically determines the proper operating mode based on the type of drive used. In order to properly function in the ATA-100 mode, a special 80 conductor cable must be used instead of the standard 40 conductor cable. This cable is typically available from the ATA-100 drive manufacturer.



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## Ethernet Controllers

The dual network capability is provided by two Intel 82559ER Ethernet Controllers. Both Ethernet controllers are PCI-based and are software configurable. The VMIVME-7765 supports dual 10BaseT and 100BaseTx Ethernet.

### 10BaseT

A network based on the 10BaseT standard uses unshielded twisted-pair cables, providing an economical solution to networking by allowing the use of existing telephone wiring and connectors. The RJ-45 connector is used with the 10BaseT standard. 10BaseT has a maximum length of 100 meters.

### 100BaseTx

The VMIVME-7765 also supports 100BaseTx Ethernet. A network based on a 100BaseTx standard uses unshielded twisted-pair cables and a RJ-45 connector. 100BaseTx has a maximum length of 100 meters.

### LANWorks

The VMIVME-7765 supports booting on LAN1 using LANWorks Ethernet BIOS. LAN2 cannot be used for remote booting. Refer to Appendix D for more information on remote Ethernet booting.



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## Video Graphics Adapter

The SVGA port on the VMIVME-7765 is controlled by the Chips and Technology 69030 graphics chip with 4 Mbyte video DRAM. The 69030 is hardware and BIOS compatible with the industry EGA and SVGA standards supporting both VESA high-resolution and extended video modes. Table 2-7 shows the graphics video modes supported by the video controller.

**Table 2-7** Supported Graphics Video Resolutions

| SCREEN RESOLUTION | MAXIMUM COLORS | REFRESH RATES (Hz) |
|---|---|---|
| 640 x 480 | 16 M | 60, 75, 85 |
| 800 x 600 | 16 M | 60, 75, 85 |
| 1024 x 768 | 16 M | 60, 75*, 85* |
| 1280 x 1024 | 16 M | 60*, 75*, 85* |
| 1600 x 1200 | 64 K | 60* |

*May exhibit objectionable ghosting

Not all SVGA monitors support resolutions and refresh rates beyond 640 x 480 at 85 Hz. Do not attempt to drive a monitor to a resolution or refresh rate beyond its capability.



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## Universal Serial Bus

The VMIVME-7765 provides a dual Universal Serial Bus (USB) connection on the front panel. The on-board USB controllers completely support the standard USB interface.

The USB Host Controller moves data between system memory and the USB by processing and scheduling data structures. The controller executes the scheduled lists, and reports status back to the system.

**NOTE:** Default CMOS settings of the VMIVME-7765 have USB functions disabled. This allows more interrupts and less Interrupt Latency for Real Time systems. If USB is enabled, be aware that Interrupt Sharing and Latency will be effected.



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# Dual Ultra 160 SCSI

The VMIVME-7765's dual 160 SCSI interface makes the unit ideal for embedded applications, particularly applications where standard hard drives and floppy disk drives cannot be used.

The VMIVME-7765 Dual-Channel Ultra160 SCSI Host Adapter incorporates the Symbios SYM53C1010, a highly integrated PCI Dual-Channel Ultra160 SCSI controller. The SYM53C1010 is 100 percent compatible with the Ultra160 SCSI initiative and provides additional features that ensure robust Ultra160 system operation. Fast SCSI, Ultra SCSI, Ultra2 SCSI and Ultra160 SCSI are all supported by the SYM53C1010. Double transition clocking enables throughput of up to 160 Mbytes on each channel for a total of 320 Mbytes, without increasing the interface clock rate.

The SYM53C1010 uses the same CRC algorithm used by FDDI, Ethernet and Fibre Channel, and detects single bit errors, double bit errors, odd number of errors, and all burst errors up to 32 bits long. To provide complete end-to-end protection of the SCSI I/O, AIP protects all non-data phases, augmenting the CRC feature of Ultra160. SureLINK domain validation technology detects the configuration of the SCSI bus and automatically tests and adjusts the SCSI transfer rate to optimize inter-operability. The SYM53C1010 controller and Ultra160 provide Basic (Level 1) and Enhanced (Level 2) domain validation, while the SYM53C1010 has an added feature of Margining (Level 3) domain validation.

## PCI Interface

The Ultra160 SCSI PCI Interface complies with *PCI Local Bus Specification Revision 2.2*, and implements a 32-bit/33 MHz PCI bus. The SYM53C1010 is a true PCI multi-function device in that it presents one electrical load to the PCI bus. It uses one REQ/-GNT/pair to arbitrate for PCI bus mastership, and separate interrupt signals are generated for SCSI Function A and SCSI Function B for maximum performance. The SYM53C1010 complies with *PCI Power Management Interface Specification Revision 1.1* and *PC 99*, supporting power states D0, D1, D2, D3hot and D3cold, power management capabilities registers, and programmable values for PCI Subsystem Vendor ID and Subsystem ID. Extended access cycles (Memory Read Line, Memory Read Multiple, and Memory Write and Invalidate) are also supported.

## Ultra160 SCSI Memory

The SYM53C1010 is located within the system BIOS. A serial 2-wire interface on each SCSI channel provides a connection to an external serial EEPROM for storing the Subsystem Vendor ID and Subsystem ID.



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## Ultra160 SCSI Processor

The SYM53C1010 provides two independent Ultra160 SCSI controllers on a single chip. Each controller supports wide Ultra160 SCSI synchronous transfer rates up to 160 Mbytes on a LVD SCSI bus. Integrated LVDlink transceivers support both LVD and single-ended signals with no external transceivers required. Fast SCSI, Ultra SCSI, Ultra2 SCSI and Ultra160 SCSI are all supported by the SYM53C1010. An on-chip SCSI clock quadrupler allows the chip to achieve Ultra160 SCSI transfer rates with an input frequency of 40 MHz. The 8 Kbytes of internal RAM per channel for SCRIPTS instruction storage allow all accesses to remain internal, reducing the time spent on the PCI bus. A 944-byte DMA FIFO on each channel allows the device to efficiently burst up to 512 bytes across the PCI bus. SCSI bus phase mismatches are handled in SCRIPTS, reducing CPU utilization.

## Ultra160 SCSI Termination

All SCSI buses require a termination network at each end to function properly. Specific termination requirements differ, depending on which types of SCSI devices are present on the bus. The SCSI Host Adapter uses the UCC5630A termination ICs to automatically sense the SCSI bus and switch the termination to either single ended (SE) or low voltage differential (LVD) SCSI, dependent on which type of devices are connected to the bus. The UCC5630A termination IC is used in multi-mode active termination applications, where SE and LVD devices might coexist. The UCC5630A has both SE and LVD termination networks integrated into a single monolithic component. The correct network is automatically determined by the SCSI bus “DIFSENS” signal. The SCSI bus DIFSENS signal line is used to identify which types of SCSI devices are present on the bus. On power-up, the UCC5630A DIFSENS drivers will attempt to deliver 1.3V to the DIFSENS line.

If only LVD devices are present, the DIFSENS line will be successfully driven to 1.3 V and the terminators will configure for LVD operation. If any single ended devices are present, they will present a short to ground on the DIFSENS line, signaling the UCC5630A(s) to configure into the SE mode, accommodating the SE devices. Or, if any high voltage differential (HVD) devices are present, the DIFSENS line is pulled high and the terminator will enter a high impedance state, effectively disconnecting from the bus.

## Media Connection

The VMIVME-7765 supports dual 68-pin VHDCI external connectors via J5 of the expansion board.



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CHAPTER 3

# Embedded PC/RTOS Features

## Contents


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## Introduction

VMIC's VMIVME-7765 features additional capabilities beyond those of a typical desktop computer system. The unit provides four software-controlled, general-purpose timers along with a programmable Watchdog Timer for synchronizing and controlling multiple events in embedded applications. The VMIVME-7765 also provides a bootable Flash Disk system, and it supports an embedded intelligent VME bridge to allow compatibility with the most demanding VME applications. These features make the unit ideal for embedded applications, particularly where standard hard drives and floppy disk drives cannot be used. The VMIVME-7765 also supports $I^2C$ by integrating specialized circuitry for these functions.



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## VMEbus Bridge

In addition to its PC / AT functions, the VMIVME-7765 has the following VMEbus features:

- Complete six-line Address Modifier (AM-Code) programmability
- VME data interface with separate hardware byte / word swapping for master and slave accesses
- Support for VME64 multiplexed MBLT 64-bit VMEbus block transfers
- User-configured interrupter
- User-configured interrupt handler
- System Controller mode with programmable VMEbus arbiter (PRI, SGL and RRS modes are supported)
- VMEbus BERR bus error timer (software programmable)
- Slave access from the VMEbus to local RAM and mailbox registers
- Full-featured programmable VMEbus requester (ROR, RWD and BCAP modes are supported)
- System Controller auto detection
- Complete VMEbus master access through five separate Protected-mode memory windows

The VMIVME-7765 VMEbus interface is provided by the PCI-to-VMEbus bridge built around the Tundra Semiconductor Corporation Universe II VMEbus interface chip. The Universe II provides a reliable high-performance 64-bit VMEbus-to-PCI interface in one design. The functions and programming of the Universe-based VMEbus interface are addressed in detail in a companion manual titled: *VMIC's Tundra Universe II Based VMEbus Interface Product Manual (500-000211-000).*



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# Embedded PCI Functions

The VMIVME-7765 provides non-volatile RAM (NVRAM), Timers and a Watchdog Timer via the PCI bus. These functions are required for embedded and real time applications. The PCI configuration space of these embedded functions are shown below.

**Table 3-1** PCI Configuration Space Registers

| 31 | 24 | 23 | 16 | 15 | 08 | 07 | 00 | Register Address |
|---|---|---|---|---|---|---|---|---|
| Device ID 0005 | | | | Vendor ID 114A | | | | 00h |
| Status | | | | Command | | | | 04h |
| Class Code | | | | | | | Revision ID | 08h |
| BIST | | Header Type | | Latency Timer | | | Cache Line Size | 0Ch |
| PCI Base Address 0 for Memory-Mapped VME Control registers (BAR0) | | | | | | | | 10h |
| PCI Base Address 2 for memory-mapped Watchdog and other timers (BAR2) | | | | | | | | 14h |
| Reserved | | | | | | | | 18h |
| Reserved | | | | | | | | 1Ch |
| Reserved | | | | | | | | 20h |
| Reserved | | | | | | | | 24h |
| Reserved | | | | | | | | 28h |
| Subsystem ID 7765 | | | | Subsystem Vendor ID 114A | | | | 2Ch |
| Reserved | | | | | | | | 30h |
| Reserved | | | | | | | | 34h |
| Reserved | | | | | | | | 38h |
| Max_Lat | | Min_gnt | | Interrupt Pin | | | Interrupt Line | 3Ch |

The “Device ID” field indicates that the device is for VME products (05) and indicates the supported embedded feature set.

The “Vender ID” and “Subsystem Vendor ID” fields indicate VMIC’s PICMG assigned Vender ID (114A).

The “Subsystem ID” field indicates the model number of the product (7765).



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## VME Control Registers

The VMEbus Control Registers, located at BAR0 of the PCI Configuration Space, contain registers that are used to configure and control Endian conversion settings, VMEbus error conditions and VMEbus SYSFAIL in relation to the Watchdog Timer. Register definitions are shown below in Table 3-2.

**Table 3-2** Register Definitions Offset From BAR0

| **Register Name** | **Offset** | |
|---|---|---|
| VMECOMM | 0x00 | |
| **Bit Name** | **Bit** | **Definition** |
| MEC_SEL | 0 | Master big-endian enable bit 1=Big Endian 0=Little Endian bit |
| SEC_SEL | 1 | Slave Big-Endian enable bit 1=Big Endian 0=Little Endian |
| ABLE | 2 | Auxiliary BERR logic enable bit 1=Aux. BERR enabled 0=Aux. BERR disabled |
| BTO | 3 | Bus error timer enabled 1=enabled 0=disabled |
| BTOV [1:0] | 5:4 | Timeout value |
| | | 00 - 16uS |
| | | 01 - 64uS |
| | | 10 -256uS |
| | | 11 - 1.00mS |
| BERRI | 6 | BERR interrupt enable 1=Interrupt enabled 0=Interrupt disabled |
| BERRST | 7 | BERR status read / clear bit 1=Clear BERR status 0=Do nothing |
| SFENA | 8 | Enables generation of VME SYSFAIL upon WDT timeout 1= enable SYSFAIL generation 0=disable |
| Unused | 9 | Not Used |
| ECENA | 10 | Endian conversion bit 1= enabled 0=disabled |
| BPENA | 11 | Endian conversion bypass bit 1=Bypass 0=Not bypassed |
| Unused | 31:12 | Not Used |



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**Table 3-2** Register Definitions Offset From BAR0 (Continued)

| Register Name | Offset | |
|---|---|---|
| **VBAR** | **0x04** | |
| VME_ADDR | All | Latched VME Address on BERR |
| **VBAM** | **0x08** | |
| VME_ADDR | 5:0 | Latched VME Address Modifier on BERR |
| Unused | 31:6 | Not Used |
| SEC_SEL | 0x001 | |



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# Timers

## General

The VMIVME-7765 provides four user-programmable timers (two 16-bit and two 32-bit) which are completely dedicated to user applications and are not required for any standard system function. Each timer is clocked by independent generators with selectable rates of 2MHz, 1MHz, 500kHz and 250kHz. Each timer may be independently enabled and each is capable of generating a system interrupt on timeout.

Events can be timed by either polling the timers or enabling the interrupt capability of the timer. A status register allows for application software to determine which timer is the cause of any interrupt.

## Timer Control Status Register 1 (TCSR1)

The timers are controlled and monitored via the Timer Control Status Register 1 (TCSR1) located at offset 0x00 from the address in BAR2. The mapping of the bits in this register are as follows:

**Table 3-3** Timer Control Status Register 1

| Field | Bits | Read or Write |
|---|---|---|
| Timer 1 Caused IRQ | TCSR1[0] | R/W |
| Timer 1 Enable | TCSR1[1] | R/W |
| Timer 1 IRQ Enable | TCSR1[2] | R/W |
| Timer 1 Clock Select | TCSR1[4..3] | R/W |
| Timer 2 Caused IRQ | TCSR1[8] | R/W |
| Timer 2 Enable | TCSR1[9] | R/W |
| Timer 2 IRQ Enable | TCSR1[10] | R/W |
| Timer 2 Clock Select | TCSR1[12..11] | R/W |
| Timer 3 Caused IRQ | TCSR1[16] | R/W |
| Timer 3 Enable | TCSR1[17] | R/W |
| Timer 3 IRQ Enable | TCSR1[18] | R/W |
| Timer 3 Clock Select | TCSR1[20..19] | R/W |
| Timer 4 Caused IRQ | TCSR1[24] | R/W |
| Timer 4 Enable | TCSR1[25] | R/W |
| Timer 4 IRQ Enable | TCSR1[26] | R/W |
| Timer 4 Clock Select | TCSR1[28..27] | R/W |
| Reserved | All Other Bits | R/W |

*All of these bits default to "0" after system reset.*



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Each timer has an independently selectable clock source which is selected by the bit pattern in the “Timer x Clock Select” field as follows:

**Table 3-4** Timer Clock Select

| Clock Rate | MSb | LSb |
|---|---|---|
| 2MHz | 0 | 0 |
| 1MHz | 0 | 1 |
| 500kHz | 1 | 0 |
| 250kHz | 1 | 1 |

Each timer can be independently enabled by writing a “1” to the appropriate “Timer x Enable” field. Similarly, the generation of interrupts by each timer can be independently enabled by writing a “1” to the appropriate “Timer x IRQ Enable” field.

If an interrupt is generated by a timer, the source of the interrupt may be determined by reading the “Timer x Caused IRQ” fields. If the field is set to “1”, then the respective timer caused the interrupt. Note that multiple timers can cause a single interrupt. Therefore, the status of all timers must be read to ensure that all interrupt sources are recognized.

A particular timer interrupt can be cleared by writing a “0” to the appropriate “Timer x Caused IRQ” field. Alternately, a write to the appropriate Timer x IRQ Clear (TxIC) register will also clear the interrupt. When clearing the interrupt using the “Timer x Caused IRQ” fields, note that it is important to ensure that a proper bit mask is used so that other register settings are not affected. The preferred method for clearing interrupts is to use the “Timer x IRQ Clear” registers described on page 66 and 67.

## Timer Control Status Register 2 (TCSR2)

The timers are also controlled by bits in the Timer Control Status Register 2 (TCSR2) located at offset 0x04 from the address in BAR2. The mapping of the bits in this register are as follows:

| Field | Bits | Read or Write |
|---|---|---|
| Read Latch Select | TCSR2[0] | R/W |
| Reserved | All Other Bits | R/W |

*All of these bits default to “0” after system reset.*



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The “Read Latch Select” bit is used to select the latching mode of the programmable timers (See “Timers” section on page 62). If this bit is set to “0”, then each timer output is latched upon a read of any one of its addresses. For example, a read to the TMRCCR12 register latches the count of timers 1 and 2. A read to the TMRCCR3 register latches the count of timer 3. This continues for every read to any one of these registers. As a result, it is not possible to capture the values of all four timers at a given instance in time. However, by setting this bit to “1”, all four timer outputs will be latched only on reads to the Timer 1 & 2 Current Count Register (TMRCCR12). Therefore, to capture the current count of all four timers at the same time, perform a read to the TMRCCR12 first (with a 32-bit read), followed by a read to TMRCCR3 and TMRCCR4. The first read (to the TMRCCR12 register) causes all four timer values to be latched at the same time. The subsequent reads to the TMRCCR3 and TMRCCR4 registers do not latch new count values, allowing the count of all timers at the same instance in time to be obtained.

## Timer 1 & 2 Load Count Register (TMRLCR12)

Timers 1 & 2 are 16-bits wide and obtain their load count from the Timer 1 & 2 Load Count Register (TMRLCR12), located at offset 0x10 from the address in BAR2. The mapping of bits in this register are as follows:

| Field | Bits | Read or Write |
|---|---|---|
| Timer 2 Load Count | TMRLCR12[31..16] | R/W |
| Timer 1 Load Count | TMRLCR12[15..0] | R/W |

When either of these fields are written (either by a single 32-bit write or separate 16-bit writes), the respective timer is loaded with the written value on the next rising edge of the timer clock, regardless of whether the timer is enabled or disabled. The value stored in this register is also automatically reloaded on terminal count (or timeout) of the timer.

## Timer 3 Load Count Register (TMRLCR3)

Timer 3 is 32-bits wide and obtains its load count from the Timer 3 Load Count Register (TMRLCR3), located at offset 0x14 from the address in BAR2. The mapping of bits in this register are as follows:

| Field | Bits | Read or Write |
|---|---|---|
| Timer 3 Load Count | TMRLCR3[31..0] | R/W |



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When this field is written, Timer 3 is loaded with the written value on the next rising edge of the timer clock, regardless of whether the timer is enabled or disabled. The value stored in this register is also automatically reloaded on terminal count (or timeout) of the timer.

## Timer 4 Load Count Register (TMRLCR4)

Timer 4 is 32-bits wide and obtains its load count from the Timer 4 Load Count Register (TMRLCR4), located at offset 0x18 from the address in BAR2. The mapping of bits in this register are as follows:

| Field | Bits | Read or Write |
|---|---|---|
| Timer 4 Load Count | TMRLCR4[31..0] | R/W |

When this field is written, Timer 4 is loaded with the written value on the next rising edge of the timer clock, regardless of whether the timer is enabled or disabled. The value stored in this register is also automatically reloaded on terminal count (or timeout) of the timer.

## Timer 1 & 2 Current Count Register (TMRCCR12)

The current count of timers 1 & 2 may be read via the Timer 1 & 2 Current Count Register (TMRCCR12), located at offset 0x20 from the address in BAR2. The mapping of bits in this register are as follows:

| Field | Bits | Read or Write |
|---|---|---|
| Timer 2 Count | TMRCCR12[31..16] | Read Only |
| Timer 1 Count | TMRCCR12[15..0] | Read Only |

When either field is read, the current count value is latched and returned. There are two modes that determine how the count is latched depending on the setting of the "Read Latch Select" bit in the WDT Control Status Register (CSR2). See the CSR2 register description for more information on these two modes.

## Timer 3 Current Count Register (TMRCCR3)

The current count of Timer 3 may be read via the Timer 3 Current Count Register (TMRCCR3), located at offset 0x24 from the address in BAR2. The mapping of bits in this register are as follows:

| Field | Bits | Read or Write |
|---|---|---|
| Timer 3 Count | TMRCCR3[31..0] | Read Only |



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When this field is read, the current count value is latched and returned. There are two modes that determine how the count is latched depending on the setting of the "Read Latch Select" bit in the WDT Control Status Register (CSR2). See the CSR2 register description for more information on these two modes.

## Timer 4 Current Count Register (TMRCCR4)

The current count of Timer 4 may be read via the Timer 4 Current Count Register (TMRCCR4), located at offset 0x28 from the address in BAR2. The mapping of bits in this register are as follows:

| Field | Bits | Read or Write |
|---|---|---|
| Timer 4 Count | TMRCCR4[31..0] | Read Only |

When this field is read, the current count value is latched and returned. There are two modes that determine how the count is latched depending on the setting of the "Read Latch Select" bit in the WDT Control Status Register (CSR2). See the CSR2 register description for more information on these two modes.

## Timer 1 IRQ Clear (T1IC)

The Timer 1 IRQ Clear (T1IC) register is used to clear an interrupt caused by Timer 1. Writing to this register, located at offset 0x30 from the address in BAR2, causes the interrupt from Timer 1 to be cleared. This can also be done by writing a "0" to the appropriate "Timer x Caused IRQ" field of the timer Control Status Register (CSR1). This register is write only and the data written is irrelevant.

## Timer 2 IRQ Clear (T2IC)

The Timer 2 IRQ Clear (T2IC) register is used to clear an interrupt caused by Timer 2. Writing to this register, located at offset 0x34 from the address in BAR2, causes the interrupt from Timer 2 to be cleared. This can also be done by writing a "0" to the appropriate "Timer x Caused IRQ" field of the timer Control Status Register (CSR1). This register is write only and the data written is irrelevant.

## Timer 3 IRQ Clear (T3IC)

The Timer 3 IRQ Clear (T3IC) register is used to clear an interrupt caused by Timer 3. Writing to this register, located at offset 0x38 from the address in BAR2, causes the interrupt from Timer 3 to be cleared. This can also be done by writing a "0" to the appropriate "Timer x Caused IRQ" field of the timer Control Status Register (CSR1). This register is write only and the data written is irrelevant.



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## Timer 4 IRQ Clear (T4IC)

The Timer 4 IRQ Clear (T4IC) register is used to clear an interrupt caused by Timer 4. Writing to this register, located at offset 0x3C from the address in BAR2, causes the interrupt from Timer 4 to be cleared. This can also be done by writing a “0” to the appropriate “Timer x Caused IRQ” field of the timer Control Status Register (CSR1). This register is write only and the data written is irrelevant.



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# Watchdog Timer

## General

The VMIVME-7765 provides a programmable Watchdog Timer (WDT) which can be used to reset the system if software integrity fails.

## WDT Control Status Register (WCSR)

The WDT is controlled and monitored by the WDT Control Status Register (WCSR) which is located at offset 0x08 from the address in BAR2. The mapping of the bits in this register are as follows:

| Field | Bits | Read or Write |
|---|---|---|
| SERR / RST Select | WCSR[16] | R / W |
| WDT Timeout Select | WCSR[10..8] | R / W |
| WDT Enable | WCSR[0] | R / W |

*All of these bits default to "0" after system reset. All other bits are reserved.*

The "WDT Timeout Select" field is used to select the timeout value of the Watchdog Timer as follows:

| Timeout | WCSR[10] | WCSR[9] | WCSR[8] |
|---|---|---|---|
| 135s | 0 | 0 | 0 |
| 33.6s | 0 | 0 | 1 |
| 2.1s | 0 | 1 | 0 |
| 524ms | 0 | 1 | 1 |
| 262ms | 1 | 0 | 0 |
| 131ms | 1 | 0 | 1 |
| 32.768ms | 1 | 1 | 0 |
| 2.048ms | 1 | 1 | 1 |

The "SERR / RST Select" bit is used to select whether the WDT generates an SERR# on the local PCI bus or a system reset. If this bit is set to "0", the WDT will generate a system reset. Otherwise, the WDT will make the local PCI bus SERR# signal active.

The "WDT Enable" bit is used to enable the Watchdog Timer function. This bit must be set to "1" in order for the Watchdog Timer to function.



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**NOTE:** As all registers default to zero after reset, the Watchdog Timer is always disabled after a reset. The Watchdog Timer must be re-enabled by the application software after reset in order for the Watchdog Timer to continue to operate.

Once the Watchdog Timer is enabled, the application software must refresh the Watchdog Timer within the selected timeout period to prevent a reset or SERR# from being generated. The Watchdog Timer is refreshed by performing a write to the WDT Keepalive register (WKPA). The data written is irrelevant.

## WDT Keepalive Register (WKPA)

When enabled, the Watchdog Timer is prevented from resetting the system by writing to the WDT Keepalive Register (WKPA) located at offset 0x0C from the address in BAR2 within the selected timeout period. The data written to this location is irrelevant.



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# Local IDE Disks

The VMIVME-7765 features an optional on-board Compact Flash and / or rotating hard drive mass storage system. The Flash Disk appears to the user as an intelligent ATA (IDE) disk drive with the same functionality and capabilities as a “rotating media” IDE hard drive. The VMIVME-7765 BIOS includes an option to allow the board to boot from any IDE device.

## Configuration

The Flash Disk and hard drive reside on the same VMIVME-7765 secondary IDE bus. The default setting in the Phoenix BIOS ‘STANDARD CMOS SETUP’ screen is the ‘AUTO’ setting. In the Phoenix BIOS ‘PERIPHERAL SETUP’ screen, the secondary PCI IDE interface must be enabled for these disks to be functional. Refer to Appendix C for additional details.

Figure 3-1 maps the configuration possibilities for a typical system consisting of the VMIVME-7765 with a resident Flash Disk, a hard drive attached to the Primary IDE interface, and a floppy drive attached to the floppy interface via the VMIACC-0562.

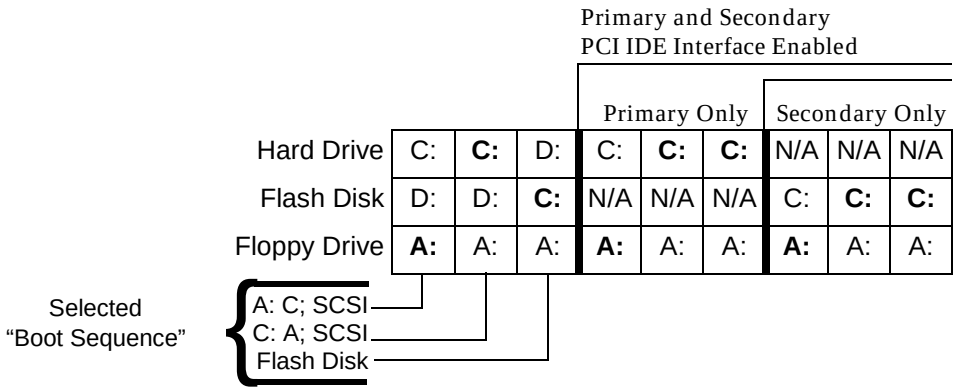



**Figure 3-1** Typical System Configuration

The Primary and Secondary PCI IDE Interfaces are controlled (enabled or disabled) in the Integrated Peripheral Setup screen of the Phoenix BIOS. The First Boot Device is selected in the BIOS Features Setup screen.

Figure 3-1 identifies the drive letter assigned to each physical device, and indicates in bold lettering the device booted from in each configuration, using devices that are bootable. A bootable device is one on which an operating system has been installed, or formatted as a system disk using MS-DOS.



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## Functionality

The Flash Disk performs identically to a standard IDE hard drive. Reads and writes to the device are performed using the same methods, utilizing DOS command line entries or the file managers resident in the chosen operating system.

### Advanced Configuration

The previous discussion is based on using the IDE disk devices formatted as one large partition per device. Some applications may require the use of multiple partitions. The following discussion of these partitions includes special procedures that must be followed to create multiple partitions on the VMIVME-7765 IDE disk devices (including the resident Flash Disk).

Partitions may be either a primary or an extended partition. An extended partition may be subdivided farther into logical partitions. Each device may have up to four main partitions; one of which may be an extended partition. However, if multiple primary partitions are created, only one partition may be active at a time. Data in the non-active partitions is not accessible.

Following the creation of the partitioning scheme, the partitions can be formatted to contain the desired file system.

As discussed earlier, a typical system consists of the VMIVME-7765 with its resident Flash Disk configured as the Secondary IDE device, a hard drive attached to the Primary IDE interface, and a floppy drive attached to the floppy interface.

Using this configuration, it may be desirable to have a logical drive on either IDE device, configured as a bootable drive. This allows the selection of the first boot device via the Advanced CMOS Setup screen. Using this capability, a user could have a system configured with multiple operating systems that would be selectable by assigning the IDE logical drive as the boot device.

The DOS utility FDISK is commonly used to configure the partition structure on a hard drive. Comments on the following page pertain to partitioning efforts using FDISK.

---

**CAUTION:** Deleting a partition will erase all the data previously stored in that partition.

---

The Flash Disk will be configured as a single partition device as delivered from the factory. The following sample sequence illustrates a proven method for creating two 8 Mbyte partitions, with one as an active primary partition. Take note of the instructions to exit FDISK. This has been shown to be an important step in a successful partitioning effort.

1. Power up the VMIVME-7765 and enter the CMOS set-up.
2. Set IDE HDD Master to “Not Installed”.



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3. Set Flash Disk Master to “AUTO”.
4. Set boot device to floppy.
5. Boot DOS from the floppy, and verify that the System Configuration Screen shows only the Flash Disk.
6. Run FDISK.
7. Delete all current partitions (any data currently stored in the partitions will be lost).
8. Exit FDISK (this will cause a reboot), then run FDISK again.
9. Create an 8 Mbyte primary partition.
10. Create an 8 Mbyte extended partition.
11. Set-up a logical device for the 8 Mbyte extended partition.
12. Set the Primary partition as an active partition.
13. Exit FDISK.

If an operating system has been installed on the Flash Disk that modifies the Master Boot Record (MBR), the following steps are required to rewrite the MBR for DOS.

14. Run FDISK/MBR.
15. Run FORMAT C: (use the extension /s option if you want the Flash Disk as a bootable DOS device).
16. Format D: (this is only required if two partitions were created).
17. Reset the CPU and enter the CMOS set-up.
18. Set Primary Master to “AUTO”.
19. Set boot device to desired boot source.

Drive letter assignments for a simple system are illustrated in Figure 3-1 on page 70. Understanding the order the operating system assigns drive letters is necessary for these multiple partition configurations. The operating system assigns drive letter C to the active primary partition on the first hard disk (the boot device). Drive D is assigned to the first recognized primary partition on the next hard disk. The operating system will continue to assign drive letters to the primary partitions in an alternating fashion between the two drives. The next logical partitions will be assigned drive letters starting on the first hard drive, lettering each logical device sequentially, until all are assigned a drive letter. The system will then perform the same sequential lettering of each logical partition on the second hard disk.

**NOTE:** Drive letter changes caused by adding an additional drive or changing the initial partitioning scheme may cause difficulties with an operating system installed prior to the changes. Plan your configuration prior to installing the operating system to minimize difficulties.



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# Remote Ethernet Booting

The VMIVME-7765 is capable of booting from a server using either LAN1 or LAN 2 utilizing Lanworks BootWare BIOS. The BootWare BIOS gives you the ability to remotely boot the VMIVME-7765 using a variety of network protocols. The Ethernet must be connected through the LAN front panel (RJ-45) connectors to boot remotely. This feature allows users to create systems without the worry of disk drive reliability, or the extra cost of adding Flash drives.

## BootWare Features

- Netware (802.1, 802.3 or EthII), TCP/IP (DHCP or BootP), RPL and PXE boot support
- Unparalleled boot sector virus protection
- Detailed boot configuration screens
- Comprehensive diagnostics
- Optional disabling of local boots
- Dual-boot option lets users select network or local booting



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CHAPTER

4

# Maintenance

If a VMIC product malfunctions, please verify the following:

1. Software resident on the product
2. System configuration
3. Electrical connections
4. Jumper or configuration options
5. Boards are fully inserted into their proper connector location
6. Connector pins are clean and free from contamination
7. No components or adjacent boards were disturbed when inserting or removing the board from the chassis
8. Quality of cables and I/O connections

If products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return**.

VMIC Customer Service is available at: 1-800-240-7782.
Or E-mail us at customer.service@vmic.com

## Maintenance Prints

User level repairs are not recommended. The drawings and diagrams in this manual are for reference purposes only.



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Appendix

A

# Connector Pinouts

## Contents


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## Introduction

The VMIVME-7765 VMEbus SBC has several connectors for its I/O ports. Wherever possible, the VMIVME-7765 uses connectors and pinouts typical for any desktop PC. This ensures maximum compatibility with a variety of systems.

Connector diagrams in this appendix are generally shown in a natural orientation with the controller board mounted in a VMEbus chassis.



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# VMEbus Connector Pinouts

Figure A-1 shows the location of the VMEbus P1 and P2 connectors and their orientation on the VMIVME-7765. Table A-1 shows the pin assignments for the VMEbus connectors on the main board. Table A-2 on page 79 shows the pin assignments for the VMEbus connectors on the expansion board. Note that only Row B of connector P2 should be bussed across the backplane; all other pins on P2 are reserved for VMIC transition cards (VMIACC-0561 and VMIACC-0562).

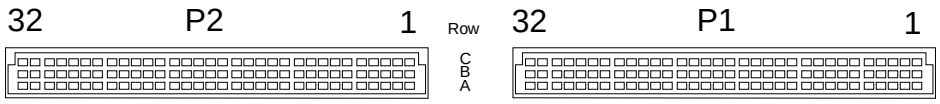



**Figure A-1** VMEbus Connector Diagram

**Table A-1** VMEbus Connector Pinout (Main Board)

| PIN # | P1 ROW A SIGNAL | P1 ROW B SIGNAL | P1 ROW C SIGNAL | P2 ROW A SIGNAL | P2 ROW B SIGNAL | P2 ROW C SIGNAL |
|---|---|---|---|---|---|---|
| 1 | D00 | BBSY | D08 | CBL_DETECT | +5 V | IDE RST# |
| 2 | D01 | BCLR | D09 | DDP8 | GND | DDP7 |
| 3 | D02 | ACFAIL | D10 | DDP9 | Reserved | DDP6 |
| 4 | D03 | BG0IN | D11 | DDP10 | A24 | DDP5 |
| 5 | D04 | BG0OUT | D12 | DDP11 | A25 | DDP4 |
| 6 | D05 | BG1IN | D13 | DDP12 | A26 | DDP3 |
| 7 | D06 | BG1OUT | D14 | DDP13 | A27 | DDP2 |
| 8 | D07 | BG2IN | D15 | DDP14 | A28 | DDP1 |
| 9 | GND | BG2OUT | GND | DDP15 | A29 | DDP0 |
| 10 | SYSCLK | BG3IN | SYSFAIL | IDE REQ0 | A30 | IOCS1.64# |
| 11 | GND | BG3OUT | BERR | IDE IOW0 # | A31 | GND |
| 12 | DS1 | BR0 | SYSRESET | IDE IOR0 # | GND | GND |
| 13 | DS0 | BR1 | LWORD | IDE IORDY0# | +5 V | GND |
| 14 | WRITE | BR2 | AM5 | GND | D16 | IDESELA |
| 15 | GND | BR3 | A23 | GND | D17 | IDE DACK0# |
| 16 | DTACK | AM0 | A22 | GND | D18 | IDE IRQ0 |
| 17 | GND | AM1 | A21 | DAP1 | D19 | DAP 2 |



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**Table A-1** VMEbus Connector Pinout (Main Board) (Continued)

| PIN # | P1 ROW A SIGNAL | P1 ROW B SIGNAL | P1 ROW C SIGNAL | P2 ROW A SIGNAL | P2 ROW B SIGNAL | P2 ROW C SIGNAL |
|---|---|---|---|---|---|---|
| 18 | AS | AM2 | A20 | IDECS01 # | D20 | DAP 0 |
| 19 | GND | AM3 | A19 | GND | D21 | IDE CS03# |
| 20 | IACK | GND | A18 | DRATE0 | D22 | REDWC |
| 21 | IACKIN | SERCLK | A17 | DASP | D23 | INDEX# |
| 22 | IACKOUT | SERDAT | A16 | DRVSB # | GND | MOTEA# |
| 23 | AM4 | GND | A15 | GND | D24 | DRVSA# |
| 24 | A07 | IRQ7 | A14 | GND | D25 | MOTEB# |
| 25 | A06 | IRQ6 | A13 | GND | D26 | STEP# |
| 26 | A05 | IRQ5 | A12 | GND | D27 | WDATA# |
| 27 | A04 | IRQ4 | A11 | GND | D28 | TRK# |
| 28 | A03 | IRQ3 | A10 | GND | D29 | RDATA# |
| 29 | A02 | IRQ2 | A09 | DSKCHG # | D30 | SIDE1# |
| 30 | A01 | IRQ1 | A08 | GND | D31 | DIR |
| 31 | -12 V | NC | +12 V | VCC | GND | WGATE |
| 32 | +5 V | +5 V | +5 V | VCC | +5 V | WPT |

**Table A-2** VMEbus Connector Pinout (Expansion Board)

| PIN # | P1 ROW A SIGNAL | P1 ROW B SIGNAL | P1 ROW C SIGNAL | P2 ROW A SIGNAL | P2 ROW B SIGNAL | P2 ROW C SIGNAL |
|---|---|---|---|---|---|---|
| 1 | NC | NC | NC | NC | +5 V | NC |
| 2 | NC | NC | NC | NC | GND | NC |
| 3 | NC | NC | NC | NC | NC | NC |
| 4 | NC | BG0 | NC | NC | NC | NC |
| 5 | NC | BG0 | NC | NC | NC | NC |
| 6 | NC | BG1 | NC | NC | NC | NC |
| 7 | NC | BG1 | NC | NC | NC | NC |
| 8 | NC | BG2 | NC | NC | NC | NC |



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**Table A-2** VMEbus Connector Pinout (Expansion Board) (Continued)

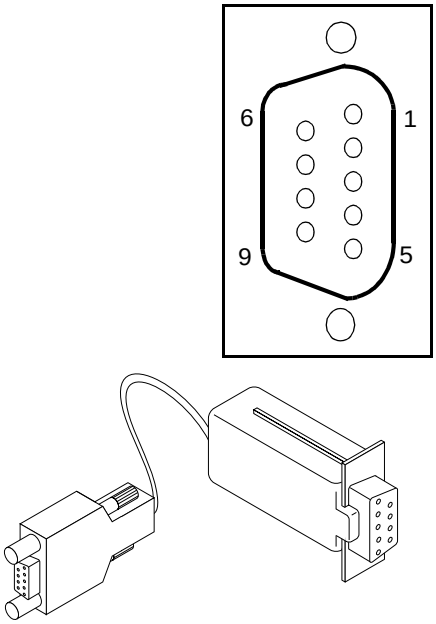
| PIN # | P1 ROW A SIGNAL | P1 ROW B SIGNAL | P1 ROW C SIGNAL | P2 ROW A SIGNAL | P2 ROW B SIGNAL | P2 ROW C SIGNAL |
|---|---|---|---|---|---|---|
| 9 | NC | BG2 | NC | NC | NC | NC |
| 10 | NC | BG3 | NC | NC | NC | NC |
| 11 | NC | BG3 | NC | NC | NC | NC |
| 12 | NC | NC | NC | NC | GND | NC |
| 13 | NC | NC | NC | NC | +5 V | NC |
| 14 | NC | NC | NC | NC | NC | NC |
| 15 | NC | NC | NC | NC | NC | NC |
| 16 | NC | NC | NC | NC | NC | NC |
| 17 | NC | NC | NC | NC | NC | NC |
| 18 | NC | NC | NC | NC | NC | NC |
| 19 | NC | NC | NC | NC | NC | NC |
| 20 | NC | GND | NC | NC | NC | NC |
| 21 | NC | NC | NC | NC | NC | NC |
| 22 | NC | NC | NC | NC | GND | NC |
| 23 | NC | GND | NC | NC | NC | NC |
| 24 | NC | NC | NC | NC | NC | NC |
| 25 | NC | NC | NC | NC | NC | NC |
| 26 | NC | NC | NC | NC | NC | NC |
| 27 | NC | NC | NC | NC | NC | NC |
| 28 | NC | NC | NC | NC | NC | NC |
| 29 | NC | NC | NC | NC | NC | NC |
| 30 | NC | NC | NC | NC | NC | NC |
| 31 | NC | NC | NC | NC | GND | NC |
| 32 | NC | +5 V | NC | NC | +5 V | NC |



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## Serial Connector Pinout (P107)

Each standard RS-232 serial port connector is a Microminiature D9 male as shown in Figure A-2. Adapters to connect standard D9 serial peripherals to the board are available. Please refer to the product specification sheet for ordering information.

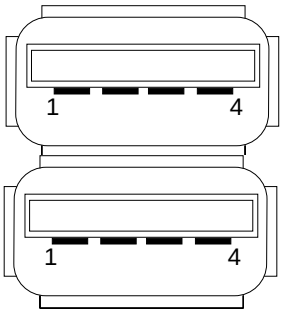



| COM 1 and COM 2 SERIAL PORT CONNECTORS | | | |
|---|---|---|---|
| **D9 PIN** | **DIR** | **RS-232 SIGNAL** | **FUNCTION** |
| 1 | In | DCD | Data Carrier Detect |
| 2 | In | RX | Receive Data |
| 3 | Out | TX | Transmit Data |
| 4 | Out | DTR | Data Terminal Ready |
| 5 | | GND | Signal Ground |
| 6 | In | DSR | Data Set Ready |
| 7 | Out | RTS | Request to Send |
| 8 | In | CTS | Clear to Send |
| 9 | In | RI | Ring Indicator |
| Shield | | | Chassis Ground |

**Figure A-2** Serial Connector Pinouts

## USB Connector (J45 and J46)

The dual USB port uses an industry-standard dual 4-position shielded connector. Figure A-3 shows the pinout of the dual USB connector.




| USB1 & 2 CONNECTOR | | |
|---|---|---|
| **PIN** | **SIGNAL** | **FUNCTION** |
| 1 | USBV | USB Power |
| 2 | USB- | USB Data - |
| 3 | USB+ | USB Data + |
| 4 | USBG | USB Ground |

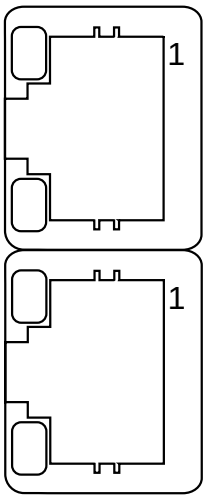
**Figure A-3** USB Connector Pinout



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## Ethernet Connector Pinout (J11)

The pinout diagram for the Ethernet 10BaseT and 100BaseTx connector is shown in Figure A-4.




| ETHERNET CONNECTOR (10BaseT, 100BaseTx) | | |
|---|---|---|
| **PIN** | **Signal Name** | |
| 1 | TD+ | Transmit Data |
| 2 | TD- | Transmit Data |
| 3 | RD+ | Receive Data |
| 4 | TX_CT_OUT | Transmit Center Tap Out |
| 5 | TX_CT_OUT | Transmit Center Tap Out |
| 6 | RD- | Receive Data |
| 7 | RX_CT_OUT | Receive Center Tap Out |
| 8 | RX_CT_OUT | Receive Center Tap Out |

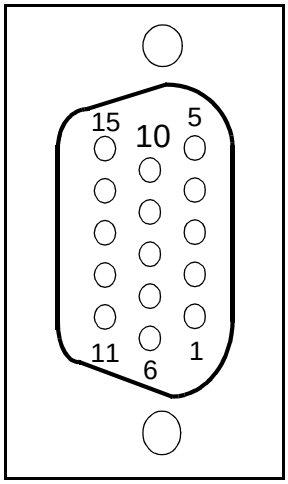
**Figure A-4** Ethernet Connector and Pinout



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# Video Connector Pinout (J13)

The video port uses a standard high-density DB15 SVGA connector. Figure A-5 illustrates the pinout.




| VIDEO CONNECTOR | | |
|---|---|---|
| **PIN** | **DIRECTION** | **FUNCTION** |
| 1 | Out | Red |
| 2 | Out | Green |
| 3 | Out | Blue |
| 4 | | Reserved |
| 5 | | Ground |
| 6 | | Ground |
| 7 | | Ground |
| 8 | | Ground |
| 9 | | +5V |
| 10 | | Ground |
| 11 | | Reserved |
| 12 | I/O | DDC Data |
| 13 | Out | Horizontal Sync |
| 14 | Out | Vertical Sync |
| 15 | I/O | DDC Clock |
| Shield | | Chassis Ground |

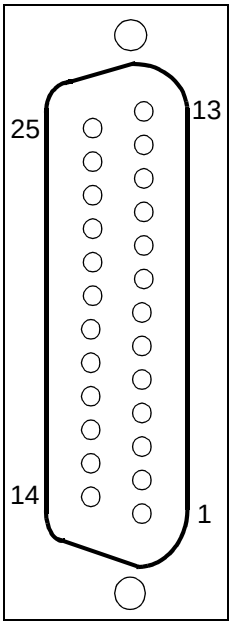
**Figure A-5** Video Connector Pinout



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## Parallel Port Connector Pinout (P108)

The parallel port shown in Figure A-6 uses a micro DB25 female connector typical of any PC / AT system.




| PARALLEL PORT CONNECTOR | | |
|---|---|---|
| **PIN** | **DIRECTION** | **FUNCTION** |
| 1 | In / Out | Data Strobe |
| 2 | In / Out | Bidirectional Data D0 |
| 3 | In / Out | Bidirectional Data D1 |
| 4 | In / Out | Bidirectional Data D2 |
| 5 | In / Out | Bidirectional Data D3 |
| 6 | In / Out | Bidirectional Data D4 |
| 7 | In / Out | Bidirectional Data D5 |
| 8 | In / Out | Bidirectional Data D6 |
| 9 | In / Out | Bidirectional Data D7 |
| 10 | In | Acknowledge |
| 11 | In | Device Busy |
| 12 | In | Out of Paper |
| 13 | In | Device Selected |
| 14 | Out | Auto Feed |
| 15 | In | Error |
| 16 | Out | Initialize Device |
| 17 | In | Device Ready for Input |
| 18 | | Signal Ground |
| 19 | | Signal Ground |
| 20 | | Signal Ground |
| 21 | | Signal Ground |
| 22 | | Signal Ground |
| 23 | | Signal Ground |
| 24 | | Signal Ground |
| 25 | | Signal Ground |
| Shield | | Chassis Ground |

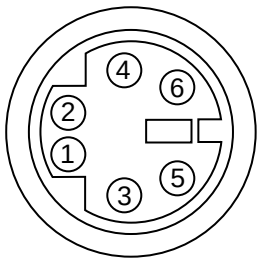
**Figure A-6** Parallel Port Connector Pinout



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# Keyboard and Mouse Connectors and Pinout (J41)

The keyboard and mouse connectors are standard 6-pin female mini-DIN PS/2 connectors as shown in Figure A-7 and Table A-3.




| Keyboard/Mouse Connector* | | |
|---|---|---|
| **Pin** | **Dir** | **Function** |
| 1 | In/Out | Mouse Data |
| 2 | In/Out | Keyboard Data |
| 3 | | Ground |
| 4 | | +5 V |
| 5 | Out | Mouse Clock |
| 6 | Out | Keyboard Clock |
| Shield | | Chassis Ground |
| *An adapter cable is included with the VMIVME-7765 to separate the keyboard and mouse connector. | | |

**Figure A-7** Keyboard/Mouse Connector and Pinout



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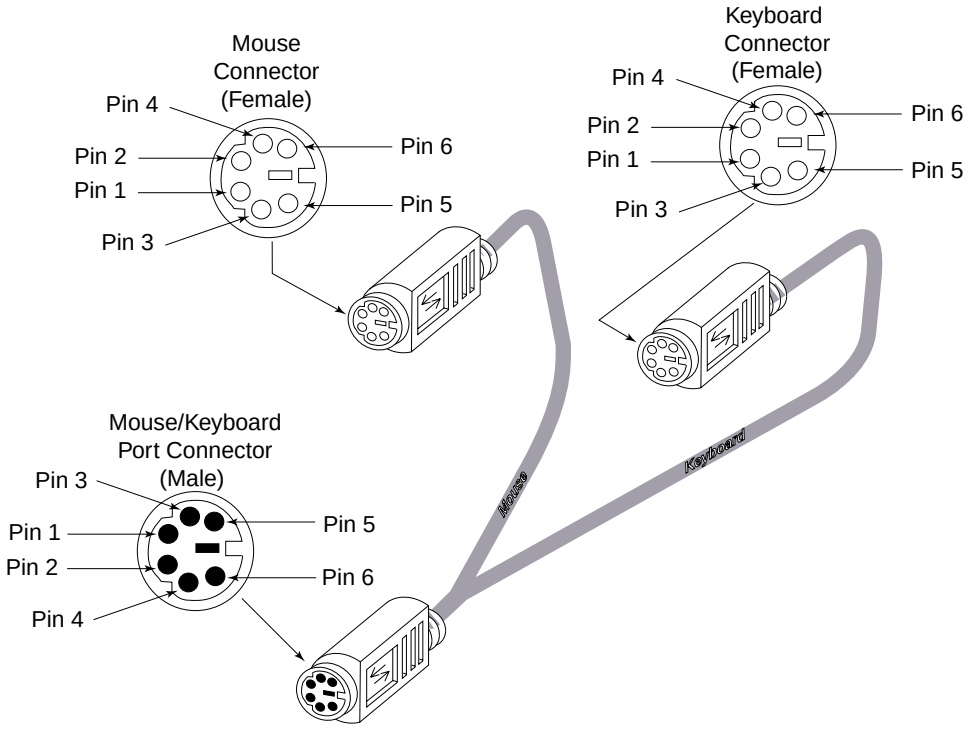



**Table A-3** Keyboard/Mouse Y Splitter Cable

| Keyboard | | | Mouse | | |
|---|---|---|---|---|---|
| **Pin** | **Dir** | **Function** | **Pin** | **Dir** | **Function** |
| 1 | In / Out | Keyboard Data | 1 | In / Out | Mouse Data |
| 2 | | Unused | 2 | | Keyboard Data |
| 3 | | Ground | 3 | | Ground |
| 4 | | +5 V | 4 | | +5 V |
| 5 | Out | Keyboard Clock | 5 | Out | Mouse Clock |
| 6 | | Unused | 6 | | Keyboard Clock |
| Shield | | Chassis Ground | Shield | | Chassis Ground |

**NOTE:** The cable shown is a PS / 2 IBM Thinkpad cable (part number 360-000153-000).



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# PMC Connector Pinouts

## PMC (J6) Connector and Pinout

The PCI Mezzanine Card (PMC) carries the same signals as the PCI standard; however, the PMC standard uses a completely different form factor. Tables A-4 through A-6 are the pinouts for the PMC connectors (J6, J2 and J7).

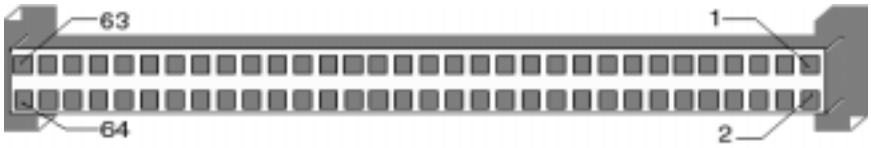



**Table A-4** PMC #1 (J6) Connector Pinout

| PMC Connector (J6) | | | | PMC Connector (J6) | | | |
|---|---|---|---|---|---|---|---|
| Left Side | | Right Side | | Left Side | | Right Side | |
| Pin | Name | Pin | Name | Pin | Name | Pin | Name |
| 1 | GND | 2 | -12 | 33 | FRAME# | 34 | GND |
| 3 | GND | 4 | INTA# | 35 | GND | 36 | IRDY# |
| 5 | INTB# | 6 | INTC# | 37 | DEVSEL# | 38 | +5 V |
| 7 | BMODE1A | 8 | +5 V | 39 | GND | 40 | LOCK# |
| 9 | INTD# | 10 | NC | 41 | SDONE# | 42 | NC |
| 11 | GND | 12 | NC | 43 | PAR | 44 | GND |
| 13 | CLK | 14 | GND | 45 | +5 V | 46 | AD[15] |
| 15 | GND | 16 | GNT# | 47 | AD[12] | 48 | AD[11] |
| 17 | REQ# | 18 | +5 V | 49 | AD[9] | 50 | +5 V |
| 19 | +5 V | 20 | AD[31] | 51 | GND | 52 | C/BE0# |
| 21 | AD[28] | 22 | AD[27] | 53 | AD[6] | 54 | AD[5] |
| 23 | AD[25] | 24 | GND | 55 | AD[4] | 56 | GND |
| 25 | GND | 26 | C/BE3# | 57 | +5 V | 58 | AD[3] |
| 27 | AD[22] | 28 | AD[21] | 59 | AD[2] | 60 | AD[1] |
| 29 | AD[19] | 30 | +5 V | 61 | AD[0] | 62 | +5 V |
| 31 | +5 V | 32 | AD[17] | 63 | GND | 64 | REQ64# |



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## PMC (J2) Connector and Pinout

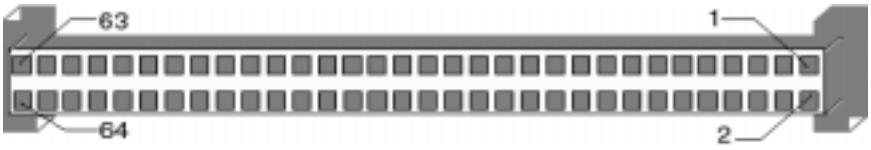



**Table A-5** PMC #1 (J2) Connector Pinout

| PMC Connector (J2) | | | | PMC Connector (J2) | | | |
|---|---|---|---|---|---|---|---|
| Left Side | | Right Side | | Left Side | | Right Side | |
| Pin | Name | Pin | Name | Pin | Name | Pin | Name |
| 1 | +12 V | 2 | +5 V | 33 | GND | 34 | NC |
| 3 | GND | 4 | NC | 35 | TRDY | 36 | +3.3 V |
| 5 | +5 V | 6 | GND | 37 | GND | 38 | STOP# |
| 7 | GND | 8 | NC | 39 | PERR# | 40 | GND |
| 9 | NC | 10 | NC | 41 | +3.3 V | 42 | SERR# |
| 11 | PRSNT2 | 12 | +3.3 V | 43 | C/BE1# | 44 | GND |
| 13 | RST# | 14 | GND | 45 | AD[14] | 46 | AD[13] |
| 15 | +3.3 V | 16 | GND | 47 | GND | 48 | AD[10] |
| 17 | NC | 18 | GND | 49 | AD[8] | 50 | +3.3 V |
| 19 | AD[30] | 20 | AD[29] | 51 | AD[7] | 52 | NC |
| 21 | GND | 22 | AD[26] | 53 | +3.3 V | 54 | NC |
| 23 | AD[24] | 24 | +3.3 V | 55 | NC | 56 | GND |
| 25 | IDSEL | 26 | AD[23] | 57 | NC | 58 | NC |
| 27 | +3.3 V | 28 | AD[20] | 59 | GND | 60 | NC |
| 29 | AD[18] | 30 | GND | 61 | ACK64# | 62 | +3.3 V |
| 31 | AD[16] | 32 | C/BE2# | 63 | GND | 64 | NC |



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## PMC (J7) Connector and Pinout

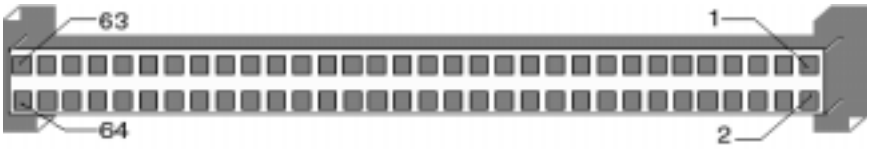



**Table A-6** PMC J7 Connector Pinout

| PMC Connector | | | | PMC Connector | | | |
|---|---|---|---|---|---|---|---|
| Left Side | | Right Side | | Left Side | | Right Side | |
| Pin | Name | Pin | Name | Pin | Name | Pin | Name |
| 1 | N/C | 2 | GND | 33 | GND | 34 | AD[48] |
| 3 | GND | 4 | C/BE7# | 35 | AD[47] | 36 | AD[46] |
| 5 | C/BE6# | 6 | C/BE5# | 37 | AD[45] | 38 | GND |
| 7 | C/BE4# | 8 | GND | 39 | +3.3V | 40 | AD[44] |
| 9 | +3.3V | 10 | PAR[64] | 41 | AD[43] | 42 | AD[42] |
| 11 | AD[63] | 12 | AD[62] | 43 | AD[41] | 44 | GND |
| 13 | AD[61] | 14 | GND | 45 | GND | 46 | AD[40] |
| 15 | GND | 16 | AD[60] | 47 | AD[39] | 48 | AD[38] |
| 17 | AD[59] | 18 | AD[58] | 49 | AD[37] | 50 | GND |
| 19 | AD[57] | 20 | GND | 51 | GND | 52 | AD[36] |
| 21 | +3.3V | 22 | AD[56] | 53 | AD[35] | 54 | AD[34] |
| 23 | AD[55] | 24 | AD[54] | 55 | AD[33] | 56 | GND |
| 25 | AD[53] | 26 | GND | 57 | +3.3V | 58 | AD[32] |
| 27 | GND | 28 | AD[52] | 59 | N/C | 60 | N/C |
| 29 | AD[51] | 30 | AD[50] | 61 | N/C | 62 | GND |
| 31 | AD[49] | 32 | GND | 63 | GND | 64 | N/C |



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## SCSI Pinout (J8)

The Dual Ultra 160 SCSI devices use a high density connector AMP-787962-1. The pinout for this connector is shown below.

**Table A-7** J8 SCSI Pinout

| Channel A External | | | | Channel B External | | | |
|---|---|---|---|---|---|---|---|
| **Pin** | **Signal** | **Pin** | **Signal** | **Pin** | **Signal** | **Pin** | **Signal** |
| 1A | A_SD(12)+ | 2A | A_SD(13)+ | 1B | B_SD(12)+ | 2B | B_SD(13)+ |
| 3A | A_SD(14)+ | 4A | A_SD(15)+ | 3B | B_SD(14)+ | 4B | B_SD(15)+ |
| 5A | A_SDP1+ | 6A | A_SD(0)+ | 5B | B_SDP1+ | 6B | B_SD(0)+ |
| 7A | A_SD(1)+ | 8A | A_SD(2)+ | 7B | B_SD(1)+ | 8B | B_SD(2)+ |
| 9A | A_SD(3)+ | 10A | A_SD(4)+ | 9B | B_SD(3)+ | 10B | B_SD(4)+ |
| 11A | A_SD(5)+ | 12A | A_SD(6)+ | 11B | B_SD(5)+ | 12B | B_SD(6)+ |
| 13A | A_SD(7)+ | 14A | A_SDP0+ | 13B | B_SD(7)+ | 14B | B_SDP0+ |
| 15A | GND | 16A | A_DIFFSEN | 15B | GND | 16B | B_DIFFSEN |
| 17A | A_TERMPWR_EX | 18A | A_TERMPWR_EX | 17B | B_TERMPWR_EX | 18B | B_TERMPWR_EX |
| 19A | N/C | 20A | GND | 19B | N/C | 20B | GND |
| 21A | A_SATN+ | 22A | GND | 21B | B_SATN+ | 22B | GND |
| 23A | A_SBSY+ | 24A | A_SACK+ | 23B | B_SBSY+ | 24B | B_SACK+ |
| 25A | A_SRST+ | 26A | A_SMSG+ | 25B | B_SRST+ | 26B | B_SMSG+ |
| 27A | A_SSEL+ | 28A | A_SC_D+ | 27B | B_SSEL+ | 28B | B_SC_D+ |
| 29A | A_SREQ+ | 30A | A_SI_O+ | 29B | B_SREQ+ | 30B | B_SI_O+ |
| 31A | A_SD(8)+ | 32A | A_SD(9)+ | 31B | B_SD(8)+ | 32B | B_SD(9)+ |
| 33A | A_SD(10)+ | 34A | A_SD(11)+ | 33B | B_SD(10)+ | 34B | B_SD(11)+ |
| 35A | A_SD(12)- | 36A | A_SD(13)- | 35B | B_SD(12)- | 36B | B_SD(13)- |
| 37A | A_SD(14)- | 38A | A_SD(15)- | 37B | B_SD(14)- | 38B | B_SD(15)- |
| 39A | A_SDP1- | 40A | A_SD(0)- | 39B | B_SDP1- | 40B | B_SD(0)- |
| 41A | A_SD(1)- | 42A | A_SD(2)- | 41B | B_SD(1)- | 42B | B_SD(2)- |
| 43A | A_SD(3)- | 44A | A_SD(4)- | 43B | B_SD(3)- | 44B | B_SD(4)- |
| 45A | A_SD(5)- | 46A | A_SD(6)- | 45B | B_SD(5)- | 46B | B_SD(6)- |



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**Table A-7** J8 SCSI Pinout (Continued)

| Channel A External | | | |
|---|---|---|---|
| **Pin** | **Signal** | **Pin** | **Signal** |
| 47A | A_SD(7)- | 48A | A_SDP0- |
| 49A | GND | 50A | NC |
| 51A | A_TERMPWR_EX | 52A | A_TERMPWR_EX |
| 53A | N/C | 54A | GND |
| 55A | A_SATN- | 56A | GND |
| 57A | A_SBSY- | 58A | A_SACK- |
| 59A | A_SRST- | 60A | A_SMSG- |
| 61A | A_SSEL- | 62A | A_SC_D- |
| 63A | A_SREQ- | 64A | A_SI_0- |
| 65A | A_SD(8)- | 66A | A_SD(9)- |
| 67A | A_SD(10)- | 68A | A_SD(11)- |

| Channel B External | | | |
|---|---|---|---|
| **Pin** | **Signal** | **Pin** | **Signal** |
| 47B | B_SD(7)- | 48B | B_SDP0- |
| 49B | GND | 50B | NC |
| 51B | B_TERMPWR_EX | 52B | B_TERMPWR_EX |
| 53B | N/C | 54B | GND |
| 55B | B_SATN- | 56B | GND |
| 57B | B_SBSY- | 58B | B_SACK- |
| 59B | B_SRST- | 60B | B_SMSG- |
| 61B | B_SSEL- | 62B | B_SC_D- |
| 63B | B_SREQ- | 64B | B_SI_0- |
| 65B | B_SD(8)- | 66B | B_SD(9)- |
| 67B | B_SD(10)- | 68B | B_SD(11)- |



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Appendix

B

# System Driver Software

## Contents


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## Introduction

The VMIVME-7765 provides high-performance video and Local Area Network (LAN) access by means of the video and LAN chipsets. The dual-channel Ultra 160 SCSI is accessed by means of on-board PCI-based adapters and associated software drivers. The two LAN adapters can be configured to allow the VMIVME-7765 access to two separate, physical networks. Each LAN adapter is capable of running 10BaseT and 100BaseTx. Ultra 160 SCSI is provided by an LSI (Symbios) 53C1010 SCSI controller chip.

To optimize performance of each of these PCI-based subsystems, install the driver software located on the distribution CD-ROM provided with the unit. Detailed instructions for installation of the drivers during the installation of Microsoft Windows NT 4.0 and Windows 2000 operating systems are provided in the following sections.



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# Driver Software Installation

In order to properly use the Video, LAN and SCSI adapters of the VMIVME-7765, the user must install the driver software located on the distribution CD-ROM provided with the unit.

## SCSI Driver Preparation

The SCSI drivers for both Windows 2000 and Windows NT 4.0 are contained on the distribution CD-ROM (385-000067-000). Before attempting to use these drivers to load an operating system on a SCSI device, they must be copied to a user supplied floppy disk. For Windows 2000, browse to the directory \SCSI\2000\. Copy all files and directories under \SCSI\2000\ to the floppy disk. For Windows NT 4.0, browse to \SCSI\NT40\. Copy all files and directories under \SCSI\NT40\ to the floppy disk.



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# Windows 2000

1. Follow the normal Windows 2000 installation manual.
2. After installing Windows 2000, and rebooting the computer, install the 69030 driver. Please read license.txt before continuing (win_drivers / win2k / license.txt).
3. Double click '**My Computer**' icon.
4. Double click on the **Control Panel** folder.
5. Double click the **System** icon.
6. Click on **Hardware** tab.
7. Click the **Device Manager** button.
8. Under **Other Devices** right click on **Video Controller** and select **Uninstall**.
9. Click **OK** and close the **Device Manager**.
10. Click **OK** to close system properties with changes.
11. Close all windows, and reboot your system.
12. After Windows reboots, the **Found New Hardware** wizard will appear. Click **Next**.
13. Insert CD-ROM **385-000067-000**.
14. Select **Search For A Suitable Driver For My Device** and click **Next**.
15. On the **Locate Drivers Files**, specify location by selecting **Browse**, browse to your CD-ROM drive then to the **Display** folder and click **Next**.
16. Select **OEMSETUP** and click **Open**.
17. When the hardware wizard is displayed click **OK** (the path to OEMSET should be displayed in the **Copy Manufacturers Files From** box).
18. The **Driver Files Search Results** dialog box will now display **Chips & Technologies 69030 AGP/PCI**.
19. Click next and complete driver installation.

## Windows 2000 82559ER Driver Installation

After installing Windows 2000 as described above, install the Ethernet drivers. To install the Ethernet drivers you must make a floppy disk to contain the files.

1. Place a blank floppy disk in drive A, then browse to the **Ethernet** folder on the VMIC distribution CD-ROM.
2. Double click **makedisk.bat**. This will format the floppy disk and copy files necessary for Ethernet drivers installation.



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3. Open **My Computer**, then open **Control Panel**.
4. From the control panel, open **System** and select the **Hardware** tab.
5. Click on the **Device Manager** button.
6. Right click **Ethernet Controller** within the **Network Adapters** menu and select **Properties**.
7. Choose **Reinstall Drivers** to start the upgrade device driver wizard.
8. Select **Next** to continue.
9. Ensure **Search For Suitable Driver For My Device** is selected, then click **Next**.
10. Click in the box next to **Floppy Disk Drives** and ensure the disk you created in steps 1 and 2 is inserted in the floppy drive, then click **Next**.
11. The **Drivers File Search Results** window should identify **A:\NET559ER.int** as the driver it found. Select **Next** to continue.
12. The **Digital Signature Not Found** box indicates this is not a Microsoft driver. Select **Yes** to continue.
13. After the files have been copied, select **Finish** to complete the driver installation.
14. You must now close the **Driver Manager** window, remove the floppy disk from the drive and reboot the system for the changes to take affect.
15. This process must be completed for both Ethernet adapters, 1 and 2.

## Windows 2000 Installation with SCSI Devices

**NOTE:** In order to use SCSI devices with Windows 2000, the SCSI drivers must be copied to a floppy as described in the previous section “SCSI Driver Preparation” on page 94. If Windows 2000 is to be loaded on a SCSI device, then the device should be listed first in the Boot Device List in the CMOS Setup Boot screen.

1. When booting Windows 2000 from the installation CD, you will be prompted to press F6 to install SCSI or other mass storage devices. Press F6 at this time.
2. The installation will then prompt the user to specify additional mass storage devices. Press S in response to the prompt.
3. Insert the SCSI Driver floppy into drive A when requested by the installation prompt. Press ENTER.
4. The **SymBIOS Ultra 3 PCI SCSI Driver** will be selected. Press ENTER to confirm the selection and continue with the Windows 2000 installation.



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## Windows NT (Version 4.0)

Windows NT 4.0 includes drivers for the on-board Ethernet and video adapters. The following steps are required to configure the Ethernet adapter for operation. To install the Ethernet drivers you must make a floppy disk to contain the files.

1. Place a blank floppy disk in drive A, then browse to the **Ethernet** folder on the VMIC distribution CD-ROM 385-000067-000.
2. Double click **makedisk.bat**. This will format the floppy disk and copy files necessary for Ethernet drivers installation.

---

**NOTE:** If installing Windows NT 4.0 with SCSI devices, see "Windows NT 4.0 Installation with SCSI Devices" on page 98.

---

3. Follow the normal Windows NT 4.0 installation until you reach the **Windows NT Workstation Setup** window which states that **Windows NT Needs To Know How This Computer Should Participate On A Network**.
4. Click on the button next to **This Computer Will Participate On A Network**.
5. Click on the box next to **Wired To The Network** and click **Next**.
6. Click the **Select From List** button.
7. Click the **Have Disk** button.
8. Insert the disk you created in steps 1 and 2 into drive **A**.
9. Click **OK**.
10. In the **Select OEM Option**, choose **Intel GD82559ER Fast Ethernet Adapter**, then click **OK**.
11. Select the above entry on the displayed list, click **Next**.
12. Select the protocol you prefer, click **Next**.
13. Click **Next** to install selected components.
14. Click **Next** to start the network connection.
15. Step through the remaining screens, providing the data pertinent to your network.
16. Continue through the setup procedure until the **Detected Display** window appears, click **OK** to continue.
17. In the **Display Properties** window, click **Test**.

---

**NOTE:** Windows NT 4.0 does not allow the selection of the Intel video drivers during initial setup.

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If the display test is successful, click **OK** to continue. If the display test is not successful, you may have to adjust the display parameter to find a functional setting, for example a lower resolution or lower number of colors.

18. Continue with the procedure to the **Windows NT Setup** window. Click **Restart Computer**.
19. When the computer reboots, double-click **My Computer** window.
20. Double-click the **Control Panel** icon in the **My Computer** window.
21. Double-click the **Display** icon in the **Control Panel** window.
22. Select the **Settings** tab in the **Display Properties** window, then click the **Display Type** button.
23. In the **Display Type** window, click **Change**.
24. In the **Change Display** window, click **Have Disk**.
25. Insert the VMIC drivers CD-ROM 385-000067-000 into the CD-ROM drive**.**
26. Click **OK**.
27. Browse to \win_drivers\display\winnt.
28. **Chips Video Accelerators** will be displayed in the **Change Display** window. Click **OK**.
29. Proceed as directed, removing the CD-ROM from the CD-ROM drive. Restart the computer to activate the new settings. When the system reboots, the **Invalid Display Settings** screen will be displayed. Click **OK**.
30. On the **Display Properties** screen click on **Settings**, then click **Test**.
31. The **Testing Mode** screen will be displayed. Click **OK**. If the bitmap test image is displayed correctly, click **OK**.

The unit should now be configured for operation under Windows NT 4.0.

## Windows NT 4.0 Installation with SCSI Devices

**NOTE:** In order to use SCSI devices with Windows NT 4.0, the SCSI drivers must be copied to a floppy as described in the previous section “SCSI Driver Preparation” on page 94. If Windows NT 4.0 is to be loaded on a SCSI device, then the device should be listed first in the Boot Device List in the CMOS Setup Boot screen.

1. After booting from the Windows NT 4.0 Installation CD, if Windows NT 4.0 is to be installed on a SCSI device, then the user must press F6 while the message “Setup is inspecting your computer hardware configuration” is displayed. If this is done, Windows NT 4.0 will allow a manual load of the SCSI driver. If Windows NT 4.0 is not being loaded on a SCSI device, then do not press F6.



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2. In either case, the installation will ask to specify additional mass storage devices. Press S in response to this request when prompted.
3. Select **Other** from the list of possible devices, and press ENTER.
4. Insert the SCSI Driver floppy into drive A when prompted and press ENTER.
5. The **SymBIOS Ultra 3 PCI SCSI Driver** will be highlighted. Press ENTER to continue.
6. The driver will then be copied and included in the list of mass storage devices. Press ENTER to continue with the loading of Windows NT 4.0.



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Appendix

C

# Phoenix BIOS

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## Introduction

The VMIVME-7765 utilizes the BIOS (Basic Input / Output System) in the same manner as other PC / AT compatible computers. This appendix describes the menus and options associated with the VMIVME-7765 BIOS.

### System BIOS Setup Utility

During system bootup, press the F2 key to access the Phoenix BIOS Main screen. From this screen, the user can select any section of the Phoenix (system) BIOS for configuration, such as floppy drive configuration or system memory. The parameters shown throughout this section are the default values.

### Help Window

The help window on the right side of each menu displays the help text for the currently selected field. It updates as you move the cursor to each field. Pressing F1 or ALT-H on any menu brings up the General Help window that describes the legend keys and their alternates. The scroll bar on the right of any window indicates that there is more than one page of information in the window. Use PGUP and PGDN to display each page. Pressing HOME and END displays the first and last page. Pressing ENTER displays each page. Press ESC to exit the current window.

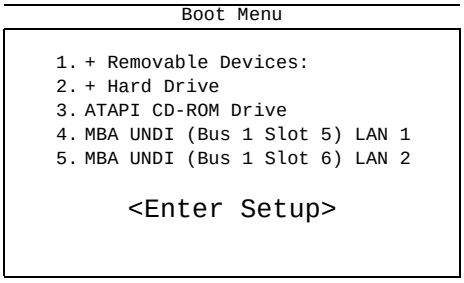


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## First Boot

The VMIVME-7765 has a First Boot menu enabling the user to, on a one time basis, select a drive device to boot from. This feature is useful when installing from a bootable disk. For example, when installing Windows NT from a CD, enter the First Boot menu and use the arrows keys to highlight ATAPI CD-ROM Drive. Press ENTER to continue with system boot.

This feature is accessed by pressing the ESC at the very beginning of the boot cycle. The selection made from this screen applies to the current boot only, and will not be used during the next boot-up of the system. If you have trouble accessing this feature, disable the QuickBoot Mode in the Main BIOS setup screen. Exit, saving changes and retry accessing the First Boot menu.

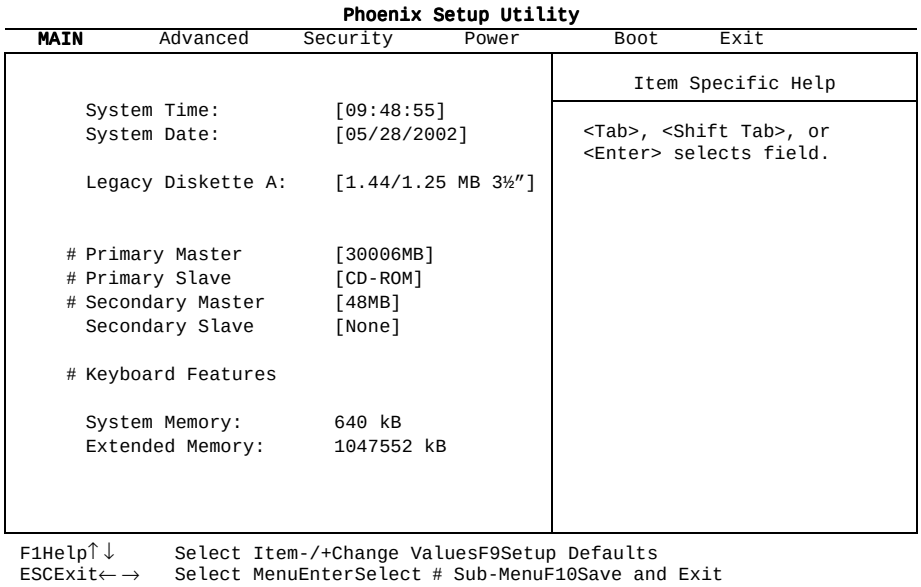





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# Main Menu

The Main menu allows the user to select QuickBoot, set the system clock and calendar, record disk drive parameters, and set selected functions for the keyboard.




## System Time

The time format is based on the 24-hour military-time clock. For example, 1 PM is 13:00:00. Press the left or right arrow key to move the cursor to the desired field (hour, minute, seconds). Press the PGUP or PGDN key to step through the available choices, or type in the information.

## System Date

Press the left or right arrow key to move the cursor to the desired field (month, day, year). Press the PGUP or PGDN key to step through the available choices, or type in the information.

## Legacy Diskette

### Floppy Drive A

The VMIVME-7765 supports one floppy disk drive. The options are:

- Disabled — No diskette drive installed
- 360K, 5.25 in — 5-1/4 inch PC-type standard drive; 360 kilobyte capacity



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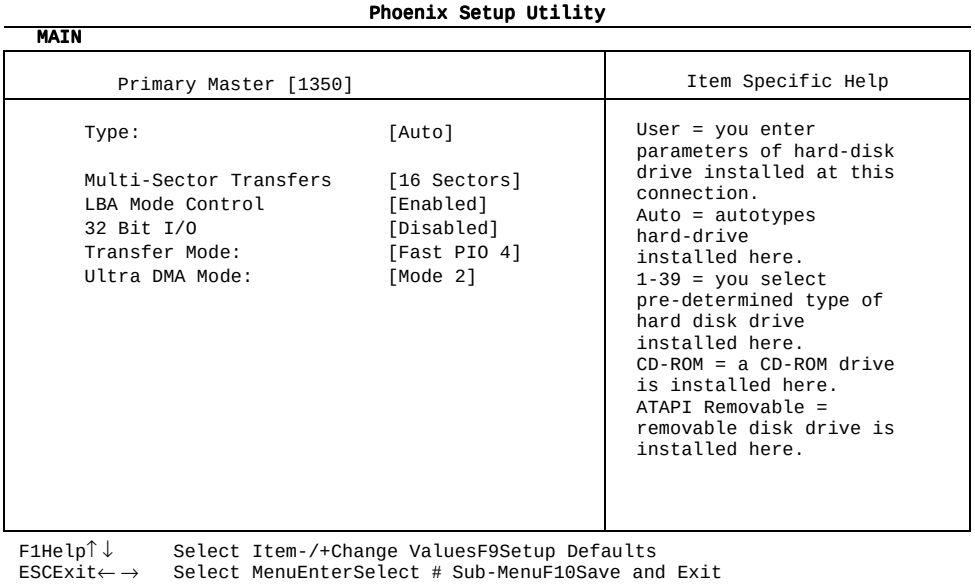
- 1.2M, 5.25 in — 5-1/4 inch AT-type high-density drive; 1.2 megabyte capacity
- 720K, 3.5 in — 3-1/2 double-sided drive; 720 kilobyte capacity
- 1.44M/1.25M, 3.5 in — 3-1/2 inch double-sided drive; 1.44 megabyte capacity
- 2.88M, 3.5 in — 3-1/2 inch double-sided drive; 2.88 megabyte capacity

Use PGUP or PGDN to select the floppy drive. The default is 1.44M, 3.5 inch.

**NOTE:** The 1.25MB 3.5 inch disk references a 1024 byte/sector Japanese media format. The 1.25MB diskette requires a 3-Mode floppy disk drive.

## Primary Master/Slave

The VMIVME-7765 is capable of utilizing two IDE devices on the Primary Master bus. The default setting is Auto. The Primary Slave is assigned to the CD-ROM (if installed). If a setting other than Auto is selected, the user must match the settings to the hardware.




## Secondary Master/Slave

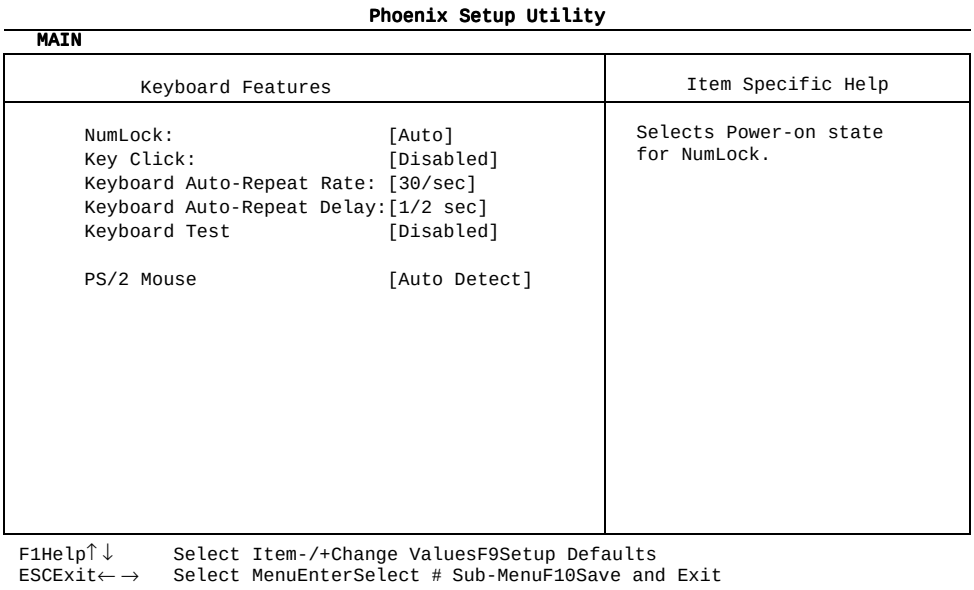
The default type in the BIOS setting is Auto.

## Keyboard Features

The Keyboard Features allows the user to set several keyboard functions.



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## NumLock

The NumLock can be set to Auto, On or Off to control the state of the NumLock key when the system boots. When set to Auto or On, the numeric keypad generates numbers instead of controlling the cursor operations. The default is Auto.

## Key Click

This option enables or disables the Keyboard Auto-Repeat Rate and Delay settings. When disabled, the values in the Keyboard Auto-repeat Rate and Delay are ignored. The default is Disabled.

## Keyboard Auto-Repeat Rate (Chars/Sec)

If the Key Click is enabled, this determines the rate a character is repeated when a key is held down. The options are: 30, 26.7, 21.8, 18.5, 13.3, 10, 6 or 2 characters per second. The default is 30.

## Keyboard Auto-Repeat Delay (sec)

If the Key Click is enabled, this determines the delay before a character starts repeating when a key is held down. The options are: 1/4, 1/2, 3/4 or 1 second. The default is 1/2.

## Keyboard Test

When enabled, this feature will test the keyboard during boot-up.



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### PS/2 Mouse

Disabled prevents any installed PS/2 mouse from functioning, but frees up IRQ12. Enabled forces the PS/2 mouse port to be enabled regardless if a PS/2 mouse is present. Auto Detect will enable the PS/2 mouse only if a PS/2 mouse is present. OS Controlled is only displayed if the operating system controls the mouse port.

## System Memory

The System Memory field is for informational purposes only and cannot be modified by the user. This field displays the base memory installed in the system.

## Extended Memory

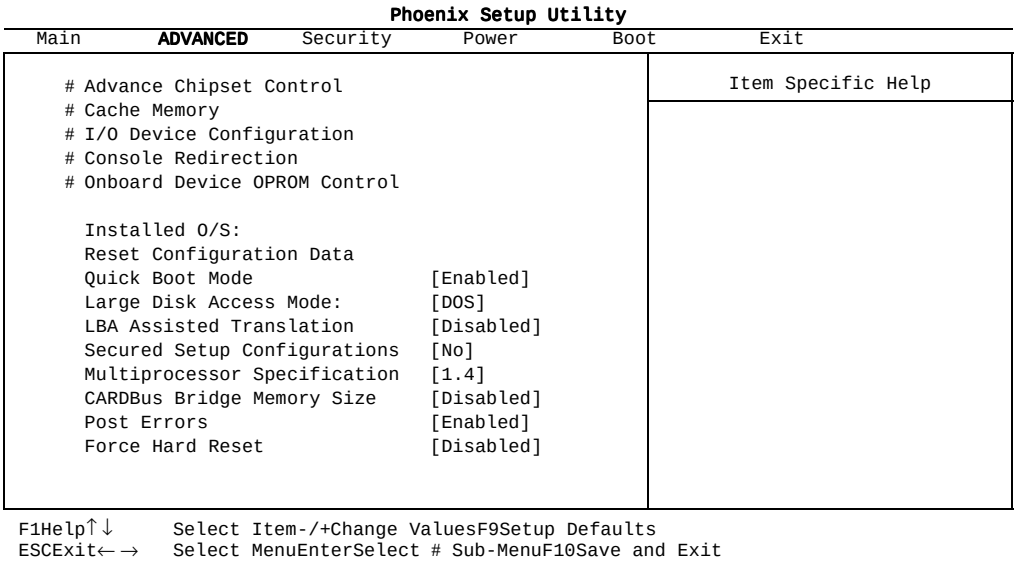
The Extended Memory field is for informational purposes only and cannot be modified by the user. This field displays the total amount of memory installed in the system in Mbytes. The amount of extended memory shown will be approximately 3Mbytes less than the amount installed. This is due to the fact that the graphics function of the Intel GMCH chip uses a portion of this memory making it unavailable to other applications.



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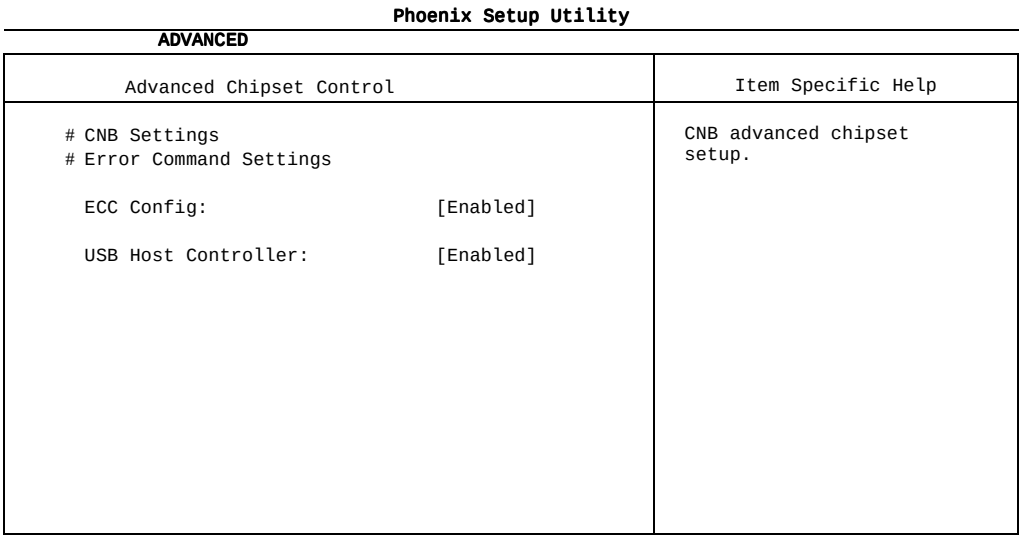
# Advanced Menu

Selecting Advanced from the Main menu will display the screen shown below.




## Advanced Chipset Control

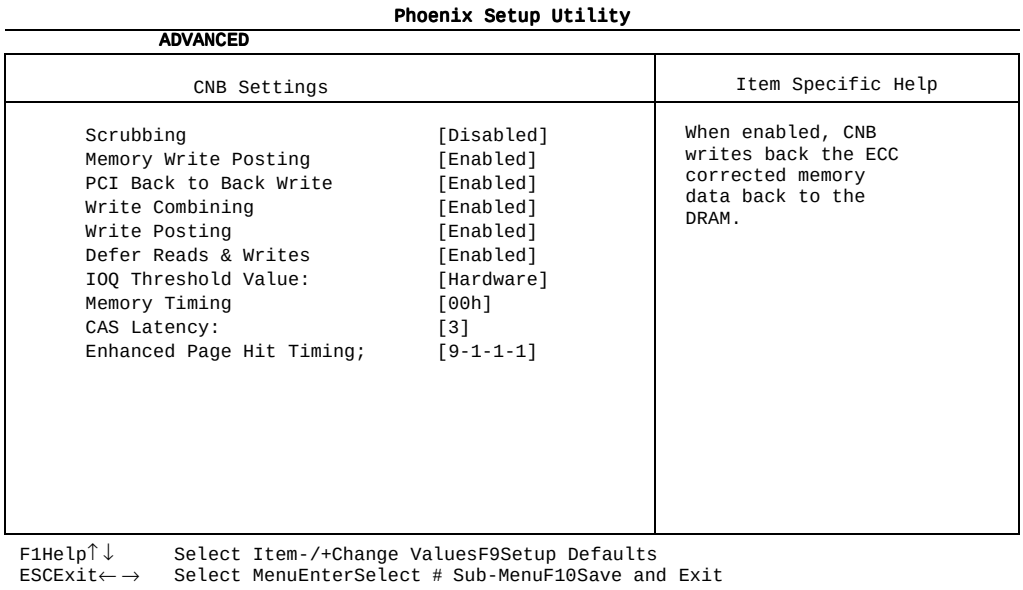
Selecting Advanced Chipset Control opens the menu below. Use this menu to change the values in the chipset register for optimizing your system's performance.






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## CNB Settings




### Scrubbing

When enabled, CNB writes the ECC corrected memory data back to the DRAM. The default is Disabled.

### Memory Write Posting

Enables or disables memory write posting in CNB. The default is Enabled.

### PCI Back-to-Back Write

PCI Back-to-Back Write enable or disable for processor Bus-to-PCI posted writes. The default is Enabled.

### Write Combining

Enables or disables write combining for processor Bus-to-PCI posted writes. The default is Enabled.

### Write Posting

Enables or disables Pentium Pro-to-PCI write posting. See REC 4B bit 1. The default is Enabled.



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### Defer Reads and Writes

Enables or disables Defer For Processor Bus-to-PCI reads and writes. The default is Enabled.

### IOQ Threshold Value

Uses hardware setting if set to Hardware, otherwise uses the IOQ value set by the user. The default is Hardware.

### Memory Timing

Used to set up the memory timing. The default is 00h.

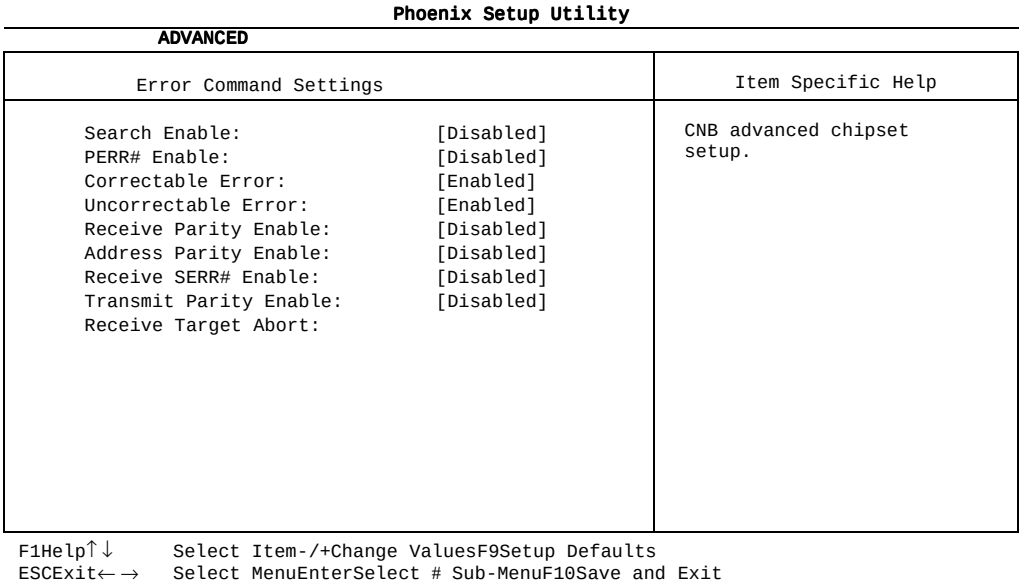
### CAS Latency

Used to set the SDRAM CAS Latency. The default is 3.

### Enhanced Page Hit Timing

This selects the Page Hit timing to be used.

## Error Command Settings






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### ECC Config

If all memory in the system supports ECC, then use this option to enable or disable ECC support. The default is Enabled.

### USB Host Controller

The USB Host Controller enables or disables the USB hardware. Disabled resources will be freed up for other uses. The default is Enabled.

## Cache Memory

Enabling the cache memory enhances the speed of the processor. When the CPU requests data, the system transfers the requested data from the main DRAM into the cache memory where it is stored until processed by the CPU. The default is Enabled.

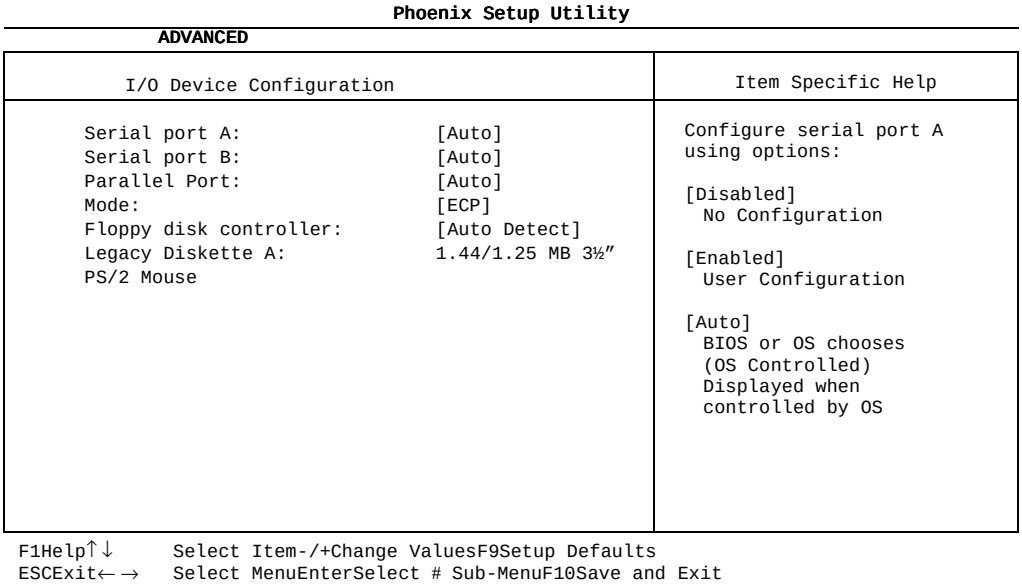
```
                              Phoenix Setup Utility
                ADVANCED
+-------------------------------------------------------------------+
|                Cache Memory                  |  Item Specific Help |
|                                              |                     |
|  Memory Cache                  [Enabled]     |  Sets the state of  |
|  Cache System BIOS area:       [Write Protect]|  the memory cache   |
|  Cache Video BIOS area:        [Write Protect]|                     |
|  Cache Base 0-512k:            [Write Back]  |                     |
|  Cache Base 512k-640k:         [Write Back]  |                     |
|  Cache Extended Memory Area:   [Write Back]  |                     |
|  Cache A000-AFFF:              [Disabled]    |                     |
|  Cache B000-BFFF:              [Disabled]    |                     |
|  Cache C800-CBFF:              [Write Through]|                    |
|  Cache CC00-CFFF:              [Write Through]|                    |
|  Cache D000-D3FF:              [Write Through]|                    |
|  Cache D400-D7FF:              [Write Through]|                    |
|  Cache D800-DBFF:              [Write Through]|                    |
|  Cache DC00-DFFF               [Write Through]|                    |
|                                              |                     |
|                                              |                     |
+-------------------------------------------------------------------+
F1Help↑↓      Select Item-/+Change ValuesF9Setup Defaults
ESCExit←→     Select MenuEnterSelect # Sub-MenuF10Save and Exit
```



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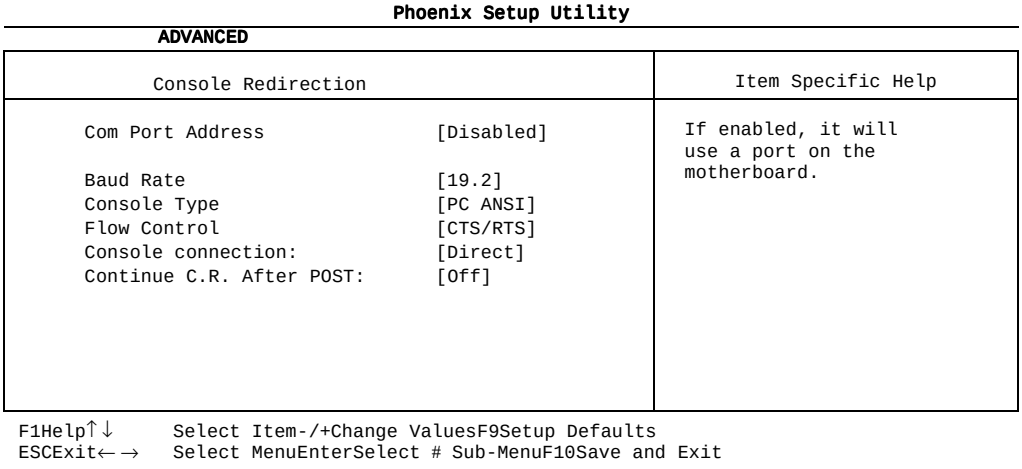
## I/O Device Configuration

Select this menu to configure your peripheral devices, if required.




## Console Redirection

Console Redirection allows for remote access and control of the PC functions to a remote terminal via the serial port. Selecting Console Redirection provides additional menus used to configure the console.





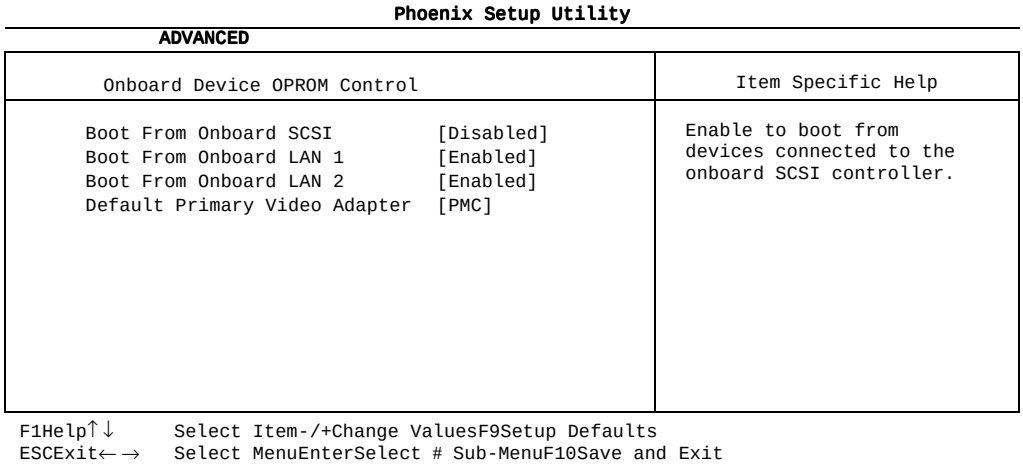

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### Continue C.R. After POST

This enables console redirection after the operating system has loaded. The options are OFF or ON. The default setting is OFF.

## Onboard Device OPROM Control

Enables or disables option ROM execution for onboard boot devices and video. Disabling boot device OPROM decreases BIOS boot time and memory requirements. Allows choice for onboard or installed video adapter to be used.




## Installed O/S

Use this feature to select the operating system to use with your system.

## Reset Configuration Data

Select Yes if you want to clear the extended system configuration data. The default is No.

## Quick Boot Mode

When enabled, certain checks normally performed during POST are omitted decreasing the time required to run the POST. The default is Enabled.

## Large Disk Access Mode

The options for the Large Disk Access Mode are UNIX Novell Netware or Other.

If you are installing new software and the drive fails, change this selection and try again. Different operating systems require different representations of drive geometries. The default is DOS.



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## LBA Assisted Translation

LBA (Logical Block Addressing): During drive accesses, the IDE controller transforms the data address described by sector, head, and cylinder number into a physical block address. This significantly improves data transfer rates for drives with greater than 1024 cylinders. The default is Disabled.

## Secured Setup Configurations

Yes prevents a Plug-N-Play operating system from changing system settings. The default is No.

## Multiprocessor Specification

This configures the microprocessor specification revision level. Some operating systems will require 1.1 for compatibility reasons. The default is 1.4.

## Cardbus Memory Size

When enabled, allows resources to be allocated from a Cardbus controller located behind a PCI-to-PCI Bridge. The default is Disabled.

## POST Errors

Pauses and displays Setup Entry or Resume Boot prompt if an error occurs on boot. If disabled, the prompt will be bypassed and the system will attempt to boot. The default is Enabled.

## Force Hard Reset

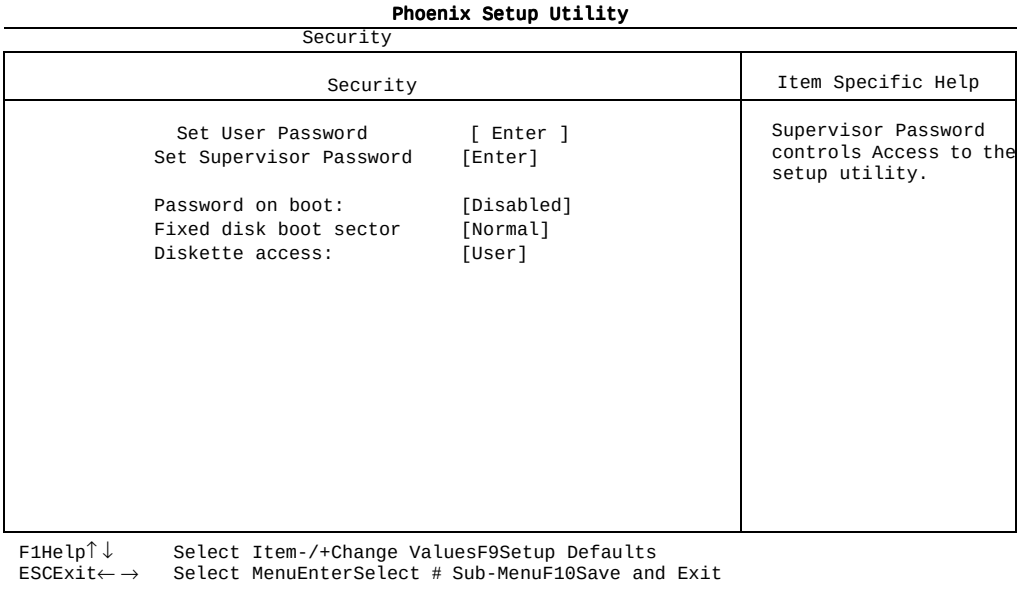
A reboot causes a warm restart which does not issue board resets and executes only a subset of BIOS POST to reduce boot time. If an OS reboot causes boot failure or a PCI device requires a reset, enable this function to force a hard reset during reboot. The default is Disabled.



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# Security

Utilize this screen to set a user password.




## Password On Boot

Enables password entry on boot. The default is Disabled.

## Fixed Disk Boot Sector

Write protects boot sector on the hard disk to protect against viruses. The default is Normal.

## Diskette Access

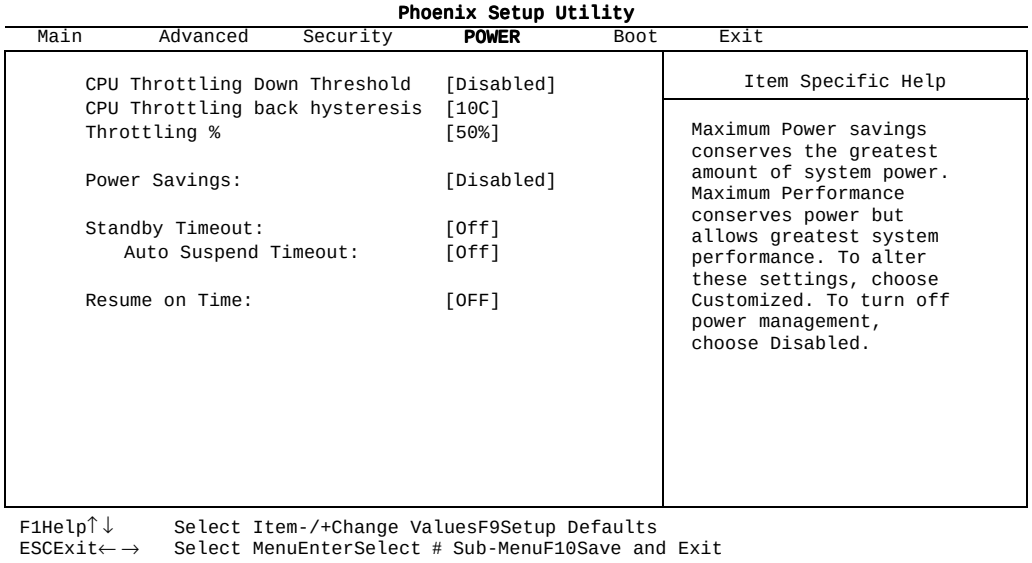
Controls access to the diskette drives. The default is User.



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# Power

This screen, selected from the Main screen, allows the user to configure power saving options on the VMIVME-7765.



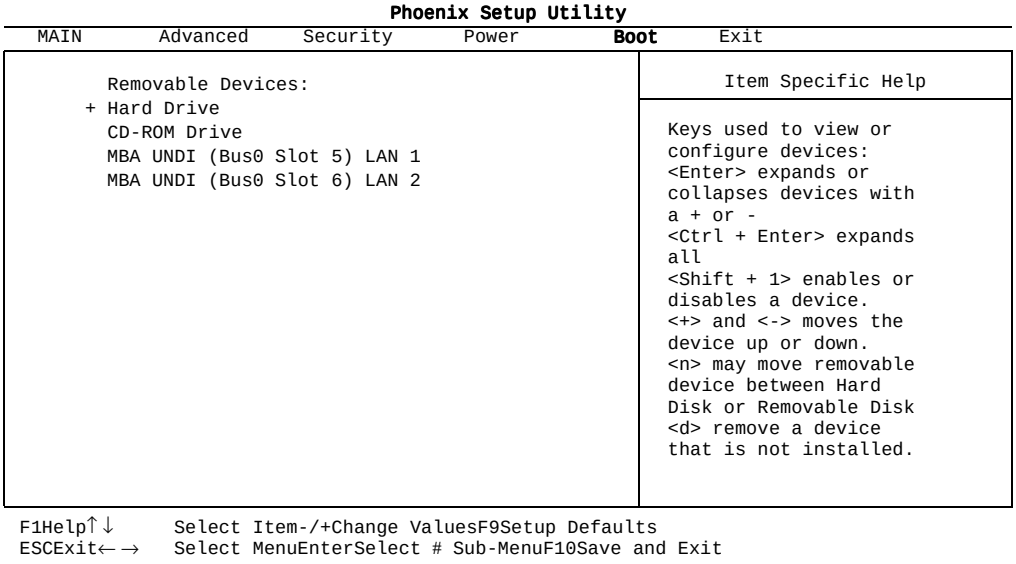

The Throttling and CPU Throttling back hysteresis selections will only be shown if “CPU Throttling Down Threshold” is enabled. The default is Disabled. The default for CPU Throttling back hysteresis is 10C. The default for Throttling is 50%.



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# Boot Menu

The Boot priority is determined by the stack order, with the top having the highest priority and the bottom the least. The order can be modified by highlighting a device and, using the <+> or <-> keys, moving it to the desired order in the stack. A device can be boot disabled by highlighting the particular device and pressing <Shift 1>. <Enter> expands or collapses devices with a + or - next to them.

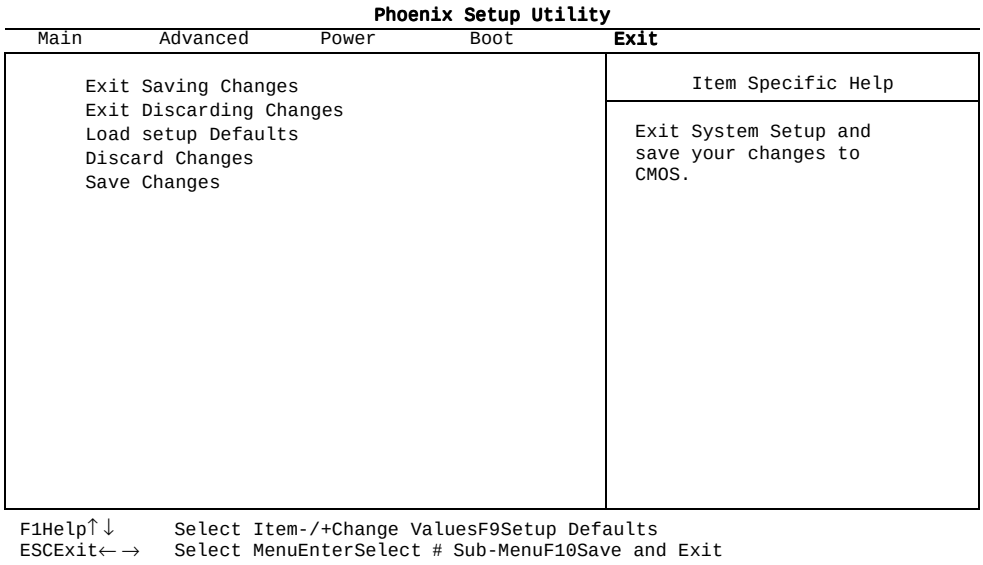





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# Exit Menu

The Exit menu allows the user to exit the BIOS program, while either saving or discarding any changes. This menu also allows the user to restore the BIOS defaults if desired.




## Exit Saving Changes

Exit System Setup and save your changes to CMOS.

## Exit Discarding Changes

Exit System Setup, discarding any changes to CMOS.

## Load Setup Defaults

Load System defaults as defined at the factory.

## Discard Changes

Discard any changes without exiting the Setup program.

## Save Changes

Save any changes made without exiting the Setup program.



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Appendix

D

# *LANWorks BIOS*

## Contents

Boot Menus . . . . . 120
BIOS Features Setup . . . . . 122

## Introduction

The VMIVME-7765 includes a LANWorks option which allows the VMIVME-7765 to be booted from a network. This appendix describes the procedures to enable this option and the LANWorks BIOS Setup screens.



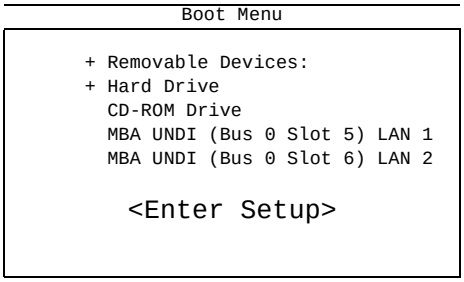
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# Boot Menus

There are two methods of enabling the LANWorks BIOS option. The first method is the *First Boot* menu. The second is the *Boot* menu from the BIOS Setup Utility.

## First Boot Menu

Press ESC at the very beginning of the boot cycle, which will access the *First Boot* menu. Selecting “Managed PC Boot Agent (MBA)” to boot from the LAN in this screen applies to the current boot only, at the next reboot the VMIVME-7765 will revert back to the setting in the main BIOS Boot menu.




Using the arrow keys, highlight *Managed PC Boot Agent (MBA),* and press the ENTER key to continue with the system boot.

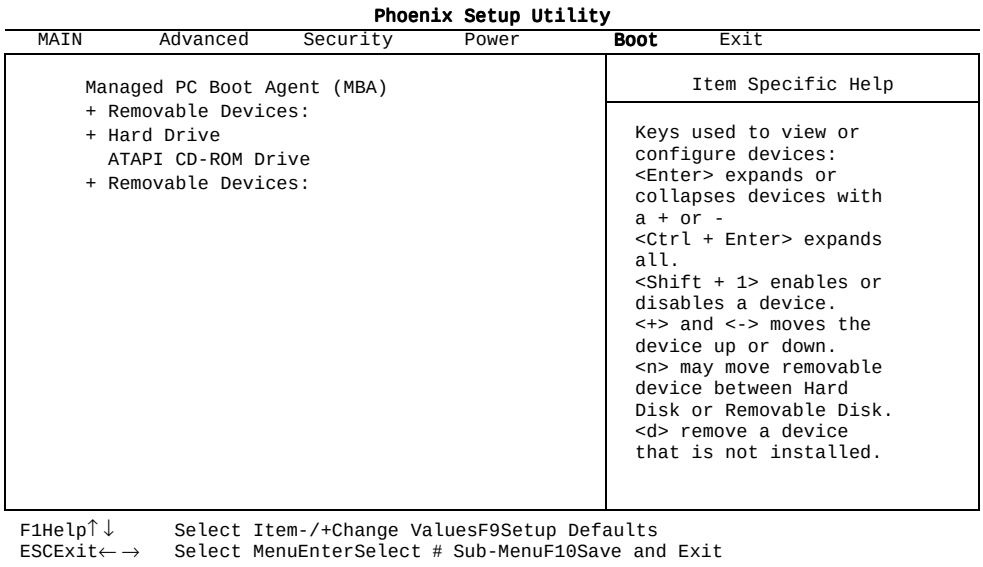
## Boot Menu

The second method of enabling the LANWorks BIOS option is to press the F2 key during system boot. This will access the BIOS Setup Utility. Advance to the Boot menu and, using the arrow keys, highlight the Managed PC Boot Agent (MBA) option. Then, using the <+> or <-> keys move the MBA option to the top of the stack.

Advance to the Exit menu and select “Exit Saving Changes”. Press ENTER. When the system prompts for confirmation, press “Y” for yes. The computer will then restart the system boot-up.



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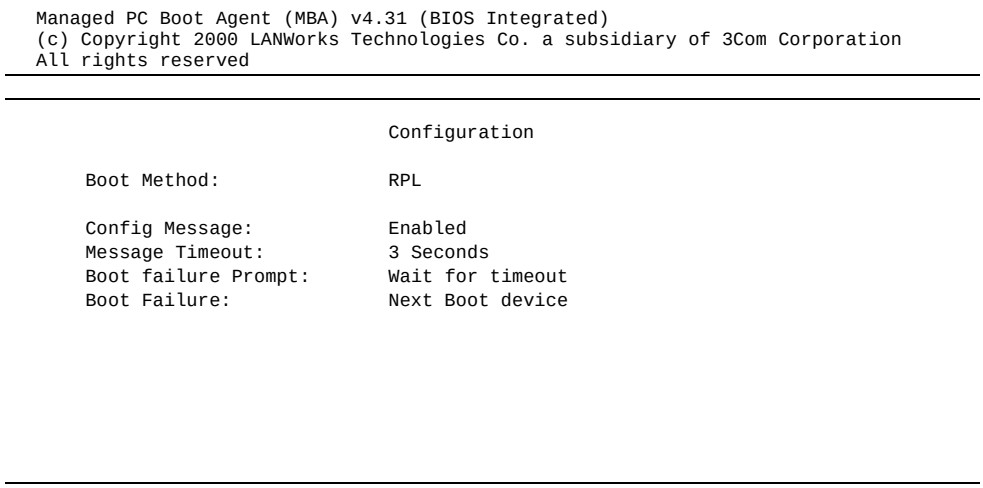



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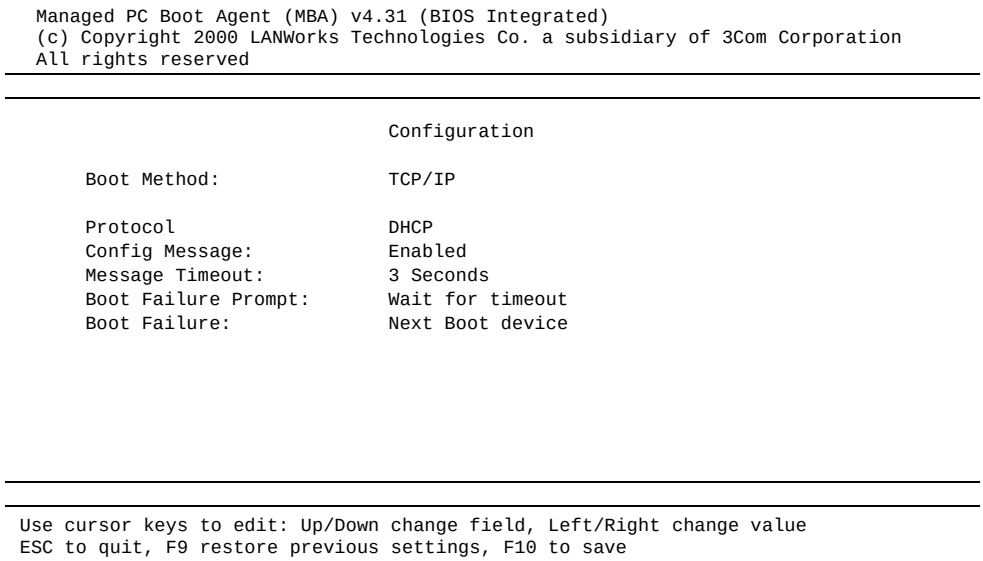
# BIOS Features Setup

After the Managed PC Boot Agent has been enabled, there are several boot options available to the user. These options are RPL (default), TCP/IP, Netware and PXE. The screens below show the defaults for each boot method.

## RPL




## TCP/IP






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## Netware

```
  Managed PC Boot Agent (MBA) v4.31 (BIOS Integrated)
  (c) Copyright 2000 LANWorks Technologies Co. a subsidiary of 3Com Corporation
  All rights reserved
```

```
                                Configuration

      Boot Method:              Netware

      Protocol                  802.3
      Config Message:           Enabled
      Message Timeout:          3 Seconds
      Boot failure Prompt:      Wait for timeout
      Boot Failure:             Next Boot device
```

```
Use cursor keys to edit: Up/Down change field, Left/Right change value
ESC to quit, F9 restore previous settings, F10 to save
```

## PXE

```
  Managed PC Boot Agent (MBA) v4.31 (BIOS Integrated)
  (c) Copyright 2000 LANWorks Technologies Co. a subsidiary of 3Com Corporation
  All rights reserved
```

```
                                Configuration

      Boot Method:              PXE


      Config Message:           Enabled
      Message Timeout:          3 Seconds
      Boot failure Prompt:      Wait for timeout
      Boot Failure:             Next Boot device
```

```
Use cursor keys to edit: Up/Down change field, Left/Right change value
ESC to quit, F9 restore previous settings, F10 to save
```



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Appendix

E

# SCSI BIOS

## Contents

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Boot Initialization with BIOS Boot Specification (BBS) . . . . . 126

## Introduction

This section presents general information about the SDMS SCSI BIOS and Configuration Utility Version 4.19.00.

A SCSI BIOS is the bootable ROM code that manages SCSI hardware resources. It is specific to a family of LSI Logic SCSI controllers or processors. An SDMS SCSI BIOS integrates with a standard system BIOS, extending the standard disk service routine provided through INT13h.

During the boot time initialization, the SCSI BIOS determines if there are other hard disks, such as an IDE drive, already installed by the system BIOS.

If there are, the SCSI BIOS maps any SCSI drives it finds behind the drive(s) already installed. Otherwise, the SCSI BIOS installs drives starting with the system boot drive. In this case, the system boots from a drive controlled by the SCSI BIOS. For 4.05 versions and higher, LSI Logic supports the BIOS Boot Specification (BBS). The section, "*Boot Initialization with BIOS Boot Specification (BBS)*," page 126 discusses selecting boot and drive order.



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## Features

The SDMS SCSI BIOS features include:

- Configuration for up to 256 adapters - any four can be chosen for INT13 (bootrom) support
- All LSI53C8xx devices including LSI53C895A
- LSI53C1510 device
- LSI53C1010 device
- SPI-3 Parallel Protocol Request (PPR)
- Basic Domain Validation

## Boot Initialization with BIOS Boot Specification (BBS)

The SDMS SCSI BIOS provides support for the BIOS Boot Specification (BBS), which allows you to choose which device to boot from by selecting the priority.

To use this feature, the system BIOS must also be compatible with the BBS. If your system supports the BBS, then you will use the system BIOS setup menu to select the boot and drive order. In the system BIOS setup, the Boot Connection Devices menu appears with a list of available boot options. Use this menu to select the device and rearrange the order, then exit to continue the boot process.

### CD-ROM Boot Initialization

The SDMS SCSI BIOS supports boot initialization from a CD-ROM drive. The five types of emulation are:

- No emulation disk
- Floppy 1.2 Mbyte emulation disk
- Floppy 1.44 Mbyte emulation disk
- Floppy 2.88 Mbyte emulation disk
- Hard disk emulation

The type of emulation assigns the drive letter for the CD-ROM. For example, if a 1.44 Mbyte floppy emulation CD-ROM was loaded, then the CD-ROM drive would become the designated A drive, and the existing floppy would become drive B.

### Starting the SCSI BIOS Configuration Utility

If you have SCSI BIOS version 4.XX, and it includes the SDMS SCSI BIOS Configuration Utility, you can change the default configuration of your SCSI host adapters. You may decide to alter these default values if there is a conflict between device settings or if you need to optimize system performance.



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You can see the version number of the SCSI BIOS in a banner displayed on your computer monitor during boot. If the utility is available, this message also appears on your monitor:

Press Ctrl-C to start LSI Logic Configuration Utility...

This message remains on your screen for about five seconds, giving you time to start the utility. If you decide to press "Ctrl-C", the message changes to:

Please wait, invoking LSI Logic Configuration Utility...

After a brief pause, your computer monitor displays the Main menu of the SDMS PCI SCSI BIOS Configuration Utility.

To make changes with this menu driven utility, one or more SDMS SCSI host adapters must have Non-Volatile Random Access Memory (NVRAM) to store the changes.

These messages may appear during the boot process:

"Adapter removed from boot order, parameters will be updated accordingly" appears when an adapter is removed from the system or relocated behind a PCI bridge.

"Configuration data invalid, saving default configuration!" appears if none of the information in the NVRAM is valid.

"Found SCSI Controller not in following Boot Order List, to Add: Press Ctrl-C to start LSI Logic Configuration Utility..." or "Adapter configuration may have changed, reconfiguration is suggested!" could appear when fewer than four adapters are in the boot order and adapters exist in the system which are not in the boot order.

---

**NOTE:** The SCSI BIOS Configuration Utility is a powerful tool. If, while using it, you somehow disable all of your controllers, pressing Ctrl-A (or Ctrl-E on version 4.04 or later) after memory initialization during reboot allows you to re-enable and reconfigure. Also, if the system locks up due to Non-Volatile Storage (NVS), press `Ctrl-N` to bypass the BIOS in order to reflash the card.

Not all devices detected by the SCSI BIOS Configuration Utility can be controlled by the BIOS. Devices such as tape drives and scanners require that a device driver specific to that peripheral be loaded. The SCSI BIOS Configuration Utility does allow parameters to be modified for these devices.

---



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# Using the Configuration Utility

## Screen Format

All SCSI BIOS Configuration Utility screens are partitioned into fixed areas as shown below.

| Header Area | | | | | |
|---|---|---|---|---|---|
| Menu Area | | | | | |
| Adapter | PCI Bus | Dev/ Func | Boot Order | Current Status | Next Boot |
| Main Area | | | | | |
| Footer Area | | | | | |
| F1 =Help<br>F2 =Menu | Arrow Keys =Select Item | | | -/+ =Change [Item] | |
| Esc =Abort/Exit | Home/End =Select Item | | | Enter =Execute <Item> | |

## Header Area

This area provides static information text, which is typically the product title and version.

## Menu Area

This area provides the current Main Area's menu, if any. This area has a cursor for menu item selection.



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## Main Area

This is the main area for presenting data. This area has a cursor for item selection, horizontal scrolling and vertical scrolling. The horizontal and vertical scroll bars appear here.

## Footer Area

This area provides general help information text.

## User Input

Throughout these screens, selections that are not permissible are grayed out.

| | |
|---|---|
| F1 = Help | Context sensitive help for the cursor-resident field. |
| F2 = Menu | Sets cursor context to the menu selection area.<br>Select a menu item and press Enter. |
| Arrow Keys = | Select Item |
| Home/End = | Select Item<br>Up, down, left, right movement to position the cursor. |
| +/- = Change [Item] | Items with values in [] brackets are modifiable.<br>Use the '+' or '-' keys in the top row of the main keyboard or use the numeric keypad '+' and '-' keys to change a modifiable field. When pressed, they toggle a modifiable field to its next relative value. For example, '+' toggles the value up and '-' toggles the value down. |
| Esc = Abort/Exit | Escape aborts the current context operation and/or exits the current screen. User confirmation is requested as required. |
| Enter = Execute <Item> | Items with values in <> brackets are executable.<br>Press Enter to execute the field's associated function. |

## Main Menu

When you invoke the SDMS SCSI BIOS Configuration Utility, the Main menu appears. This menu displays a scrolling list of up to 256 LSI Logic PCI to SCSI host adapters in the system and information about each of them.

Use the arrow keys to select an adapter, then press Enter to view and modify the selected adapter's properties (and to gain access to the attached devices).

Only adapters with LSI Logic Control enabled can be accessed. Adapters with no NVM will show default settings and cannot be changed. After selecting an adapter and pressing Enter, the adapter's SCSI bus is scanned and the Adapter Properties menu appears. An example is shown after the descriptions about the Boot Adapter List and Global Properties menus.



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On the Main menu, two selections are: Boot Adapter List and Global Properties. Press F2 to access these menus, use the arrow keys to select the desired menu, and press Enter.

“Boot Adapter List” allows selection and ordering of boot adapters.

“Global Properties” allows changes to global scope settings.

To execute an item, select it and press Enter. Here is an example of the Main menu:

**Symbios SDMS (TM) PCI SCSI Configuration Utility Version PCI-4.19.00**

<Boot Adapter List> <Global Properties>

Symbios Host Bus Adapters

| Adapter | PCI Bus | Dev/ Func | Port Number | IRQ | NVM | Boot Order | LSI Logic Control |
|---|---|---|---|---|---|---|---|
| <53C1010-66 | 1 | 68> | 1400 | 11 | Yes | 0 | Enabled |
| <53C1010-66 | 1 | 69> | 1800 | 11 | Yes | 1 | Enabled |

F1 =Help Arrow Keys =Select Item -/+ =Change [Item]
F2 =Menu

Esc =Abort/Exit Home/End =Select Item Enter =Execute <Item>

## Field Descriptions

### Adapter

Indicates the specific family of LSI Logic Host Adapters.

### PCI Bus

Indicates the PCI Bus number (range 0x00 - 0xFF, 0 - 255 decimal) assigned by the system BIOS to an adapter.



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### Dev/Func

Indicates the PCI Device/Function assigned by the system BIOS to an adapter.

This is an 8-bit value mapped as follows:

Bit # 7 6 5 4 3 2 1 0
> Bits 2-0: Function (range 0 - 7)

> Bits 7-3: Device (range 0x00 - 0x1F, 0 - 31 decimal).

### Port Number

Indicates the I/O Port Number that communicates with an adapter. The system BIOS assigns this number.

### IRQ

Indicates the Interrupt Request Line used by an adapter. The system BIOS also assigns this value.

### NVM

Indicates whether an adapter has non-volatile memory (NVM) associated with it. An adapter's configuration is stored in its associated NVM. NVM can refer to NVRAM that is resident on a host adapter or to the system NVM.

### Boot Order

Indicates the relative boot order (0 to 3) of an adapter. The SDMS SCSI BIOS traverses up to four adapters in the specified order in search of bootable media. Access the "Boot Adapter List" Menu to modify this item.

### LSI Logic Control

Indicates whether an adapter is eligible for LSI Logic software control, or is reserved for control by non-LSI Logic software.

### Global

Indicates global properties that are not associated with a Properties specific adapter or device.



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## Boot Adapter List

The Boot Adapter List menu specifies the order in which adapters will boot when more than one LSI Logic adapter is in a system. Up to four of the total adapters in a system can be selected as bootable. Adapters can be added or deleted using this menu.

To add an adapter to the boot list, press the `Insert` key while on the Boot Adapter List. This puts the cursor on the adapter select list. Use the arrow keys to select the desired adapter and press `Enter` to add it to the end of Boot Adapter List.

To remove an adapter from the boot list, press the `Delete` key while on the desired adapter in the Boot Adapter List. You can also change the boot order by using the '+' or '-' keys. For example, place the cursor on the adapter that you want to change, and use the '+' or '-' key to raise or lower the boot order.

Here is an example of the Boot Adapter List menu:

**Symbios SDMS (TM) PCI SCSI Configuration Utility Version PCI-4.19.00**

Boot Adapter List

Insert=Add an adapter Delete=Remove an adapter

| Adapter | PCI Bus | Dev / Func | Boot Order | Current Status | Next Boot |
|---|---|---|---|---|---|
| <53C1010-66 | 1 | 68> | [0] | On | [On] |
| <53C1010-66 | 1 | 69> | [1] | On | [On] |

Hit Insert to select an adapter from this list:

| | | |
|---|---|---|
| <53C1010-66 | 1 | 68> |
| <53C1010-66 | 1 | 69> |

```
F1  =Help            Arrow Keys =Select Item          -/+   =Change  [Item]
F2  =Menu

Esc =Abort/Exit      Home/End  =Select Item          Enter =Execute <Item>
```



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## Field Descriptions

### Adapter

Indicates the specific family of LSI Logic Host Bus Adapters.

### PCI Bus

Indicates the PCI Bus number (range 0x00 - 0xFF, 0 - 255 decimal) assigned by the system BIOS to an adapter.

### Dev/Func

Indicates the PCI Device / Function assigned by the system BIOS to an adapter.

This is an 8-bit value mapped as follows:

Bit # 7 6 5 4 3 2 1 0
> Bits 2-0: Function (range 0 - 7)

> Bits 7-3: Device (range 0x00 - 0x1F, 0 - 31 decimal).

### Boot Order

Specifies the relative boot order (0 to 3) of an adapter.

- \- : decreases an adapter's relative boot order.
- \+ : increases an adapter's relative boot order.

### Current Status

Indicates whether an adapter in the boot list was enabled during the most recent boot. Disabled adapters and their attached devices are ignored by the SDMS SCSI BIOS; they are still visible to the configuration utility.

### Next Boot

Specifies whether to enable an adapter upon the next boot. The SDMS SCSI BIOS ignores disabled adapters and their attached devices although they are still visible to the configuration utility.



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## Global Properties

The Global Properties option on the Main menu allows you to view boot information, set display and video modes, pause if an alert message has been displayed, and other options. Here is an example of the Global Properties menu:

```
Symbios SDMS (TM) PCI SCSI Configuration Utility  Version PCI-4.19.00

Global Properties

Pause When Boot Alert Displayed          [No]
Boot Information Display Mode            [Verbose]
Negotiate With Devices                   [Supported]
Video Mode                               [Color]
Support Interrupt                        [Hook interrupt, the Default]

<Restore Defaults>

F1  =Help          Arrow Keys =Select Item        -/+   =Change  [Item]
F2  =Menu

Esc =Abort/Exit    Home/End =Select Item          Enter =Execute <Item>
```

## Field Descriptions

### Pause When Boot Alert Displayed

This option specifies whether to pause for user acknowledgment after displaying an alert message during boot. The Boot Alert setting can be either No or Yes. To continue after displaying a message, specify No. To wait for any key after displaying a message, specify Yes.



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## Boot Information Display Mode

This option specifies the information display mode of the BIOS during boot. It controls how much information about adapters and devices are displayed during boot. The Display Mode setting can be either Terse or Verbose. To display minimum information, specify Terse mode. To display detailed information, specify Verbose mode.

## Negotiate With Devices

This option sets the default value for synchronous and wide negotiations with specified devices. Options are: All, None or Supported.

## Video Mode

This option specifies the default video mode for the SCSI BIOS Configuration Utility. The Video Mode setting can be either Color or Monochrome. The monochrome setting enhances readability on a monochrome monitor.

## Support Interrupt

This option allows the ability to prevent a hook on INT40h, if required. The two settings are: Hook Interrupt, the default, and Bypass Interrupt Hook. Hook Interrupt is the normal operation that supports booting CD-ROMs in floppy emulation mode on most machines.

On certain platforms, the system BIOS uses the INT40h interrupt chain in a non-standard way. On these platforms, you should use the "Bypass Interrupt Hook" setting. This setting prevents a hook into the INT40h chain. If the "Bypass Interrupt Hook" setting is used on systems that do not require it, the CD-ROM may fail to boot and an error message may appear and indicate it is unable to read the boot device.

**NOTE:** Try toggling this value if your machine fails to boot a CD-ROM in floppy emulation mode.

## Restore Defaults

Press `Enter` to obtain default settings.



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## Adapter Properties

The Adapter Properties menu allows you to view and modify adapter settings and SCSI devices connected to it. It also provides access to an adapter's device settings. To display this menu, select a device under the Adapter field on the Main menu and press Enter. Here is an example of the Adapter Properties menu:

```
Symbios SDMS (TM) PCI SCSI Configuration Utility  Version PCI-4.19.00

Adapter Properties

Adapter          PCI Bus   Dev / Func

<53C1010-66      1         68

                 <Device Properties>
                 SCSI Parity                 [Yes]
                 Host SCSI ID                [ 7]
                 SCSI Bus Scan Order         [Low to High (0..Max)]
                 Removable Media Support     [None]
                 CHS Mapping                 [SCSI Plug and Play Mapping]
                 Spinup Delay (Secs)         [ 2]
                 Secondary Cluster Server    [No]
                 Termination Control         [Auto]
                 <Restore Defaults>

F1  =Help          Arrow Keys =Select Item        -/+   =Change  [Item]
F2  =Menu

Esc =Abort/Exit    Home/End =Select Item          Enter =Execute <Item>
```



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## Field Descriptions

If the field displays in grey or yellow text, it is available for changes. If it displays in white text, it is not available.

### Device Properties

This option allows you to view and modify device properties. The Device Properties menu appears. Refer to *Device Properties* on page 137 for information about this menu.

### SCSI Parity

This field indicates whether SCSI parity is enabled for an adapter. When disabled, it is also necessary to disable disconnects for all devices, as parity checking for the reselection phase is NOT disabled. If a non-parity generating device disconnects, its operation will never complete because the reselection fails due to parity error.

### Host SCSI ID

This field indicates the SCSI identifier of an adapter [0-7] or [0-15]. It is recommended that this field be set to the highest priority SCSI identifier, which is 7.

**NOTE:** 8-bit SCSI devices cannot see identifiers greater than 7.

### SCSI Bus Scan Order

This field indicates the order in which to scan SCSI identifiers on an adapter. Changing this item will affect drive letter assignment(s) if more than one device is attached to an adapter.

**NOTE:** Changing this item may conflict with an operating system that automatically assigns drive order.

### Removable Media Support

This field specifies the removable media support option for an adapter. Three settings are allowed:

**None** indicates no removable media support whether the drive is selected as first (BBS), or is first in the scan order (non-BBS).

**Boot Drive Only** provides removable media support for a removable hard drive if it is first in the scan order.

**With Media Installed** provides removable media regardless of the drive number assignment.



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## CHS Mapping

This field defines how the Cylinder Head Sector values are mapped onto a disk without pre-existing partition information. CHS Mapping allows two settings:

**SCSI Plug and Play Mapping** (default value) automatically determines the most efficient and compatible mapping.

**Alternate CHS Mapping** utilizes an alternate, possibly less efficient mapping that may be required if a device is moved between adapters from different vendors.

---

**CAUTION:** Neither of these options has any effect after a disk has been partitioned using the FDISK command. The FDISK utility is a tool that you can use to delete partition entries, one or all of them.

If all partition entries are deleted, it is necessary to reboot to clear memory or the old partitioning data will be reused, thus nullifying the previous operation. Use care to ensure that the correct disk is the target of an FDISK command.

---

## Spinup Delay (Secs)

This field indicates the delay in seconds between spinups of devices attached to an adapter. Staggered spinups will balance the total electrical current load on the system during boot. The default value is 2 seconds, with choices between 1 and 10 seconds.

## Secondary Cluster Server

This field indicates whether an adapter has one or more devices attached that are shared with one or more other adapters. If so, the SDMS SCSI BIOS should avoid SCSI Bus resets as much as possible.

This option allows you to enable an adapter to join a cluster of adapters without performing any SCSI bus resets. This is a requirement for Microsoft Cluster Server. The default value is No.

## Termination Control

This field indicates whether an adapter has automatic termination control. If not available, its current status is either Auto or Off.

Auto means that the adapter automatically determines whether it should enable or disable its termination.

Off means termination at the adapter is off, and the devices at the ends of the SCSI bus must terminate the bus.



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**NOTE:** If Auto is grayed out, it means that termination is automatic, not programmable.

### Restore Defaults

To obtain default settings, press Enter.

## Device Properties

The Device Properties menu allows you to view and update individual device settings for an adapter. Changing a setting for the host device (for example, SCSI ID 7) changes the setting for all devices.

The number of fields displayed requires the menu to scroll left/right in order to display the information. When accessing this menu on-line, use the Home/End keys to scroll to columns currently not displayed. The scroll indicator on the bottom of the menu shows where the cursor is relative to the first and last columns.

Here is an example of the Device Properties menu:

**Symbios SDMS (TM) PCI SCSI Configuration Utility Version PCI-4.19.00**

Device Properties

| SCSI Device Identifier | MB/Sec | MT/Sec | Data Width | Scan ID | Scan LUNs>0 | Disconnect |
|---|---|---|---|---|---|---|
| 0 | [160] | [80] | [16] | [Yes] | [Yes] | [On] |
| 1 | [160] | [80] | [16] | [Yes] | [Yes] | [On] |
| 2 | [160] | [80] | [16] | [Yes] | [Yes] | [On] |
| 3 SEAGATE ST31055N | [160] | [80] | [16] | [Yes] | [Yes] | [On] |
| 4 | [160] | [80] | [16] | [Yes] | [Yes] | [On] |
| 5 | [160] | [80] | [16] | [Yes] | [Yes] | [On] |
| 6 | [160] | [80] | [16] | [Yes] | [Yes] | [On] |
| 7 53C1010-33 | [160] | [80] | [16] | [Yes] | [Yes] | [On] |
| 8 | [160] | [80] | [16] | [Yes] | [Yes] | [On] |
| 9 | [160] | [80] | [16] | [Yes] | [Yes] | [On] |
| 10 | [160] | [80] | [16] | [Yes] | [Yes] | [On] |
| 11 | [160] | [80] | [16] | [Yes] | [Yes] | [On] |
| 12 | [160] | [80] | [16] | [Yes] | [Yes] | [On] |
| 13 | [160] | [80] | [16] | [Yes] | [Yes] | [On] |
| 14 | [160] | [80] | [16] | [Yes] | [Yes] | [On] |
| 15 | [160] | [80] | [16] | [Yes] | [Yes] | [On] |



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| SCSI Device Identifier | SCSI Timeout | Queue Tags | Boot Choice | Format | Verify | Restore Defaults |
|---|---|---|---|---|---|---|
| 0 | < 10> | [On] | [No] | <Format> | <Verify> | <Defaults> |
| 1 | < 10> | [On] | [No] | <Format> | <Verify> | <Defaults> |
| 2 | < 10> | [On] | [No] | <Format> | <Verify> | <Defaults> |
| 3 SEAGATE ST31055N | < 10> | [On] | [No] | <Format> | <Verify> | <Defaults> |
| 4 | < 10> | [On] | [No] | <Format> | <Verify> | <Defaults> |
| 5 | < 10> | [On] | [No] | <Format> | <Verify> | <Defaults> |
| 6 | < 10> | [On] | [No] | <Format> | <Verify> | <Defaults> |
| 7 | < 10> | [On] | [No] | <Format> | <Verify> | <Defaults> |
| 8 | < 10> | [On] | [No] | <Format> | <Verify> | <Defaults> |
| 9 | < 10> | [On] | [No] | <Format> | <Verify> | <Defaults> |
| 10 | < 10> | [On] | [No] | <Format> | <Verify> | <Defaults> |
| 11 | < 10> | [On] | [No] | <Format> | <Verify> | <Defaults> |
| 12 | < 10> | [On] | [No] | <Format> | <Verify> | <Defaults> |
| 13 | < 10> | [On] | [No] | <Format> | <Verify> | <Defaults> |
| 14 | < 10> | [On] | [No] | <Format> | <Verify> | <Defaults> |
| 15 | < 10> | [On] | [No] | <Format> | <Verify> | <Defaults> |

```
F1  =Help                  Arrow Keys =Select Item          -/+   =Change  [Item]
F2  =Menu

Esc =Abort/Exit            Home/End =Select Item          Enter =Execute <Item>
```

## Field Descriptions

### SCSI Device Identifier

This field indicates the device's SCSI Identifier.

### Device Identifier

This field indicates the ASCII device identifier string extracted from the device's Inquiry Data.

### Sync Rate (MB/Sec and MT/Sec)

MB/Sec displays the maximum synchronous data transfer rate [0/ 5/ 10/ 20/ 40/ or 160] of the adapter in mega bytes per second corresponding to the width and transfer rate settings that follow.



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MT/Sec is a configuration field where these values [0/ 5/ 10/ 20/ 40/ or 80] can be changed. This field indicates the maximum synchronous data transfer rate of the adapter in mega transfers per second. It can be changed to a lower transfer rate.

### Data Width

This field indicates the maximum data width in bits.

### Scan ID

This field indicates whether to scan for this SCSI identifier at boot time. This item can be used to ignore a device and to decrease boot time by disabling the inquiry of unused SCSI identifiers.

Set this option to "No" if there is a device that you do not want to be available to the system. Also, on a bus with only a few devices attached, the user can speed up boot time by changing this setting to "No" for all unused SCSI IDs.

### Scan LUNs > 0

This field indicates whether to scan for LUNs greater than zero for a device. LUN zero is always queried. This option should be used if a multi-LUN device responds to unoccupied LUNs or if it is desired to reduce the visibility of a multi-LUN device to LUN zero only.

Set this option to "No" if you have problems with a device that responds to all LUNs whether they are occupied or not. Also, if a SCSI device with multiple LUNs exists on your system but you do not want all of those LUNs to be available to the system, then set this option to "No." This will limit the scan to LUN 0 only.

### Disconnect

This field indicates whether to allow a device to disconnect during SCSI operations. Some (mostly newer) devices run faster with disconnect enabled, while some (mostly older) devices run faster with disconnect disabled.

### SCSI Timeout

This field indicates the maximum amount of time [0 to 9999] in seconds to wait for a SCSI operation to complete.

Since timeouts provide a safeguard that allows the system to recover should an operation fail, it is recommended that a value greater than zero be used. A value of zero allows unlimited time for an operation to complete and could result in the system hanging (waiting forever) should an operation fail.

Press Enter, type in a value, and then press Enter again to specify a new timeout value.



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## Queue Tags

This field indicates whether to allow the use of queue tags for a device. Currently the BIOS does not use queue tags. This item specifies queue tag control to higher level device drivers.

## Boot Choice

This field indicates whether this device may possibly be selected as the boot device. This option is only applicable to devices attached to adapter number zero (in the boot list) on non-BBS systems. It provides primitive BBS flexibility to non-BBS systems.

## Format

Press Enter to low-level format the device. If enabled, this option allows low-level formatting on a disk drive. Low-level formatting will completely and irreversibly erase all data on the drive.

**NOTE:** Formatting will default the drive to a 512-byte sector size even if the drive had previously been formatted to another sector size.

## Verify

Press Enter to verify all sectors on the device and to reassign defective Logical Block Addresses (LBAs).

## Restore Defaults

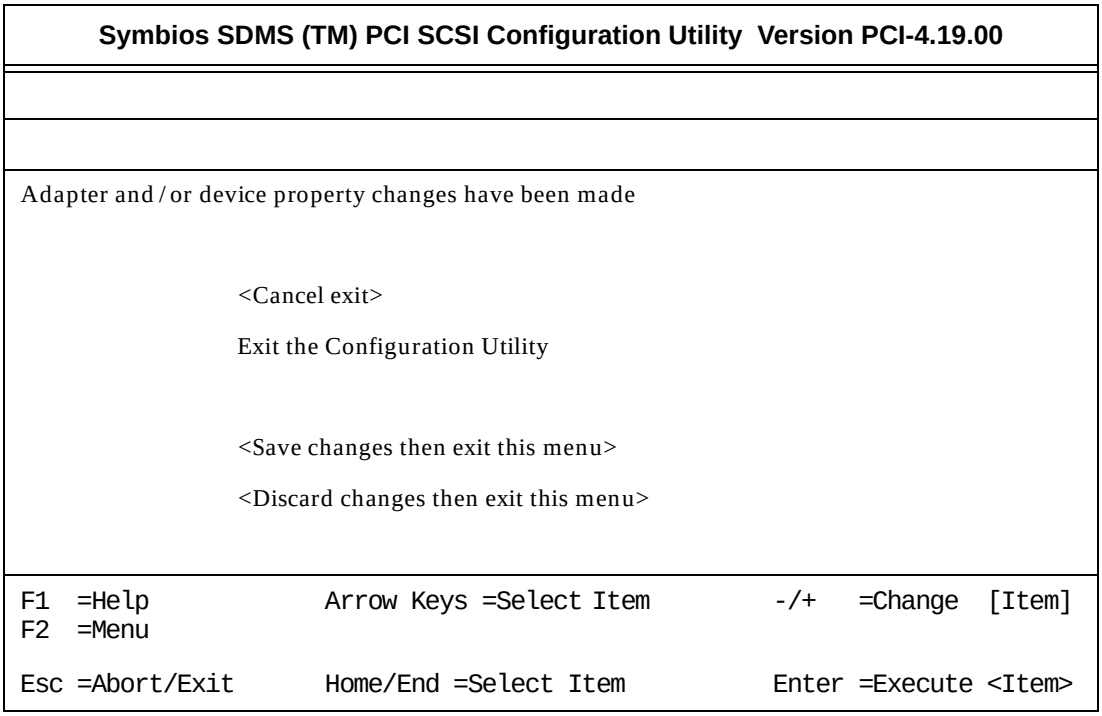
Press Enter to obtain default settings.



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## Exiting the SCSI BIOS Configuration Utility

The Exit menu for the SCSI BIOS Configuration Utility is used for all five of the configuration menus. However, the available functionality is different for the Main menu and the four subordinate menus. Here is an example of the Exit menu:




To exit from the Adapter Properties, Device Properties, Boot Adapter List or Global Properties menus, use these exit options:

### Cancel Exit

This option returns you to the previous menu.

### Save changes then exit this menu

This option implements any changes you made on the previous menu and returns you to the Main menu.

### Discard changes then exit this menu

This option restores the default settings and returns you to the Main menu.



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To exit from the Main menu, use these exit options:

## Cancel Exit

This returns you to the Main menu.

## Exit the Configuration

This option exits the configuration utility and automatically reboots your system.

**NOTE:** If you reboot the system without properly exiting from this utility, some changes may not take effect.



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Appendix

F

# Sample C Software

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## Introduction

This appendix provides listings of a library of sample code that the programmer may utilize to build applications. These files are provided in the directory "\sample code" on CD 385-000067-000, labeled "Windows Drivers", included with the VMIVME-7765.

These files are provided without warranty. All source code is ©2001, VMIC Corporation.

### Directory \VME

This directory contains code used to set up the Universe IIB chip with one PCI-to-VME window and enable Universe IIB registers to be accessed from the VMEbus to allow mailbox access.

### Directory \fpga

This directory contains code used to test the functions of the VMIC-designed FPGA such as timers and the Watchdog Timer.



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## Directory \include

This directory contains common files required to compile several of the sample code applications.

## Directory \max1805

This directory contains code that demonstrates how to read the temperatures from the max1617 device on the VMIVME-7765.

## Directory \support

This directory contains memory and PCI access routines used by many of the sample code applications.



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