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VMIVME-HSDA

VMEbus-TO-ENCORE HSD/IBL INTERFACE

INSTRUCTION MANUAL

DOCUMENT NO. 500-000111-000 P

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VMIVME-HSDA
VMEbus-TO-ENCORE HSD/IBL INTERFACE

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SECTION 1

INTRODUCTION

1.1 INTRODUCTION

The VMIVME-HSDA, shown in Figure 1.1-1, is a 32-bit high performance DMA Interface designed to be compatible with the VMEbus and the Encore High-Speed Data (HSDA) Interface Model 9132 and Encore Model 9136 Inter-bus Link (IBL). Its features include:

a. 32-bit DMA transfers
b. HSD compatibility
c. IBL compatibility
d. Operates as an HSD slave or HSD master (Revision F board)
e. Also operates as an IBL high priority interface or IBL low priority interface
f. Two board set can be used as a VME-to-VME Link
g. VMEbus (IEEE P1014) compatible
h. Programmable interrupt vectors and levels
i. Programmable VMEbus address modifiers
j. Fail LED
k. Switch selectable board address
l. Uses VME short I/O address space for on-board register addressing

NOTICE

WHEN THE VMIVME-HSDA IS USED IN THE ENCORE EF "MASTER" MODE, THE VMEbus PROCESSOR MUST BE CAPABLE OF 32-BIT TRANSFERS INTO SHORT I/O ADDRESS SPACE.

1.2 FUNCTIONAL DESCRIPTION

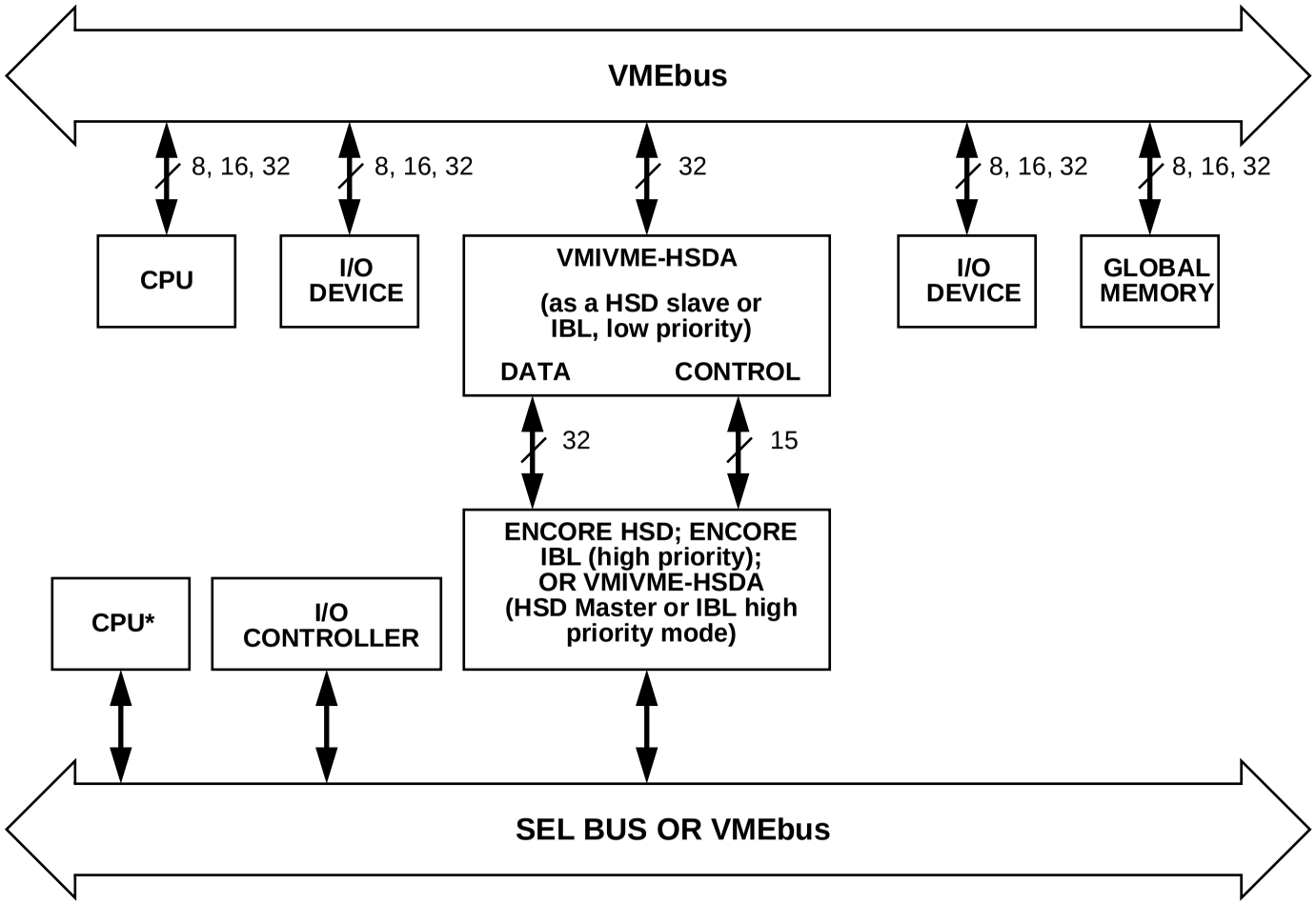
The VMIVME-HSDA provides a high performance 32-bit DMA Link between the VMEbus and the Encore HSD Model 9132 and Encore Model 9136 Inter-bus Link (IBL). The VMIVME-HSDA incorporates a 68430 DMA controller chip to perform its DMA transfers and provides the logic necessary to control the VMEbus during transfers to/from the Encore HSD. The VMIVME-HSDA also contains logic to implement a VMEbus interrupter and logic to allow the VMEbus to interrupt the Encore HSD. A VMEbus-to-HSD Link block diagram is shown in Figure 1.2-1.

1.3 REFERENCE MATERIAL LIST

The reader should refer to "The VMEbus Specification" for a detailed explanation of the VMEbus. "The VMEbus Specification" is available from the following source:

MHSDA/F1.1-1

Figure 1.1-1. VMIVME-HSDA



*For VMEbus-to-VMEbus Links, the CPU must support 32-bit transfers into short I/O address space. All 68020 base CPU boards do not necessarily support this requirement.

MHSDA/F1.2-1

Figure 1.2-1. Encore-to-VMEbus System Block Diagram

VITA
VMEbus International Trade Association
10229 N. Scottsdale Rd.
Scottsdale, AZ 85253
(602) 951-8866

Additional information concerning the HSDA protocols is contained in the Encore 32 Series "High-Speed Data Interface Model 9132", Technical Manual Publication Number 303-000270-200 which is available from the following source:

Encore Inc., Computer Systems Division
6901 W. Sunrise Blvd.
Fort Lauderdale, FL 33340-9148
(305) 587-2900

The SCB68430 manufactured specifications are included in Appendix B to this manual. Specific information concerning the SCB68430 may be obtained from the following source:

Signetics Corporation
811 E. Arques Ave.
P.O. Box 3409
Sunnyvale, CA, 94088-3409
(408) 991-2000

SECTION 2

PHYSICAL DESCRIPTION AND SPECIFICATIONS

REFER TO 800-000111-000 SPECIFICATION

SECTION 3

THEORY OF OPERATION

3.1 OPERATIONAL OVERVIEW

The VMIVME-HSDA Board provides an interface between the VMEbus and the Encore Model 9136 High-Speed Inter-bus Link (IBL). The VMIVME-HSDA can be configured to operate in the IBL MODE or in the EF MODE (under software control). A functional block diagram of the VMIVME-HSDA is shown in Figure 3.1-1.

Interface signals utilized by the VMIVME-HSDA are shown interconnected in Figures 3.1-2 and 3.1-3. As shown in Figure 3.1-2, the signal mnemonics used in this manual are identical to those used in the Encore HSD/IBL Interface. Interface signal functions are described in Section 3.3 and timing relationships are shown in Figures 3.1-4 and 3.1-5.

3.2 IBL MODE LINK CONTROL ARBITRATION

When configured in the IBL MODE this interface allows two computers to arbitrate for control of the link. Each computer can request control of the link. The first computer to generate a request is granted control of the link. However, when both requests are generated simultaneously the interface selected as high priority is granted the link. One interface board must be designated as high priority mode and the other as low priority. A jumper is provided on the Encore HSD Board; whereas, for the VMIVME-HSDA Board the priority is selected in software.

Arbitration for control of the link is controlled by four signals on the VMIVME-HSDA Board: a. LINK REQUEST OUT, b. LINK REQUEST IN, c. LINK ACKNOWLEDGE CMD (to acknowledge the LINK REQUEST IN signal), and d. LINK ACKNOWLEDGE STATUS (receive acknowledge for the LINK REQUEST OUT Signal).

All signals on the VMIVME-HSDA Board are connected to the cable in such a manner that the VMIMVE-HSDA Board can operate with the Encore HSD Board via a flat cable. Two VMIVME-HSDA Boards can also operate back-to-back over a flat cable. Thus, there is no need for a specially wired cable.

The VMIVME-HSDA Board provides for the generation of an interrupt upon the assertion of the LINK REQUEST IN signal and for the LINK ACKNOWLEDGE IN signal.

Arbitration of the link is handled by software for the VMIVME-HSDA Board. Two sets of software routines are required: one set for the high priority mode and one set for the low priority mode.

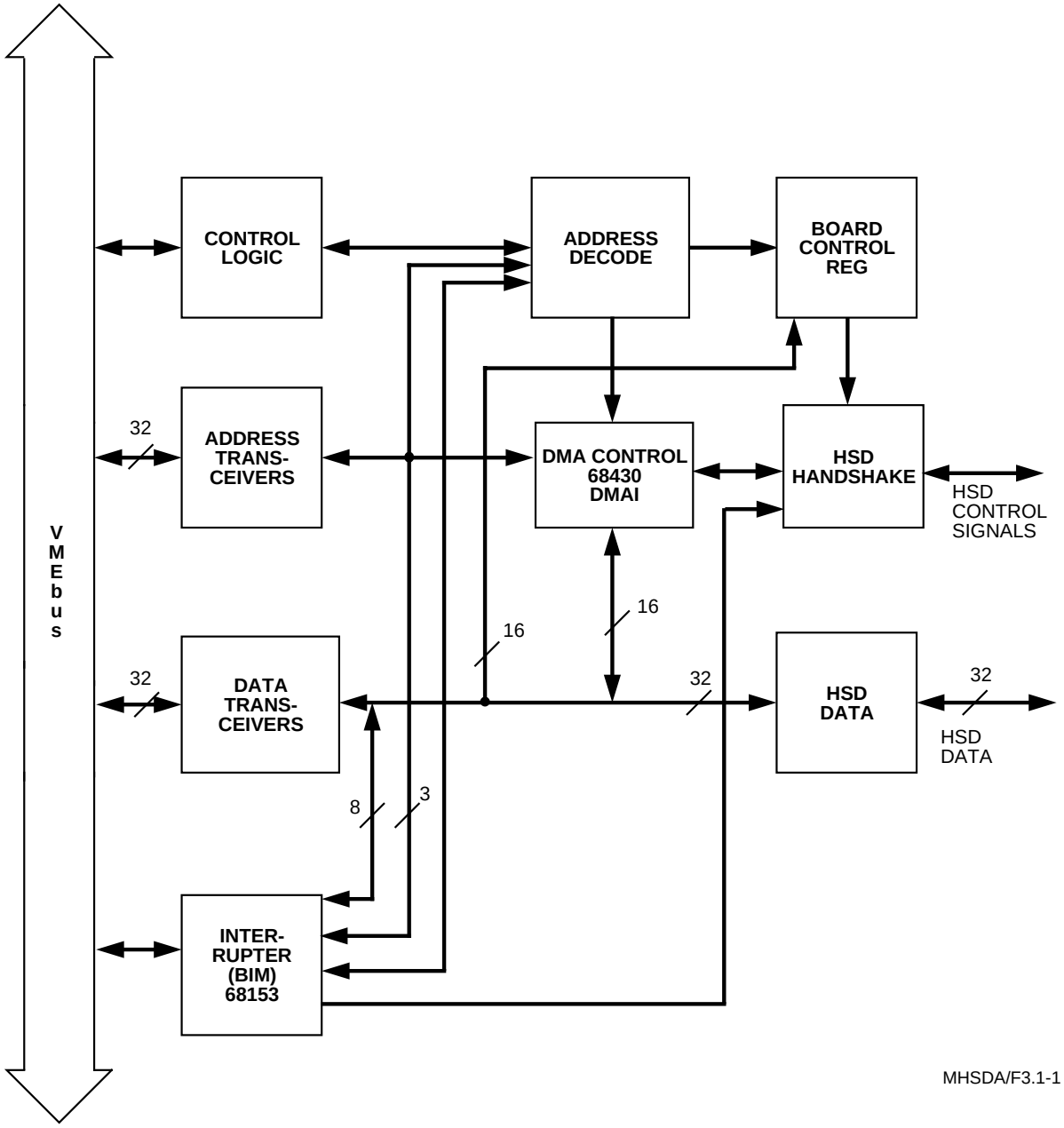
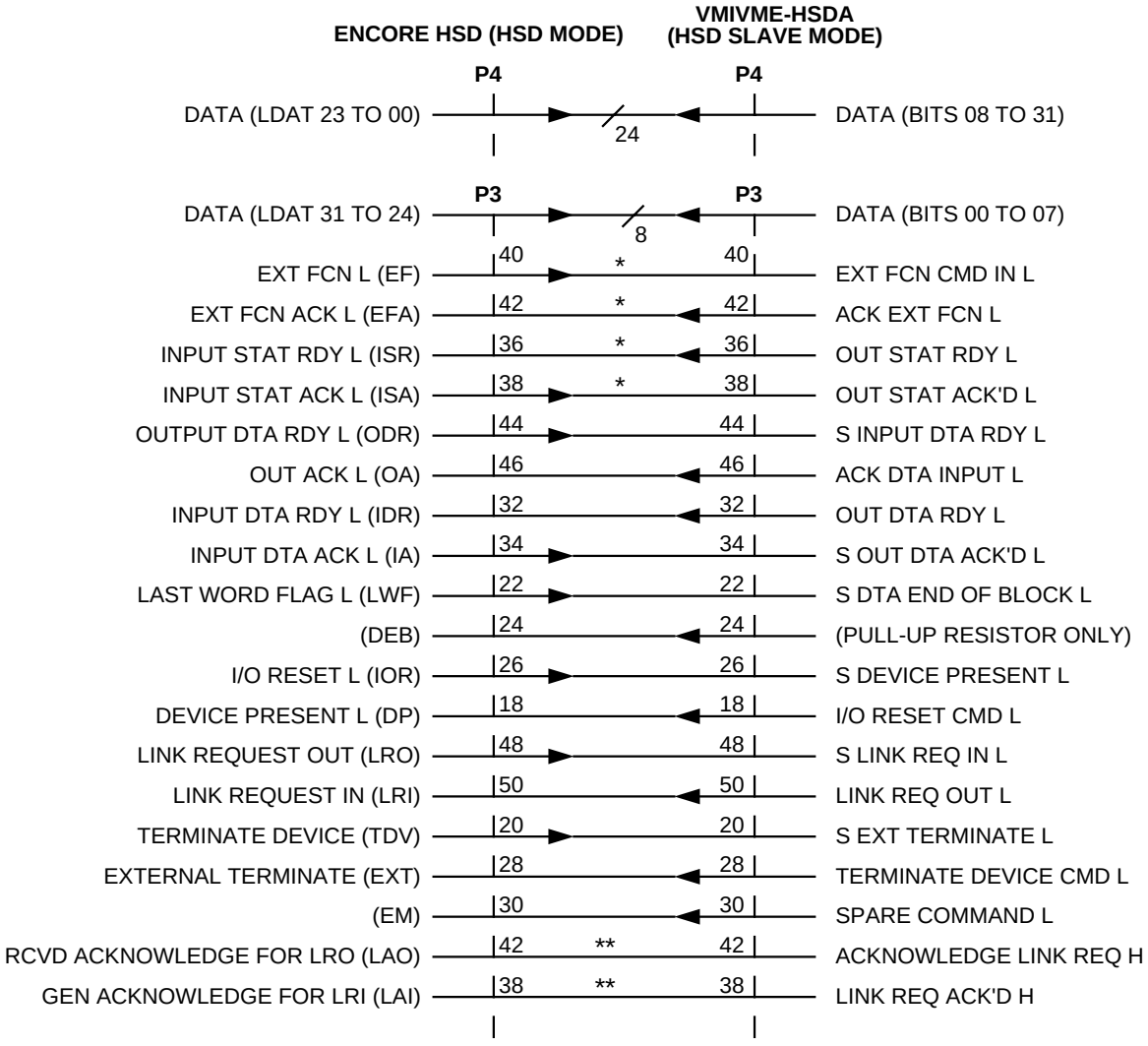


Figure 3.1-1. VMIVME-HSDA Block Diagram



*Signals used in HSD mode only.
**Signals used in IBL mode only.

MHSDA/F3.1-2

Figure 3.1-2. Interface Interconnection for the VMIVME-HSDA Connected to the Encore HSD

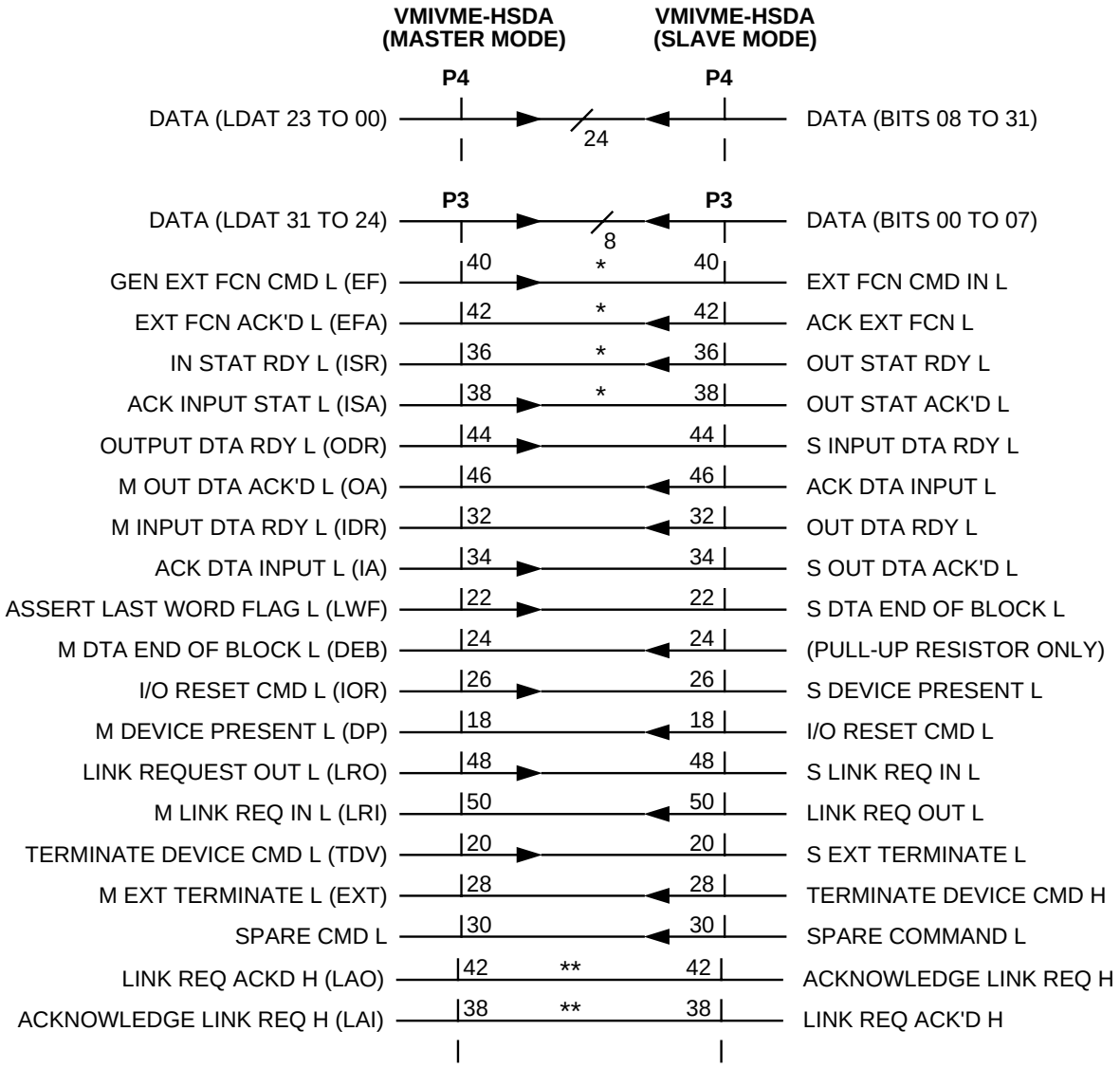


Figure 3.1-3. Interface Interconnection for Two VMIVME-HSDAs Connected Back-to-Back

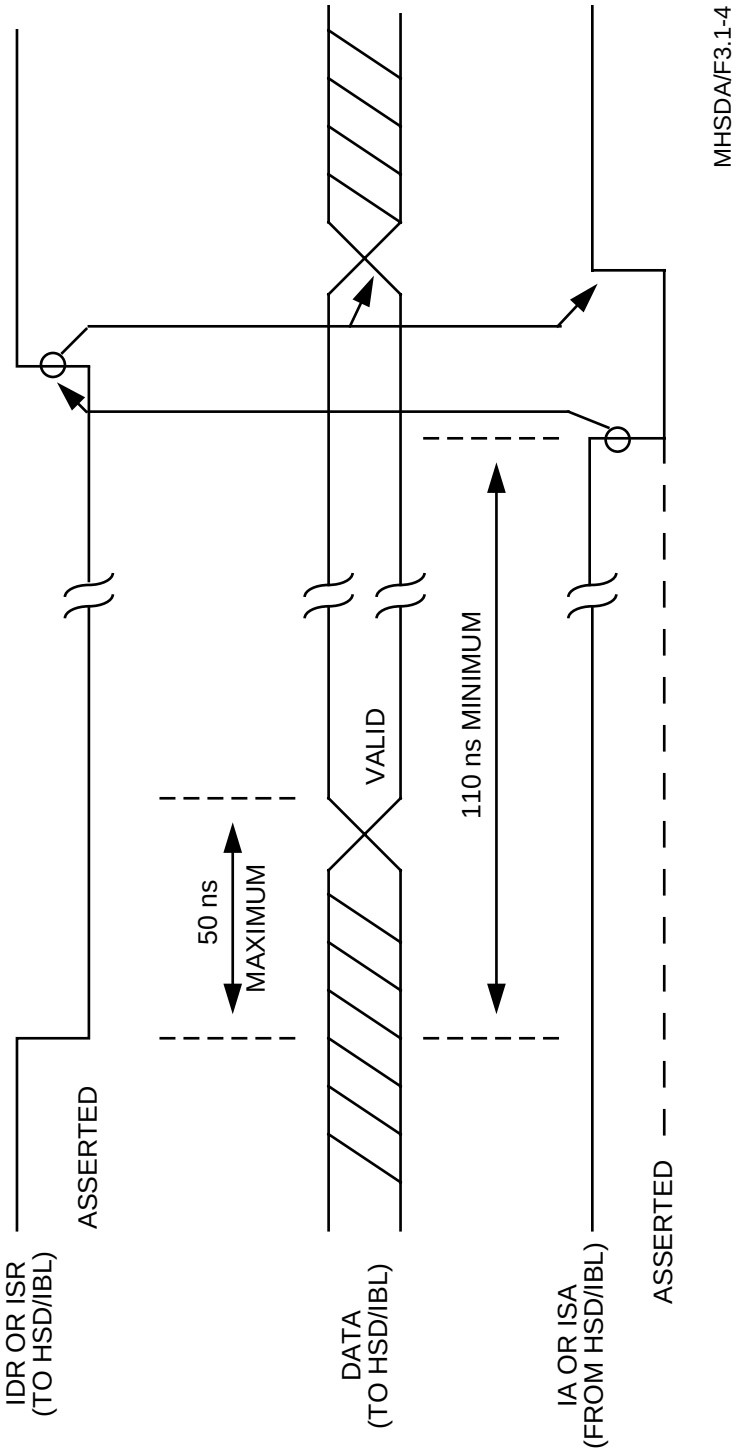
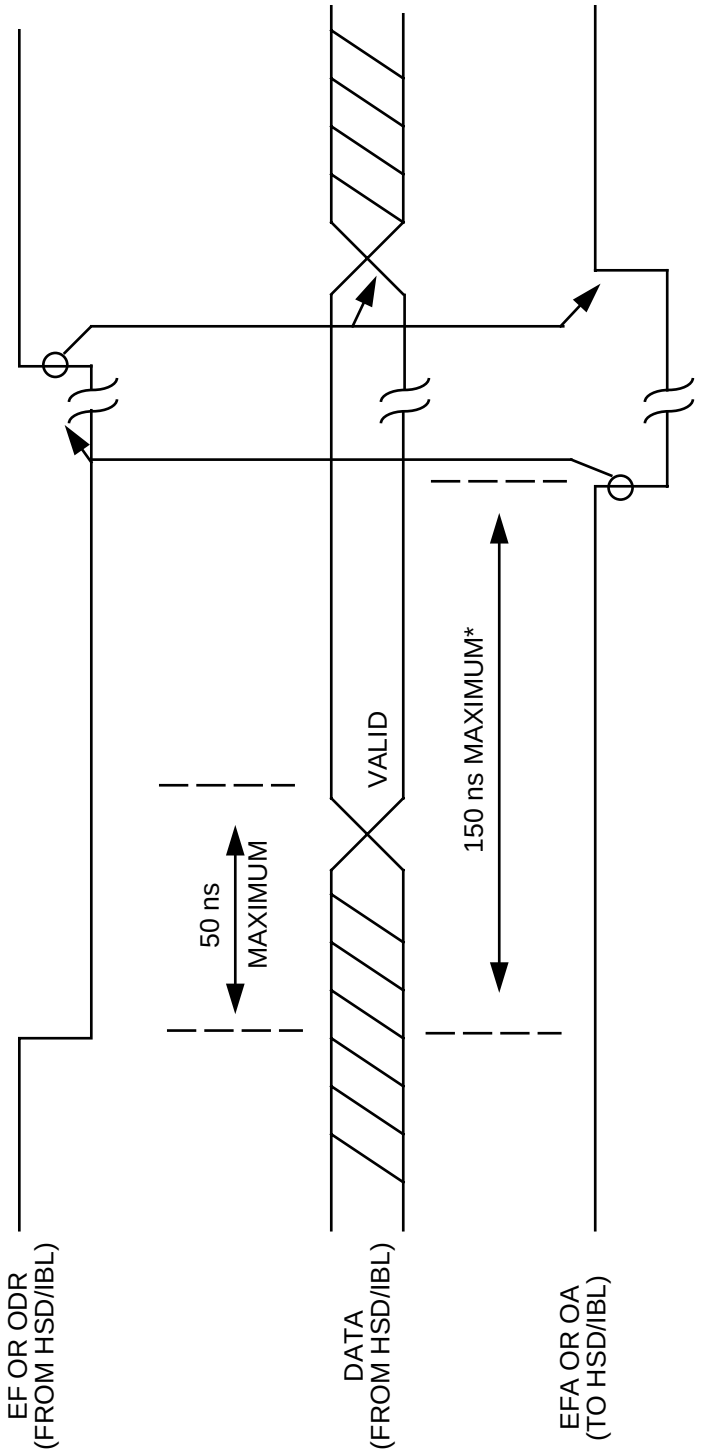


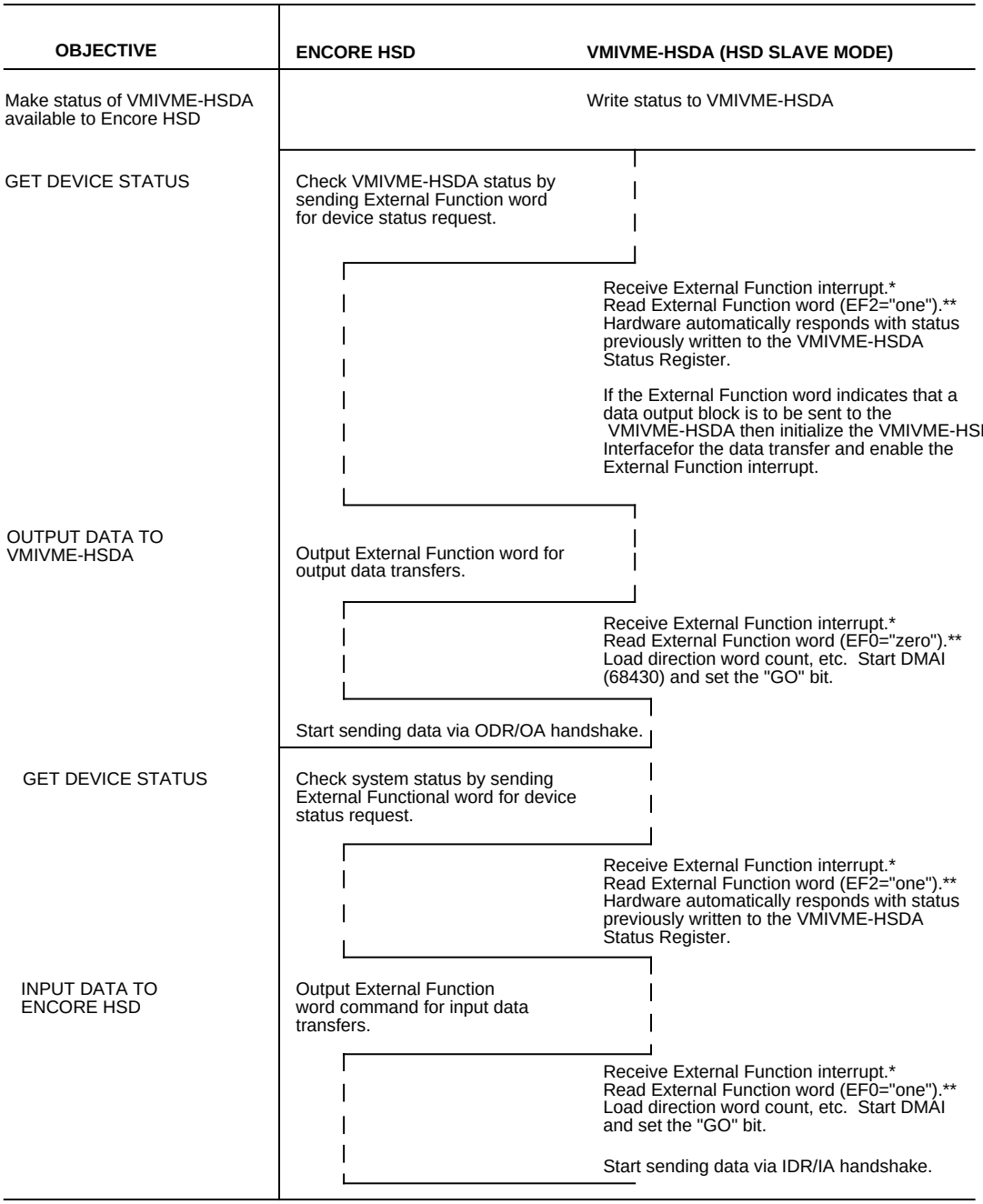
Figure 3.1-4. Input Data Cycle (to Encore HSD/IBL) Timing Relationship



*150 ns will sustain maximum HSD/IBL transfer rate. Longer times will merely decrease this rate.

MHSDA/F3.1-5

Figure 3.1-5. Output Data Cycle (from Encore HSD/IBL) Timing Relationship

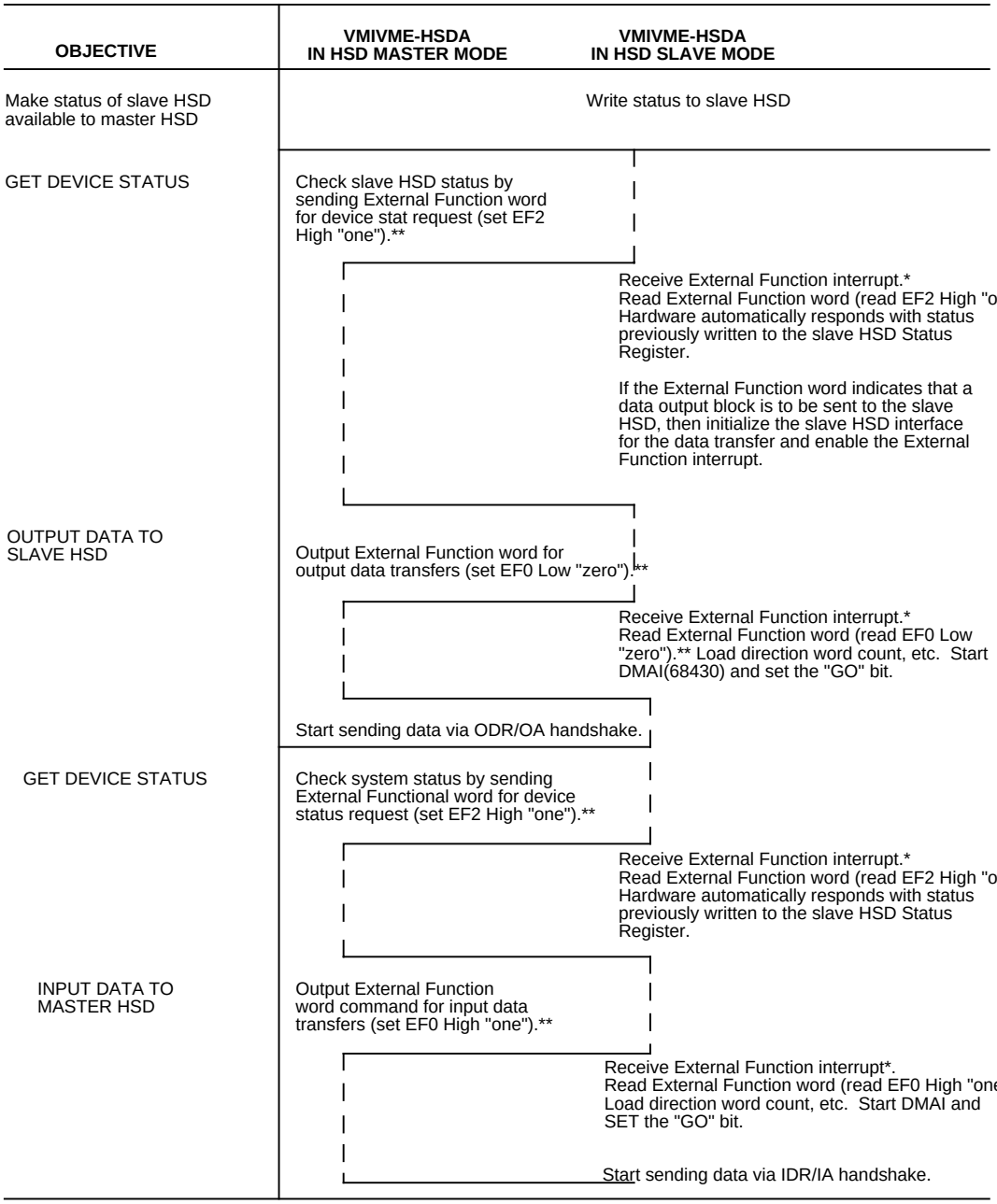


*The External Function Interrupt enable bit (Board Control Register bit 02) must be set. It is automatically cleared when the interrupt occurrs.

**The EF word is 32 bits with EF0 being the Most Significant Bit (MSB).

MHSDA/F3.2-1

Figure 3.2-1. Typical Sequence of Sending Data, Retrieving Status, and Receiving Data When the VMIVME-HSDA (HSD Slave Mode) is Interfaced to an Encore HSD



*The External Function Interrupt enable bit (Board Control Register bit 02) must be set. It is automatically cleared when the interrupt occurrs.

**The EF word is 32 bits with EF0 being the Most Significant Bit (MSB).

MHSDA/F3.2-2

Figure 3.2-2. Typical Sequence of Sending Data, Retrieving Status, and Receiving Data When Two VMIVME-HSDAs are Interfaced Back-to-Back (HSD Mode)

3.2.1 High Priority Link Arbitration Mode (IBL Mode)

High priority arbitration software consists of two routines which use a semaphore to determine which interface is granted control of the link. The two routines used are the LINK REQUEST OUT routine which is used to request the link, and a LINK REQUEST IN interrupt routine which processes the LINK REQUEST IN interrupt.

The LINK REQUEST OUT routine tests and sets (if not already set) the link busy semaphore. If the semaphore was already set it returns a flag indicating that the link is busy, i.e., under control of the other interface. If the semaphore was not already set (it is then set) the routine generates a link request to the other interface and waits for an acknowledge response. The response should be rapid. When the acknowledge response is received the routine clears the link request to the other interface and then returns a flag indicating that this interface is in control of the link.

The LINK REQUEST IN interrupt routine tests and sets (if not already set) the link busy semaphore. If the semaphore was already set it re-enables the LINK REQUEST IN interrupt and does a return from interrupt (since the link is busy, i.e., under control of the other interface). If the semaphore was not already set (it is then set) the routine generates a LINK ACKNOWLEDGE to the other interface, thus placing the other interface board in control of the link. It then monitors the LINK REQUEST IN signal and clears the LINK REQUEST OUT signal as soon as the LINK REQUEST IN signal is cleared.

A protocol must be established for clearing the link busy semaphore when set by a LINK REQUEST IN from the other interface. The link busy semaphore should be cleared as soon as a predetermined transfer sequence is completed.

3.2.2 Low Priority Link Arbitration Mode (IBL Mode)

Low priority arbitration software consists of two routines which monitor the LINK REQUEST IN signal to determine which interface is granted control of the link. The two routines used are the LINK REQUEST OUT routine which is used to request the link, and a LINK REQUEST IN interrupt routine which processes the LINK REQUEST IN interrupt.

The LINK REQUEST OUT routine checks the LINK REQUEST IN signal. If the LINK REQUEST IN signal is set it returns a flag indicating that the link is busy, i.e., under control of the other interface. If the LINK REQUEST signal is not set it generates a link request to the other interface and waits for an acknowledge response. The response should be rapid. While waiting it monitors the LINK REQUEST IN signal; if this signal gets set this routine will clear the LINK REQUEST OUT signal and return a flag indicating that the link is busy, i.e., under control, of the other interface. If the LINK ACKNOWLEDGE response is received the routine

clears the LINK REQUEST OUT signal and returns a flag indicating that this interface is in control of the link.

The LINK REQUEST IN interrupt routine generates a LINK ACKNOWLEDGE to the other interface, thus placing the other interface board in control of the link. It monitors the LINK REQUEST IN signal and clears the LINK ACKNOWLEDGE to the other interface when the LINK REQUEST IN signal becomes inactive.

The user must set up a protocol for clearing the semaphore in the other computer. The semaphore can be cleared at the end of a single block transfer (for simplicity).

3.3 DATA TRANSFER PROTOCOL

The VMIVME-HSDA is compatible with the command chaining and data chaining (single cycle mode only) features of the Encore HSD.

When the VMIVME-HSDA transfers data blocks to or from another VMIVME-HSDA Interface, it becomes the VMEbus master and transfers the data via DMA transfers to or from memory. It asserts the VMEbus address, control lines, address modifier, and sends or receives data. The data transfers are controlled by a 68430 DMA Interface chip. Handshake signals to/from the 68430 are converted to or from VMIVME-HSDA compatible handshake signals.

3.4 SIGNAL FUNCTIONAL DESCRIPTION

The VMIVME-HSDA can be programmed to operate as an HSD master, an HSD slave, or an IBL Interface. The SYSRESET signal on the VMEbus resets the Master Control Register (MCR) and places the VMIVME-HSDA in the slave mode (Encore compatible mode); however, when the MASTER MODE bit in the MCR is set to a "one" the VMIVME-HSDA operates in master mode and all control signals reverse direction (inputs become outputs and vice versa).

The primary function of the MASTER MODE bit is to control cable interface transceiver direction; however, in the HSD EF mode, the MASTER MODE bit also configures the EF/status handshake logic.

3.4.1 Slave Mode Signal Functional Description

To support the HSD master mode, the VMIVME-HSDA requires a VMEbus CPU that is capable of 32-bit transfers into short I/O Address space. (All 68020 CPUs do not necessarily support this capability.)

The slave mode will always be selected when interfacing to an Encore Computer via a flat cable (both HSD EF mode or IBL mode). The slave mode is selected by clearing bit 7 of the Master Control Register (MASTER MODE bit).

**LAO - ACKNOWLEDGE LINK REQ H (OUTPUT ON PIN 42). This signal indicates to the Encore IBL Board that the VMIVME-HSDA Board has granted control of the link to the Encore Board.

**LAI - LINK REQUEST ACKNOWLEDGED H (INPUT ON PIN 38). This signal indicates that the Encore IBL Board has granted control of the interface to this board.

*EF - EXTERNAL FUNCTION COMMAND IN (INPUT ON PIN 40). This signal output from the master HSD indicates that it has placed Function (Command) Data on the Data Bus. EF remains asserted until the slave HSD returns EFA. When the External Function Interrupt enable bit is set, the VMIVME-HSDA will latch the Function Data into the External Functional Register and assert Acknowledge Enternal Function (EFA); then, if the EF bit 2 in the External Function Register is a "one" the VMIVME-HSDA will assert the output status READY signal.

*EFA - ACKNOWLEDGE EXTERNAL FUNCTION (OUTPUT ON PIN 42). This signal indicates to the Encore HSD that the Function (Command) Data has been latched by the VMIVME-HSDA. EFA remains active until EF goes inactive.

*ISR - OUTPUT STATUS READY (OUTPUT ON PIN 36). This signal indicates to the Encore HSD that status information is present on the data lines. This signal is automatically asserted by the VMIVME-HSDA 490 nanoseconds after it asserts the Acknowledge External Function signal providing that status was requested by the Encore HSD (External Function Command bit EF2=1).

*ISA - OUTPUT STATUS ACKNOWLEDGED (INPUT ON PIN 38). This signal is asserted by the Encore HSD to indicate that it has latched the status information. The VMIVME-HSDA immediately releases the OUTPUT STATUS READY (ISR) signal when ISA is received from the Encore HSD.

ODR - SLAVE INPUT DATA READY (INPUT ON PIN 44). This signal indicates that the Encore HSD has placed output data for the VMIVME-HSDA on the Data Bus. ODR remains asserted until the VMIVME-HSDA returns OA.

OA - ACKNOWLEDGE DATA INPUT (OUTPUT ON PIN 40). This signal indicates to the Encore HSD that the VMIVME-HSDA has latched the output data. It remains asserted until ODR goes inactive.

*Used in HSD mode only.
**Used in IBL mode only.

IDR - OUTPUT DATA READY (OUTPUT ON PIN 32). This signal indicates to the Encore HSD that input data for the HSD has been placed on the Data Bus. IDR remains asserted until the other board returns IA.

IA - SLAVE OUTPUT ACKNOWLEDGED (INPUT ON PIN 34). This signal output from the Encore HSD indicates that it has latched the input data. IA remains asserted until IDR goes inactive.

LWF - SLAVE DATA END OF BLOCK (INPUT ON PIN 22). When this flag accompanies an ODR in Output Mode or an IA in Input Mode, it indicates to the VMIVME-HSDA that the current transfer is the end of the block.

IOR - SLAVE DEVICE PRESENT (INPUT ON PIN 26). This signal, when absent, causes the VMIVME-HSDA handshaking circuiting to be reset. However, the Master Control Register is not cleared by this signal.

DP - I/O RESET COMMAND (OUTPUT ON PIN 18). This signal indicates to the Encore HSD that the VMIVME-HSDA is connected and powered up.

LRO - SLAVE LINK REQUEST IN (INPUT ON PIN 48). Level signal sent from the Encore HSD indicating a desire to transfer data. The level remains true until LAO is returned by the VMIVME-HSDA. LRO may also be reset by the firmware in the sending HSD.

LRI - LINK REQUEST OUT (OUTPUT ON PIN 50). Level signal sent to the Encore HSD indicating a desire by the VMIVME-HSDA to transfer data. This output signal is generated by the Master Control Register.

TDV - SLAVE EXTERNAL TERMINATE (INPUT ON PIN 20). Asynchronous signal sent to the VMIVME-HSDA to indicate an unusual terminate condition in the Encore HSD. The VMIVME-HSDA receiving this should not attempt to send or receive more data. The Encore HSD sending this signal will store its normal error and SI status; thus, indicating the condition which caused the TDV.

EXT - TERMINATE DEVICE COMMAND (OUTPUT ON PIN 28). This is an Asynchronous Signal which indicates to the Encore HSD that an unusual terminate condition has occurred. This results in the generation of an interrupt by the Encore HSD.

EM - SPARE COMMAND (OUTPUT ON PIN 30). The VMIVME-HSDA does NOT provide any hardware support for the external mode of the Encore HSD.

3.4.2 Master Mode Signal Functional Description

The following paragraphs describe the HSD signals used by the VMIVME-HSDA in the master mode. The Encore mnemonic is listed for each signal followed

by the signal name utilized on the VMIVME-HSDA schematic. See Figure 3.1-3 for signal interconnection between two VMIVME-HSDA Boards connected back-to-back.

**LAO - LINK REQ ACK'D H (INPUT ON PIN 42). This signal indicates that the other IBL Board has granted the link to this VMIVME-HSDA Board.

**LAI - ACKNOWLEDGE LINK REQUEST H (OUTPUT ON PIN 38). This signal indicates that this board is granting control of the interface to the other board.

*EF - GEN EXTERNAL FUNCTION COMMAND (OUTPUT ON PIN 40). This signal output from the master HSD indicates that it has placed Function (Command) Data on the Data Bus. EF remains asserted until the slave HSD returns EFA. When the External Function Interrupt enable bit is set, the slave HSD will latch the Function Data into the External Functional Register and assert Acknowledge External Function (EFA); then, if the EF2 bit in the External Function Register is a "one" the slave HSD will assert the output status READY (ISR) signal.

*EFA - EXTERNAL FUNCTION ACKNOWLEDGE (INPUT ON PIN 42). This signal indicates to the master HSD that the Function (Command) Data has been latched by the slave HSD. EFA remains active until EF goes inactive.

*ISR - INPUT STATUS READY (INPUT ON PIN 36). This signal indicates to the master HSD that status information is present on the data lines. This signal is automatically asserted by the slave HSD 490 nanoseconds after it asserts the Acknowledge External Function signal providing that status was requested by the master (External Function Command bit ED2="one").

*ISA - ACK STATUS INPUT (OUTPUT ON PIN 38). This signal is asserted by the master HSD to indicate that it has latched the status information. The slave HSD immediately releases the output status READY signal when ISA is received from the master HSD.

ODR - OUTPUT DATA READY (OUTPUT ON PIN 44). This signal indicates that the master HSD has placed output data for the slave HSD on the Data Bus. ODR remains asserted until the slave HSD returns OA.

OA - MASTER OUTPUT DATA ACKNOWLEDGE (INPUT ON PIN 40). This signal indicates to the Encore HSD that the slave HSD has latched the output data. It remains asserted until ODR goes inactive.

*Used in HSD mode only.
**Used in IBL mode only.

IDR - MASTER INPUT DATA READY (INPUT ON PIN 32). This signal indicates to the master HSD that input data for the master HSD has been placed on the Data Bus. IDR remains asserted until the master HSD returns IA.

IA - ACKNOWLEDGED DATA INPUT (OUTPUT ON PIN 34). This signal output from the master HSD indicates that it has latched the input data. IA remains asserted until IDR goes inactive.

LWF - ASSERT LAST WORD FLAG (OUTPUT ON PIN 22). When this flag accompanies an ODR in Output Mode or an IA in Input Mode, it indicates to the slave HSD that the current transfer is the end of the block.

DEB - MASTER DATA END OF BLOCK (INPUT ON PIN 24). Flag accompanying the last IDR in the input mode or the last IA in the output mode. Sent from the slave HSD to the master HSD signifying end-of-block. When the master HSD receives DEB it will not try to send more data in the output mode or expect to receive more data in the input mode.

IOR - I/O RESET COMMAND (OUTPUT ON 26). This signal, when absent, causes the slave HSD handshaking circuiting to be reset. However, the Master Control Register is not cleared by this signal.

DP - MASTER DEVICE PRESENT (INPUT ON PIN 18). This signal indicates to the master HSD that the slave HSD is connected and powered up.

LRO - LINK REQUEST OUT (OUTPUT ON PIN 48). Level signal sent from the master HSD indicating a desire to transfer data. The level remains true until LAO is returned by the slave HSD. LRO is controlled by the firmware in the sending HSD.

LRI - MASTER LINK REQUEST IN (INPUT ON PIN 50). Level signal sent to the master HSD indicating a desire by the slave HSD to transfer data. This output signal is generated by the Master Control Register in the slave HSD.

TDV - TERMINATE DEVICE COMMAND (OUTPUT ON PIN 20). Asynchronous signal sent to the slave HSD to indicate an unusual terminate condition in the master HSD. The slave HSD receiving this signal should not attempt to send or receive more data. The master HSD sending this signal should store its normal error and status; thus, indicating the condition which caused the TDV.

EXT - MASTER EXTERNAL TERMINATE (INPUT ON PIN 28). This is an Asynchronous Signal which indicates to the master HSD that an unusual terminate condition has occurred. This results in the generation of an interrupt by the master HSD.

EM - SPARE COMMAND (OUTPUT ON PIN 30). The VMIVME-HSDA does NOT provide any hardware support for the external mode.

SECTION 4

PROGRAMMING

4.1 PROGRAMMING OVERVIEW

The VMIVME-HSDA has three types of devices that must be programmed for proper operation. These are the SCB68430 DMA controller module, the MC68153 Bus Interrupter Module (BIM), and on-board registers. The on-board registers are provided to allow the user the capability of programming the address modifiers, to interrupt the Encore HSD/IBL, and to provide control of handshaking between the DMA chip, the BIM chip, and the HSD/IBL Interface. Programming the VMIVME-HSDA includes executing a transfer protocol (see Section 3.2), handling interrupts, and handling errors for the IBL mode. The user must also execute a link control protocol (see Section 3.3) .

A register address map is shown in Table 4.1-1 and the function of individual bits in each register are described in Section 4.3. Sample software listings are provided in Appendix C. Data sheets on the MC68153 and SCB68430 are provided in Appendix B.

When the VMIVME-HSDA is used in the "Encore HSD Master" mode, a VMEbus CPU is required that supports 32-bit transfers into short I/O address space.

4.2 SEQUENCE OF REGISTER LOADING FOR DATA BLOCK TRANSFER

The VMIVME-HSDA is designed such that the first word in will not be missed even though it is clocked into the Input Data Register (IDR) before the VMIVME-HSDA is set up to receive it. Note that when the VMIVME-HSDA is selected as the HSD master, its received status is in the IDR and, therefore, the received status data will be overwritten by the first data word received.

The programming sequence of the VMIVME-HSDA should be as follows to transfer a block of data:

a. Load the registers in the 68153 and 68430.
b. The CCR should be the last register loaded in the 68430.
c. Load the address modifier register (on-board).
d. Load the Board Control Register (BCR) (on-board) with the GO bit (bit 0) set to "zero".
e. Reload the BCR with the GO bit set to "one".

Table 4.1-1. VMIVME-HSDA Register Address Map

HEX ADDRESS	ACRONYM	REGISTER NAME	PHYSICAL LOCATION
00	CSR	Channel Status Register	SCB68430 DMAI, U17
01	CER	Channel Error Register	SCB68430 DMAI, U17
04	DCR	Device Control Register	SCB68430 DMAI, U17
05	OCR	Operation Control Register	SCB68430 DMAI, U17
06	SCR*	Sequence Control Register	SCB68430 DMAI, U17
07	CCR	Channel Control Register	SCB68430 DMAI, U17
0A	MTCH	Memory Transfer Count High	SCB68430 DMAI, U17
0B	MTCL	Memory Transfer Count Low	SCB68430 DMAI, U17
0C	MACH*	Memory Address Counter High	SCB68430 DMAI, U17
0D	MACMH	Memory Address Count Mid-High	SCB68430 DMAI, U17
0E	MACML	Memory Address Counter Mid-Low	SCB68430 DMAI, U17
0F	MACL	Memory Address Counter Low	SCB68430 DMAI, U17
25	DIVR	Interrupt Vector Register	SCB68430 DMAI, U17
27	DIVR***	Interrupt Vector Register	SCB68430 DMAI, U17
2D	CPR*	Channel Priority Register	SCB68430 DMAI, U17
41	ISCR	Input Status Control Register	MC68153 BIM, U24
43	RICR	Restart Interrupt Control Register	MC68153 BIM, U24
45	EICR (CR2)	External Interrupt Control Register	MC68153 BIM, U24
47	DICR (CR3)	DMA Interrupt Control Register	MC68153 BIM, U24
49	ISVR	Input Status Vector Register	MC68153 BIM, U24
4B	RIVR	Restart Interrupt Vector Register	MC68153 BIM, U24
4D	EIVR (VR2)	External Interrupt Vector Register	MC68153 BIM, U24
4F	VR3**	Vector Register 3	MC68153 BIM, U24
61	BCRH	Board Control Register Hi	Sheets 10, 11
63	DSR	Device Status Register	Sheet 16
65	AMR	Address Modifier Register	Sheet 8
66	EFRH	External Function Register Hi	Sheets 19, 20
67	EFRMH	External Function Register Mid-Hi	Sheets 19, 20
68	EFRML	External Function Register Mid-Lo	Sheets 17, 18
69	EFRL	External Function Register Lo	Sheets 17, 18
6A	MCR	Master Control Register	Sheet 15
6B	MSR	Master Status Register	Sheets 15, U29
6D	EMA	Extended Memory Address	Sheets 15, U43
70	ODR	Output Data Register	Sheets 17, 18, 19, 20
70	IDR	Input Data Register	Sheets 17, 18, 19, 20

*Included for software compatibility.
**Register is not used.
***The DIVR has two addresses for software compatibility (see spec sheet).

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Note that the start bit (CCR bit 07) must be set in the 68430 chip before the GO bit is set in the BCR. The start bit in the 68430 is independent of the GO bit in the BCR.

Also, note that when the VMIVME-HSDA is in the slave mode the External Function bit ED0 controls the direction of the data transceivers, while the direction bit in the 68430 (OCR bit 07) controls the transfer direction of the 68430. These two bits must match with regard to transfer direction, i.e., must be in opposite states for correct operation. When the VMIVME-HSDA is in the HSD master mode or in the IBL mode the data transceivers are controlled by or in the IBL mode the Master Control Register (MCR) (bit 1).

An example of register initialization sequence for transmitting data (from memory) is shown in Table 4.2-1. After the first DMA transfer is complete, the VMIVME-HSDA can be re-initialized with only six steps to transmit a second block of data (see Table 4.2-2).

An example of a register initialization sequence for receiving data (transfer to memory) is shown in Table 4.2-3. After the first block transfer is complete, the VMIVME-HSDA can be initialized with only six steps to receive a second block of data (see Table 4.2-4).

4.3 REGISTER BIT DEFINITIONS

For register bit definitions see Tables 4.3-1, 4.3-2, and 4.3-3.

4.4 PROGRAMMING THE SCB68430 DMAI

4.4.1 Channel Status Register (CSR)/Channel Error Register (CER)

These two registers are used together to determine status and error conditions related to the DMA controller.

4.4.1.1 Channel Status Register (CSR)

BIT 15 - CHANNEL OPERATION COMPLETE*. This bit will be set when the DMA operation is complete. If interrupts are enabled, an interrupt will be generated at this time.

BITS 14 and 13. Not used.

BIT 12 - ERROR*. This bit will be set if the DMA operation was terminated due to an error condition.

Table 4.2-1. Register Initialization Sequence for Transmitting a 4 Kword Block Starting Data Address $40000

STEP	REGISTER LOCATION	REGISTER NAME	REGISTER ADDRESS OFFSET	DATA LOADED (HEXADECIMAL)	COMMENT
1	68430	DCR	04	B8	Cycle Steal
2	68430	OCR	05	32	32-bit word from memory
3	68430	MTC	0A	1000	16-bit transfer count
4	68430	MACMH	0D	04	Upper 8 bits of memory address
5	68430	MAC	0E	0000	Lower 16 bits of memory address
6	68430	DIVR	25	46	Done interrupt vector
7	68153	EIVR	4D	45	External function interrupt vector
8	68153	EICR	45	1E	Select internal vector
9	68153	DICR	47	3D	Select external vector
10	On-Board	AMR	65	39	Longword, ADDR MOD=39
11	68430	CSR	00	FF	Clear Channel Status Register
12	68430	CCR	07	88	Start DMA chip
13	On-Board	BCR	61	01	Go

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Table 4.2-2. Register Initialiation Sequence for Transmitting a Second 4 Kword Block Starting Data Address $20000

STEP	REGISTER LOCATION	REGISTER NAME	REGISTER ADDRESS OFFSET	DATA LOADED (HEXADECIMAL)	COMMENT
1	68430	MTC	0A	1000	16-bit transfer count
2	68430	MACMH	0D	02	Upper 8 bits of memory address
3	68430	MAC	0E	0000	Lower 16 bits of memory address
4	68153	DICR	47	3D	Enable interrupts
5	68430	CSR	00	FF	Clear Channel Status Register
6	68430	CCR	07	88	Start DMA chip
7	On-Board	BCR	61	01	Go

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Table 4.2-3. Register Initialization Sequence for Receiving a 4 Kword Block Starting Data Address $40000

STEP	REGISTER LOCATION	REGISTER NAME	REGISTER ADDRESS OFFSET	DATA LOADED (HEXADECIMAL)	COMMENT
1	68430	DCR	04	B8	Cycle Steal
2	68430	OCR	05	B2	32-bit word to memory
3	68430	MTC	0A	1000	16-bit transfer count
4	68430	MACMH	0D	04	Upper 8 bits of memory address
5	68430	MAC	0E	0000	Lower 16 bits of memory address
6	68430	DIVR	25	46	Done interrupt vector
7	68153	EIVR	4D	45	External function interrupt vector
8	68153	EICR	45	1E	Select internal vector
9	68153	DICR	47	3D	Select external vector
10	On-Board	AMR	65	39	Longword, ADDR MOD=39
11	68430	CSR	00	FF	Clear Channel Status Register
12	68430	CCR	07	88	Start DMA chip
13	On-Board	BCR	61	01	Go

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Table 4.2-4. Register Initialization Sequence for Receiving a Second 4 Kword Block Starting Data Address $20000

STEP	REGISTER LOCATION	REGISTER NAME	REGISTER ADDRESS OFFSET	DATA LOADED (HEXADECIMAL)	COMMENT
1	68430	MTC	0A	1000	16-bit transfer count
2	68430	MACMH	0D	02	Upper 8 bits of memory address
3	68430	MAC	0E	0000	Lower 16 bits of memory address
4	68153	DICR	47	3D	Enable interrupts
5	68430	CSR	00	FF	Clear Channel Status Register
6	68430	CCR	07	88	Start DMA chip
7	On-Board	BCR	61	01	Go

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Table 4.3-1. DMAI (68430) Register Bit Definitions

CHANNEL STATUS REGISTER ($XX00) - READ ONLY

CSR

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
CHANNEL OPERATION COMPLETE	NOT USED	NORMAL DEVICE TERMINATE	ERROR	CHANNEL ACTIVE	NOT USED	NOT USED	READY INPUT STATE
0=NO 1=YES	(0)	0=NO 1=YES	0=NO 1=YES	0=NO 1=YES	(0)	(0)	0=0V 1=>2V

CHANNEL ERROR REGISTER ($XX01)

CER

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NOT USED	NOT USED	NOT USED	ERROR CODE				
(0)	(0)	(0)	0000=NO ERROR 01001=BUS ERROR 10001=SOFTWARE ABORT				

DEVICE CONTROL REGISTER ($XX04)

DCR

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
EXTERNAL REQUEST MODE	NOT USED	NOT USED	NOT USED	OCR (5:4) =00 → 0	NOT USED	NOT USED	NOT USED
0=BURST 1=CYCLE STEAL	(0)	(1)	(1)	OCR (5:4) =00 → 1	(0)	(0)	(0)

OPERATION CONTROL REGISTER ($XX05)

OCR

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIRECTION	NOT USED	OPERAND SIZE		NOT USED	NOT USED	NOT USED	NOT USED
0=MEM TO DEV 1=DEV TO MEM	(0)	00=BYTE 01=WORD 10=DUAL 16-BIT WORDS* 11=32-BIT WORD		(0)	(0)	(1)	(0)

*The VMIVME-HSDA Board does not support dual 16-bit word operations.

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Table 4.3-1. DMAI (68430) Register Bit Definitions (Continued)

SEQUENCE CONTROL REGISTER ($XX06)

	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
SCR*	**NOT USED***							
	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

*Dummy register.

CHANNEL CONTROL REGISTER ($XX07)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CCR	START	NOT USED	NOT USED	SOFTWARE ABORT	INTERRUPT ENABLE	NOT USED	NOT USED	NOT USED
	0=NO 1=YES	(0)	(0)	(0)	(0)	(0)	(0)	(0)

MEMORY TRANSFER COUNT HIGH ($XX0A)

	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
MTCH	**MEMORY TRANSFER COUNT MSB**							
	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8

MEMORY TRANSFER COUNT LOW ($XX0B)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MTCL	**MEMORY TRANSFER COUNT LSB**							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

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Table 4.3-1. DMAI (68430) Register Bit Definitions (Continued)

MEMORY ADDRESS COUNTER HIGH ($XX0C)

MACH

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
NOT USED*							
(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

*Dummy Register.

MEMORY ADDRESS COUNTER MID-HIGH ($XX0D)

MACMH

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MEMORY ADDRESS COUNTER							
BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16

MEMORY ADDRESS COUNTER MID-LOW ($XX0E)

MACML

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
MEMORY ADDRESS COUNTER							
BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8

MEMORY ADDRESS COUNTER LOW ($XX0F)

MACL

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MEMORY ADDRESS COUNTER							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

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Table 4.3-1. DMAI (68430) Register Bit Definitions (Concluded)

DMA INTERRUPT VECTOR REGISTER ($XX25. $XX27)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIVR	**DONE INTERRUPT VECTOR**							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	NOTE 1

NOTE 1: This bit is automatically set if an error occurred. This register is mapped to two locations to provide compatibility with other controllers.

CHANNEL PRIORITY REGISTER ($XX2D)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CPR	**NOT USED***							
	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

*Dummy Register.

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Table 4.3-2. BIM (68153) Register Bit Definitions

INPUT STATUS INTERRUPT CONTROL REGISTER ($XX41)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ISCR	FLAG BIT	FLAG BIT AUTO CLEAR	VECTOR 0=INT 1=EXT	INTER-RUPT ENABLE	INTER-RUPT AUTO CLEAR	IRQ LEVEL 2	IRQ LEVEL 1	IRQ LEVEL 0

RESTART INTERRUPT CONTROL REGISTER ($XX43)**

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RICR	FLAG BIT	FLAG BIT AUTO CLEAR	VECTOR 0=INT 1=EXT	INTER-RUPT ENABLE	INTER-RUPT AUTO CLEAR	IRQ LEVEL 2	IRQ LEVEL 1	IRQ LEVEL 0

EXTERNAL INTERRUPT CONTROL REGISTER ($XX45)*

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
EICR	FLAG BIT	FLAG BIT AUTO CLEAR	VECTOR 0=INT 1=EXT	INTER-RUPT ENABLE	INTER-RUPT AUTO CLEAR	IRQ LEVEL 2	IRQ LEVEL 1	IRQ LEVEL 0

DMA INTERRUPT CONTROL REGISTER ($XX47)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DICR	FLAG BIT	FLAG BIT AUTO CLEAR	VECTOR 0=INT 1=EXT	INTER-RUPT ENABLE	INTER-RUPT AUTO CLEAR	IRQ LEVEL 2	IRQ LEVEL 1	IRQ LEVEL 0

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* In IBL mode the EXTERNAL FUNCTION INTERRUPT may be initialized and used to respond to LINK ACKNOWLEDGE (master and slave mode) to avoid polling for LINK ACKNOWLEDGE.

** In IBL mode the RESTART INTERRUPT is initialized and used to respond to LINK REQUESTs to avoid polling for LINK REQUEST input status.

Table 4.3-2. BIM (68153) Register Bit Definitions (Concluded)

INPUT STATUS VECTOR REGISTER ($XX49)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ISVR	**INTERRUPT VECTOR**							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

RESTART INTERRUPT VECTOR REGISTER ($XX4B)**

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RIVR	**INTERRUPT VECTOR**							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

EXTERNAL INTERRUPT VECTOR REGISTER ($XX4D)*

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
EIVR	**EXTERNAL FUNCTION INTERRUPT VECTOR**							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

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* In IBL mode the EXTERNAL FUNCTION INTERRUPT may be initialized and used to respond to LINK ACKNOWLEDGE (master and slave mode) to avoid polling for LINK ACKNOWLEDGE.

** In IBL mode the RESTART INTERRUPT is initialized and used to respond to LINK REQUESTs to avoid polling for LINK REQUEST input status.

Table 4.3-3. Discrete On-Board Register Bit Definitions

BOARD CONTROL REGISTER ($XX61) (WRITE ONLY)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BCR	NOT USED	NOT USED	NOT USED	NOT USED	LED CONTROL 0=OFF 1=ON	ENABLE EXT FCN INTER-RUPT	EXTERNAL TERMINATE	GO

DEVICE STATUS REGISTER ($XX63) (WRITE ONLY)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DSR	**DEVICE STATUS INFORMATION**							
	BIT 24	BIT 25	BIT 26	BIT 27	BIT28	BIT 29	BIT 30	BIT 31

ADDRESS MODIFIER REGISTER ($XX65) (WRITE ONLY)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
AMR	NOT USED	$\overline{\text{LONGWORD}}$	**ADDRESS MODIFIER**					
			AM5	AM4	AM3	AM2	AM1	AM0

EXTERNAL FUNCTION REGISTER HI ($XX66) (READ ONLY)*

	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
EFRH	**EXTERNAL FUNCTION INPUT INFORMATION**							
	EF0	EF1	EF2	EF3	EF4	EF5	EF6	EF7

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*Not used in IBL mode.

Table 4.3-3. Discrete On-Board Register Bit Definitions (Continued)

EXTERNAL FUNCTION REGISTER MID-HI ($XX67) (READ ONLY)*

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DFRMH	**EXTERNAL FUNCTION INPUT INFORMATION**							
	EF8	EF9	EF10	EF11	EF12	EF13	EF14	EF15

EXTERNAL FUNCTION REGISTER MID-LO ($XX68) (READ ONLY)*

	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
EFRML	**EXTERNAL FUNCTION INPUT INFORMATION**							
	EF16	EF17	EF18	EF19	EF20	EF21	EF22	EF23

EXTERNAL FUNCTION REGISTER LO ($XX69) (READ ONLY)*

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
EFRL	**EXTERNAL FUNCTION INPUT INFORMATION**							
	EF24	EF25	EF26	EF27	EF28	EF29	EF30	EF31

MASTER CONTROL REGISTER (XX6A); WORD WRITE ONLY

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
EXTERNAL FUNCTION CMD 1=EF CMD 0=NULL	ACK'D LINK REQ H 1 = ACK 0 = NO ACK	**NOT USED**					
		(0)	(0)	(0)	(0)	(0)	(0)

*Not used in IBL mode.

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Table 4.3-3. Discrete On-Board Register Bit Definitions (Concluded)

MASTER CONTROL REGISTER (XX6A); WORD WRITE ONLY (Concluded)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MASTER MODE 1=M 0=SLAVE	CLEAR STATUS CMD 1=CLR 0=OPER	IBL MODE H* 1=IBL 0=HSD	LINK REQUEST 1=REQ	RESET INTERFACE CMD 1=RES 0=OPER	I/O RESET CMD 1=RES	MASTER TRANSFER DIRECTION 1=OUT 0=IN	ENABLE LWF 1=EN 0=DIS

*The VMIVME-HSDA does not support HSD external mode operations.

MASTER STATUS REGISTER; BYTE (XX6B) OR WORD (XX6A) READ ONLY

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
NOT USED							

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
INPUT STATUS INTERRUPT REQUEST 0=REQ 1=STATUS WAS READ	RCVD LINK REQ ACK'D H 1=ACK'D 0=NO ACK'D	DEVICE PRESENT INPUT 1=PRES.	LINK REQUEST INPUT 1=REQ	EXT TERMINATE INPUT 1=TERM	I/O RESET CMD	TRANSFER DIRECTION	ENABLE LWF
					READS BACK MASTER CONTROL REGISTER BITS 2, 1, 0		

EXTENDED MEMORY ADDRESS (XX6D) WRITE ONLY

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
EMA	**EXTENDED MEMORY ADDRESS (VMEbus A24 THROUGH A31 DURING DMA TRANSFERS)**							
	BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24

*Not used in IBL mode.

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Table 4.3-3. Discrete On-Board Register Bit Definitions (Continued)

INPUT DATA REGISTER ($XX70); BYTE (BITS 0 TO 7), WORD (BITS 0 TO 15), OR LONGWORD READ ONLY

BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24
DEVICE STATUS INPUT INFORMATION*							
DS0	DS1	DS2	DS3	DS4	DS5	DS6	DS7

BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
DEVICE STATUS INPUT INFORMATION*							
DS8	DS9	DS10	DS11	DS12	DS13	DS14	DS15

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
DEVICE STATUS INPUT INFORMATION*							
DS16	DS17	DS18	DS19	DS20	DS21	DS22	DS23

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DEVICE STATUS INPUT INFORMATION*							
DS24	DS25	DS26	DS27	DS28	DS29	DS30	DS31

*Not used in IBL mode.

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Table 4.3-3. Discrete On-Board Register Bit Definitions (Concluded)

OUTPUT DATA REGISTER ($XX70) LONGWORD WRITE ONLY

BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24
EXTERNAL FUNCTION OUTPUT INFORMATION							
EF0	EF1	EF2	EF3	EF4	EF5	EF6	EF7

BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
EXTERNAL FUNCTION OUTPUT INFORMATION							
EF8	EF9	EF10	EF11	EF12	EF13	EF14	EF15

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
EXTERNAL FUNCTION OUTPUT INFORMATION							
EF16	EF17	EF18	EF19	EF20	EF21	EF22	EF23

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
EXTERNAL FUNCTION OUTPUT INFORMATION							
EF24	EF25	EF26	EF27	EF28	EF29	EF30	EF31

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BIT 11 - CHANNEL ACTIVE. This bit indicates that a DMA operation is in progress and is automatically cleared upon termination of the operation.

BITS 10 and 9. Not used.

BIT 8 READY INPUT. Indicates the state of the RDY input signal, i.e., a "zero" indicates 0 volts and that data is ready.

4.4.1.2 Channel Error Register (CER)

BITS 7, 6, and 5. Not used.

BITS 4, 3, 2, 1, and 0 - ERROR CODE. These 5 bits indicate the error type when an error occurs. This register is cleared when the error bit (CSR BIT 12) is cleared.

ERROR CODE	FUNCTION
00000	No Error
01001	Bus Error
10001	Software Abort

NOTICE

CSR BIT 15 AND CSR BIT 12 MUST BE CLEARED IF SET, BEFORE ANOTHER DMA OPERATION CAN BE STARTED. THESE BITS MAY BE CLEARED BY WRITING A "ONE" TO EACH BIT THAT IS SET. THE FOLLOWING 68000 INSTRUCTION WILL ACCOMPLISH THIS WITHOUT TESTING EACH OF THE BITS.

```
MOVE.B    CSR, CSR
```

THE OTHER BITS IN THE CSR ARE UNAFFECTED BY A WRITE.

4.4.2 Device Control Register (DCR)/Operation Control Register (OCR)

These two registers control the data direction, data size, and request mode of the DMA transfers.

4.4.2.1 Device Control Register (DCR)

BIT 15 - EXTERNAL REQUEST MODE. This bit is set to perform single cycle transfers and cleared to perform burst transfers.

BITS 14, 13, and 12. Not used.

BIT 11 - SIZE. This bit is read and written as the Logical OR of bits 4 and 5 in the OCR .

BITS 10, 9, and 8. Not used.

4.4.2.2 Operation Control Register (OCR)

BIT 7 - DIRECTION.

This bit contains the DMA transfer direction.
0=Read from Memory
Write to External Device
1=Write to Memory
Read from External Device

BIT 6. Not used.

BIT 5 and 4 OPERAND SIZE. These bits control the operand size

BIT 5	BIT 4	OPERAND SIZE
0	0	BYTE
0	1	WORD
1	0	DUAL 16-BIT*
1	1	DOUBLEWORD (32-BIT PER TRANSFER)

*The VMIVME-HSDA does not support dual 16-bit operations.

BITS 3, 2, 1, and 0. Not used.

4.4.3 Sequence Control Register (SCR)

The SCR is a dummy register provided for compatibility with other DMA Controllers.

4.4.4 Channel Control Register (CCR)

BIT 15 - START. This bit causes the DMA controller to start its operation.

BITS 6 and 5. Not used.

BIT 4 - SOFTWARE ABORT. This bit allows current DMA operation to be aborted under software control. It sets the error bit in the CSR and the error code in the CER. The software abort bit must be cleared to clear the error bit lin the CSR and to clear the error code in the CER.

Software Abort Procedure: DMA transfers must be terminated on the transmitting end first. The state of the Ready Input State bit of the CSR (register address $XX00) should be monitored. The software abort bit should only be set when the Ready Input State is a logic "one" (an indication that no DMA cycle request is pending).

BIT 3 - INTERRUPT ENABLE. This bit enables the DMA interrupt request when a DMA operation is completed.

BITS 2, 1, and 0. Not used.

4.4.5 Memory Transfer Count Register (MTCR)

This register holds the number of desired transfers for the current operation. The transfer count can be set to FFFF (64 k to 1) if the VMIVME-HSDA is in the slave mode. The last word flag (LWF) signal is used to terminate the transfers in this case. However, setting the transfer counter to FFFF does cause an extra memory cycle to be requested beyond the actual word count (only if a read from memory). This should not be a problem unless it happens to be at the end of memory, in that case it will generate a bus error trap.

4.4.6 Memory Address Counter Registers (MACRs)

These four registers hold the memory address for the DMA operation. The MACH Register is a dummy register and is provided for compatibility with other DMA controllers. The three real registers provide a 24-bit memory address for the DMA transfers. These registers should be loaded with the starting memory address before an operation is started. The registers are incremented during operation and may be read while an operation is in progress.

4.4.7 DMA Interrupt Vector Register (DIVR)

This register is used to store the interrupt vector used for the DMA complete (done) interrupt. This register is resident inside the SCB68430. It is mapped to two locations to provide compatibility with other DMA Controllers. Note: Bit 0 is automatically set when an error occurs, and cannot be written. Thus, a DMA interrupt vector for normal conditions must be even and the error vector is automatically the next higher odd vector. Note that although the 68430 supplies the interrupt vector, the 68153 provides the interrupt handshake; therefore, the 68153 must be programmed to handle the external vector from the 68430.

4.4.8 Channel Priority Register (CPR)

This register is a dummy register provided for compatibility with other DMA Controllers.

4.5 PROGRAMMING THE MC68153 BIM

Data sheets for the MC68153 are provided in Appendix B. The MC68153 contains 8 registers, but one Vector Register is not used since the DMA DONE interrupt vector is originated in the 68430 IC.

In the IBL mode the restart interrupt is generated whenever a link request is received from the other IBL board if enabled. External function interrupt may be initialized to respond with a LINK ACKNOWLEDGE INTERRUPT.

4.5.1 Input Status Control Register (ISCR) Restart Interrupt Control Register (RICR)

EXTERNAL INTERRUPT CONTROL REGISTER (EICR) AND DMA INTERRUPT CONTROL REGISTER (DICR).

BITS 7 and 6 - FLAG CONTROL. Not Used.

BIT 5 - VECTOR LOCATION. This bit should be cleared so that the MC68153 may use its Internal Vector Register for an interrupt acknowledge and set to use an external interrupt vector. For the VMIVME-HSDA, this bit should be cleared in all control registers except for the DICR; it should be set in the DICR because an external vector is generated by the 68430 DMA Controller Vector Register (DIVR).

BIT 4 - INTERRUPT ENABLE. This bit should be set to enable the corresponding interrupt.

BIT 3 - INTERRUPT AUTO CLEAR. This bit automatically clears the interrupt enable bit and the interrupt request output whenever the interrupt is acknowledged. It must be set in all control registers to provide VMEbus compatible timing; therefore, the interrupt enable bit is to be set after each interrupt.

BITS 2,1, and 0 - IRQ LEVEL BITS. These bits determine the interrupt level at which an interrupt request is made.

LEVEL	BIT 2	BIT 1	BIT 0
7	1	1	1
6	1	1	0
5	1	0	1

4	1	0	0
3	0	1	1
2	0	1	0
1	0	0	1

4.5.2 Input Status Vector Register (ISVR) Restart Interrupt Vector Register (RIVR)

EXTERNAL INTERRUPT VECTOR REGISTER (EIVR). This register contains the vector used for the (EIVR) external interrupt. Any 8-bit integer may be used as determined by the system vector address configuration.

4.6 PROGRAMMING THE ON-BOARD REGISTERS

BOARD CONTROL REGISTER (BCR, WRITE ONLY).

BITS 7, 6, 5, and 4. Not used.

BIT 3 - LED CONTROL. This bit controls the front panel LED.

BIT 3	LED
0	OFF
1	ON

BIT 2 - ENABLE EXTERNAL FUNCTION INTERRUPT. This bit enables the external function interrupt flip-flop. It must be set in addition to EICR - Bit 4 to enable external function interrupts. It is automatically cleared by the hardware after each external function interrupt is acknowledged which allows the Encore HSD and VMIVME-HSDA to remain synchronized during command chaining.

BIT 1 - EXTERNAL TERMINATE. Setting this bit causes an external terminate to occur by asserting LIDR and LEXT simultaneously.

BIT 0 - GO. This bit "primes" the handshake logic to perform transfers with the Encore HSD. This bit will also initiate the first transfer cycle when transferring data to the Encore.

4.6.1 Device Status Register (DSR) (Write Only)

This 8-bit register is used to store user-defined status information to be transferred to the Encore HSD via an Input Status Request. This register transmits the 8 least significant bits (24 to 31) of the Encore status word (HSD mode only).

4.6.2 Address Modifier Register (AMR) (Write Only)

This write only register contains the address modifier and longword bits which are asserted while the VMIVME-HSDA is bus master.

BIT 7. Not used.

BIT 6 - LONGWORD. This bit controls the assertion of the VMEbus LWORDL signal and selects either 16- or 32-bit VMEbus transfers. The operand size selected in the OCR bits 4 and 5 (in the 68430 at address XX05) must be programmed for the same transfer size as shown in the following table.

LONGWORD	TRANSFER SIZE	BITS 5 and 4 OF OCR
0	32-Bit	11
1	16-Bit	01
1	8-Bit	00

BITS 5, 4, 3, 2, 1, and 0 ARE THE ADDRESS MODIFIER BITS. See Table 4-6.2-1 for VMEbus Address Modifier Codes.

4.6.3 External Function Registers (EFRs) (Read Only)

These read only Registers contain (HSD slave mode only) the External Function information transferred from the Encore HSD and may be accessed as 4 bytes or two words. (Not used in IBL mode).

EFRH. Contains 8 most significant bits of External Function data. (EF0 to EF7) EF2 is the device status bit and EF0 is the direction bit.

EFRMH. Contains Bits EF8 to EF15 of External Function data.

EFRML. Contains Bits EF16 to EF23 of External Function data.

EFRL. Contains 8 least significant bits of External Function data (EF24 to EF31).

4.6.4 Output Data Register (ODR)

The Output Data Register (ODR) is written to by the CPU only when the VMIVME-HSDA is programmed to operate in the HSD master mode. It is used to store the external function command data 32 bits prior to asserting the EXTERNAL FUNCTION COMMAND bit in the Master Control Register. The Output Data Register must be written as a longword only (32 bits per cycle). In the master mode, EF2 is set high "one" to request status from the slave HSD. EF0 determines the direction of data transfers. When the Master sets EF0 low, the direction of data transfers is from the Master to the Slave HSD. When the Master HSD sets EF0 high

the direction of data transfers is from slave to the Master HSD. EF0 is the most significant data bit. (Not used in IBL mode).

Table 4.6.2-1. Address Modifier Codes

HEXADECIMAL CODE	ADDRESS MODIFIER 5	4	3	2	1	0	FUNCTION	DEFINED BY
3F	H	H	H	H	H	H	Standard Supervisory Ascending Access	VMEbus Spec.
3E	H	H	H	H	H	L	Standard Supervisory Program Access	VMEbus Spec.
3D	H	H	H	H	L	H	Standard Supervisory Data Access	VMEbus Spec.
3C	H	H	H	H	L	L	Undefined	Reserved
3B	H	H	H	L	H	H	Standard Nonprivileged Ascending Access	VMEbus Spec.
3A	H	H	H	L	H	L	Standard Nonprivileged Program Access	VMEbus Spec.
39	H	H	H	L	L	H	Standard Nonprivileged Data Access	VMEbus Spec.
38	H	H	H	L	L	L	Undefined	Reserved
30 to 37	H	H	L	X	X	X	Undefined	Reserved
2F	H	L	H	H	H	H	Undefined	Reserved
2E	H	L	H	H	H	L	Undefined	Reserved
2D	H	L	H	H	L	H	Short Supervisory I/O Access	VMEbus Spec.
2C	H	L	H	H	L	L	Undefined	Reserved
2B	H	L	H	L	H	H	Undefined	Reserved
2A	H	L	H	L	H	L	Undefined	Reserved
29	H	L	H	L	L	H	Short Nonprivileged Access	VMEbus Spec.
28	H	L	H	L	L	L	Undefined	Reserved
20 to 27	H	L	L	X	X	X	Undefined	Reserved
10 to 1F	L	H	X	X	X	X	Undefined	User
0F	L	L	H	H	H	H	Extended Supervisory Ascending Access	VMEbus Spec.
0E	L	L	H	H	H	L	Extended Supervisory Program Access	VMEbus Spec.
0D	L	L	H	H	L	H	Extended Supervisory Data Access	VMEbus Spec.
0C	L	L	H	H	L	L	Undefined	Reserved
0B	L	L	H	L	H	H	Extended Nonprivileged Ascending Access	VMEbus Spec.
0A	L	L	H	L	H	L	Extended Nonprivileged Program Access	VMEbus Spec.
09	L	L	H	L	L	H	Extended Nonprivileged Data Access	VMEbus Spec.
08	L	L	H	L	L	L	Undefined	Reserved
00 to 07	L	L	L	X	X	X	Undefined	Reserved

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4.6.5 Input Data Register (IDR)

The Input Data Register, read as a byte at address XX73, is used only in the master mode and contains the status data after a device status request command is executed and acknowledged.

4.6.6 Master Control Register (MCR)

The Master Control Register is used to select the master mode of operation and to generate the External Function Link Request and I/O reset commands. It is also used to select the direction of data transfers while in the HSD master mode and IBL mode. It is cleared by system reset and is not required to operate the VMIVME-HSDA in the slave mode. It must be written as a word only.

BIT 15 - EXTERNAL FUNCTION COMMAND (used in HSD master mode only). This bit is set to a "one" to assert the External Function Command signal. It is automatically cleared when acknowledged by the HSD slave. The external function command data must be loaded into the Output Data Register before this bit is set.

BIT 14 - ACKNOWLEDGE LINK REQ H (IBL mode only). This bit is set to "one" to send an acknowledge to the other board. This bit is set in response to a link request from the other board.

BITS 13 through 08. Not used.

BIT 07 - MASTER MODE. This bit selects the master mode when it is set to a logic "one". It is cleared by system reset and if this board is to operate as an HSD master this bit should be set before any other registers are written.

BIT 06 - CLEAR STATUS. This bit is set to a logic "one" to clear three flip-flops: a. the EXTERNAL TERMINATE flip-flop, b. the LAST WORD FLAG flip-flop and, c. the READY flip-flop. This bit should be immediately set to zero to enable continued operation. This bit should be set to a "one" then reset to "zero" by software after a data block has been transferred, and before the next data block is transferred.

BIT 05 - IBL MODE H. This bit must be set to "one" to select the IBL mode.

BIT 04 - LINK REQUEST. This bit (when set to "one") asserts the LINK REQUEST signal on the IBL link. It is cleared under program control.

BIT 03 - RESET INTERFACE COMMAND. This bit (when set) resets the VMIVME-HSDA transceiver logic. It should be cleared back to "zero" to allow normal operation to resume.

BIT 02 - I/O RESET COMMAND. When the VMIVME-HSDA is in the HSD master mode, this bit (when set to "one") resets the slave HSD. When the VMIVME-HSDA is in the HSD slave mode this bit (when set to "one") precludes the assertion of the DEVICE PRESENT signal. This bit should be reset to "zero" to allow normal operation to resume.

BIT 01 - TRANSFER DIRECTION. When the VMIVME-HSDA is programmed for an IBL or HSD master, this bit controls the direction of data transceivers during a data block transfer. When this bit is set to a "one" the transfer direction is from global memory to the device.

BIT 00 - ENABLE LWF. When this bit set to "one" it enables the generation of the LAST WORD FLAG (LWF on pin 22). The LAST WORD FLAG is generated in the master mode and monitored in the slave mode.

4.6.7 Master Status Register (MSR)

The Master Status Register monitors the status of the link control signals. It can be read as a byte at address XX73.

BIT 07 - INPUT STATUS INTERRUPT REQUEST. Monitors the status of the INPUT STATUS READY flip-flop. The INPUT STATUS READY flip-flop is set by the INPUT STATUS READY signal (ISR on pin 36). This bit applies only when the VMIVME-HSDA is in the master mode.

BIT 06 - EXTERNAL FUNCTION COMMAND (HSD mode) OR RCVD LINK REQ ACK'D H (IBL mode). It monitors the status of the GENERATE EXTERNAL FUNCTION COMMAND flip-flop when the VMIVME-HSDA is operated in the HSD master mode. The GENERATE EXTERNAL FUNCTION COMMAND flip-flop is set by writing a "one" to bit 15 of the Master Control Register; it is cleared by reading the input status (i.e., a read of the Input Data Register).

In the IBL mode it monitors the status of the LINK REQUEST ACKNOWLEDGE from the other board. If initialized may generate a LINK ACKNOWLEDGE INTERRUPT through the EF Interrupt control.

BIT 05 - DEVICE PRESENT. In the master mode, this bit indicates the status of the DEVICE PRESENT signal (DP on pin 18). In the slave mode this bit indicates the status of the I/O RESET signal (IOR on pin 26). This bit is a logic "one" when an HSD interface is connected and power has been applied.

BIT 04 - LINK REQUEST INPUT. This bit monitors the status of the LINK REQUEST signal input. In the master mode it monitors pin 50 (LRI); whereas, in the slave mode it monitors the status of pin 48 (LRO).

BIT 03 - EXTERNAL TERMINATE INPUT. This bit monitors the state of the EXTERNAL TERMINATE flip-flop. In the slave mode the EXTERNAL TERMINATE flip is set by the TERMINATE DEVICE signal (TDV on pin 20); whereas, in the master mode, it is set by the EXTERNAL TERMINATE signal (EXT on pin 28). This flip-flop is cleared by the CLEAR STATUS COMMAND (Master Control Register, bit 06).

BITS 00, 01, and 02. These three bits reflect the status of corresponding bits in the Master Control Register.

4.6.8 Extended Memory Address Register (EMAR)

This register holds bits A24 through A31 of VMEbus addresses for DMA transfers. It is cleared at power up (by SYSRESET) and must be loaded when the Address Modifier Register selects an extended address.

4.7 SAMPLE SOFTWARE LISTINGS

VMIC has provided sample software listings in Appendix C to assist the user in programming the VMIVME-HSDA when connected to a Encore computer and when connected as a VMEbus-to-VMEbus link. The VMIVME-HSDA board is directly compatible with the standard Encore HSD generic handler.

Two listings are provided for interfacing to a Encore HSD:

a. A detailed FORTRAN code listing for the Encore;
b. A detailed sample Assembly code listing for a 68000 VMEbus CPU.

Two sample listings are provided for operating two VMIVME-HSDA Boards in a VMEbus-to-VMEbus Link:

a. 68020 Assembly code for a VMIVME-HSDA operating as an HSD master (back-to-back with another VMIVME-HSDA)
b. 68000 Assembly code for a VMIVME-HSDA operating as an HSD slave (back-to-back with another VMIVME-HSDA).

SECTION 5

CONFIGURATION AND INSTALLATION

5.1 UNPACKING PROCEDURES

```
*****************
*     CAUTION   *
*****************
```

SOME OF THE COMPONENTS ASSEMBLED ON VMIC'S PRODUCTS MAY BE SENSITIVE TO ELECTROSTATIC DISCHARGE AND DAMAGE MAY OCCUR ON BOARDS THAT ARE SUBJECTED TO A HIGH ENERGY ELECTROSTATIC FIELD. WHEN THE BOARD IS TO BE LAID ON A BENCH FOR CONFIGURING, ETC., IT IS SUGGESTED THAT CONDUCTIVE MATERIAL BE INSERTED UNDER THE BOARD TO PROVIDE A CONDUCTIVE SHUNT. UNUSED BOARDS SHOULD BE STORED IN THE SAME PROTECTIVE BOXES IN WHICH THEY WERE SHIPPED.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice concerning disposition of the damaged item(s).

5.2 PHYSICAL INSTALLATION

```
*****************
*     CAUTION   *
*****************
```

DO NOT INSTALL OR REMOVE BOARDS WHILE POWER IS APPLIED.

De-energize the equipment and insert the board into an appropriate slot of the chassis, while ensuring that the board is properly aligned and oriented in the supporting card guides. Slide the board smoothly forward against the mating connector until firmly seated.

5.3 JUMPER INSTALLATIONS

The Revision F and all subsequent revision boards provide for jumper selection of the VMEbus priority level. See Figure 5.3-1 for jumper locations.

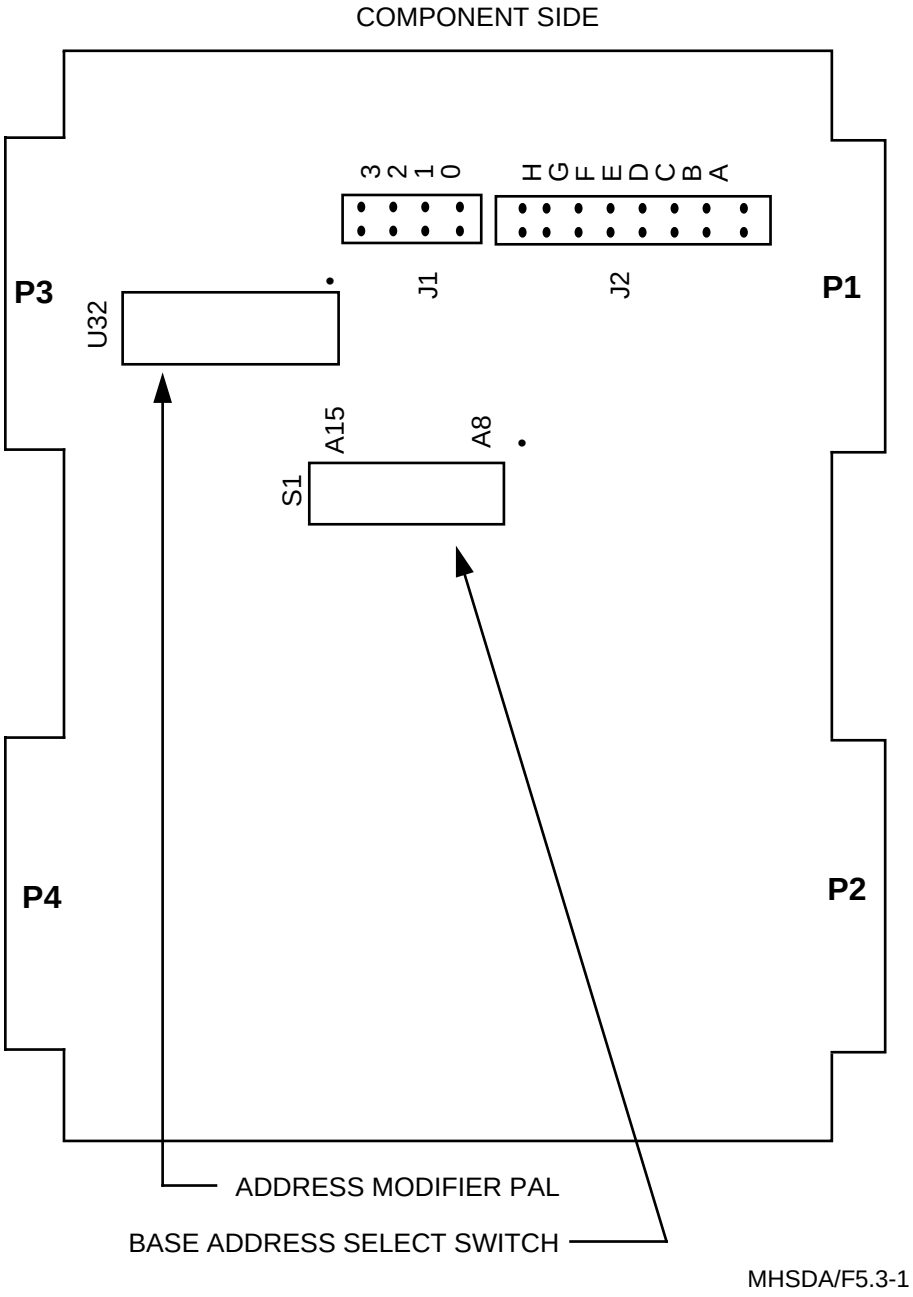


Figure 5.3-1. VMIVME-HSDA Configuration Information

5.3.1 VMEbus Priority Jumpers

Jumpers J2 and J3 provide for the selection of bus request level and grant level, respectively. See Figure 5.3.1-1 for selection of bus priority level (3, 2, 1, or 0). The factory configuration is Level 3.

5.4 BOARD BASE ADDRESS

The VMIVME-HSDA occupies 256 bytes of the VMEbus short I/O space. The upper eight bits of the address are DIP switch selectable. Refer to Figure 5.4-1 for configuration of this address selection.

5.5 ADDRESS MODIFIERS

The board is factory configured via a programmed PAL to respond to either of two address modifier codes in the VMEbus slave short I/O address space: Short Supervisory ($2D) and Short Nonprivileged access ($29).

5.6 I/O CABLES

The VMIVME-HSDA is designed to be connected to the Encore HSD Interface via two 50-conductor flat-ribbon cables using standard mass terminate style header socket connectors. Two cables of the same length are required and the total length of the cable assembly must not exceed 250 feet. The cables should be connected as shown in Figure 5.6-1. The Interface Signal list is shown in Table 5.6-1. Connect P3 to P3 and P4 to P4 when using VMIVME-HSDA boards in a VMEbus-toVMEbus Link.

5.7 CABLE CONNECTOR

A compatible cable connector for the VMIVME-HSDA is Panduit No. 050-050-435 and the strain relief is Panduit No. 050-000-050. The header connector soldered to the P.C. board is Panduit No. 050-050-033A.

5.8 INSTALLATION

The VMIVME-HSDA is compatible with any VMEbus chassis which can accept double Eurocard form factor boards with front panels. The board requires that the P2 backplane and a memory capable of supporting 32-bit transfers. Two captive screws are provided on the front panel to secure the board to the chassis, and handles are provided for removal and installation. Operation in the Encore

MASTER mode requires a VMEbus CPU that is capable of supporting 32-bit transfers to short I/O address space.

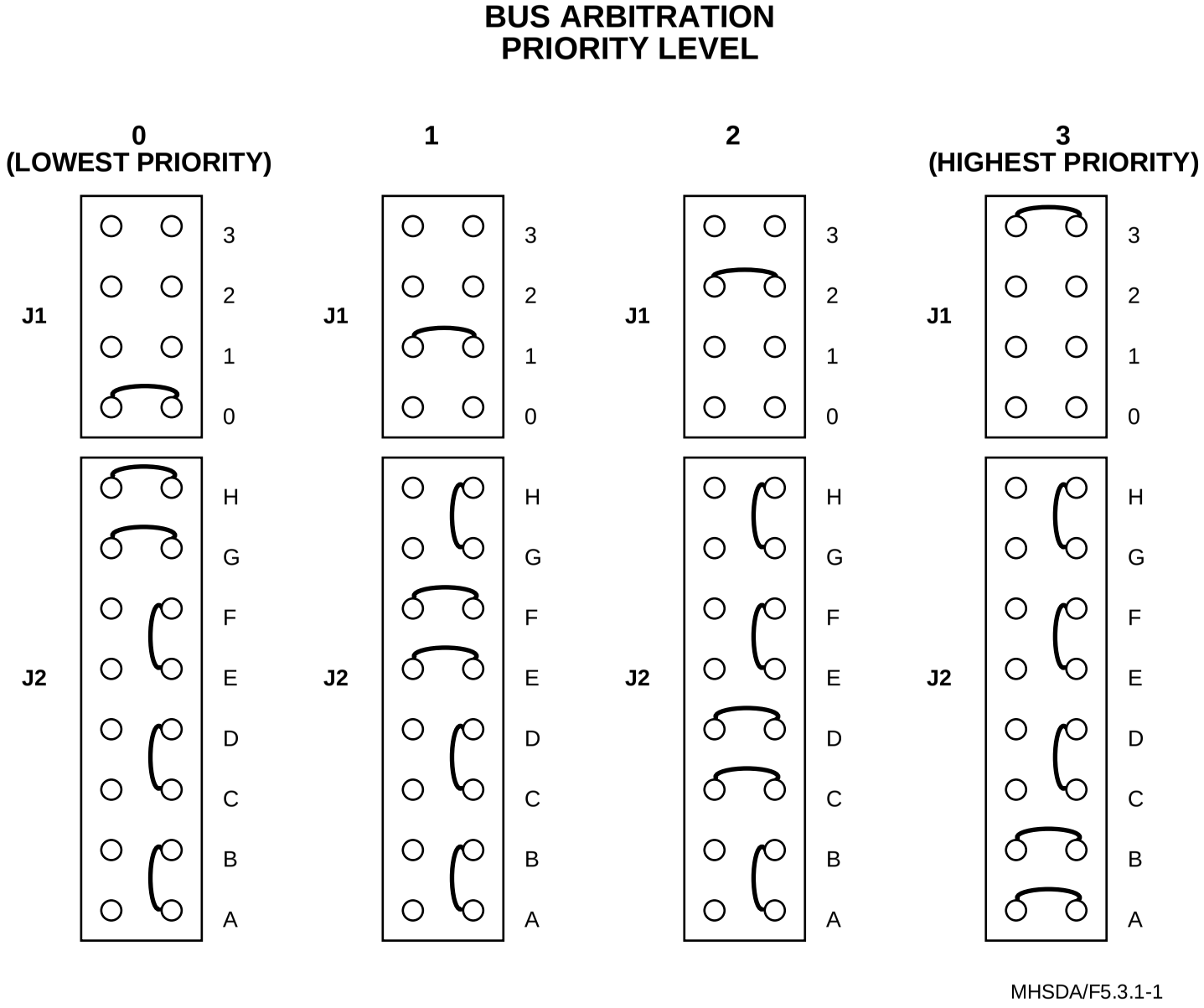


Figure 5.3.1-1. Jumper Installation for Selection of VMEbus Priority Level (Rev. F Board and Subsequent Revisions), this Board is Factory Configured for Level 3

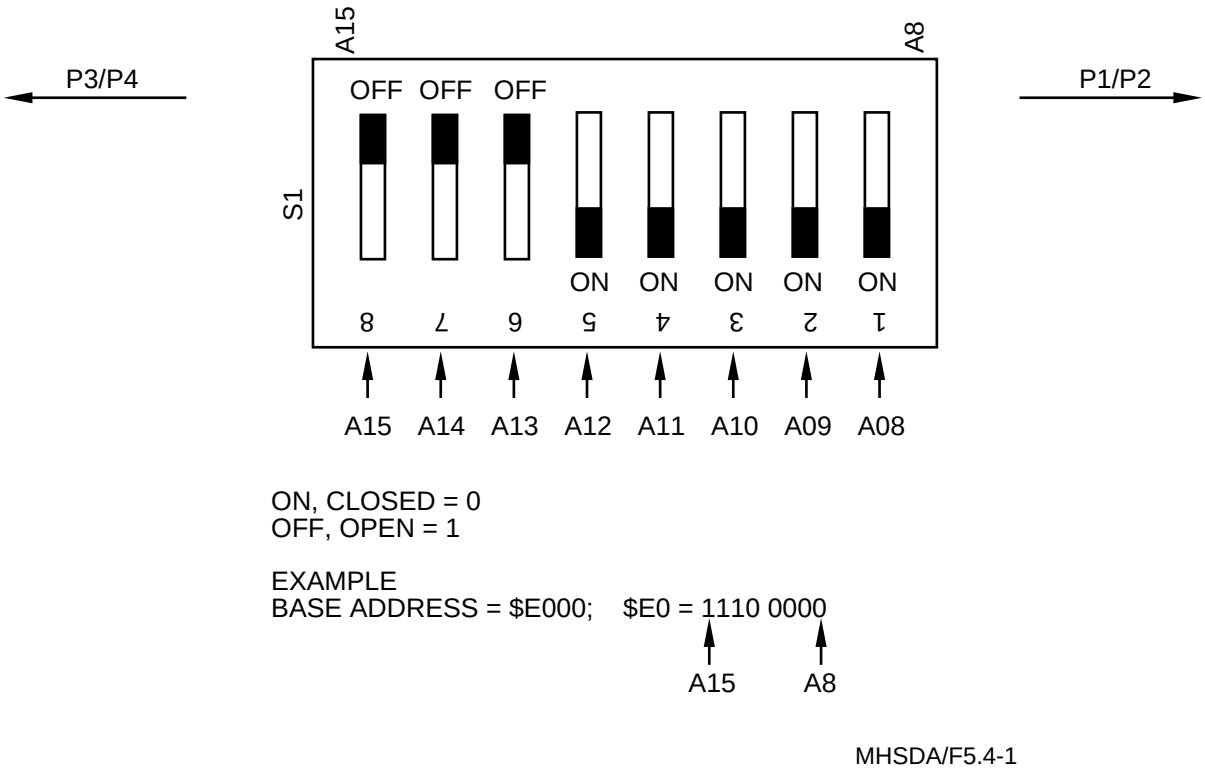


Figure 5.4-1. VMIVME-HSDA Base Address Configuration, the Factory Configuration for this Switch is $E000

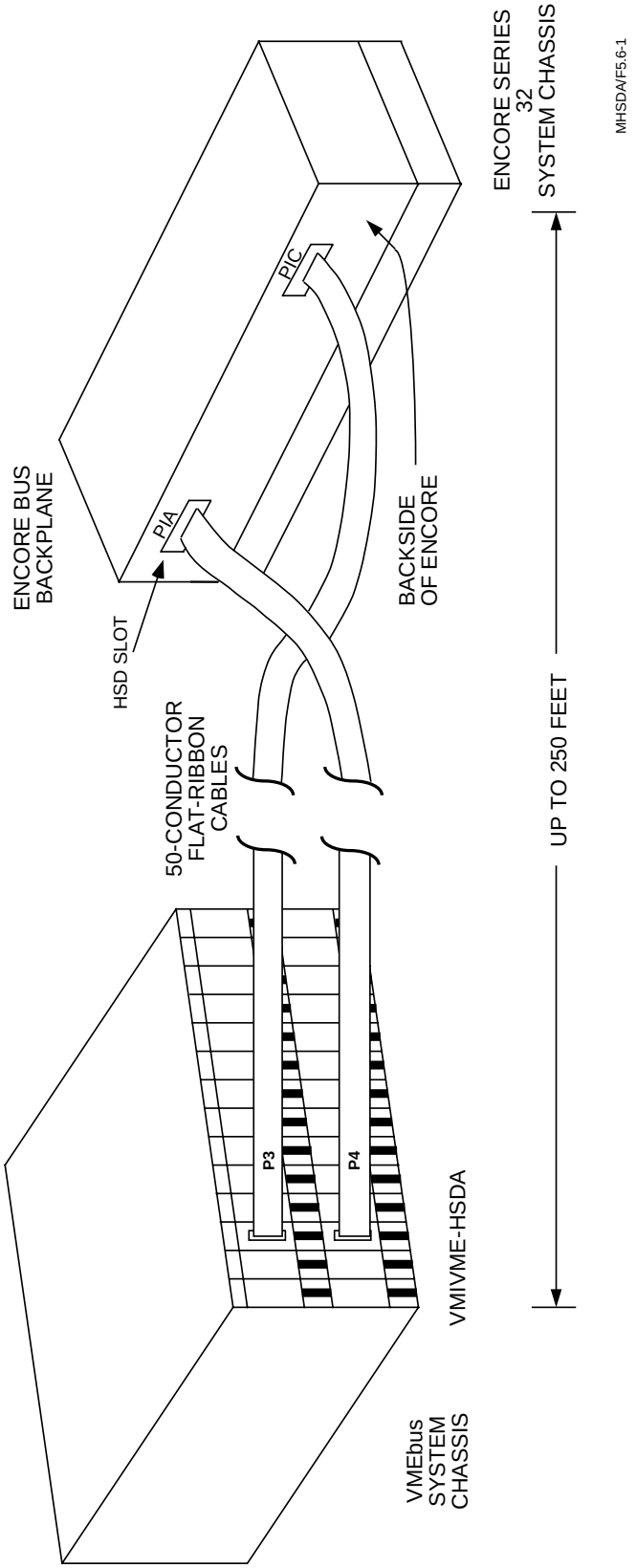


Figure 5.6-1. System Interconnection Pictorial Diagram

Table 5.6-1. User Interface Signal List

P4			P3		
P1A	BACKPLANE CONNECTOR PIN	SIGNAL NAME	P1C	BACKPLANE CONNECTOR PIN	SIGNAL NAME
	1	GND		1	GND
	2	DAT00		2	DAT24
	3	GND		3	GND
	4	DAT01		4	DAT25
	5	GND		5	GND
	6	DAT02		6	DAT26
	7	GND		7	GND
	8	DAT03		8	DAT27
	9	GND		9	GND
	10	DAT04		10	DAT28
	11	GND		11	GND
	12	DAT05		12	DAT29
	13	GND		13	GND
	14	DAT06		14	DAT30
	15	GND		15	GND
	16	DAT07		16	DAT31
	17	GND		17	GND
	18	DAT08		18	DP
	19	GND		19	GND
	20	DAT09		20	TDV
	21	GND		21	GND
	22	DAT10		22	LWF
	23	GND		23	GND
	24	DAT11		24	DEB
	25	GND		25	GND
	26	DAT12		26	IOR
	27	GND		27	GND
	28	DAT13		28	EXT
	29	GND		29	GND
	30	DAT14		30	EM*
	31	GND		31	GND
	32	DAT15		32	IDR
	33	GND		33	GND
	34	DAT16		34	IA
	35	GND		35	GND
	36	DAT17		36	ISR
	37	GND		37	GND
	38	DAT18		38	ISA (LAI)
	39	GND		39	GND
	40	DAT19		40	EF
	41	GND		41	GND
	42	DAT20		42	EFA (LAO)
	43	GND		43	GND
	44	DAT21		44	ODR
	45	GND		45	GND
	46	DAT22		46	OA
	47	GND		47	GND
	48	DAT23		48	LRO
	49	GND		49	GND
	50	UNUSED		50	LRI

Encore (Master) mnemonics are shown for all signals.
*The External Mode (EM) is not supported.

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SECTION 6

MAINTENANCE

6.1 MAINTENANCE

This section provides information relative to the care and maintenance of VMIC's products. If the products malfunction, verify the following:

a. Software
b. System configuration
c. Electrical connections
d. Jumper or configuration options
e. Boards are fully inserted into their proper connector location
f. Connector pins are clean and free from contamination
g. No components of adjacent boards are disturbed when inserting or removing the board from the chassis
h. Quality of cables and I/O connections

If the products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return.**

6.2 MAINTENANCE PRINTS

User-level repairs are not recommended. The appendix to this manual contains drawings and diagrams for reference purposes only.

APPENDIX A

ASSEMBLY DRAWING, PARTS LIST, AND SCHEMATIC

APPENDIX B

INTEGRATED CIRCUIT SPECIFICATIONS

DESCRIPTION	PART NO.
Bus Interrupter Module	MC68153
Direct Memory Access Interface (DMAI)	SCB68430

APPENDIX C

SAMPLE SOFTWARE LISTINGS

The following two listings are provided for interfacing to a Encore/Gould HSD:

Listing 1: Fortran code for Gould Host Computer
Listing 2: Assembly listing for Gould Host Computer
Listing 3: 68000 assembly code for the VMIVME-HSD in a VME system.

Two sample listings are provided for operating two VMIVME-HSD boards in a VMEbus-to-VMEbus link:

Listing 4: 68020 assembly code for a VMIVME-HSD operating as an HSD master (back-to-back with another VMIVME-HSD)

Listing 5: 68000 assembly code for a VMIVME-HSD operating as an HSD slave (back-to-back with another VMIVME-HSD)

Listing 1: Fortran Code for Gould Host Computer.

Listing 2: Assembly Listing for Gould Host Computer.

Listing 3: 68000 Assembly Code for a VMIVME-HSD in a VME System linked to a Gould Computer.

Listing 4: 68020 Assembly Code for a VMIVME-HSD operating as an HSD Master (back-to-back with another VMIVME-HSD)

Listing 5: 68000 Assembly Code for a VMIVME-HSD operating as an HSD Slave (back-to-back with another VMIVME-HSD)

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