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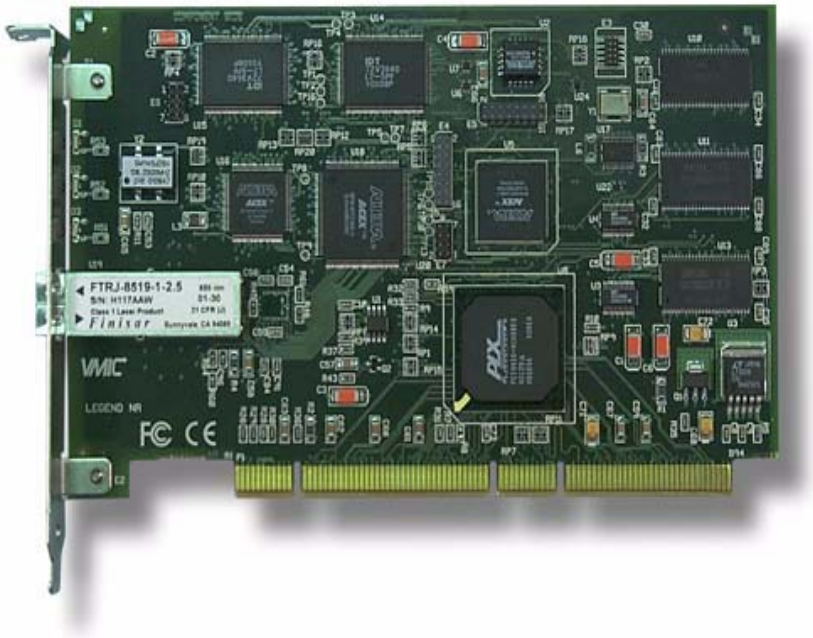
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GE Fanuc Automation



VMIPCI-5565

Ultrahigh Speed Fiber-Optic Reflective Memory with Interrupts

PRODUCT MANUAL
500-855565-000 REV G

Embedded Systems

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Overview

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Introduction

The VMIPCI-5565 is the PCI-based member of GE Fanuc Embedded Systems' family of Reflective Memory real time fiber-optic network products. Two or more VMIPCI-5565s and other members of this family can be integrated into a network using standard fiber-optic cables. Each board in the network is referred to as a node.

Reflective Memory allows computers, workstations, PLCs and other embedded controllers with different architectures and dissimilar operating systems to share data in real time. The VMIxxx-5565 family of Reflective Memory is fast, flexible and easy to operate. Data is transferred by writing to memory (SDRAM), which appears to reside globally in all boards on the network. Onboard circuitry automatically performs the transfer to all other nodes with little or no involvement of any host processor or system. A block diagram of the VMIPCI-5565 is shown in Figure 1 on page 15.

Features

- High speed, easy to use fiber-optic network (2.12 Gbaud serially)
- PCI 64-bit 66MHz transfers
- No host processor involvement in the operation of the network
- Redundant Mode of Operation
- Up to 256 nodes
- Connectivity with multimode fiber up to 300 meters
- Dynamic packet size, 4 to 64 bytes of data per packet
- Transfer rate 47.1MB/s (4 byte packet) to 174 MB/s (64 byte packet)
- 64MB or 128MB SDRAM Reflective Memory with parity
- Two independent Direct Memory (DMA) channels
- Configurable endian conversion for multiple CPU architectures on the same network

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PCI Local Bus Compliance

The VMIPCI-5565 complies with requirements of the *PCI Local Bus Specification, version 2.2*.

Vendor and Device Identification

The PCI Configuration register reserved for the vendor ID has the value of $114A, which designates GE Fanuc Embedded Systems. The PCI Configuration register reserved for the device ID has the value of $5565, which is GE Fanuc Embedded Systems' board type.

Subsystem Vendor ID and Subsystem ID

The PCI Configuration register reserved for the subsystem vendor ID has the value of $10B5, which designates PLX Technology. The PCI Configuration register reserved for the subsystem ID has the value of $9656, which is the PLX device part number.

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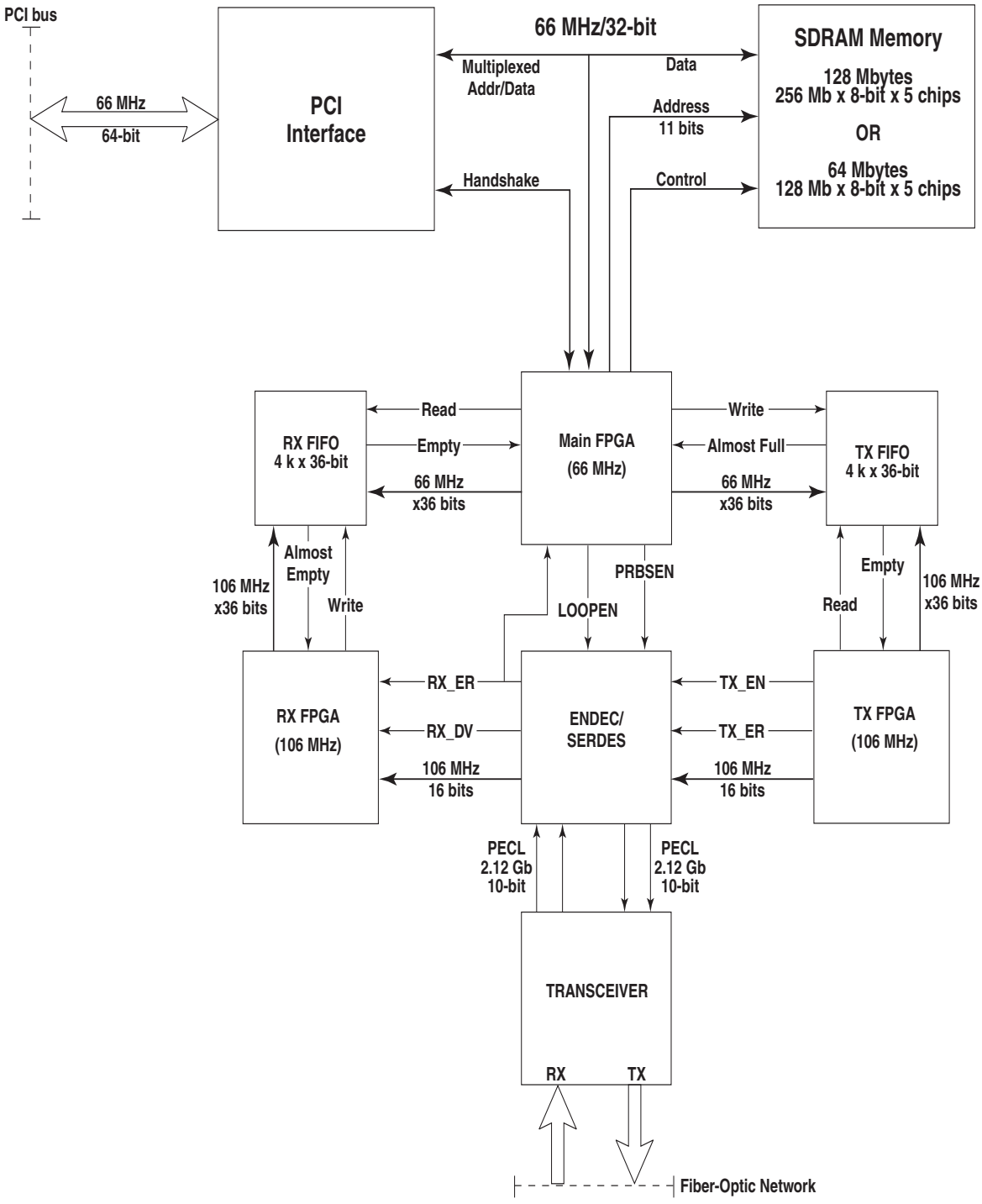


Figure 1 VMIPCI-5565 Block Diagram

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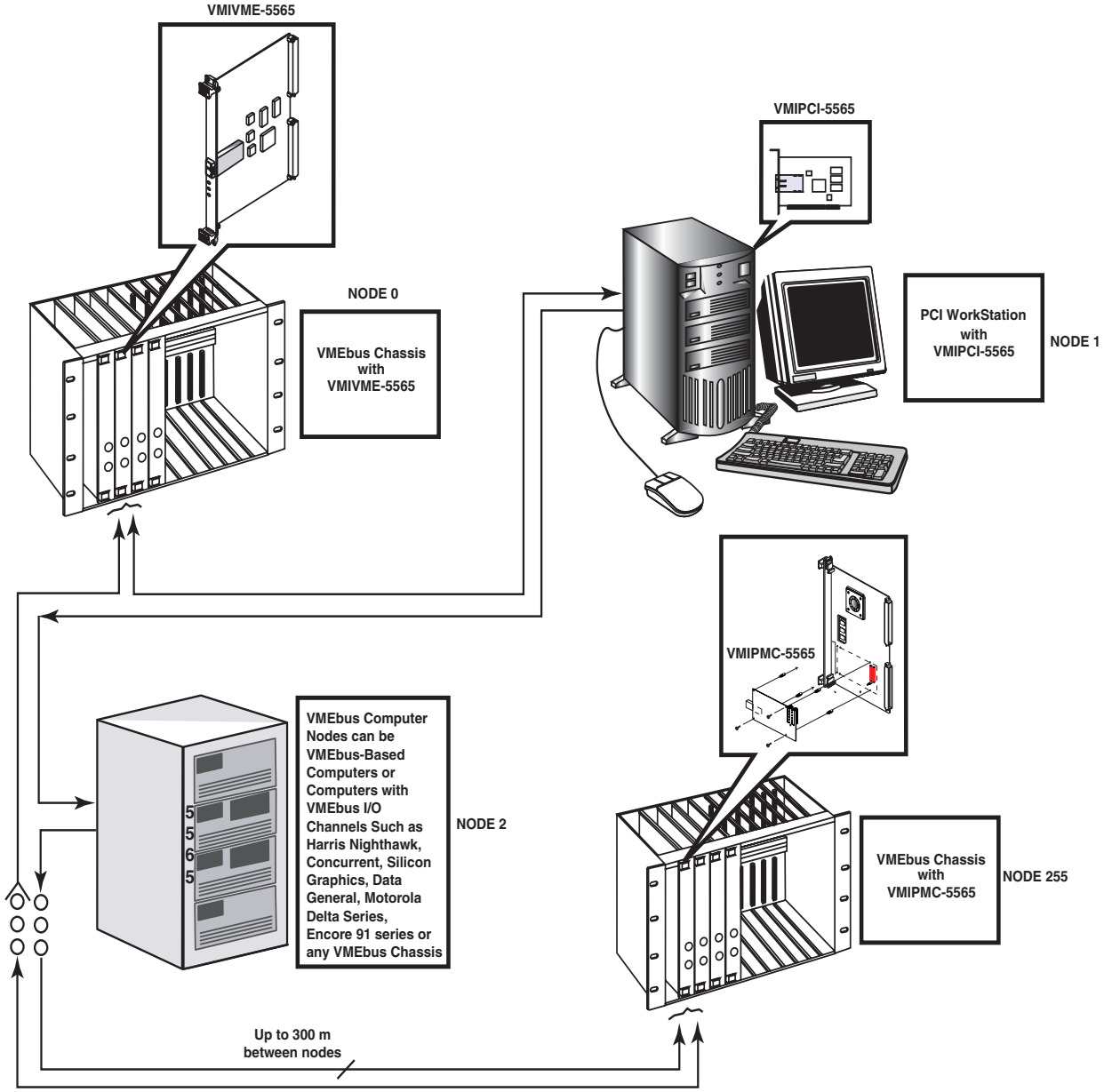


Figure 2 Typical Reflective Memory Network

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Organization of the Manual

This manual is composed of the following chapters:

Overview **-** provides an introduction of the VMIPCI-5565, Organization of the manual, References, Safety summary and Saftey symbols.

Chapter 1 - Theory of Operation describes the functionality of the VMIPCI-5565 Reflective Memory board and provides descriptions of the major sub-circuits and their operation.

Chapter 2 - Configuration and Installation describes unpacking, inspection, hardware jumper settings, connector definitions, installation, cable configuration and board layout.

Chapter 3 - Programming describes registers like PCI Configuration, Local Configuration, Runtime, DMA Control, RFM Control and Status Registers.

Maintenance **-** provides information relative to the care and maintenance of the unit.

Compliance **-** provides the applicable information regarding regulatory compliance for the VMIPCI-5565.

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References

GE Fanuc Embedded Systems' Physical Description and Specifications
Doc. No. 800-855565-000
GE Fanuc Embedded Systems
12090 South Memorial Pkwy.
Huntsville, AL 35803-3308
(800) 322-3616
www.gefanucembedded.com

Refer to PCI Local Bus Specification for a detailed explanation of the PCI Local bus. The PCI Local bus Specification is available from the following source:

PCI Special Interest Group
P.O. Box 14070
Portland, OR 97214
U.S.: (800) 433-5177
International: (503) 797-4207
FAX: (503) 234-6762

For a detailed explanation of the PCI-9656 I/O Accelerator, refer to *PLX PCI-9656 Data Book Revision 0.90* from:

PLX Technology Inc.
870 Maude Av.
Sunnyvale, CA 94085
U.S.: (408) 774-9060
(800) 759-3735
FAX: (408) 774-2169
www.plxtech.com
E-mail: 9656@plxtech.com

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Safety Summary

The following general safety precautions must be observed during all phases of the operation, service and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture and intended use of this product.

GE Fanuc Embedded Systems assumes no liability for the customer's failure to comply with these requirements.

Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person capable of rendering first aid and resuscitation is present.

Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to GE Fanuc Embedded Systems for service and repair to ensure that safety features are maintained.

Dangerous Procedure Warnings

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING: Dangerous voltages, capable of causing death, are present in this system. Use extreme caution when handling, testing and adjusting.

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Safety Symbols Used in This Manual

STOP: Informs the operator that a practice or procedure should not be performed. Actions could result in injury or death to personnel, or could result in damage to or destruction of part or all of the system.

WARNING: Denotes a hazard. It calls attention to a procedure, a practice, a condition, which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION: Denotes a hazard. It calls attention to an operating procedure, a practice, or a condition, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE: Denotes important information. It calls attention to a procedure, a practice, a condition or the like, which is essential to highlight.

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CHAPTER

1

Theory of Operation

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Introduction

The following sections describe the functionality of the VMIPCI-5565 Reflective Memory board. A description of the major sub-circuits and their operation are included. This section will also occasionally mention Control and Status registers related to operations. To see a detailed description of these Control and Status registers please refer to the *"Programming"* section of this manual.

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Basic Operation

Each node (VMIxxx-5565 Reflective Memory boards) in the network is interconnected using fiber-optic cables in a daisy chain loop. The transmitter of the first board must be tied to the receiver of the second board. The transmitter of the second board is tied to the receiver of the third, and so on, until the loop is completed back at the receiver of the first board. Each node must have a unique node ID, which is accomplished using a bank of eight (8) onboard jumpers. The order of the node IDs is unimportant; they just have to be unique (i.e. no two nodes can have the same node ID).

A transfer of data over the network is initiated by a write to onboard SDRAM from the PCI host system. The write can be as simple as a PCI target write, or it can be due to a DMA cycle by one of the two resident DMA engines. When the write to the SDRAM is occurring, circuitry on the VMIPCI-5565 automatically writes the data, along with other pertinent information, into the transmit FIFO. From the transmit FIFO, a transmit circuit retrieves the data and forms it into variable length packets of from 4 to 64 bytes, which pass over the fiber-optic interface to the receiver of the next board. When data is received, a circuit opens the packets and stores the data in the board's receive FIFO. From the receive FIFO, a third circuit writes the data into local onboard SDRAM at the same relative location in memory as that of the originating node. The third circuit also simultaneously routes the data into the board's own transmit FIFO. From there, the process is repeated until the data returns to the receiver of the originating node. At the originating node, the data packet is removed from the network.

Front Bezel LED Indicators

The VMIPCI-5565 has three LED indicators located on the bezel. The top red LED is a status indicator, its power up default state is "ON". The status LED may be toggled "OFF" or "ON" by writing to a bit (Bit 31 of the Control and Status register), which indicates a user defined board status. The middle yellow LED is the signal detect indicator. The signal detect LED turns "ON" if the receiver detects light. It can be used as a simple method of checking that the optical network is properly connected to the receiver. The bottom green LED is the OWN DATA indicator. When a board detects its own data returning on the network, it sets this LED "ON".

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VMIPCI-5565 Register Sets

To go beyond the simple target read and write operation of the board, the user must understand and manipulate bits within five register sets. The five register sets are referred to as:

- PCI Configuration Registers
- Local Configuration Registers
- Runtime Registers
- DMA Control Registers
- Reflective Memory (RFM) Control and Status Registers

PCI Configuration Registers – This set of registers is predefined by the PCI Local bus Specification and is standard for all PCI devices. This register set contains the Vendor ID, Device ID, Subsystem Vendor ID, Subsystem ID and Base Address registers. The PCI Configuration Registers are first initialized by a serial EEPROM and then modified as needed by the PCI bus system BIOS. The register set is rarely altered by the user.

Local Configuration Registers – This set of registers resides in the PLX PCI interface device. Like the previous set of registers, the Local Configuration registers are also initialized to a normal operating configuration from a serial EEPROM. Occasionally, a user may wish to modify a Local Configuration Register to better match the VMIxxx-5565 to the host system at start up. After that, the Local Configuration Register settings are seldom modified. The starting location of the Local Configuration Registers is defined in the PCI Configuration Registers, Base Address Register 0 and/or Base Address Register 1.

Runtime Registers – This set of registers is actually a subset of the Local Configuration Registers and is accessed at locations offset from the value in the Base Address Registers 0 or 1. Unlike the other registers, the Runtime Registers frequently change during operation. One significant register in this register set is the PLX Interrupt Control and Status register (INTCSR).

DMA Control Registers – This register set, like the Runtime Registers, is actually a subset of the Local Configuration Registers and is accessed at locations offset from the value in Base Address Registers 0 or 1. The DMA Control Registers are used to operate the two DMA engines.

Reflective Memory (RFM) Control and Status Registers – Unlike the previous four register sets, the RFM Control and Status Registers do not reside in the PLX PCI interface device but, rather are located in additional board circuitry. The RFM Control and Status Registers implement the functions unique to the VMIxxx-5565 Reflective Memory board. These functions include RFM operation status, detailed control of the RFM sources for the PCI interrupt, and network interrupt access. The RFM Control and Status Registers are accessed at locations offset from the value in Base Address Register 2 (PLX also refers to this address space as “Local Address Space 0”).

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Reflective Memory RAM

The actual onboard Reflective Memory SDRAM is available in two sizes: 64MB or 128MB with parity. The SDRAM starts at the location specified in Base Address Register 3 (PLX refers to this address space as “Local Address Space 1”). Unlike the previous versions of GE Fanuc Embedded Systems’ Reflective Memory products, the RFM Control and Status Registers do NOT replace the first $40 locations of RAM. The offset address range is $0 to $3FFFFFF for the 64MB option, or $0 to $7FFFFFF for the 128MB option.

Parity Function

The parity function is not enabled at power up and must be enabled by setting bits 0, 6 and 7 in the Local Configuration Register’s INTCSR at offset $68, and also by setting Bit 13 in the RFM Control and Status Register’s Local Interrupt Enable (LIER) register at offset $14. To use the parity function, writes must occur on 32-bit (Lword) or 64-bit (Qword) boundaries. While parity is active, 8-bit (byte) writes and 16-bit (word) writes are prohibited. In addition, since the RAM does not power up in a valid parity state, any location that is to be read with parity must first be initialized by a write of some data pattern. Otherwise the read will assert an erroneous parity error.

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Interrupt Circuits

The VMIPCI-5565 has a single PCI interrupt output (INTA#). One or more events on the VMIPCI-5565 can cause the interrupt. The sources of the PCI interrupt can be individually enabled and monitored through several registers.

The interrupt circuitry of the VMIPCI-5565 is arranged in two tiers. The first tier of interrupts are enabled and monitored in the PLX device by the Local Configuration Register's INTCSR register at offset $68. The optional sources for monitoring of the first tier interrupts include:

1. Local-to-PCI Doorbell register
2. Messaging Outbound Post Queue not empty
3. Master/Target Abort Status condition
4. 256 consecutive PCI Retries as PCI bus master
5. DMA Ch 0 Done/Terminal Count
6. DMA Ch 1 Done/Terminal Count
7. Local Interrupt Input (LINTi#)

The first tier sources (1) and (2) listed above have limited use in the VMIPCI-5565. The first tier sources (3) and (4) are used at the discretion of the host system requirements. The first tier sources (5) and (6) are used during DMA cycles and must be further configured in the DMA registers.

The final first tier interrupt source (7) is the Local Interrupt Input (LINTi#). The LINTi# signal is an actual physical input to the PLX device and is significant due to the fact that all secondary tier interrupts are funneled through the LINTi#. Second tier interrupts include several operational faults and four network interrupts. The second tier interrupts are selected and monitored through the two RFM Control and Status Registers referred to as the Local Interrupt Status Register (LISR) and the LIER. For a detailed description of the two registers refer to the ***Programming*** section. A block diagram of the main interrupt circuitry is shown in Figure 1-1 on page 26.

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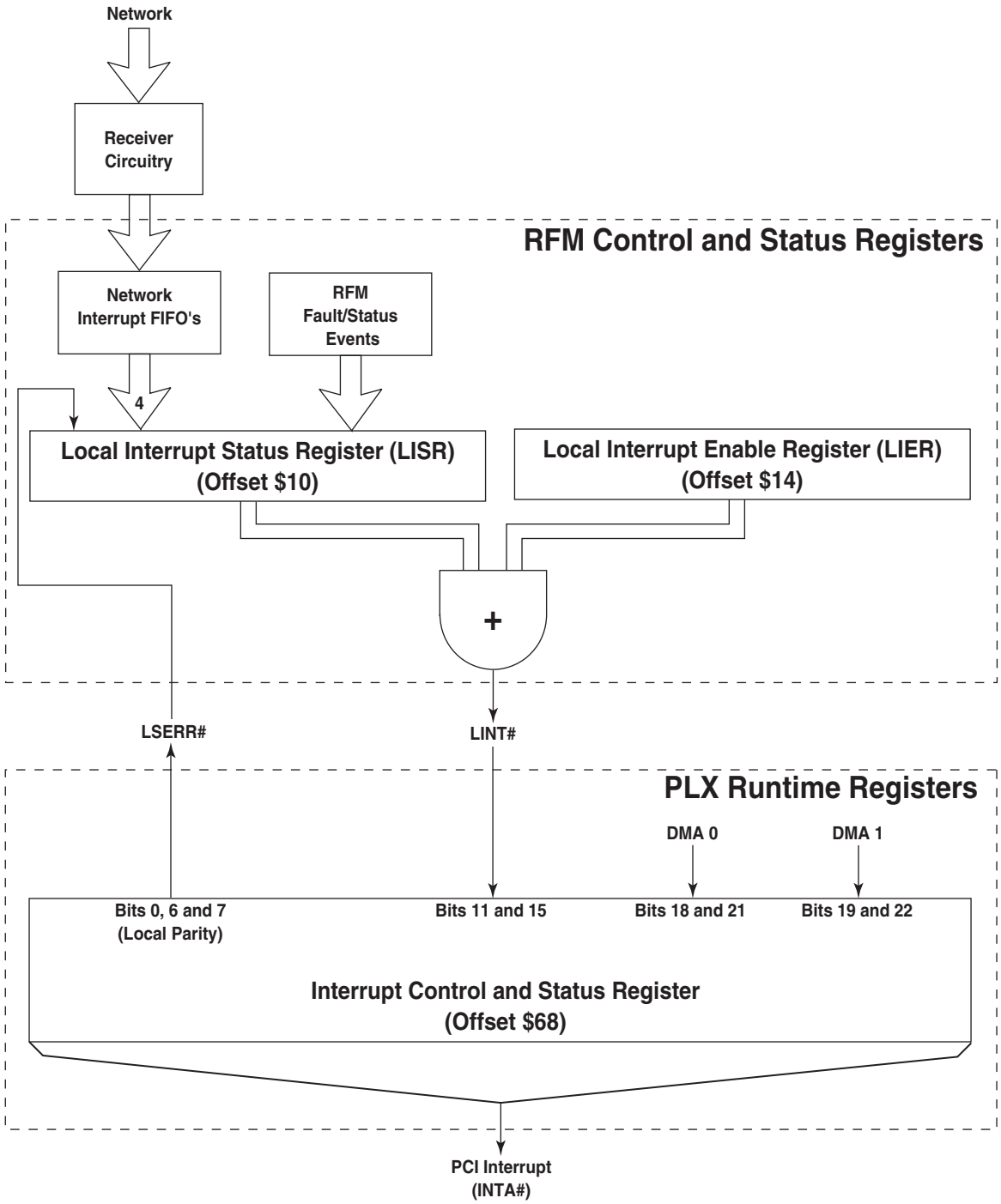


Figure 1-1 VMIPCI-5565 Interrupt Circuitry Block Diagram

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Network Interrupts

The VMIPCI-5565 has the capability of passing interrupts packets over the network in addition to data. The network interrupt packets can be directed to a specific node or broadcast globally to all nodes on the network. Each network interrupt packet contains the sender's node ID, the target (destination) node ID, the interrupt type information and 32 bits of user defined data.

The types of network interrupts include three (3) general purpose interrupts, a network initialized interrupt and a reset node request interrupt. The sending node specifies the target (destination) node, the interrupt type and 32 bits of data using three RFM Control and Status registers. Each receiving node evaluates the interrupt packets as they pass through. If the interrupt is directed to that node, then the sender's node ID is stored in the appropriate Sender ID FIFO (one of four). The Sender ID FIFO is 127 locations deep. The data will be stored in a companion 127 locations deep data FIFO.

If enabled through the LISR, LIER and INTCSR registers, any of the four possible network interrupts can also generate a host PCI interrupt at each receiving node.

The network initialized interrupt is much like one of the three general purpose interrupts and can be used as a fourth general purpose interrupt if desired. However, it does have an additional function. When a VMIPCI-5565 is initialized due to power up or a reset, the local processor can generate a network initialized interrupt globally to all other nodes on the network. This event can be used to inform the host system or another (master) node that some portion of the memory on that node needs to be re-initialized.

The reset node request interrupt is not stored in a FIFO like the other four network interrupts. Furthermore, it does not cause an immediate reset of the board. Instead, it can only set a bit in the LISR register, which will result in a PCI interrupt if enabled. The actual board reset should be performed by the host system in an orderly fashion.

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Redundant Transfer Mode of Operation

The VMIPCI-5565 is capable of operating in a redundant transfer mode. The board is configured for redundant mode when the jumper shunt between pins 1 and 2 of jumper E7 is removed. While in the redundant transfer mode, each packet will be transferred twice, regardless of the dynamic packet size. The receiving circuitry of each node on the network evaluates each of the redundant transfers. If no errors are detected in the first transfer, it is used to update the onboard memory and the second transfer is discarded. However, if the first transfer does contain an error, the second transfer is used to update the onboard memory provided it has no transmission errors. If errors are detected in both transfers, the transfers will not be used and the data is completely removed from the network.

Statistically, redundant transfer mode greatly reduces the chance that any data is dropped from the network. However, the redundant transfer mode also reduces the effective network transfer rates. The single Lword (4 byte) transfer rate drops from the non-redundant rate of 47.1MB/s to approximately 20MB/s. The 16 Lword (64 byte) transfer rate drops from the non-redundant rate of 174MB/s to the redundant rate of 87MB/s.

Rogue Packet Removal Operation

A rogue packet is a packet that does not belong to any node on the network. Recalling the basic operation of Reflective Memory, one node originates a packet on the network in response to a memory write from the host. The packet is transferred around the network to all nodes until it returns to the originating node. It is then a requirement of the originating node to remove the packet from the network. If, however, the packet somehow gets altered as it passes through another node or if the originating node begins to malfunction, then the originating node may fail to recognize the packet as its own and will not remove the packet from the network. In this case, the packet will continue to traverse the network.

Rogue packets are extremely rare. Their existence indicates a malfunctioning board due to true component failure, or due to operation in an overly harsh environment. Normally, the solution is to isolate and replace the malfunctioning board and/or improve the environment. However, some users prefer to tolerate sporadic rogue packets rather than halt the system for maintenance provided the rogue packets are removed from the network.

To provide tolerance to rogue packet faults, the VMIPCI-5565 contains circuitry which allows it to operate as one of two Rogue Masters. A rogue master alters each packet as it passes through from another node. If the same packet returns to the rogue master a second time, the Rogue Master recognizes that it is a rogue packet and removes it from the link. When a rogue packet is detected, a rogue packet fault flag is set in the register called the LISR. The assertion of the rogue packet fault bit may optionally assert a PCI interrupt to inform the host that the condition exists.

Two rogue masters, Rogue Master 0 and Rogue Master 1, are provided to cross check each other. Rogue Master 0 is enabled by removing the jumper shunt between pins 3 and 4 of jumper block E7. Rogue Master 1 is enabled by removing the jumper shunt between pins 5 and 6 of jumper block E7. Just as two boards in a network should not have the same node ID, two boards in the same network should not be set as the same Rogue Master. Otherwise, one of the two will erroneously remove packets originated by the other.

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CHAPTER 2

Configuration and Installation

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Introduction

This chapter describes the installation and configuration of the board. Cable configuration and board layout are illustrated in this chapter.

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Unpacking Procedures

CAUTION: Some of the components assembled on GE Fanuc Embedded Systems' products may be sensitive to electrostatic discharge and damage may occur on boards that are subjected to a high-energy electrostatic field. When the board is placed on a bench for configuring, etc., it is suggested that conductive material should be inserted under the board to provide a conductive shunt. Unused boards should be stored in the same protective boxes in which they were shipped.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to GE Fanuc Embedded Systems together with a request for advice concerning the disposition of the damaged item(s).

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Jumper Configuration and Location

Prior to installing the VMIPCI-5565 on a host board, the desired node ID must be set by installing or removing the jumper shunts on jumper block E4. Each node in the network must have a unique node ID. See Figure 2-1 on page 32 for the location of jumper block E4. Jumper block E4 can accommodate 8 jumper shunts, which correspond to 8 node ID select signal lines. The 8 node ID select lines permit any binary node ID from 0 to $FF (255 decimal). Jumper block E4, pins 1 and 2 correspond to the least significant node ID line and pins 15 and 16 correspond to the most significant node ID line. Installing a jumper shunt sets the binary node ID line low (0), while removing a jumper shunt sets the binary node ID line high (1). The Table 2-1 below provides examples of possible node IDs.

Table 2-1 Example Node ID

E4 1 to 2	E4 3 to 4	E4 5 to 6	E4 7 to 8	E4 9 to 10	E4 11 to 12	E4 13 to 14	E4 15 to 16	Node ID Hex (Dec.)
Installed	Installed	Installed	Installed	Installed	Installed	Installed	Installed	$0 (0)
Removed	Installed	Installed	Installed	Installed	Installed	Installed	Installed	$1 (1)
Installed	Removed	Installed	Installed	Installed	Installed	Installed	Installed	$2 (2)
Installed	Installed	Removed	Installed	Installed	Installed	Installed	Installed	$4 (4)
Installed	Installed	Installed	Removed	Installed	Installed	Installed	Installed	$8 (8)
Installed	Installed	Installed	Installed	Removed	Installed	Installed	Installed	$10 (16)
Installed	Installed	Installed	Installed	Installed	Removed	Installed	Installed	$20 (32)
Installed	Installed	Installed	Installed	Installed	Installed	Removed	Installed	$40 (64)
Installed	Installed	Installed	Installed	Installed	Installed	Installed	Removed	$80 (128)
Removed	Removed	Removed	Removed	Removed	Removed	Removed	Removed	$FF (255)

Jumper E7 Configuration

Prior to installing the VMIPCI-5565 in the host system, jumper E7 must be configured for the appropriate mode of operation. Jumper E7 controls three functions on the board:

1. Pins 1 and 2 select the non-redundant (fast) or redundant network transfer modes.
2. Pins 3 and 4 enable or disable the Rogue Master 0 function
3. Pins 5 and 6 enable or disable the Rogue Master 1 function.

Pins 7 and 8, are currently reserved and should not be used. Table 2-2 on page 32 details the functions selected by the installation or removal of the jumper shunts. The default factory configuration is all jumper shunts installed (except pins 7 and 8).

NOTE: Pins 7 and 8 of Jumper E7 are not used (reserved), and should not have jumper shunts installed.

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Table 2-2 E7 Jumper Configuration

E7 Pins	Installed/Omitted	Function/Mode Selected
1 to 2	Installed	Non-redundant (Fast) network transfer mode selected
	Omitted	Redundant network transfer mode selected
3 to 4	Installed	Rogue Master 0 function disabled
	Omitted	Rogue Master 0 function enabled
5 to 6	Installed	Rogue Master 1 function disabled
	Omitted	Rogue Master 1 function enabled
7 to 8	**None**	**These pins are RESERVED, NO jumper shunt should be installed.**

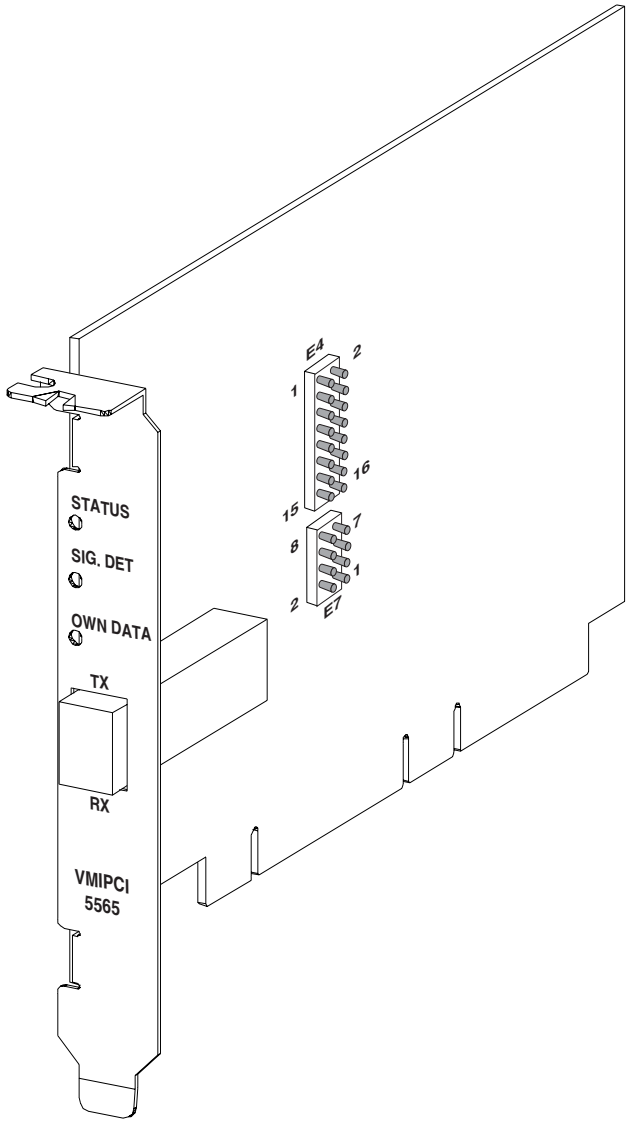


Figure 2-1 VMIPCI-5565 Jumper Location

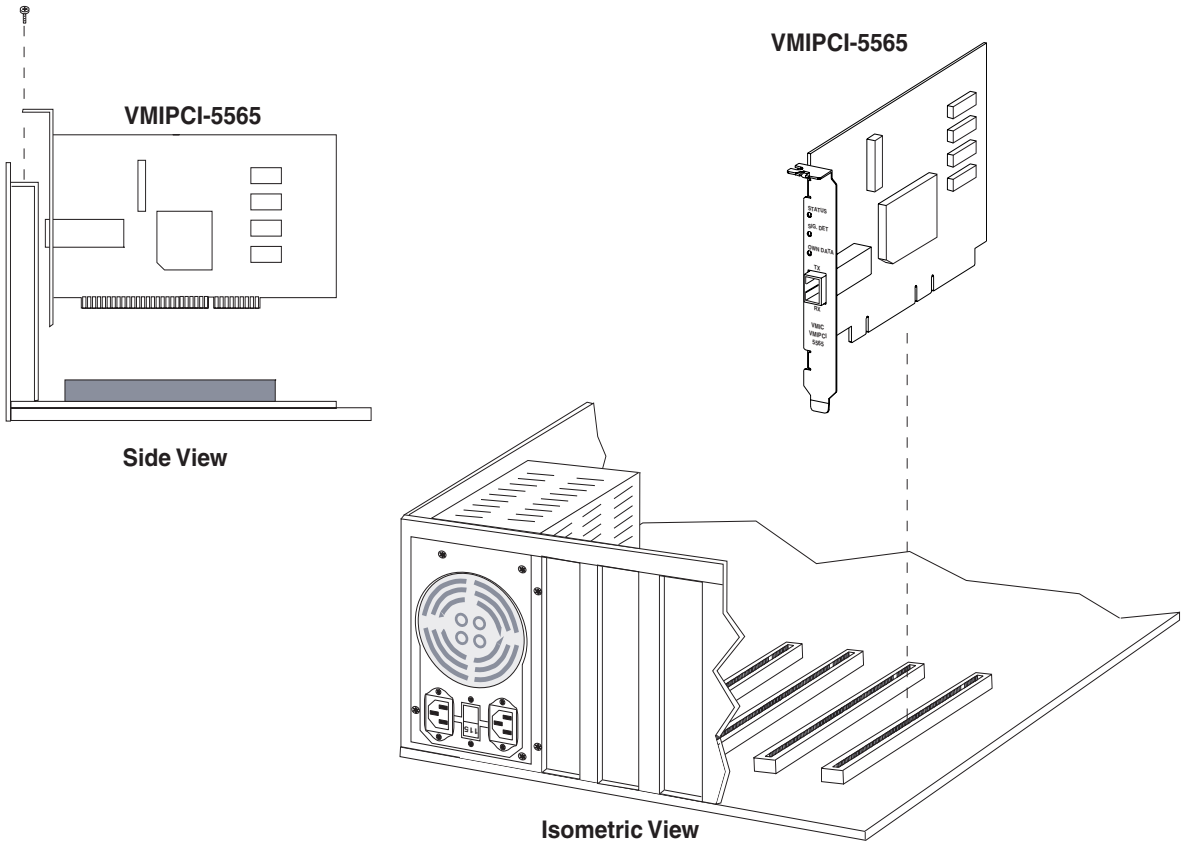
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Physical Installation

CAUTION: Do not install or remove the board while power is applied.

Host PCI compatible sites vary widely in appearance and board installation procedures. GE Fanuc Embedded Systems recommends examining the host system installation procedures prior to installing this board. The following procedure outlines the installation of the VMIPCI-5565 onto a suitable PCI bus motherboard with an available PCI connector.

1. Remove the cover from the chassis. Ensure that the node ID has been set prior to installation. Also setup board for the desired mode of operation. See "Jumper Configuration and Location" on page 31.
2. Install the VMIPCI-5565 firmly onto the PCI connector (refer to Figure 2-2 for installation of the VMIPCI-5565). Install the screws to secure the VMIPCI-5565 to the chassis retaining bracket.
3. Re-install the cover on the chassis, apply power.



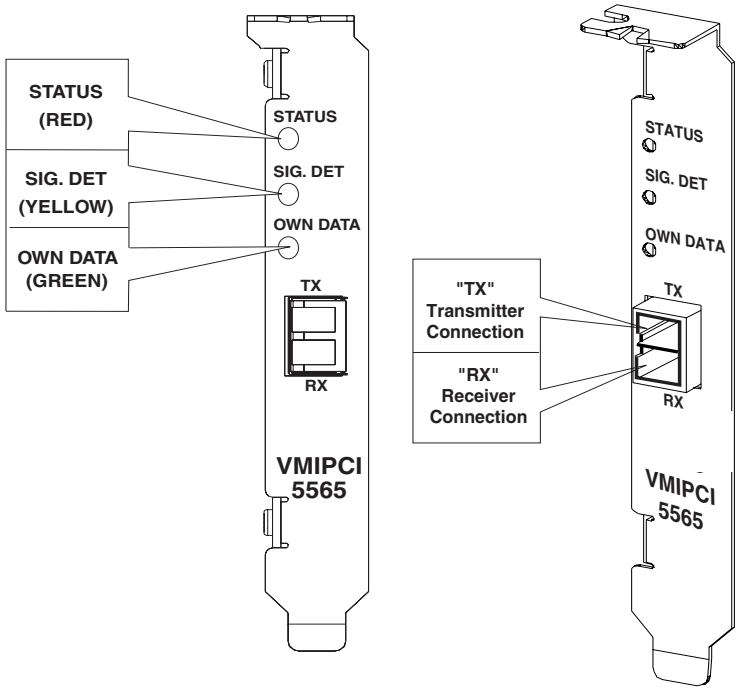
NOTE: The VMIPCI-5565 is designed to interface with any suitable PCI compliant motherboard using a direct PCI bus interface, compliant with v2.2 of the PCI signalling specification as defined by *IEEE P1386.1 Draft 2.0*.

Figure 2-2 Installing the VMIPCI-5565

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Front Panel Description

The VMIPCI-5565 has an optical transceiver located on the front panel. Figure 2-3 below is an illustration of the front panel. The Reflective Memory board has three LED indicators located on the front panel. Table 2-3 below outlines the front panel LEDs. The port above the label “RX” is the receiver and the port below the “TX” is the transmitter. The VMIPCI-5565 uses “LC” type fiber-optic cables.



CAUTION: When the fiber-optic cables are not connected, the supplied dust caps need to be installed to keep dust and dirt out of the optics. Do not power up the VMIPCI-5565 without the fiber-optic cables installed. This could cause eye injures.

Figure 2-3 VMIPCI-5565 Front Panel

Table 2-3 LED Descriptions

LED	Color	Description
Status	Red	User defined board status indicator.
SIG. DET.	Yellow	Indicates optical network connection.
Own Data	Green	Detects when own data is received.

The status LED’s power up default state is “ON”. The LED is a user defined board status indicator. The status LED can toggle “ON” or “OFF” by writing to Bit 31 of the Control and Status register. The signal detect LED turns “ON” if the receiver detects light and can be used as a simple method of checking that the optical network is properly connected to the receiver. The Own Data LED is turned “ON” when the board detects its own data returning over the network.

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Cable Configuration

The VMIPCI-5565 is available with a multimode or single mode fiber-optic interface. Figure 2-4 is an illustration of the 'LC' type multimode or single mode fiber-optic connector.

Cable Specification:

- Simplex, multi-mode, graded index glass fiber
- Core diameter = 62.5 ±3µM
- Cladding diameter = 125 ±2µM
- Jacket outer diameter = 3.0mm ±.1mm
- Attenuation: 4.0dB/Km (max) at 850nm, 1.75dB/Km (max) at 1300nm
- Bandwidth: 160 to 300MHz-Km (min) at 850nm, 300 to 700MHz-Km (min) at 1300nm
- UL type OFNR, CSA type OFN FT4

Connector Specification:

- Compatible with NTT SC standard and JIS C 5973 compliant
- Ceramic ferrule
- Insertion loss: 0.35dB (max) multi-mode
- Fiber clad diameter: 125µM
- Jacket diameter: 3.0mm
- Temperature range: -20 °C to +85 °C

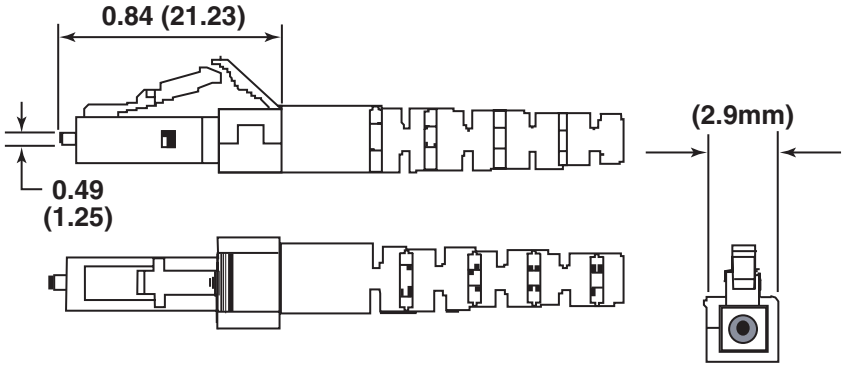


Figure 2-4 'LC' Type Multimode Fiber-Optic Cable Connector

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VMIPCI-5565 Connectivity

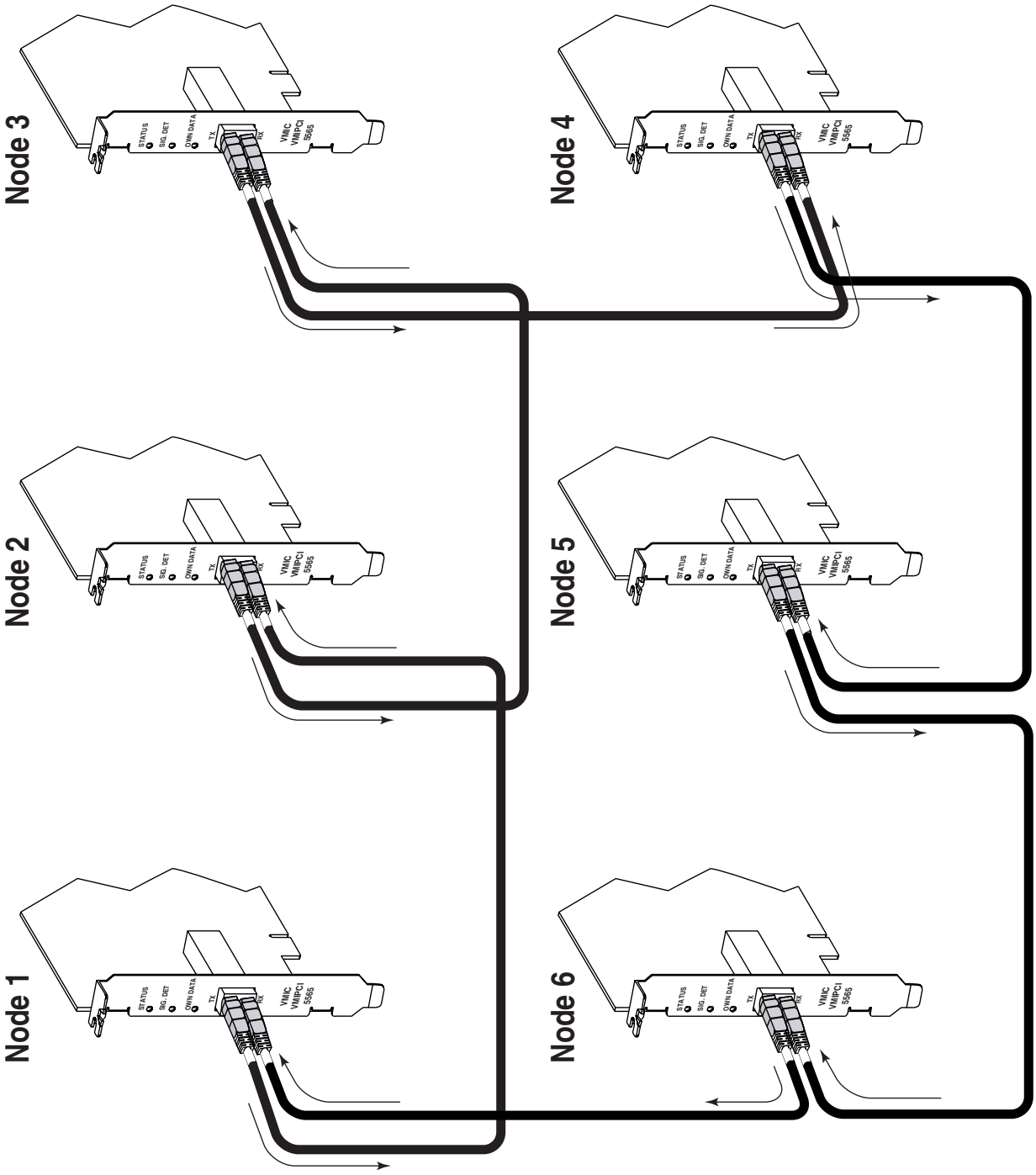


Figure 2-5 Example: Six Node Ring Connectivity

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CHAPTER 3

Programming

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Introduction

Basic target write and read operations of the VMIPCI-5565 require little or no software. The board will power up in a functional mode. However, the user will have to examine the PCI Configuration registers (Base Address Register 0, 1, 2 and 3) at least once when the board is installed in a new system to learn where the system BIOS has located the other register sets and the Reflective Memory. The location of the register sets and the Reflective Memory will vary from system to system, and can even vary from slot to slot within a system. For operations beyond the basic setup, such as enabling or disabling interrupts or performing DMA cycles, the user must know the specific bit assignments of the registers within the five register sets. That information is provided in this Chapter.

The five register sets are:

- PCI Configuration Registers
- Local Configuration Registers
- Runtime Registers
- DMA Control Registers
- RFM Control and Status Registers

The PLX 9656 PCI interface device is a highly versatile device, which was intended for many types of operation. As a result, many registers within these sets and many bit functions within each register do not apply to VMIPCI-5565 operation. The following sections will make an effort to point out those registers and bit functions that clearly do not apply. However, to maintain versatility those registers that might have a use are included. The PLX 9656 PCI interface device is capable of operating in three different local bus modes. The three modes are “M”, “C” and “J”. Furthermore, the local bus may be constructed in widths of 8, 16 or 32 bits. The bus mode and width has an influence on which registers and bit functions apply. Please note for the VMIPCI-5565, the PLX 9656 device is hardwired to operate in the J mode with a bus width of 32 bits.

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PCI Configuration Registers

The PCI Configuration registers are located in 256 bytes of the PCI Configuration Space, which follows a template defined by the *PCI Specification v2.2*. The first 64 bytes of the PCI Configuration Space are composed of a fully predefined header. Within that header region, each device implements only the necessary and relevant registers. However, all registers and bit functions within the header region, that are present, must comply with the definitions of the PCI Specification. Beyond the first 64 byte boundary, each device can implement additional device unique registers. Currently the PLX 9656 implements 14 additional registers. Although the PCI Configuration registers are accessible at all times, they are rarely altered by the user.

Table 3-1 PCI Configuration Registers

PCI Configuration Register Address	To ensure software compatibility with other versions of the PLX 9656 family and to ensure compatibility with future enhancements, write zero (0) to all unused bits. 31 30 24 23 16 15 8 7 0	PCI Writable	Serial EEPROM Writable
$00	Device ID / Vendor ID	N	Y
$04	Status / Command	Y	N
$08	Class Code / Revision ID	N	Y [31:8]
$0C	BIST / Header Type / PCI Bus Latency Timer / Cache Line Size	Y [7:0}	N
$10	PCI Base Address 0; used Memory-Mapped Configuration Registers (PCIBAR0)	Y	N
$14	PCI Base Address 1; used I/O-Mapped Configuration Registers (PCIBAR1)	Y	N
$18	PCI Base Address 2; used for Local Address Space 0 (PCIBAR2)	Y	N
$1C	PCI Base Address 3; used for Local Address Space 1 (PCIBAR3)	Y	N
$20	PCI Base Address 4; used for Local Address Space 2 (PCIBAR4)	Y	N
$24	PCI Base Address 5; used for Local Address Space 3 (PCIBAR5)	Y	N
$28	Cardbus CIS Pointer **(Not Supported)**	N	N
$2C	Subsystem ID / Subsystem Vendor ID	N	Y
$30	PCI Base Address for Local Expansion ROM	Y	N
$34	**Reserved** / Next_Cap Pointer	Y [7:0]	N
$38	**Reserved**	N	N
$3C	Max_Lat / Min_Gnt / Interrupt Pin / Interrupt Line	Y [7:0] Local [31:0]	Y [31:0]
$40	Power Management Capabilities / Next_Cap Pointer / Capabilities ID	Y [31:8]	N
$44	Data / PMCSR Bridge Support Extensions / Power Management Control/Status Register	Y [15,12:8,1:0]	N
$48	**Reserved** / Control/Status Register / Next_Cap Pointer / Capabilities ID	Y [23:16], Local [15:0]	Y [15:0]
$4C	F / VPD Address / Next_Cap Pointer / Capabilities ID	Y [31:16], Local [15:8]	N
$50	VPD Data	Y	N

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NOTE: All registers can be written to or read from in Byte, Word or Longword (Lword) accesses.

Table 3-2 PCI Configuration ID Register

PCI Configuration ID: PCIIDR, Offset $00				
Bit	**Description**	**Read**	**Write**	**Value after PCI Reset**
15:0	**Vendor ID**. Identifies manufacturer of device. Defaults to the PCI SIG-issued Vendor ID of PLX ($10B5) if blank or if no serial EEPROM is present.	Yes	Local/ Serial EEPROM	$114A or 0
31:16	**Device ID**. Identifies particular device. Defaults to PLX part number for PCI interface chip ($9656) if blank or no serial EEPROM is present.	Yes	Local/ Serial EEPROM	$5565 or 0

Table 3-3 PCI Command Register

PCI Command: PCICR, Offset $04				
Bit	**Description**	**Read**	**Write**	**Value after *PCI Reset**
0	**I/O Space**. Writing a one (1) allows the device to respond to I/O Space accesses. Writing a zero (0) disables the device from responding to I/O Space accesses.	Yes	Yes	0
1	**Memory Space**. Writing a one (1) allows device to respond to Memory Space accesses. Writing a zero (0) disables the device from responding to Memory Space accesses.	Yes	Yes	0
2	**Master Enable**. Writing a one (1) allows the device to behave as a bus master. Writing a zero (0) disables the device from generating bus master accesses.	Yes	Yes	0
3	**Special Cycle. Not Supported**	Yes	No	0
4	**Memory Write and Invalidate Enable**. Writing a one (1) enables the Memory Write and Invalidate mode for Direct Master and DMA. (Refer to the DMA Mode registers, DMAMODE0[13] and/or DMAMODE1[13].)	Yes	Yes	0
5	**VGA Palette Snoop. Not Supported**	Yes	No	0
6	**Parity Error Response**. Writing a zero (0) indicates parity error is ignored and the operation continues. Writing a one (1) indicates parity checking is enabled.	Yes	Yes	0
7	**Wait Cycle Control**. Controls whether a device does address/data stepping. Writing a zero (0) indicates the device never does stepping. Writing a one (1) indicates the device always does stepping. (**NOTE:** Hardwired to zero (0).)	Yes	No	0
8	**SERR# Enable**. Writing a 1 enables SERR# driver. Writing a zero (0) disables SERR# driver.	Yes	Yes	0
9	**Fast Back-to-Back Enable**. Indicates what type of fast back-to-back transfers a master can perform on the bus. Writing a one (1) indicates fast back-to-back transfers can occur to any agent on the bus. Writing a zero (0) indicates fast back-to-back transfers can only occur to the same agent as in the previous cycle. (**NOTE:** Hardwired to zero (0).)	Yes	No	0
15:10	**Reserved**	Yes	No	$0
***NOTE:** These values will be altered by system BIOS during the system boot process.				

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Table 3-4 PCI Status Register

PCI Status: PCISR, Offset $06				
Bit	**Description**	**Read**	**Write**	**Value after PCI Reset**
3:0	**Reserved**	Yes	No	$0
4	**New Capabilities Functions Support**. Writing a one (1) supports New Capabilities Function. If enabled, the first New Capability Function ID is located at PCI Configuration offset [$40]. Can be written only from the Local bus. Read-only from the PCI bus.	Yes	Local	1
5	**66MHz Capable**. If set to one (1), this device supports 66MHz PCI clock environment.	Yes	Local	1
6	**User Definable Functions.** If set to one (1), this device supports user definable functions. Can be written from the Local bus only. Read-only from the PCI bus.	Yes	Local	0
7	**Fast Back-to-Back Capable**. Writing a one (1) indicates an adapter can accept fast back-to-back transactions. (**NOTE:** Hardwired to one (1).)	Yes	No	1
8	**Master Data Parity Error Detected.** Set to one (1) when three conditions are met: 1). PLX 9656 asserted PERR# or acknowledged PERR# asserted. 2). PLX 9656 was Bus Master for operation in which error occurred. 3). Parity Error Response bit is set (PCICR[6]=1). Writing a one (1) clears this bit to zero (0).	Yes	Yes/Clr	0
10:9	**DEVSEL# Timing**. Indicates timing for DEVSEL# assertion. Writing a 01 sets this bit to medium. (**NOTE:** Hardwired to 01.)	Yes	No	01
11	**Target Abort**. When set to one (1), indicates the PLX 9656 has signaled a Target Abort. Writing a one (1) clears this bit to zero (0).	Yes	Yes/Clr	0
12	**Received Target Abort**. When set to one (1), indicates the PLX 9656 has received a Target Abort signal. Writing a 1 clears this bit to zero (0).	Yes	Yes/Clr	0
13	**Received Master Abort**. When set to one (1), indicates the PLX 9656 has received a Master Abort signal. Writing a 1 clears this bit to zero (0).	Yes	Yes/Clr	0
14	**Signal System Error**. When set to one (1), indicates the PLX 9656 has reported a system error on SERR#. Writing a one (1) clears this bit to zero (0).	Yes	Yes/Clr	0
15	**Detected Parity Error**. When set to one (1), indicates the PLX 9656 has detected a PCI bus parity error, even if parity error handling is disabled (the Parity Error Response bit in the Command register is clear). One of three conditions can cause this register to be set: 1). PLX 9656 detected parity error during PCI Address phase. 2). PLX 9656 detected data parity error when it is the target of a write. 3). PLX 9656 detected data parity error when performing Master Read operation. Writing a one (1) clears this bit to zero (0).	Yes	Yes/Clr	0

Table 3-5 PCI Revision ID Register

PCI Revision ID: PCIREV, Offset $08				
Bit	**Description**	**Read**	**Write**	**Value after PCI Reset**
7:0	**Revision ID**. Revision of board	Yes	Local/ Serial EEPROM	Current Rev#

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Table 3-6 PCI Class Code Register

PCI Class Code: PCICCR, Offset $09				
Bit	**Description**	**Read**	**Write**	***Value after Initialization**
7:0	**Register Level Programming Interface**. None defined.	Yes	Local/ Serial EEPROM	$0
15:8	**Subclass Code**	Yes	Local/ Serial EEPROM	$80
23:16	**Base Class Code**	Yes	Local/ Serial EEPROM	$02
Base Class Code of $02 equals Network Controller. Subclass Code of $80 equals other network controller.				
***NOTE:** Values listed are present after initialization by a serial EEPROM.				

Table 3-7 PCI Cache Line Size Register

PCI Cache Line Size: PCICLSR, Offset $0C				
Bit	**Description**	**Read**	**Write**	***Value after PCI Reset**
7:0	**System Cache Line Size**. Specified in units of 32-bit words (8 or 16 Lwords). If a size other than 8 or 16 is specified, the PLX 9656 performs Write transfers rather than Memory Write and Invalidate transfers.	Yes	Yes	$0
***NOTE**: These values can be altered by system BIOS during the system boot process.				

Table 3-8 PCI Latency Timer Register

PCI Latency Timer: PCILTR, Offset $0D				
Bit	**Description**	**Read**	**Write**	***Value after PCI Reset**
7:0	**PCI Bus Latency Timer.** Specified amount of time (in units of PCI bus clocks) the PLX 9656, as a bus master can burst data on the PCI bus.	Yes	Yes	$0
***NOTE**: These values can be altered by system BIOS during the system boot process.				

Table 3-9 PCI Header Type Register

PCI Header Type: PCIHTR, Offset $0E				
Bit	**Description**	**Read**	**Write**	**Value after PCI Reset**
6:0	**Configuration Layout Type**. Specifies layout of bits $10 through $3F in Configuration Space. Only one encoding, $0, is defined. All other encoding are reserved.	Yes	Local	$0
7	**Header Type**. Writing a one (1) indicates multiple functions. Writing a zero (0) indicates single function.	Yes	Local	0

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Table 3-10 PCI Built-in Self Test Register

PCI Built-in Self Test: PCIBISTR, Offset $0F				
Bit	**Description**	**Read**	**Write**	**Value after PCI Reset**
3:0	**BIST Pass/Failed**. Writing $0 indicates a device passed its test. Non-$0 values indicate a device failed its test. Device-specific failure codes can be encoded in a non-$0 value	Yes	Local	$0
5:4	**Reserved.**	Yes	No	00
6	**PCI BIST Interrupt Enable.** The PCI bus writes a one (1) to enable BIST, which generates an interrupt to the Local bus. The Local bus resets this bit when BIST is complete. The software should fail device if BIST is not complete after two seconds. Refer to the Runtime registers for interrupt Control and Status.	Yes	Yes	0
7	**BIST Support**. Returns a one (1) if device supports BIST. Returns a zero (0) if device is not BIST-compatible.	Yes	Local	0

PCI Base Address Register 0 contains the starting address for memory mapped accesses to Local, Runtime and DMA Registers. The value in this register is loaded by the system BIOS.

Table 3-11 PCI Base Address Register 0 for Memory Accesses to Local, Runtime and DMA Registers

PCI Base Address Register 0: PCIBAR0, Offset $10				
Bit	**Description**	**Read**	**Write**	**Value after PCI Reset**
0	**Memory Speed Indicator**. Writing zero (0) indicates the register maps into Memory Space. Writing a one (1) indicates the register maps into I/O Space. (**NOTE**: Hardcoded to zero (0).)	Yes	No	0
2:1	**Register Location.** Values: 00 - Locate anywhere in 32-bit Memory Address Space. 01 - Locate below 1MB Memory Address Space. 10 - Locate anywhere in 64-bit Memory Address Space. 11 - Reserved (**NOTE**: Hardcoded to 00.)	Yes	No	00
3	**Prefetchable.** Writing a one (1) indicates there are no side effects on reads. Does not affect operation of the PLX 9656. (**NOTE:** Hardcoded to zero (0).)	Yes	No	0
7:4	**Memory Base Address**. Memory Base Address for access to Local, Runtime and DMA registers (requires 256 bytes). (**NOTE**: Hardcoded to $0.)	Yes	No	$0
31:8	**Memory Base Address**. Memory Base Address for access to Local, Runtime and DMA registers.	Yes	Yes	*$0
***NOTE**: This value can be altered by system BIOS during the system boot process.				

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PCI Base Address Register 1 contains the starting address for I/O mapped accesses to Local Configuration, Runtime and DMA Registers. The value in this register is loaded by the system BIOS.

Table 3-12 PCI Base Address Register 1 for Memory Accesses to Local, Runtime and DMA Registers

PCI Base Address Register 1: PCIBAR1, Offset $14				
Bit	**Description**	**Read**	**Write**	**Value after PCI Reset**
0	**Memory Space Indicator**. Writing a zero (0) indicates the register maps into Memory Space. Writing a one (1) indicates the register maps into I/O Space. **(NOTE:** Hardcoded to one (1).)	Yes	No	1
1	**Reserved.**	Yes	No	0
7:2	**I/O Base Address.** Base Address for I/O access to Local, Runtime and DMA registers (requires 256 bytes). (**NOTE:** Hardcoded to $0.)	Yes	No	$0
31:8	**I/O Base Address**. I/O Base Address for access to Local, Runtime and DMA registers. PCIBAR1 can be enabled or disabled by setting or clearing the Base Address Register 1 Enable bit (LMISC1[0]).	Yes	Yes	*$0
***NOTE**: This value will be altered by the system BIOS during the system boot process.				

PCI Base Address Register 2 contains the starting address for memory mapped accesses to the RFM Control and Status Registers. The value in this register is loaded by the system BIOS.

Table 3-13 PCI Base Address Register 2 for Memory Accesses to Local Address Space 0

PCI Base Address Register 2: PCIBAR2, Offset $18				
Bit	**Description**	**Read**	**Write**	**Value after PCI Reset**
0	**Memory Space Indicator**. Writing zero (0) indicates the register maps into Memory Space. Writing a one (1) indicates the register maps into I/O Space. (Specified in LAS0RR register.)	Yes	No	0
2:1	**Register Location.** Values: 00 - Locate anywhere in 32-bit Memory Address Space. 01 - Locate below 1MB Memory Address Space. 10 - Locate anywhere in 64-bit Memory Address Space 11 - Reserved (Specified in LAS0RR register.) If I/O Space, Bit 1 is always 0 and Bit 2 is included in the base address.	Yes	Mem: No I/O: Bit 1 no, Bit 2 yes	00
3	**Prefetchable (If Memory Space).** Writing a one (1) indicates there are no side effects on reads. Reflects value of LAS0RR[3] and provides only status to the system. Does not affect operation of the PLX 9656. The associated Bus Region Descriptor register controls prefetching functions of this address space. (Specified in LAS0RR register.) If I/O Space, Bit 3 is included in the base address.	Yes	Mem: No I/O: Yes	0
31:4	**Memory Base Address**. Memory Base Address for access to Local Address Space 0. PCIBAR2 can be enabled or disabled by setting or clearing the Space 0 Enable bit (LAS0BA[0]).	Yes	Yes	*$0
***NOTE**: This value can be altered by system BIOS during the system boot process.				

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PCI Base Address Register 3 contains the starting address for memory mapped accesses to the Reflective Memory RAM. The address offset range is $0 to $3FFFFFF for the 64MB option or $0 to $FFFFFFF for the 128MB option. The value in this register is loaded by the system BIOS.

Table 3-14 PCI Base Address Register 3 for Memory Accesses to Local Address Space 1

PCI Base Address Register 3: PCIBAR3, Offset $1C				
Bit	**Description**	**Read**	**Write**	**Value after PCI Reset**
0	**Memory Space Indicator**. Writing zero (0) indicates the register maps into Memory Space. Writing a one (1) indicates the register maps into I/O Space. (Specified in LAS1RR register.)	Yes	No	0
2:1	**Register Location.** Values: 00 - Locate anywhere in 32-bit Memory Address Space. 01 - Locate below 1MB Memory Address Space. 10 - Locate anywhere in 64-bit Memory Address Space. 11 - Reserved (Specified in LAS1RR register.) If I/O Space, Bit 1 is always 0 and Bit 2 is included in the base address.	Yes	Mem: No I/O: Bit 1 no, Bit 2 yes	00
3	**Prefetchable (If Memory Space).** Writing a one (1) indicates there are no side effects on reads. Reflects value of LAS0RR[3] and provides only status to the system. Does not affect operation of the PLX 9656. The associated Bus Region Descriptor register controls prefetching functions of this address space. (Specified in LAS1RR register.) If I/O Space, Bit 3 is included in the base address.	Yes	Mem: No I/O: Yes	0
31:4	**Memory Base Address**. Memory Base Address for access to Local Address Space 1. PCIBAR2 can be enabled or disabled by setting or clearing the Space 1 Enable bit (LAS1BA[0]=1), PCIBAR3 returns $0	Yes	Yes	*$0
***NOTE**: This value can be altered by system BIOS during the system boot process.				

Table 3-15 PCI Base Address Register 4

PCI Base Address 4: PCIBAR4, Offset $20				
Bit	**Description**	**Read**	**Write**	**Value after PCI Reset**
31:0	**Reserved**.	Yes	No	$0

Table 3-16 PCI Base Address Register 5

PCI Base Address 5: PCIBAR5, Offset $24				
Bit	**Description**	**Read**	**Write**	**Value after PCI Reset**
31:0	**Reserved**.	Yes	No	$0

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Table 3-17 PCI Cardbus CIS Pointer Register

PCI Cardbus CIS Pointer: PCICIS, Offset $28				
Bit	**Description**	**Read**	**Write**	**Value after PCI Reset**
31:0	**Cardbus Information Structure Pointer for PCMCIA**. Not Supported.	Yes	No	$0

Table 3-18 PCI Subsystem Vendor ID Register

PCI Subsystem Vendor ID: PCISVID, Offset $2C				
Bit	**Description**	**Read**	**Write**	**Value after Initialization**
15:0	Subsystem Vendor ID (unique add-in board Vendor ID).	Yes	Local/ Serial EEPROM	$10B5
***NOTE**: The value $10B5 denotes GE Fanuc Embedded Systems' as the system vendor.				

Table 3-19 PCI Subsystem ID Register

PCI Subsystem ID: PCISID, Offset $2E				
Bit	**Description**	**Read**	**Write**	**Value after Initialization**
15:0	Subsystem ID (unique add-in board device ID).	Yes	Local/ Serial EEPROM	$9656
***NOTE**: The value $5565 denotes GE Fanuc Embedded Systems board type (VMIxxx-5565).				

Table 3-20 PCI Expansion ROM Base Register

PCI Expansion ROM Base: PCIERBAR, Offset $30				
Bit	**Description**	**Read**	**Write**	**Value after PCI Reset**
0	**Address Decode Enable**. Writing a one (1) indicates a device accepts accesses to the Expansion ROM address. Writing a zero (0) indicates a device does not accept accesses to Expansion ROM space. Should be set to zero (0) if there is no Expansion ROM. Works in conjunction with EROMRR[0].	Yes	No	0
10:1	**Reserved.**	Yes	No	$0
31:11	**Expansion ROM Base Address (upper 21 bits)**.	Yes	Yes	$0
NOTE: PCI Expansion ROM and related registers are not applicable to the VMIPCI-5565.				

Table 3-21 New Capability Pointer Register

New Capability Pointer: CAP_PTR, Offset $34				
Bit	**Description**	**Read**	**Write**	**Value after PCI Reset**
7:0	**New Capability Pointer**. Offset into PCI Configuration Space for the location of the first item in the New Capabilities Linked List.	Yes	Local	$40

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Table 3-21 New Capability Pointer Register (Continued)

New Capability Pointer: CAP_PTR, Offset $34				
Bit	**Description**	**Read**	**Write**	**Value after PCI Reset**
31:8	**Reserved**.	Yes	No	$0

Table 3-22 PCI Interrupt Line

PCI Interrupt Line: PCIILR, Offset $3C				
Bit	**Description**	**Read**	**Write**	**Value after PCI Reset**
7:0	**Interrupt Line Routing Value**. Value indicates which input of the system interrupt controller(s) is connected to each interrupt line of the device.	Yes	Yes	$0

Table 3-23 PCI Interrupt Pin

PCI Interrupt Pin: PCIIPR, Offset $3D				
Bit	**Description**	**Read**	**Write**	**Value after Initialization**
7:0	**Interrupt Pin Register**. Indicates which interrupt pin the device uses. The following values are decoded (the PLX 9656 supports only INTA#). 1 = INTA# 2 = INTB# 3 = INTC# 4 = INTD#	Yes	Local/ Serial EEPROM	$1

Table 3-24 PCI Min_Gnt

PCI Min_Gnt: PCIMGR, Offset $3E				
Bit	**Description**	**Read**	**Write**	**Value after Initialization**
7:0	**Min_Gnt**. Specifies how long of a burst period a device needs, assuming a clock rate of 33MHz. Value is a multiple of ¼ µsec increments.	Yes	Local/ Serial EEPROM	$0

Table 3-25 PCI Max_Lat

PCI Max_Lat: PCIMLR, Offset $3F				
Bit	**Description**	**Read**	**Write**	**Value after Initialization**
7:0	**Max_Lat**. Specifies how often the device must gain access to the PCI bus. Value is a multiple of ¼ µsec increments.	Yes	Local/ Serial EEPROM	$0

NOTE: The VMIPCI-5565 does not support the optional Power Management, Hot Swap and Vital features of the PCI Specification.

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Local Configuration Registers

The Local Configuration Registers are memory cycle accessible at the offsets from the value stored in Base Address Register 0. They are also I/O cycle accessible at the offsets from the value stored in Base Address Register 1. The offsets are specified below.

Table 3-26 Local Configuration Registers

PCI (Offset from Base Address)	To ensure software compatibility with other versions of the PLX 9656 family and to ensure compatibility with future enhancements, write zero (0) to all unused bits. 31 24 23 16 15 8 7 0	PCI/Local Writable	Serial EEPROM Writable
$00	Range for PCI-to-Local Address Space 0	Y	Y
$04	Local Base Address (Remap) for PCI-to-Local Address Space 0	Y	Y
$08	Mode/DMA Arbitration	Y	Y
$0C	Local Miscellaneous Control | Serial EEPROM Write-Protected Address Boundary | Local Miscellaneous Control 1 | Big/Little Endian Descriptor	Y	Y
$10	Range for PCI-to-Local Expansion ROM	Y	Y
$14	Local Base Address (Remap) for PCI-to-Local Expansion ROM and BREQ0 Control	Y	Y
$18	Local Bus Region Descriptors (Space 0 and Expansion ROM) for PCI-to-Local Accesses	Y	Y
$1C	Range for Direct Master-to-PCI	Y	Y
$20	Local Base Address for Direct Master-to-PCI Memory	Y	Y
$24	Local Base Address for Direct Master-to-PCI I/O Configuration	Y	Y
$28	PCI Base Address (Remap) for Direct Master-to-PCI	Y	Y
$2C	PCI Configuration Address Register for Direct Master-to-PCI I/O Configuration	Y	Y
$F0	Range for PCI-to-Local Address Space 1	Y	Y
$F4	Local Base Address (Remap) for PCI-to-Local Address Space 1	Y	Y
$F8	Local Bus Region Descriptor (Space 1) for PCI-to-Local Accesses	Y	Y
$FC	PCI Base Dual Address Cycle (Remap) for Direct Master-to-PCI (Upper 32 bits)	Y	Y
$100	Reserved | PCI Arbiter Control	Y	Y
$104	PCI Abort Address	N	N

The following Local Configuration Registers, although present in the PLX device, are not applicable to the VMIPCI-5565 board:

- Expansion ROM Range (EROMRR; PCI:$10)
- Expansion ROM Local Base Address (Remap) and BREQo Control (EROMBA; PCI:$14)
- Local Range Register for Direct Master-to-PCI (DMRR; PCI:$1C)
- Local Bus Base Address Register for Direct Master-to-PCI Memory (DMLBAM; PCI:$20)
- Local Base Address Register for Direct Master-to-PCI I/O Config. (DMLBAI; PCI$24)

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- PCI Base Address (Remap) Register for Direct Master-to-PCI Memory (DMPBAM; PCI:$28)
- PCI Configuration Address Register for Master-to-PCI I/O Config. (DMCFGA; PCI:$2C)
- Direct Master PCI Dual Address Cycle Upper Address (DMDAC; PCI:$FC)

Table 3-27 Local Address Space 0 Range Register for PCI-to-Local Bus

Local Address Space 0 Range Register for PCI-to-Local Bus: LAS0RR, Offset $00				
Bit	**Description**	**Read**	**Write**	**Value after Initialization**
0	**Memory Speed Indicator**. Writing zero (0) indicates the register maps into PCI Memory Space. Writing a one (1) indicates Local Address Space 0 maps into PCI I/O Space.	Yes	Yes	0
2:1	When mapped into Memory space, encoding is as follows: 2/1 Meaning 00 Locate anywhere in 32-bit PCI Address Space. 01 Locate below 1MB in PCI Address Space. 10 Locate anywhere in 64-bit PCI Address Space. 11 Reserved When mapped into I/O Space, Bit 1 must be set to zero (0). Bit 2 is included with bits [31:3] to indicate the decoding range.	Yes	Yes	00
3	When mapped into Memory Space, writing a one (1) indicates reads are prefetchable (does not affect operation of the PLX 9656, but is used for system status). When mapped into I/O Space, it is included with bits [31:2] to indicate the decoding range.	Yes	Yes	0
31:4	Specifies which PCI Address bits to use for decoding a PCI access to Local Bus Space 0. Each bit corresponds to a PCI Address bit. Bit 31 corresponds to address Bit 31. Write a one (1) to all bits that must be included in decode and a zero (0) to all others (used in conjunction with PCIBAR2). Default is 1MB. **NOTE**: Range (**not** Range register) must be power of 2. "Range register value" is inverse of range. User should limit all I/O Spaces to 256 bytes per PCI r2.1 spec.	Yes	Yes	$FFF FFFC

Table 3-28 Local Address Space 0 Local Base Address (Remap)

Local Address Space 0 Local Base Address (Remap): LAS0BA, Offset $04				
Bit	**Description**	**Read**	**Write**	**Value after Initialization**
0	**Space 0 Enable**. Writing a one (1) enables decoding of PCI addresses for Direct Slave access to Local Bus Space 0. Writing a zero (0) disables decoding.	Yes	Yes	0
1	**Reserved.**	Yes	No	0
3:2	If Local Bus Space 0 is mapped into Memory Space, bits are not used. When mapped into I/O Space, included with bits [31:4] for remapping.	Yes	Yes	00
31:4	**Remap PCI Address to Local Address Space 0 into Local Address Space.** Bits in this register remap (replace) PCI Address bits used in decode as Local Address bits. **NOTE:** Remap Address value must be a multiple of the Range (**not** the Range register).	Yes	Yes	$C00 0000

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Table 3-29 Mode/DMA Arbitration Register

Mode/DMA Arbitration: MARBR, Offset $08 or $AC				
Bit	**Description**	**Read**	**Write**	**Value after Initialization**
7:0	**Local Bus Latency Timer**. Number of Local Bus clock cycles to occur before de-asserting HOLD and releasing the Local Bus.	Yes	Yes	$00
15:8	**Local Bus Pause Timer**. Number of local Bus clock cycles to occur before reasserting HOLD after releasing the Local Bus. The pause timer is valid only during DMA.	Yes	Yes	$00
16	**Local Bus Latency Timer Enable**. Writing a one (1) enables the pause timer. Writing a zero (0) disables the pause timer.	Yes	Yes	0
17	**Local Bus Pause Timer Enable.** Writing a one (1) enables the pause timer. Writing a zero (0) disables the pause timer.	Yes	Yes	0
18	**Local Bus BREQ Enable**. Writing a one (1) enables the Local Bus BR#/BREQi. When BR#/BREQi is active, the PLX 9656 de-asserts HOLD and releases the Local Bus.	Yes	Yes	1
20:19	**DMA Channel Priority.** When set to 00, these bits indicate a rotational priority scheme**.** Writing a 01 indicates Channel 0 has priority. Writing a 10 indicates Channel 1 has priority. Writing an 11 indicates reserved.	Yes	Yes	00
21	**Local Bus Direct Slave Release Bus Mode**. When set to one (1), the PLX 9656 de-asserts HOLD and releases the Local Bus when the Direct Slave Write FIFO becomes empty during a Direct Slave Write or when the Direct Slave Read FIFO becomes full during a Direct Slave Read.	Yes	Yes	0
22	**Direct Slave LOCK# Enable**. Writing a one (1) enables Direct Slave locked sequences. Writing a zero (0) disables Direct Slave locked sequences.	Yes	Yes	0
23	**PCI Request Mode**. Writing a one (1) causes the PLX 9656 to de-assert REQ# when it asserts FRAME during a master cycle. Writing a zero (0) causes the PLX 9656 to leave REQ# asserted for the entire Bus Master cycle.	Yes	Yes	0
24	**Delayed Read Mode**. When set to a one (1), the PLX 9656 operates in Delayed Transaction mode for Direct Slave reads. The PLX 9656 issues a retry to the PCI Host and prefetches read data.	Yes	Yes	1
25	**PCI Read No Write Mode**. Writing a one (1) forces a retry on writes if a read is pending. Writing a zero (0) allows writes to occur while a read is pending.	Yes	Yes	1
26	**PCI Read with Write Flush Mode**. Writing a one (1) submits a request to flush a pending read cycle if a write cycle is detected. Writing a zero (0) submits a request to not affect pending reads when a write cycle occurs (PCI Specification r2.1 compatible).	Yes	Yes	0
27	**Gate Local Bus Latency Timer with BREQi (C and J modes only).**	Yes	Yes	0
28	**PCI Read No Flush Mode**. Writing a one (1) submits a request to not flush the read FIFO if the PCI read cycle completes (Read Ahead mode). Writing a zero (0) submits a request to flush the read FIFO if a PCI read cycle completes.	Yes	Yes	0
29	When set to zero (0), reads from the PCI Configuration register address $00 returns Device ID and Vendor ID. When set to a one (1), reads from the PCI Configuration register address $00 returns Subsystem ID and Subsystem Vendor ID.	Yes	Yes	0
30	**FIFO Full Status Flag**. When set to a one (1), the Direct Master Write FIFO is almost full. Reflects the value of the DMPAF pin.	Yes	Yes	0
31	**BIGEND#/WAIT# Input/Output Select (M mode only)**. Writing a one (1) selects the wait functionality of the signal. Writing a zero (0) selects Big Endian input functionality.	Yes	Yes	0

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Table 3-30 Big/Little Endian Descriptor Register

Big/Little Endian Descriptor: BIGEND, Offset $0C				
Bit	**Description**	**Read**	**Write**	**Value after Initialization**
0	**Configuration Register Big Endian Mode (Address Invariance)**. Writing a one (1) specifies use of Big Endian data ordering for Local accesses to the Configuration registers. Writing a zero (0) specifies Little Endian ordering. Big Endian mode can be specified for Configuration register accesses by asserting BIGEND# during the address phase of the access.	Yes	Yes	0
1	**Direct Master Big Endian Mode (Address Invariance)**. Writing a one (1) specifies use of Big Endian data ordering for Direct Master accesses. Writing a zero (0) specifies Little Endian ordering. Big Endian mode can be specified for Direct Master accesses by asserting BIGEND# input pin during the address phase of the access.	Yes	Yes	0
2	**Direct Slave Address Space 0 Big Endian Mode (Address Invariance)**. Writing a one (1) specifies use of Big Endian data ordering for Direct Slave accesses to Local Address Space 0. Writing a zero (0) specifies Little Endian ordering.	Yes	Yes	0
3	**Direct Slave Address Expansion ROM 0 Big Endian Mode (Address Invariance)**. Writing a one (1) specifies use of Big Endian data ordering for Direct Slave accesses to Expansion ROM. Writing a zero (0) specifies Little Endian ordering.	Yes	Yes	0
4	**Big Endian Byte Lane Mode**. Writing a one (1) specifies that in any Endian mode, use the following byte lanes for the modes listed. **M Mode** [0:15] for a 16-bit Local Bus [0:7] for an 8-bit Local Bus **C and J Modes** [31:16] for a 16-bit Local Bus [31:24] for an 8-bit Local Bus Writing a zero (0) specifies that in any Endian mode, use the following byte lanes for the modes listed: **M Mode** [16:31] for a 16-bit Local Bus [24:31] for an 8-bit Local Bus **C and J Modes** [15:0] for a 16-bit Local Bus [7:0] for an 8-bit Local Bus	Yes	Yes	0
5	**Direct Slave Address Space 1 Big Endian Mode (Address Invariance)**. Writing a one (1) specifies use of Big Endian data ordering for Direct Slave accesses to Local Address Space 1. Writing a zero (0) specifies Little Endian ordering.	Yes	Yes	0
6	**DMA Channel 1 Big Endian Mode (Address Invariance)**. Writing a one (1) specifies the use of Big Endian data ordering for DMA Channel 1 accesses to the Local Address Space. Writing a zero (0) specifies Little Endian ordering.	Yes	Yes	0
7	**DMA Channel 0 Big Endian Mode (Address Invariance)**. Writing a one (1) specifies use of Big Endian data ordering for DMA Channel 0 accesses to the Local Address Space. Writing a zero (0) specifies Little Endian ordering.	Yes	Yes	0

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Table 3-31 Local Miscellaneous Control 1 Register

Local Miscellaneous Control 1: LMISC1, Offset $0D				
Bit	**Description**	**Read**	**Write**	**Value after Initialization**
0	**Base Address Register 1 Enable**. If set to a one (1), the Base Address 1 register for I/O accesses to Configuration registers is enabled. If set to a zero (0), the Base Address 1 register for I/O accesses to Configuration registers is disabled.	Yes	Yes	1
1	**Base Address Register 1 Shift**. If Base Address Register 1 Enable is low, and this bit is set to zero (0), then PCIBAR2 and PCIBAR3 remain at PCI Configuration addresses $18 and $1C. If Base Address Register 1 Enable is low, and this bit is set to one (1), then PCIBAR2 (Local Address Space 0) and PCIBAR3 (Local Address Space 1) are shifted to become PCIBAR1 and PCIBAR2 at PCI Configuration addresses $14 and $18. Set if a blank region in Base Address Register Space could not be accepted by system BIOS.	Yes	Yes	0
2	**Local INIT Status**. Writing a one (1) indicates Local INIT done. Response to PCI accesses are Retrys until this bit is set. If the PLX 9656 has a blank serial EEPROM attached, the Local processor must set the Local INIT Status bit to one (1).	Yes	Local/ Serial EEPROM	1
3	**Direct Master (PCI Initiator) Write FIFO Flush during PCI Master Abort**. When set to a one (1), the PLX 9656 flushes the Direct Master Write FIFO each time the Direct Slave or Master Abort occurs. When set to zero (0), the PLX 9656 keeps data in the Direct Master Write FIFO.	Yes	Yes	0
4	**M Mode Direct Master Delayed Read Enable**. Writing a one (1) enables the PLX 9656 to operate in Delayed Transaction mode for Direct Master reads. The PLX 9656 issues a RETRY# to the M mode master and prefetches read data from the PCI bus.	Yes	Yes	0
5	**M Mode TEA# Input Interrupt Mask**. When set to a one (1), TEA# input causes SERR# output on the PCI bus if enabled (PCICR[8]=1) and the Signaled System Error bit is set (PCISR[14]=1). Writing zero (0) masks the TEA# input to create SERR#. The SERR# Status bit is set in both cases.	Yes	Yes	0
6	**Direct Master Write FIFO Almost Full RETRY# Output Enable**. When set to a one (1), the PLX 9656 issues a RETRY# to the MPC850 or MPC860.	Yes	Yes	0
7	**Disconnect with Flush Read FIFO**. A value of one (1) causes a disconnect with flushing of the Read FIFO in Delayed Read mode (MARBR[24]). A value of zero (0) causes a disconnect without flushing the Read FIFO (as a retry).	Yes	Yes	0

Table 3-32 Serial EEPROM Write-Protected Address Boundary Register

Serial EEPROM Write-Protected Address Boundary: PROT_AREA, Offset $0E				
Bit	**Description**	**Read**	**Write**	**Value after Initialization**
6:0	**Serial EEPROM Starting at Lword Boundary (48 Lwords = 192 bytes) for VPD Accesses**. Any serial EEPROM address below this boundary is read-only. **NOTE:** Anything below the programmed address may contain the PLX 9656 Configuration Data.	Yes	Yes	0110000
7	**Reserved**.	Yes	No	0

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Table 3-33 Local Miscellaneous Control 2

Local Miscellaneous Control 2: LMISC2, Offset $0F				
Bit	**Description**	**Read**	**Write**	**Value after Initialization**
0	**READY# Time-out Enable**. Value of one (1) enables READY# Time-out Enable.	Yes	Yes	1
1	**READY# Time-out Select.** Values: 1 = 64 clocks 0 = 32 clocks	Yes	Yes	0
4:2	**Direct Slave Write Delay.** Delay in LCLK of TS#/AD# from a valid address. 0 = 0 LCLK 2 = 8 LCLK 4 = 20 LCLK 6 = 28 LCLK 1 = 4 LCLK 3 = 16 LCLK 5 = 24 LCLK 7 = 32 LCLK	Yes	Yes	000
5	**Direct Slave Write FIFO Full Condition**. Value of one (1) guarantees that when the Direct Slave Write FIFO is full with Direct Slave Write data, there is always one (1) location remaining empty for the Direct Slave Read address to be accepted by the PLX 9656. A value of zero (0) retries all Direct Slave Read accesses when the Direct Slave Write FIFO is full with Direct Slave Write data.	Yes	Yes	1
7:6	**Reserved.**	Yes	Yes	00

Table 3-34 Local Address Space 0/Expansion ROM Bus Region Descriptor

Local Address Space 0/Expansion ROM Bus Region Descriptor: LBRD0, Offset $18				
Bit	**Description**	**Read**	**Write**	**Value after Initialization**
1:0	**Memory Space 0 Local Bus Width**. Writing 00 indicates an 8-bit bus width. Writing 01 indicates a 16-bit bus width. Writing 10 or 11 indicates a 32-bit bus width.	Yes	Yes	M = 11 J = 11 C = 11
5:2	**Memory Space 0 Internal Wait States (data-to-data; 0-15 wait states)**.	Yes	Yes	$0
6	**Memory Space 0 TA#/READY# Input Enable**. Writing a one (1) enables TA#/READY# input. Writing a zero (0) disables TA#/READY# input.	Yes	Yes	1
7	**Memory Space 0 BTERM# Input Enable.** Writing a one (1) enables BTERM# input. Writing a zero (0) disables BTERM# input. For more information, refer to the section for M mode or the section for C and J modes.	Yes	Yes	0
8	**Memory Space 0 Prefetch Disable**. When mapped into Memory Space, writing a zero (0) enables Read Prefetching. Writing a one (1) disables prefetching. If prefetching is disabled, the PLX 9656 disconnects after each memory read.	Yes	Yes	1
9	**Expansion ROM Space Prefetch Disable.** Writing a zero (0) enables Read prefetching. Writing a one (1) disables prefetching. If prefetching is disabled, the PLX 9656 disconnects after each memory read.	Yes	Yes	0
10	**Prefetch Counter Enable**. When set to one (1) and memory prefetching is enabled, the PLX 9656 prefetches up to the number of Lwords specified in prefetch count. When set to a zero (0), the PLX 9656 ignores the count and continues prefetching until it is terminated by the PCI bus.	Yes	Yes	0
14:11	**Prefetch Counter**. Number of Lwords to prefetch during memory read cycles (0-15). A count of zero (0) selects a prefetch of 16 Lwords.	Yes	Yes	0
15	**Reserved**.	Yes	No	0
17:16	**Expansion ROM Space Local Bus Width**. Writing 00 indicates an 8-bit bus width. Writing a 01 indicates a 16-bit bus width. Writing 10 or 11 indicates a 32-bit bus width.	Yes	Yes	M = 11 J = 11 C = 11
21:18	**Expansion ROM Space Internal Wait States (data-to-data; 0-15 wait states)**.	Yes	Yes	$0

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Table 3-34 Local Address Space 0/Expansion ROM Bus Region Descriptor (Continued)

Local Address Space 0/Expansion ROM Bus Region Descriptor: LBRD0, Offset $18				
Bit	**Description**	**Read**	**Write**	**Value after Initialization**
22	**Expansion ROM Space TA#/READY# Input Enable**. Writing a one (1) enables TA#/READY# input. Writing a zero (0) disables TA#/READY# input.	Yes	Yes	0
23	**Expansion ROM Space BTERM# Input Enable.** Writing a one (1) enables BTERM# input. Writing a zero (0) disables BTERM# input. For more information, refer to the M, C or J mode sections of this manual.	Yes	Yes	1
24	**Memory Space 0 Burst Enable**. Writing a one (1) enables bursting. Writing a zero (0) disables bursting.	Yes	Yes	0
25	**Extra Long Load from Serial EEPROM.** Writing a one (1) loads the Subsystem ID and Local Address Space 1 registers. Writing a zero (0) indicates not to load them.	Yes	Serial EEPROM Only	1
26	**Expansion ROM Space Burst Enable**. Writing a one (1) enables bursting. Writing a zero (0) disables bursting.	Yes	Yes	0
27	**Direct Slave PCI Write Mode**. Writing a zero (0) indicates the PLX 9656 should disconnect when the Direct Slave Write FIFO is full. Writing a one (1) indicates the PLX 9656 should de-assert TRDY# when the Direct Slave Write FIFO is full.	Yes	Yes	0
31:28	**Direct Slave Retry Delay Clocks**. Contains the value (multiplied by 8) of the number of PCI bus clocks after receiving a PCI-to-Local Read or Write access and not successfully completing a transfer. Pertains only to Direct Slave writes when the Direct Slave PCI Write Mode bit is set (bit[27] = 1).	Yes	Yes	$4 (32 clocks)

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Table 3-35 Local Address Space 1 Range Register for PCI-to-Local Bus

Local Address Space 1 Range Register for PCI-to-Local Bus: LASIRR, Offset $F0				
Bit	**Description**	**Read**	**Write**	**Value after Initialization**
0	**Memory Space Indicator**. Writing a zero (0) indicates Local Address Space 1 maps into PCI Memory Space. Writing a one (1) indicates Address Space 1 maps into PCI I/O Space.	Yes	Yes	0
2:1	When mapped into Memory Space, encoding is as follows: **2/1** **Meaning** 00 Locate anywhere in 32-bit PCI Address Space. 01 Locate below 1MB in PCI Address Space. 10 Locate anywhere in 64-bit PCI Address Space. 11 Reserved When mapped into I/O Space, Bit 1 must be set to zero (0). Bit 2 is included with bits [31:3] to indicate the decoding range.	Yes	Yes	00
3	When mapped into Memory Space, writing a one (1) indicates reads are prefetchable (does not affect operation of the PLX 9656, but is used for system status). When mapped into I/O space, included with bits [31:2] to indicate the decoding range.	Yes	Yes	0
31:4	Specifies which PCI Address bits to use for decoding a PCI access to Local Bus Space 1. Each bit corresponds to a PCI Address bit. Bit 31 corresponds to address Bit 31. Write a one (1) to all bits that must be included in decode and a zero (0) to all others. (Used in conjunction with PCIBAR3.) Default is 1MB. If QSR[0] = 1, defines PCI Base Address 0. **NOTE:** Range (not the Range register) must be power of 2. "Range register value" is inverse of range. User should limit all I/O spaces to 256 bytes per PCI Specification r2.1	Yes	Yes	$FC0 0000 (64MB) $F80 0000 (128MB)

Table 3-36 Local Address Space 1 Local Base Address (Remap)

Local Address Space 1 Local Base Address (Remap): LAS1BA, Offset $F4				
Bit	**Description**	**Read**	**Write**	**Value after Initialization**
0	**Space 1 Enable**. Writing a one (1) enables decoding of PCI addresses for Direct Slave access to Local Bus Space 1. Writing a zero (0) disables decoding.	Yes	Yes	1
1	**Reserved**	Yes	No	0
3:2	Not used if Local Bus Space 1 is mapped into Memory Space. Included with bits [31:4] for remapping when mapped into I/O Space.	Yes	Yes	00
31:4	**Remap PCI Address to Local Address Space 1 into Local Address Space.** Bits in this register remap (replace) the PCI Address bits used in decode as Local Address bits. **NOTE**: Remap Address value must be a multiple of the Range (**not** the Range register).	Yes	Yes	$0

Table 3-37 Local Address Space 1 Bus Region Descriptor

Local Address Space 1 Bus Region Descriptor: LBRD1, Offset $F8				
Bit	**Description**	**Read**	**Write**	**Value after Initialization**
1:0	**Memory Space 1 Local Bus Width**. Writing a 00 indicates an 8-bit bus width. Writing a 01 indicates a 16-bit bus width. Writing a 10 or 11 indicates a 32-bit bus width.	Yes	Yes	M = 11 J = 11 C = 11

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Table 3-37 Local Address Space 1 Bus Region Descriptor (Continued)

Local Address Space 1 Bus Region Descriptor: LBRD1, Offset $F8				
Bit	**Description**	**Read**	**Write**	**Value after Initialization**
5:2	**Memory Space 1 Internal Wait States (data-to-data; 0-15 wait states)**.	Yes	Yes	$0
6	**Memory Space 1 TA#/READY# Input Enable**. Writing a one (1) enables TA#/READY# input. Writing a zero (0) disables TA#/READY# input.	Yes	Yes	1
7	**Memory Space 1 BTERM# Input Enable**. Writing a one (1) enables BTERM# input. Writing a zero (0) disables BTERM# input. For information, refer to M, C or J modes in this manual.	Yes	Yes	0
8	**Memory Space 1 Burst Disable**. Writing a one (1) enables bursting. Writing a zero (0) disables bursting.	Yes	Yes	1
9	**Memory Space 1 Prefetch Disable**. When mapped into Memory Space, writing a zero (0) enables read prefetching. Writing a one (1) disables prefetching. If prefetching is disabled, the PLX 9656 disconnects after each memory read.	Yes	Yes	1
10	**Prefetch Count Enable**. When set to a one (1) and memory prefetching is enabled, the PLX 9656 prefetches up to the number of Lwords specified in prefetch count. When set to zero (0), the PLX 9656 ignores the count and continues prefetching until it is terminated by the PCI bus.	Yes	Yes	0
14:11	**Prefetch Counter**. Number of Lwords to prefetch during Memory Read cycles (0-15). A count of zero (0) selects a prefetch of 16 Lwords.	Yes	Yes	$0
31:15	**Reserved**.	Yes	Yes	$0

Table 3-38 PCI Abort Address

PCI Abort Address: PABTADR, Offset $104				
Bit	**Description**	**Read**	**Write**	**Value after Initialization**
31:0	**PCI Abort Address**. When a PCI Master/Target abort occurs, the starting address of the current access is returned to this register.	Yes	No	$0000

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Runtime Registers

The Runtime Registers are memory cycle accessible at the offsets from the value stored in the Base Address Register 0. They are also I/O cycle accessible at the offsets from the value stored in the Base Address Register 1. The offsets are specified below. Runtime Registers are not initialized by a serial EEPROM during the system boot process. Instead, these registers remain at the default states that were set by a PCI bus reset. Therefore, the user must modify the states of several bits within these registers to activate the desired operating modes.

Table 3-39 Runtime Registers

PCI (Offset from Base Address)	To ensure software compatibility with other versions of the PLX 9656 family and to ensure compatibility with future enhancements, write zero (0) to all unused bits. 31 16 15 0		PCI/Local Writable	Serial EEPROM Writable
$40	Mailbox Register 0		Y	Y
$44	Mailbox Register 1		Y	Y
$48	Mailbox Register 2		Y	N
$4C	Mailbox Register 3		Y	N
$50	Mailbox Register 4		Y	N
$54	Mailbox Register 5		Y	N
$58	Mailbox Register 6		Y	N
$5C	Mailbox Register 7		Y	N
$60	PCI-to-Local Doorbell Register		Y	N
$64	Local-to-PCI Doorbell Register		Y	N
$68	Interrupt Control and Status		Y	N
$6C	Serial EEPROM Control, PCI Command Codes, User I/O Control and INIT Control		Y	N
$70	Device ID	Vendor ID	N	N
$74	Unused	Revision ID	N	N
$78	Mailbox Register		Y	N
$7C	Mailbox Register		Y	N

NOTE: The Runtime Registers listed in Table 3-39 that pertain to the Mailbox or Doorbell Control registers are **NOT** applicable to the VMIPCI-5565.

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Interrupt Control and Status Register

Within the INTCSR register, the following bit functions have no direct application and should remain at their default state:

Bits 1, 3, 4, 5, 9, 11, 13, 14, 16, 17, 20, 23, 24, 25, 26, 27, 28, 29, 30 and 31.

Within the INTCSR register, the following bits may have limited use depending on the host system requirements:

Bits 2, 10, 12, 25 and 26.

Table 3-40 Interrupt Control and Status Register

Interrupt Control and Status: INTCSR, Offset $68				
Bit	**Description**	**Read**	**Write**	**Value after PCI Reset**
0	**Enable Local Bus TEA#/LSERR#**. Writing a one (1) enables the PLX 9656 to assert TEA#/LSERR# interrupt when the Received Master Abort is set (PCISR[13] = 1 or INTCSR[6] = 1).	Yes	Yes	0
1	Enable Local bus TEA#/LSERR# when a PCI parity error occurs during a PLX 9656 Master Transfer or a PLX 9656 Slave access.	Yes	Yes	0
2	**Generate PCI bus SERR# Interrupt**. When set to zero (0), writing a one (1) asserts the PCI bus SERR# interrupt.	Yes	Yes	0
3	**Mailbox Interrupt Enable.** Writing a one (1) enables a Local interrupt to be asserted when the PCI bus writes to MBOX0 through MBOX3. To clear a Local interrupt, the Local bus Master must read the Mailbox. Used in conjunction with the Local interrupt Output Enable bit (INTCSR[16]).	Yes	Yes	0
4	**Power Management Interrupt Enable**. Writing a one (1) enables the Local interrupt to be asserted when the Power Management Power State changes.	Yes	Yes	0
5	**Power Management Interrupt.** When set to a one (1), indicates a Power Management interrupt is pending. A Power Management interrupt is caused by a change in the Power State register (PMCSR). Writing a one (1) clears the interrupt.	Yes	Yes	0
6	**Direct Master Write/Direct Slave Read Local Data Parity Check Error Enable**. Writing a one (1) enables a Local Data Parity error signal to be asserted through the LSERR#/TEA# pin. INTCSR[0] must be enabled for this to have an effect.	Yes	Yes	0
7	**Direct Master Write/Direct Slave Read Local Data Parity Check Error Status**. When set to a one (1), indicates the PLX 9656 has detected a Local Data Parity check error, even if the Check Parity Error bit is disabled. Writing a one (1) clears this bit to zero (0).	Yes	Yes	0
8	**PCI Interrupt Enable**. Writing a one (1) enables PCI interrupts.	Yes	Yes	1
9	**PCI Doorbell Interrupt Enable**. Writing a one (1) enables Doorbell Interrupts. Used in conjunction with the PCI Interrupt Enable bit (INTCSR[8]). Clearing the doorbell interrupt bit that caused the interrupt also clears the interrupt.	Yes	Yes	0
10	**PCI Abort Interrupt Enable**. Values of one (1) enables Master abort or Master detect of a Target abort to assert a PCI interrupt. Used in conjunction with the PCI Interrupt Enable bit (INTCSR[8]). Clearing the abort status bits also clears the PCI interrupt.	Yes	Yes	0
11	**Local Interrupt Input Enable**. Writing a one (1) enables a Local interrupt input to assert a PCI interrupt. Used in conjunction with the PCI Interrupt Enable bit (INTCSR[8]). Clearing the Local bus cause of the interrupt also clears the interrupt.	Yes	Yes	0
12	**Retry Abort Enable.** Writing a one (1) enables the PLX 9656 to treat 256 Master consecutive Retrys to a Target as a Target abort. Writing a zero (0) enables the PLX 9656 to attempt Master Retrys indefinitely.	Yes	Yes	0

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Table 3-40 Interrupt Control and Status Register (Continued)

Interrupt Control and Status: INTCSR, Offset $68				
Bit	**Description**	**Read**	**Write**	**Value after PCI Reset**
13	**PCI Doorbell Interrupt Active**. When set to one (1), indicates the PCI Doorbell interrupt is active.	Yes	Yes	0
14	**PCI Abort Interrupt Active**. When set to one (1), indicates the PCI Abort interrupt is active.	Yes	Yes	0
15	**Local Input Interrupt Active**. When set to a one (1), indicates the Local input interrupt is active.	Yes	Yes	0
16	**Local Interrupt Output Enable**. Writing a one (1) enables Local interrupt output. Used in conjunction with the Mailbox Interrupt Enable bit (INTCSR[3]).	Yes	Yes	1
17	**Local Doorbell Interrupt Enable.** Writing a one (1) enables Doorbell interrupts. Used in conjunction with the Local Interrupt Enable bit. Clearing the Local Doorbell Interrupt bits that caused the interrupt also clears the interrupt.	Yes	Yes	0
18	**Local DMA Channel 0 Interrupt Enable**. Writing a one (1) enables DMA Channel 0 interrupts. Used in conjunction with the Local Interrupt Enable bit. Clearing the DMA status bits also clears the interrupt.	Yes	Yes	0
19	**Local DMA Channel 1 Interrupt Enable.** Writing a one (1) enables DMA Channel 1 interrupts. Used in conjunction with the Local Interrupt Enable bit. Clearing the DMA status bits also clears the interrupt.	Yes	Yes	0
20	**Local Doorbell Interrupt Active.** Reading a one (1) indicates the Local Doorbell interrupt is active.	Yes	No	0
21	**DMA Channel 0 Interrupt Active.** Reading a one (1) indicates the DMA Channel 0 interrupt is active.	Yes	No	0
22	**DMA Channel 1 Interrupt Active**. Reading a one (1) indicates the DMA Channel 1 interrupt is active.	Yes	No	0
23	**BIST Interrupt Active**. Reading a one (1) indicates the BIST interrupt is active. The BIST (built-in self test) interrupt is asserted by writing a one (1) to Bit 6 of the PCI Configuration BIST register. Clearing Bit 6 clears the interrupt. Refer to the PCIBISTR register for a description of the self test.	Yes	No	0
24	Reading a zero (0) indicates the Direct Master was the Bus Master during a Master or Target abort.	Yes	No	1
25	Reading a zero (0) indicates DMA CH0 was the Bus Master during a Master or Target abort.	Yes	No	1
26	Reading a zero (0) indicates DMA CH1 was the Bus Master during a Master or Target abort.	Yes	No	1
27	Reading a zero (0) indicates a Target abort was asserted by the PLX 9656 after 256 consecutive Master retries to a Target.	Yes	No	1
28	Reading a one (1) indicates the PCI bus wrote data to MBOX0. Enabled only if the Mailbox Interrupt Enable bit is set (INTCSR[3]=1).	Yes	No	0
29	Reading a one (1) indicates the PCI bus wrote data to MBOX1. Enabled only if the Mailbox Interrupt Enable bit is set (INTCSR[3]=1).	Yes	No	0
30	Reading a one (1) indicates the PCI bus wrote data to MBOX2. Enabled only if the Mailbox Interrupt Enable bit is set (INTCSR[3]=1).	Yes	No	0
31	Reading a one (1) indicates the PCI bus wrote data to MBOX3. Enabled only if the Mailbox Interrupt Enable bit is set (INTCSR[3]=1).	Yes	No	0

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The PCI Interrupt Enable (Bit 8) functions as a global PCI interrupt enable. It must be set high (1) in addition to other enable bits before any first or second tier interrupt source will result in a PCI interrupt.

INTCSR Bits 0, 6 and 7 are involved with the memory parity checking circuit. Unfortunately, the PLX 9656 does not provide a direct, first tier, way of asserting a PCI interrupt from a parity error. Instead, setting both Bit 0 and Bit 6 high only enables a parity error to assert an external pin called LSERR#. The LSERR# signal is routed to the second tier interrupt control register called the LISR. The LISR is an RFM Control and Status register. Through the LISR, a parity fault must assert yet another external signal called LINTi#, which passes back through the INTCSR at Bit 15 and finally to the PCI interrupt. See the VMIPCI-5565 Interrupt Circuit Block diagram Figure 1 on page 15 for a visual representation of the parity error interrupt path. Table 3-41 summarizes the INTCSR Interrupt Enables that pertain to VMIPCI-5565 operation.

Table 3-41 INTCSR Interrupt Enables

Enable the interrupt source:	Set the following Bit high (1):
Global PCI interrupt enable for all sources	8
Any second tier int. through Local Int. Input (LINTi#)	11
Local DMA Channel 0 interrupt	18
Local DMA Channel 1 interrupt	19

Table 3-42 summarizes the INTCSR Interrupt Status bits that pertain to VMIPCI-5565 operation.

Table 3-42 INTCSR Interrupt Status

To check the assertion of the following interrupt source:	Check for a high (1) at Bit:
Memory Parity Error	7
Any second tier int. through Local Int. Input (LINTi#)	15
Local DMA Channel 0 interrupt	21
Local DMA Channel 1 interrupt	22

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Serial EEPROM Control, PCI Command Codes, User I/O Control and INIT Control Register

Table 3-43 Serial EEPROM Control, PCI Command Codes, User I/O Control and INIT Control Register

Serial EEPROM Control, PCI Command Codes, User I/O Control and INIT Control: CNTRL, Offset $6C				
Bits	**Description**	**Read**	**Write**	**Value after PCI Reset**
3:0	**PCI Read Command Code for DMA**.	Yes	Yes	1110
7:4	**PCI Write Command Code for DMA**.	Yes	Yes	0111
11:8	**PCI Memory Read Command Code for Direct Master**.	Yes	Yes	0110
15:12	**PCI Memory Write Command Code for Direct Master.**	Yes	Yes	0111
16	**General Purpose Output**. Writing a one (1) causes USERo output to go high. Writing a zero (0) causes USERo output to go low.	Yes	Yes	1
17	**General Purpose Input**. Reading a one (1) indicates USERi input pin is high. Reading a zero (0) indicates USERi input pin is low.	Yes	Yes	---
18	Writing a one (1) selects USERi to be an input to the chip. Writing a zero (0) selects LLOCKi# as an input. Enables the user to select between the USERi and LLOCKi# functions when USERi is chosen to be an input. The select bit(s) for the pin is DMAMODE0[12] and/or DMAMODE1[12].	Yes	Yes	1
19	Writing a one (1) selects USERo to be an output from the chip. Writing a zero (0) selects LLOCKi# as an input. Enable the user to select between the USERo and LLOCKo# functions when USERo is chosen to be an output. The select bit(s) for the pin is DMAMODE0[12] and/or DMAMODE1[12].	Yes	Yes	1
20	**LINTo# Interrupt Status**. When HOSTEN# is enabled, reading a one (1) indicates the LINTo# interrupt is active by way of the INTA# PCI interrupt. Writing a one (1) clears this bit.	Yes	Yes/Clr	0
21	**TEA#/SERR# Interrupt Status**. When HOSTEN# is enabled, reading a one (1) indicates the TES#/SERR# interrupt is active by way of the SERR# PCI System Error. Writing a one (1) clears this bit.	Yes	Yes/Clr	0
23:22	**Reserved**.	Yes	No	00
24	**Serial EEPROM Clock for Local or PCI Bus Reads or Writes to Serial EEPROM**. Toggling this bit asserts the serial EEPROM clock. (Refer to manufacturer's data sheet for particular serial EEPROM being used.)	Yes	Yes	0
25	**Serial EEPROM Chip Select.** For Local or PCI bus reads or writes to the serial EEPROM, setting this bit to one (1) provides the serial EEPROM Chip Select.	Yes	Yes	0
26	**Write Bit to Serial EEPROM**. For writes, this output bit is input to the serial EEPROM. Clocked into the serial EEPROM by the serial EEPROM clock.	Yes	Yes	0
27	**Read Bit from Serial EEPROM**. (Refer to the sections pertaining to M, C and J modes of the manual.)	Yes	No	---
28	**Programmed Serial EEPROM Present.** When set to a one (1), indicates that a blank or programmed serial EEPROM is present.	Yes	No	0
29	**Reload Configuration Registers**. When set to zero (0), writing a one (1) causes the PLX 9656 to reload the Local Configuration registers from the serial EEPROM.	Yes	Yes	0
30	**PCI Adapter Software Reset when HOSTEN#=1**. Writing a one (1) holds the PLX 9656 Local bus logic in a reset state, and asserts LRESET# output. Contents of the PCI Configuration registers and the shared Runtime registers are not set. A software reset can only be cleared from the PCI bus.	Yes	Yes	0
31	**EEDO Input Enable**. When set to a one (1) the EEDI/EEDO I/O buffer is placed in bus high-impedance state, enabling the serial EEPROM data to be read. The serial EEPROM data resides in CNTRL[27].	Yes	No	0

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The CNTRL register has limited uses during normal operation of the VMIPCI-5565. Most bits within the CNTRL register will remain at their PCI reset default value. One exception is Bit 28 (Programmed Serial EEPROM Present), which should change from the default value of 0 to a 1 once the serial EEPROM initialization is complete.

Bit 30 of the CNTRL register functions as a partial software reset. When bit 30 is set high (1) by a PCI write, the Runtime registers and the DMA registers within the PLX device are not affected. However, the PLX Local Configuration registers and all portions of VMIPCI-5565 beyond the PLX device are held in reset until Bit 30 is set low (0). This includes all RFM Control and Status Registers and their associated circuitry, the transmit FIFO and transmitter circuitry, the receiver FIFO and receiver circuitry. While held in a software reset, PCI bus access to the RFM Control and Status registers and access to the Reflective Memory is inhibited. Also, since the refresh of the Reflective Memory is inhibited, all data previously stored in the Reflective Memory may be corrupted. Finally, while being held in reset, network data passed to the reset node and all down stream nodes will be lost. Down stream nodes are those tied to the transmitter of the node in reset. Once Bit 30 of the CNTRL register is set low (0), the user must set Bit 29 of the CNTRL register high (1), then to a low (0) to re-initialize the PLX Local Configuration registers.

In addition, the CNTRL register contains several bits that can be used to modify the serial EEPROM, which contains the initialization data that is loaded into various PCI Configuration and Local Configuration registers at power up. Also the serial EEPROM is a 2k bit device and only the first 1536 bits are currently being used for configuration. The remaining bits may be used for user specific configuration data such as electronic serial numbers or date codes. However, altering the serial EEPROM through the CNTRL register is rather complex and would suggest the use of a special software utility.

CAUTION: Altering the configuration data could render the board nonfunctional. Only experienced users should attempt to alter the serial EEPROM.

PCI Hardcoded Configuration ID Register

Table 3-44 PCI Hardcoded Configuration ID Register

PCI Hardcoded Configuration ID: PCIHIDR, Offset $70				
Bits	**Description**	**Read**	**Write**	**Value after PCI Reset**
15:0	**Vendor ID**. Identifies manufacturer of device. Hardcoded to the PCI SIG-issued Vendor ID of PLX ($10B5).	Yes	No	$10B5
31:16	**Device ID**. Identifies a particular device. Hardcoded to the PLX part number for interface chip $9656.	Yes	No	$9656

PCI Hardcoded Revision ID

Table 3-45 PCI Hardcoded Revision ID

PCI Hardcoded Revision ID: PCIHREV, Offset $74				
Bits	**Description**	**Read**	**Write**	**Value after PCI Reset**
7:0	**Revision ID**. Hardcoded silicon revision of the PLX 9656.	Yes	No	Current Rev#

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DMA Control Registers

The DMA Control Registers are memory cycle accessible at the offsets from the value stored in the Base Address Register 0. They are also I/O cycle accessible at the offsets from the value stored in the Base Address Register 1. The offsets are specified below. DMA Control Registers are not initialized by a serial EEPROM during the system boot process. Instead, these registers remain at their default states that were set by a PCI reset. Therefore, the user must modify the states of several bits within these registers to activate the desired operating modes.

Table 3-46 DMA Registers

PCI (Offset from Base Address)	To ensure software compatibility with other versions of the PLX 9656 family and to ensure compatibility with future enhancements, write zero (0) to all unused bits. 31 16 15 8 7 0			PCI/Local Writable	Serial EEPROM Writable
$80	DMA Channel 0 Mode			Y	N
$84	DMA Channel 0 PCI Address			Y	N
$88	DMA Channel 0 Local Address			Y	N
$8C	DMA Channel 0 Transfer Byte Count			Y	N
$90	DMA Channel 0 Descriptor Pointer			Y	N
$94	DMA Channel 1 Mode			Y	N
$98	DMA Channel 1 PCI Address			Y	N
$9C	DMA Channel 1 Local Address			Y	N
$A0	DMA Channel 1 Transfer Byte Count			Y	N
$A4	DMA Channel 1 Descriptor Pointer			Y	N
$A8	**Reserved**	DMA Channel 1 Command/Status	DMA Channel 0 Command/Status	Y	N
$AC	Mode/DMA Arbitration			Y	N
$B0	DMA Threshold			Y	N
$B4	DMA Channel 0 PCI Dual Address Cycle (Upper 32 bits)			Y	N
$B8	DMA Channel 1 PCI Dual Address Cycle (Upper 32 bits)			Y	N

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DMA Channel 0 Mode Register

For normal operation of DMA channel 0 the following bits should remain at their default values: 0 through 6, 12, 14, 15, 19 and 22 through 31. To enable the faster memory burst mode, Bits 7 and 8 of this register should be changed from the default value of zero (0) to a one (1). The remaining bits of the DMA Channel 0 Mode register depend on the desired mode of DMA the user requires.

Table 3-47 DMA Channel 0 Mode Register

DMA Channel 0 Mode: DMAMODE0, Offset $80				
Bits	**Description**	**Read**	**Write**	**Value after PCI Reset**
1:0	**Local Bus Width**. Writing 00 indicates an 8-bit bus width. Writing 01 indicates a 16-bit bus width. Writing a 10 or 11 indicates a 32-bit bus width.	Yes	Yes	M = 11 J = 11 C = 11
5:2	**Internal Wait States (date-to-date)**.	Yes	Yes	$0
6	**TA#/READY# Input Enable**. Writing a one (1) enables TA#/READY# input. Writing a zero (0) disables TA#/READY# input.	Yes	Yes	1
7	**BTERM# Input Enable.** Writing a one (1) enables BTERM# input. Writing a zero (0) disables BTERM# input. Refer to M, C and J modes for more information.	Yes	Yes	0
8	**Local Burst Enable**. Writing a one (1) indicates Local Bursting. Writing a zero (0) disables Local Bursting.	Yes	Yes	0
9	**Scatter/Gather Mode**. Writing a one (1) indicates Scatter/Gather mode is enabled. For Scatter/Gather mode, DMA source address, destination address and byte count are loaded from memory in PCI or Local Address spaces. Writing a zero (0) indicates block mode is enabled.	Yes	Yes	0
10	**Done Interrupt Enable**. Writing a one (1) enables an interrupt when done. Writing a zero (0) disables an interrupt when done. If DMA Clear Count mode is enabled, the interrupt does not occur until the byte count is cleared.	Yes	Yes	0
11	**Local Addressing Mode**. Writing a one (1) holds the Local Address bus constant. Writing a zero (0) indicates the Local Address is incremented.	Yes	Yes	0
12	**Demand Mode**. Writing a one (1) causes the DMA controller to operate in Demand mode. In Demand mode, the DMA controller transfers data when its DREQ0# input is asserted. Asserts DACK0# to indicate the current Local bus transfer is in response to DREQ0# input. DMA controller transfers Lwords (32 bits) of data. This may result in multiple transfers for an 8- or 16-bit bus.	Yes	Yes	0
13	**Memory Write and Invalidate Mode for DMA Transfers**. When set to one (1), the PLX 9656 performs Memory Write and Invalidate cycles to the PCI bus. The PLX 9656 supports Memory Write and Invalidate sizes of 8 or 16 Lwords. Size is specified in the System Cache Line Size bits (PCICLSR[7:0]). If a size other than 8 or 16 is specified, the PLX 9656 performs Write transfers rather than Memory Write and Invalidate transfers. Transfers must start and end at cache line boundaries.	Yes	Yes	0
14	**DMA EOT# Enable**. Writing a one (1) enables the EOT# input pin. Writing a zero (0) disables the EOT# input pin.	Yes	Yes	0
15	**Fast/Slow Terminate Mode Select**. Writing a zero (0) sets PLX 9656 into the Slow Terminate mode. As a result in C or J modes, BLAST# is asserted on the last Data Transfer to terminate DMA transfer. As a result in M mode, BDIP# is de-asserted at the nearest 16-byte boundary and stops the DMA transfer. Writing a one (1) indicates that if EOT# is asserted or DREQ0# is de-asserted in Demand mode during DMA will immediately terminate the DMA transfer. In M mode, writing a one (1) indicates BDIP# output is disabled. As a result, the PLX 9656 DMA transfer terminates immediately when EOT# is asserted or when DREQ# is de-asserted in Demand mode.	Yes	Yes	0
16	**DMA Clear Count Mode.** Writing a one (1) clears the byte count in each Scatter/Gather descriptor when the corresponding DMA transfer is complete.	Yes	Yes	0

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Table 3-47 DMA Channel 0 Mode Register (Continued)

DMA Channel 0 Mode: DMAMODE0, Offset $80				
Bits	**Description**	**Read**	**Write**	**Value after PCI Reset**
17	**DMA Channel 0 Interrupt Select**. Writing a one (1) routes the DMA Channel 0 interrupt to the PCI bus interrupt. Writing a zero (0) routes the DMA Channel 0 interrupt to the Local bus interrupt.	Yes	Yes	0
18	**DAC Chain Load**. When set to a one (1), enables the descriptor to load the PCI Dual Address Cycle value. Otherwise, it uses the contents of the register.	Yes	Yes	0
19	**EOT# End Link.** Used only for Scatter/Gather DMA transfers. When EOT# is asserted, value of one (1) indicates the DMA transfer ends the current Scatter/Gather link and continues with the remaining Scatter/Gather transfers. When EOT# is asserted, value of zero (0) indicates the DMA transfer ends the current Scatter/Gather transfer and does not continue with the remaining Scatter/Gather transfers.	Yes	Yes	0
20	**Valid Mode Enable**. Value of zero (0) indicates the Valid bit (DMASIZ0[31]) is ignored. Value of one (1) indicates the DMA descriptors are processed only when the Valid bit is set (DMASIZ0[31]). If the Valid bit is set, the transfer count is zero (0), and the descriptor is not the last descriptor in the chain. The DMA controller then moves to the next descriptor in the chain.	Yes	Yes	0
21	**Valid Stop Control**. Value of zero (0) indicates the DMA Chaining controller continuously polls a descriptor with the Valid bit set to zero (0) (invalid descriptor) if the Valid Mode Enable bit is set (bit[20] = 1). Value of one (1) indicates the Chaining controller stops polling when the Valid bit with a value of zero (0) is detected (DMASIZ0[31]=0). In this case, the CPU must restart the DMA controller by setting the Start bit (DMACSR0[1]=1). A pause sets the DMA Done register.	Yes	Yes	0
31:22	**Reserved**.	Yes	No	$0

DMA Channel 0 PCI Address Register

Table 3-48 DMA Channel 0 PCI Address Register

DMA Channel 0 PCI Address: when DMAMODE0[20]=0; Offset $84, when DMAMODE0[20]=1; Offset $88				
Bits	**Description**	**Read**	**Write**	**Value after PCI Reset**
31:0	**PCI Address Register**. Indicates from where in PCI Memory space DMA transfers (read or write) start.	Yes	Yes	$0

DMA Channel 0 Local Address Register

Table 3-49 DMA Channel 0 Local Address Register

DMA Channel 0 Local Address: when DMAMODE0[20]=0; Offset $88, when DMAMODE0[20]=1; Offset $8C				
Bits	**Description**	**Read**	**Write**	**Value after PCI Reset**
31:0	**PCI Address Register**. Indicates from where in Local Memory space DMA transfers (read or write) start.	Yes	Yes	$0

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DMA Channel 0 Transfer Size (Bytes) Register

Table 3-50 DMA Channel 0 Transfer Size (Bytes) Register Bit Map

DMA Channel 0 Transfer Size (Bytes): when DMAMODE0[20]=0; Offset $8C, when DMAMODE0[20]=1; Offset $84				
Bit	**Description**	**Read**	**Write**	**Value after PCI Reset**
22:0	**DMA Transfer Size (Bytes)**. Indicates the number of bytes to transfer during a DMA operation.	Yes	Yes	$0
30:23	**Reserved**	Yes	No	$0
31	**Valid.** When the Valid Mode Enable bit is set (DMAMODE0[20]=1), indicates the validity of this DMA descriptor.	Yes	Yes	$0

DMA Channel 0 Descriptor Pointer Register

Table 3-51 DMA Channel 0 Descriptor Pointer Register Bit Map

DMA Channel 0 Descriptor Pointer: DMADPR0, Offset $90				
Bit	**Description**	**Read**	**Write**	**Value after PCI Reset**
0	**Descriptor Location**. Writing a one (1) indicates PCI Address space. Writing a zero (0) indicates Local Address space.	Yes	Yes	0
1	**End of Chain.** Writing a one (1) indicates end of chain. Writing a zero (0) indicates not end of chain descriptor. (Same as Block mode.)	Yes	Yes	0
2	**Interrupt after Terminal Count**. Writing a one (1) causes an interrupt to be asserted after the terminal count before this descriptor is reached. Writing a zero disables interrupts from being asserted.	Yes	Yes	0
3	**Direction of Transfer**. Writing a one (1) indicates transfers from the Local bus to the PCI bus. Writing a zero (0) indicates transfer from the PCI bus to the Local bus.	Yes	Yes	0
31:4	**Next Descriptor Address.** Qword-aligned (bits[3:0]=0000).	Yes	Yes	$0

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DMA Channel 1 Mode Register

For the normal operation of DMA Channel 1 Mode register, the following bits should remain at their default values: 0 through 6, 12, 14, 15, 19 and 22 through 31. To enable the faster memory burst mode, Bits 7 and 8 of this register should be changed from the default value of zero (0) to a one (1). The remaining bits of the DMA Channel 1 Mode register depend on the desired mode of DMA the user requires.

Table 3-52 DMA Channel 1 Mode Register

DMA Channel 1 Mode: DMAMODE1, Offset $94				
Bits	**Description**	**Read**	**Write**	**Value after PCI Reset**
1:0	**Local Bus Width**. Writing 00 indicates an 8-bit bus width. Writing 01 indicates a 16-bit bus width. Writing a 10 or 11 indicates a 32-bit bus width.	Yes	Yes	M = 11 J = 11 C = 11
5:2	**Internal Wait States (date-to-date)**.	Yes	Yes	$0
6	**TA#/READY# Input Enable**. Writing a one (1) enables TA#/READY# input. Writing a zero (0) disables TA#/READY# input.	Yes	Yes	1
7	**BTERM# Input Enable.** Writing a one (1) enables BTERM# input. Writing a zero (0) disables BTERM# input. Refer to M, C and J modes for more information.	Yes	Yes	0
8	**Local Burst Enable**. Writing a one (1) indicates Local Bursting. Writing a zero (0) disables Local Bursting.	Yes	Yes	0
9	**Scatter/Gather Mode**. Writing a one (1) indicates Scatter/Gather mode is enabled. For Scatter/Gather mode, DMA source address, destination address and byte count are loaded from memory in PCI or Local Address spaces. Writing a zero (0) indicates block mode is enabled.	Yes	Yes	0
10	**Done Interrupt Enable**. Writing a one (1) enables an interrupt when done. Writing a zero (0) disables an interrupt when done. If DMA Clear Count mode is enabled, the interrupt does not occur until the byte count is cleared.	Yes	Yes	0
11	**Local Addressing Mode**. Writing a one (1) holds the Local Address bus constant. Writing a zero (0) indicates the Local Address is incremented.	Yes	Yes	0
12	**Demand Mode**. Writing a one (1) causes the DMA controller to operate in Demand mode. In Demand mode, the DMA controller transfers data when its DREQ0# input is asserted. Asserts DACK0# to indicate the current Local bus transfer is in response to DREQ0# input. DMA controller transfers Lwords (32 bits) of data. This may result in multiple transfers for an 8- or 16-bit bus.	Yes	Yes	0
13	**Memory Write and Invalidate Mode for DMA Transfers**. When set to one (1), the PLX 9656 performs Memory Write and Invalidate cycles to the PCI bus. The PLX 9656 supports Memory Write and Invalidate sizes of 8 or 16 Lwords. Size is specified in the System Cache Line Size bits (PCICLSR[7:0]). If a size other than 8 or 16 is specified, the PLX 9656 performs Write transfers rather than Memory Write and Invalidate transfers. Transfers must start and end at cache line boundaries.	Yes	Yes	0
14	**DMA EOT# Enable**. Writing a one (1) enables the EOT# input pin. Writing a zero (0) disables the EOT# input pin.	Yes	Yes	0
15	**Fast/Slow Terminate Mode Select**. Writing a zero (0) sets PLX 9656 into the Slow Terminate mode. As a result in C or J modes, BLAST# is asserted on the last Data Transfer to terminate DMA transfer. As a result in M mode, BDIP# is de-asserted at the nearest 16-byte boundary and stops the DMA transfer. Writing a one (1) indicates that if EOT# is asserted or DREQ0# is de-asserted in Demand mode during a DMA will immediately terminate the DMA transfer. In M mode, writing a one (1) indicates BDIP# output is disabled. As a result, the PLX 9656 DMA transfer terminates immediately when EOT# is asserted or when DREQ# is de-asserted in Demand mode.	Yes	Yes	0

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Table 3-52 DMA Channel 1 Mode Register (Continued)

DMA Channel 1 Mode: DMAMODE1, Offset $94				
Bits	**Description**	**Read**	**Write**	**Value after PCI Reset**
16	**DMA Clear Count Mode.** Writing a one (1) clears the byte count in each Scatter/Gather descriptor when the corresponding DMA transfer is complete.	Yes	Yes	0
17	**DMA Channel 1 Interrupt Select**. Writing a one (1) routes the DMA Channel 1 interrupt to the PCI bus interrupt. Writing a zero (0) routes the DMA Channel 1 interrupt to the Local bus interrupt.	Yes	Yes	0
18	**DAC Chain Load**. When set to a one (1), enables the descriptor to load the PCI Dual Address Cycle value. Otherwise, it uses the contents of the register.	Yes	Yes	0
19	**EOT# End Link.** Used only for Scatter/Gather DMA transfers. When EOT# is asserted, value of one (1) indicates the DMA transfer ends the current Scatter/Gather link and continues with the remaining Scatter/Gather transfers. When EOT# is asserted, value of zero (0) indicates the DMA transfer ends the current Scatter/Gather transfer and does not continue with the remaining Scatter/Gather transfers.	Yes	Yes	0
20	**Valid Mode Enable**. Value of zero (0) indicates the Valid bit (DMASIZ0[31]) is ignored. Value of one (1) indicates the DMA descriptors are processed only when the Valid bit is set (DMASIZ0[31]). If the Valid bit is set, the transfer count is zero (0), and the descriptor is not the last descriptor in the chain. The DMA controller then moves to the next descriptor in the chain.	Yes	Yes	0
21	**Valid Stop Control**. Value of zero (0) indicates the DMA Chaining controller continuously polls a descriptor with the Valid bit set to zero (0) (invalid descriptor) if the Valid Mode Enable bit is set (bit[20] = 1). Value of one (1) indicates the Chaining controller stops polling when the Valid bit with a value of zero (0) is detected (DMASIZ0[31]=0). In this case, the CPU must restart the DMA controller by setting the Start bit (DMACSR0[1]=1). A pause sets the DMA Done register.	Yes	Yes	0
31:22	**Reserved**.	Yes	No	$0

DMA Channel 1 PCI Address Register

Table 3-53 DMA Channel 1 PCI Address Register

DMA Channel 1 PCI Address: when DMAMODE1[20]=0; Offset $98, when DMAMODE1[20]=1; Offset $9C				
Bits	**Description**	**Read**	**Write**	**Value after PCI Reset**
31:0	**PCI Address Register**. Indicates from where in PCI Memory space DMA transfers (read or write) start.	Yes	Yes	$0

DMA Channel 1 Local Address Register

Table 3-54 DMA Channel 1 Local Address Register

DMA Channel 1 Local Address: when DMAMODE1[20]=0; Offset $9C, when DMAMODE1[20]=1; Offset $A0				
Bits	**Description**	**Read**	**Write**	**Value after PCI Reset**
31:0	**PCI Address Register**. Indicates from where in Local Memory space DMA transfers (read or write) start.	Yes	Yes	$0

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DMA Channel 1 Descriptor Pointer Register

Table 3-55 DMA Channel 1 Descriptor Pointer Register Bit Map

DMA Channel 1 Descriptor Pointer: DMADPR1, Offset $A4				
Bit	**Description**	**Read**	**Write**	**Value after PCI Reset**
0	**Descriptor Location**. Writing a one (1) indicates PCI Address space. Writing a zero (0) indicates Local Address space.	Yes	Yes	0
1	**End of Chain.** Writing a one (1) indicates end of chain. Writing a zero (0) indicates not end of chain descriptor. (Same as Block mode.)	Yes	Yes	0
2	**Interrupt after Terminal Count**. Writing a one (1) causes an interrupt to be asserted after the terminal count before this descriptor is reached. Writing a zero disables interrupts from being asserted.	Yes	Yes	0
3	**Direction of Transfer**. Writing a one (1) indicates transfers from the Local bus to the PCI bus. Writing a zero (0) indicates transfer from the PCI bus to the Local bus.	Yes	Yes	0
31:4	**Next Descriptor Address.** Qword-aligned (bits[3:0]=0000).	Yes	Yes	$0

DMA Channel 0 Command/Status Register

Table 3-56 DMA Channel 0 Command/Status Register Bit Map

DMA Channel 0 Command/Status: DMACSR0, Offset $A8				
Bit	**Description**	**Read**	**Write**	**Value after PCI Reset**
0	**Channel 0 Enable**. Writing a one (1) enables channel to transfer data. Writing a zero (0) disables the channel from starting a DMA transfer, and if in the process of transferring data, suspends the transfer (pause).	Yes	Yes	0
1	**Channel 0 Start.** Writing a one (1) causes channel to start transferring data if the channel is enabled.	No	Yes/Set	0
2	**Channel 0 Abort**. Writing a one (1) causes channel to abort current transfer. Channel 0 Enable bit must be cleared (bit[0]=0). Sets Channel 0 Done (bit[4]=1) when abort is complete.	No	Yes/Set	0
3	**Channel 0 Clear Interrupt**. Writing a one (1) clears Channel 0 interrupts.	No	Yes/Clr	0
4	**Channel 0 Done**. Reading a one (1) indicates a channel transfer is complete. Reading a zero (0) indicates a channel transfer is not complete.	Yes	No	1
7:5	**Reserved.**	Yes	No	000

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DMA Channel 1 Command/Status Register

Table 3-57 DMA Channel 1 Command/Status Register Bit Map

DMA Channel 1 Command/Status: DMACSR1, Offset $A8				
Bit	**Description**	**Read**	**Write**	**Value after PCI Reset**
0	**Channel 1 Enable**. Writing a one (1) enables channel to transfer data. Writing a zero (0) disables the channel from starting a DMA transfer, and if in the process of transferring data, suspends the transfer (pause).	Yes	Yes	0
1	**Channel 1 Start.** Writing a one (1) causes channel to start transferring data if the channel is enabled.	No	Yes/Set	0
2	**Channel 1 Abort**. Writing a one (1) causes channel to abort current transfer. Channel 1 Enable bit must be cleared (bit[0]=0). Sets Channel 1 Done (bit[4]=1) when abort is complete.	No	Yes/Set	0
3	**Channel 1 Clear Interrupt**. Writing a one (1) clears Channel 1 interrupts.	No	Yes/Clr	0
4	**Channel 1 Done**. Reading a one (1) indicates a channel transfer is complete. Reading a zero (0) indicates a channel transfer is not complete.	Yes	No	1
7:5	**Reserved.**	Yes	No	000

DMA Arbitration Register

Table 3-58 Mode/DMA Arbitration Register Bit Map

Mode/DMA Arbitration: MARBR, Offset $AC or $12C				
Bit	**Description**	**Read**	**Write**	**Value after Initialization**
7:0	**Local Bus Latency Timer**. Number of Local Bus clock cycles to occur before de-asserting HOLD and releasing the Local Bus.	Yes	Yes	$0
15:8	**Local Bus Pause Timer**. Number of Local Bus clock cycles to occur before reasserting HOLD after releasing the Local Bus. The pause timer is valid only during DMA.	Yes	Yes	$0
16	**Local Bus Latency Timer Enable**. Writing a one (1) enables the pause timer. Writing a zero (0) disables the pause timer.	Yes	Yes	0
17	**Local Bus Pause Timer Enable.** Writing a one (1) enables the Pause Timer. Writing a zero (0) disables the Pause Timer.	Yes	Yes	0
18	**Local Bus BREQ Enable**. Writing a one (1) enables the Local Bus BR#/BREQi. When BR#/BREQi is active, the PLX 9656 de-asserts HOLD and releases the Local Bus.	Yes	Yes	1
20:19	**DMA Channel Priority.** When a 00 these bits indicate a rotational priority scheme**.** Writing a 01 indicates Channel 0 has priority. Writing a 10 indicates Channel 1 has priority. Writing 11 indicates reserved.	Yes	Yes	00
21	**Local Bus Direct Slave Release Bus Mode**. When set to one (1), the PLX 9656 de-asserts HOLD and releases the Local Bus when the Direct Slave Write FIFO becomes empty during a Direct Slave Write or when the Direct Slave Read FIFO becomes full during a Direct Slave Read.	Yes	Yes	1
22	**Direct Slave LOCK# Enable**. Writing a one (1) enables Direct Slave locked sequences. Writing a zero (0) disables Direct Slave locked sequences.	Yes	Yes	0
23	**PCI Request Mode**. Writing a one (1) causes the PLX 9656 to de-assert REQ# when it asserts FRAME during a master cycle. Writing a zero (0) causes the PLX 9656 to leave REQ# asserted for the entire Bus Master cycle.	Yes	Yes	0

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Table 3-58 Mode/DMA Arbitration Register Bit Map (Continued)

Mode/DMA Arbitration: MARBR, Offset $AC or $12C				
Bit	**Description**	**Read**	**Write**	**Value after Initialization**
24	**Delayed Read Mode**. When set to a one (1), the PLX 9656 operates in Delayed Transaction mode for Direct Slave reads. The PLX 9656 issues a retry to the PCI Host and prefetches read data.	Yes	Yes	0
25	**PCI Read No Write Mode**. Writing a one (1) forces a retry on writes if a read is pending. Writing a zero (0) allows writes to occur while a read is pending.	Yes	Yes	0
26	**PCI Read with Write Flush Mode**. Writing a one (1) submits a request to flush a pending read cycle if a write cycle is detected. Writing a zero (0) submits a request to not affect pending reads when a write cycle occurs (PCI Specification r2.1 compatible).	Yes	Yes	0
27	**Gate Local Bus Latency Timer with BREQi (C and J modes only).**	Yes	Yes	0
28	**PCI Read No Flush Mode**. Writing a one (1) submits a request to not flush the read FIFO if the PCI read cycle completes (Read Ahead mode). Writing a zero (0) submits a request to flush the read FIFO if a PCI read cycle completes.	Yes	Yes	0
29	When set to zero (0), reads from the PCI Configuration register address $00 returns Device ID and Vendor ID. When set to a one (1), reads from the PCI Configuration register address $00 returns Subsystem ID and Subsystem Vendor ID.	Yes	Yes	0
30	**FIFO Full Status Flag**. When set to a one (1), the Direct Master Write FIFO is almost full. Reflects the value of the DMPAF pin.	Yes	Yes	0
31	**BIGEND#/WAIT# Input/Output Select (M mode only)**. Writing a one (1) selects the wait functionality of the signal. Writing a zero (0) selects Big Endian input functionality.	Yes	Yes	0

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DMA Threshold Register

Table 3-59 DMA Threshold Register Bit Map

DMA Threshold: DMATHR; Offset $B0				
Bits	**Description**	**Read**	**Write**	**Value after PCI Reset**
3:0	**DMA Channel 0 PCI-to-Local Almost Full (C0PLAF)**. Number of full entries (divided by two, minus one) in the FIFO before requesting the Local bus for writes. (C0PLAF + 1) + (C0PLAE + 1) should be ≤ a FIFO depth of 32.	Yes	Yes	$0
7:4	**DMA Channel 0 Local-to-PCI Almost Empty (C0LPAE)**. Number of empty entries (divided by two, minus one) in the FIFO before requesting the Local bus for reads. (C0PLAF + 1) + (C0LPAE + 1) should be ≤ a FIFO depth of 32.	Yes	Yes	$0
11:8	**DMA Channel 0 Local-to-PCI Almost Full (C0LPAF).** Number of full entries (divided by two, minus one) in the FIFO before requesting the PCI bus for writes.	Yes	Yes	$0
15:12	**DMA Channel 0 PCI-to-Local Almost Empty (C0PLAE).** Number of empty entries (divided by two, minus one) in the FIFO before requesting the PCI bus for reads.	Yes	Yes	$0
19:16	**DMA Channel 1 PCI-to-Local Almost Full (C1PLAF)**. Number of full entries (divided by two, minus one) in the FIFO before requesting the Local bus for writes. (C1PLAF + 1) + (C1PLAE + 1) should be ≤ a FIFO depth of 32.	Yes	Yes	$0
23:20	**DMA Channel 1 Local-to-PCI Almost Empty (C1LPAE)**. Number of empty entries (divided by two, minus one) in the FIFO before requesting the Local bus for reads. (C1PLAF + 1) + (C1LPAE + 1) should be ≤ a FIFO depth of 32.	Yes	Yes	$0
27:24	**DMA Channel 1 Local-to-PCI Almost Full (C1LPAF).** Number of full entries (divided by two, minus one) in the FIFO before requesting the PCI bus for writes.	Yes	Yes	$0
31:28	**DMA Channel 1 PCI-to-Local Almost Empty (C1PLAE).** Number of empty entries (divided by two, minus one) in the FIFO before requesting the PCI bus for reads.	Yes	Yes	$0

NOTE: ***For DMA Channel 0 only***, if number of entries needed is x, then the value is one less than half the number of entries (that is, x/2 - 1).

DMA Channel 0 PCI Dual Address Cycle Upper Address Register

Table 3-60 DMA Channel 0 PCI Dual Address Cycle Upper Address Register Bit Map

DMA Channel 0 PCI Dual Address Cycle Upper Address: DMADAC0; Offset $B4				
Bits	**Description**	**Read**	**Write**	**Value after PCI Reset**
31:0	**Upper 32 Bits of the PCI Dual Address Cycle PCI Address during DMA Channel 0 Cycles**. If set to $0, the PLX 9656 performs a 32-bit DMA Channel 0 Address access.	Yes	Yes	$0

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DMA Channel 1 PCI Dual Address Cycle Upper Address Register

Table 3-61 DMA Channel 1 PCI Dual Address Cycle Upper Address Register Bit Map

DMA Channel 1 PCI Dual Address Cycle Upper Address: DMADAC0; Offset $B8				
Bits	**Description**	**Read**	**Write**	**Value after PCI Reset**
31:0	**Upper 32 Bits of the PCI Dual Address Cycle PCI Address during DMA Channel 1 Cycles**. If set to $0, the PLX 9656 performs a 32-bit DMA Channel 0 Address access.	Yes	Yes	$0

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RFM Control and Status Registers

The RFM Control and Status registers for the VMIPCI-5565 are located in the PLX Local Address Space 0. The base address for this group of registers is contained in the PCI Configuration Register "PCI Base Address 2". The space reserved for this group of registers is 64 bytes.

Table 3-62 Memory Map of the Local Control and Status Registers

Offset	Mnemonic	Description	Access	Comments
$0	BRV	Board Revision	Read Only	Current board revision/model
$1	BID	Board ID Register	Read Only	BID is $65 for VMIPCI-5565
$3…2	--	Reserved	--	
$4	NID	Node ID Register	Read Only	Set by 8 board jumpers
$7…5	--	Reserved	--	
$B…8	LCSR1	Local Control & Status Reg. 1	Read/Write	Some bits reserved. Some bits read only.
$F...C	--	Reserved	--	
$13…10	LISR	Local Interrupt Status Reg.	Read/Write	Some bits reserved. Some bits read only.
$17…14	LIER	Local Interrupt Enable R.	Read/Write	
$1B…18	NTD	Network Target Data	Read/Write	32 Data bits for network target
$1C	NTN	Network Target Node	Read/Write	Target node ID for network Int.
$1D	NIC	Network Interrupt Command	Read/Write	Select Int type and initiate interrupt
$1F…1E	--	Reserved	--	
$23…20	ISD1	Int. 1 Sender Data	Read/Write	127 loc. By 32 bit FIFO for network Int. 1
$24	SID1	Int. 1 Sender ID	Read/Write	127 loc. Deep FIFO/ write clears pointers
$27…25	--	Reserved	--	
$2B…28	ISD2	Int. 2 Sender Data	Read/Write	127 loc. By 32 bit FIFO for network Int. 2
$2C	SID2	Int. 2 Sender ID	Read/Write	127 loc. Deep FIFO/ write clears pointers
$2F…2D	--	Reserved	--	
$33…30	ISD3	Int. 3 Sender Data	Read/Write	127 loc. By 32 bit FIFO for network Int. 3
$34	SID3	Int. 3 Sender ID	Read/Write	127 loc. Deep FIFO/ write clears pointers
$37...35	--	Reserved		
$3B.38	INITD	Initialized Node Data	Read/Write	127 loc. By 32 bit FIFO for opt. Data
$3C	INITN	Initialized Node ID	Read/Write	127 loc. Deep FIFO/ write clears pointers
$3F.3D	--	Reserved	--	

Board Revision Register

Board Revision (BRV) (Offset $0): An 8-bit register used to represent revisions or model numbers. This register is read only.

Board ID Register

Board ID (BID) (Offset $1): An 8-bit register which contains an 8-bit code unique to the VMIxxx-5565 type boards. The code is $65. This register is read only.

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Node ID Register

Node ID (NID) (Offset $4): An 8-bit register containing the node ID of the board. This register reflects the setting of the eight onboard jumpers and is read only. Each board on a network must have a unique node ID.

Local Control and Status Register 1

Local Control and Status Register 1 (LCSR1): Offset $8, Read/Write, Lword, Word, Byte							
Bit 31	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
Status LED Off	Transmitter Disable	Dark-on-Dark Enable	Loopback Enable	Local Bus Parity Enable	Redundant Mode Enabled	Rogue Master 1 Enabled	Rogue Master 0 Enabled

Bit 23	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
Reserved		Config 1	Config 0	Reserved		Offset 1	Offset 0

Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
Reserved							

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
TX FIFO Empty	TX FIFO Almost Full	Latched RX FIFO Full	Latched RX FIFO Almost Full	Latched Sync Loss	RX Signal Detect	Bad Data	Own Data

Local Control and Status Register 1 Bit Definitions

Bit 31: **Status LED Off** – The board contains a user defined RED status LED. Setting this bit low (0) turns off the LED. The default state of this bit after reset is high (1) and the LED will be ON.

Bit 30: **Transmitter Disable** – Setting this bit high (1) will manually turn off the board's transmitter. The default state of this bit after reset is low (0) and the transmitter is enabled. When turning the board's transmitter back "on" by setting this bit back to low (0), an unspecified amount of time must be allowed to provide for the turn-on time of the optics.

Bit 29: **Dark-on-Dark Enable** – When this bit is set high (1), the board's transmitter will be turned OFF if the board's receiver does not detect a signal or if the receiver detects invalid data patterns. The dark-on-dark feature is useful in hub configurations.

Bit 28: **Loopback Enable** – When this bit is set high (1), the fiber optic transmitter and receiver are disabled and the transmit signal is looped back to the receiver circuit internally. This allows basic functional testing with or without an external cable.

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Local Control and Status Register 1 Bit Definitions (Continued)

Bit 27: **Local Bus Parity Enable** – When this bit is set high (1), parity is enabled on all onboard memory accesses. While the parity is enabled, writes to the memory are only allowed as 32-bit Lwords or 64-bit Qwords. Write accesses as 16-bit words or 8-bit bytes shall be prohibited.

Bit 26: **Redundant Mode Enabled** - When this bit is set high (1), redundant mode of network transfers has been enabled. This bit is read-only. Redundant mode is enabled by the removal of the jumper shunt between pins 1 and 2 of jumper E7.

Bit 25: **Rogue Master 1 Enabled** - When this bit is set high (1), the board is operating as Rogue Master 1. This bit is read-only. Rogue Master 1 operation is enabled by the removal of the jumper shunt between pins 3 and 4 of E7.

Bit 24: **Rogue Master 0 Enabled** - When this bit is set high (1), the board is operating as Rogue Master 0. This bit is read-only. Rogue Master 0 operation is enabled by the removal of the jumper shunt between pins 5 and 6 of E7.

Bits 23 and 22: **Reserved** - These bits are reserved.

Bits 21 and 20: **Config 1 and Config 0** – These two bits indicated the memory size as defined in the following table. The two bits are read only.

Config 1	Config 0	Memory Size
0	0	64MB
0	1	128MB
1	0	Reserved
1	1	Reserved

Bits 19 and 18: **Reserved** - These bits are reserved.

Bits 17 and 16: **Offset 1 and Offset 0** – When the host PCI system writes to the onboard memory and initiates a packet over the network, Offset 1 and Offset 0 will apply an offset to the network address as it is sent or received over the network. The offset does not appear on local access to the memory, and the offset does not alter network packets as they pass through the board. Offset 1 and Offset 0 provide four possible binary increments of 64MB each through the 256MB network address range. When the address and offset exceeds the 256MB network address range, the address bits beyond 256MB will be truncated. This causes the write to wrap around into a lower memory location. Offsets 1 and 0's bits correspond to the network address bits A27 and A26 respectively.

Offset 1	Offset 0	Offset Applied
0	0	0
0	1	$4000000
1	0	$8000000
1	1	$C000000

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Local Control and Status Register 1 Bit Definitions (Concluded)

Bits 15 through 08: **Reserved** - These bits are reserved.

Bit 07: **TX FIFO Empty** – A logic high (1) indicates the TX FIFO is currently empty. This bit provides immediate status only (not latched) and is read only.

Bit 06: **TX FIFO Almost Full** – A logic high (1) indicates the TX FIFO is currently almost full. This bit provides immediate status only (not latched) and is read only. Periodic assertion of this bit is normal.

Bit 05: **Latched RX FIFO Full** – A logic high (1) indicates the RX FIFO has experienced a full condition at least once. This bit is read only within this register. To clear this condition write to the corresponding bit within the Local Interrupt Status Register.

NOTE: The occurrence of the Latched RX FIFO Full signal is a fault condition due to a board malfunction and indicates that the received data may have been lost.

Bit 04: **Latched RX FIFO Almost Full** – A logic high (1) indicates the RX FIFO is operating at the maximum acceptable rate. Under normal operating conditions, this event should not occur. This bit is read only within this register. To clear this condition, write to the corresponding bit within the Local Interrupt Status Register.

Bit 03: **Latched Sync Loss** – A logic high (1) indicates the receiver circuitry has detected the loss of a valid signal at least once since the last time the flag has been cleared. Under normal operating conditions, this event should not occur and may indicate a loss of data. A logic high may indicate the receiver's link was intentionally or unintentionally disconnected.

Bit 02: **RX Signal Detect** – A logic high (1) indicates the board receiver is currently detecting light. This bit provides immediate status only (not latched) and is read only.

Bit 01: **Bad Data** – A logic high (1) indicates the board receiver circuit has detected bad (invalid) data at least once since power up or since the flag had previously been cleared. Under normal operating conditions, this event should not occur and may indicate a loss of data. This bit is read only within this register. To clear this condition, write to the corresponding bit within the Local Interrupt Status Register.

Bit 00: **Own Data** – A logic high (1) indicates the board has detected the return of its own data packet at least once since this bit has previously been cleared. This bit serves as an indicator that the link is intact. The Own Data bit should be set anytime a write to the onboard memory occurs or any time network interrupt is initiated. This bit is both read and write accessible.

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Local Interrupt Control Registers (LISR and LIER)

The VMIPCI-5565 contains a number of sources for the PCI interrupt. The second tier of interrupts that are not sourced from within the PLX PCI interface device but rather come from local onboard devices are called the LISR as shown in Table 3-63 below and the LIER shown in Table 3-64 on page 79. All Local Interrupts are logically "ORed" together into the single interrupt input to the PLX device. This input is the LINTi#. The LINTi# line is, in turn, controlled by Bit 11 of the PLX Local Configuration register (INTCSR at offset $68 to Base address 0). The control and status of local interrupts are implemented in the two local registers (LISR and LIER). The bit functions of these two registers mirror each other.

Local Interrupt Status Register

The LISR contains a group of interrupt status flags, while the LIER contains a corresponding group of enables. Before any local interrupt can cause an interrupt on the LINTi# line, the status bit, its enable and the Global Enable must be asserted.

Table 3-63 Local Interrupt Status Register Bit Map

Local Interrupt Status Register (LISR): Offset $10, Read/Write, Lword, Word or Byte accesses							
Bit 31	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
Reserved							

Bit 23	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
Reserved							

Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
Auto Clear Flag	Global Interrupt Enable	Local Mem. Parity Error	Mem. Write Inhibited	Latched Sync Loss	RX FIFO Full	RX FIFO Almost Full	Bad Data

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
Pending Init. Interrupt	Rogue Packet Fault	Reserved		Reset Node Request	Pending Net. Int 3	Pending Net. Int 2	Pending Net. Int 1

Local Interrupt Control Register Bit Definitions

Bits 31 through 16: **Reserved** - These bits are reserved.

Bit 15: **Auto Clear Flag** – This bit is a read only status indicator of the corresponding bit in the LIER Register. When this bit is high (1), the Global Interrupt Enable (Bit 14) will automatically be cleared as this register (LISR) is being read. Clearing the Global Interrupt Enable de-asserts the LINTi# and, in turn, releases the PCI Interrupt.

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Local Interrupt Control Register Bit Definitions (Continued)

Bit 14: **Global Interrupt Enable** – This bit must be set high (1) in addition to any interrupt flag and its associated enable bit in the LIER before the LINTi# line is asserted and a PCI interrupt can result. If the Auto Clear enable bit in the LIER is set high (1), the Global Interrupt Enable bit will automatically be cleared as this register (LISR) is being read. This bit is read and write accessible with this register and thus allows a single read-modify-write operation to service the local interrupts.

Bit 13: **Local Memory Parity Error** – When this bit is high (1), one or more parity errors have been detected on local memory accesses. This bit is latched. Once set, it must be cleared by writing a zero to this bit location. Note that Bit 27 of the LCSR1 must be set high before parity is active. Also note that parity works only on Lword and Qword accesses. Word (16-bit) and byte (8-bit) memory write access are inhibited.

Bit 12: **Mem. Write Inhibited** – When this bit is high (1), a 16-bit word or an 8-bit byte write to local memory was attempted and inhibited while the board was in the parity enabled mode. This bit is latched. Once set, it must be cleared by writing a zero to this bit location.

Bit 11: **Latched Sync Loss** – When this bit is high (1), the receiver circuit has lost synchronization with the incoming signal one or more times. This bit is latched. Once set, it must be cleared by writing a zero to this bit location. The assertion of the Latched Sync Loss usually indicates the receiver link was or is disconnected, either intentionally or unintentionally, and data may have been lost. This event will also occur if the upstream node tied to the receiver is powered off or is disabled.

Bit 10: **RX FIFO Full** – When this bit is high (1), the RX FIFO has been full one or more times. This bit is latched. Once set, it must be cleared by writing a zero to this bit location. This is a fault condition and data may have been lost.

Bit 09: **RX FIFO Almost Full** – When this bit is high (1), the RX FIFO has been almost full one or more times. This bit is latched. Once set, it must be cleared by writing a zero to this bit location. The assertion of the RX FIFO Almost Full bit indicates the receiver circuit is operating at maximum capacity and, under normal operating conditions, this event should not occur. If it does occur, the PCI bus master should temporarily suspend all write and read operations to the board.

Bit 08: **Bad Data** – When this bit is high (1), the receiver circuit has detected invalid data one or more times. This bit is latched. Once set, it must be cleared by writing a zero to this bit location.

Bit 07: **Pending Init. Interrupt** – When this bit is high (1), the board has detected one or more initialization interrupts from other nodes on the network. To see which nodes have sent an initialization interrupt, read the Initialized Node ID (INITN) FIFO at offset $3C.

Bit 06: **Rogue Packet Fault** - When this bit is set high (1), the board is operating as either Rogue Master 1 or 0 and has detected and removed a rogue packet. This bit is latched. Once set, it must be cleared by writing a zero (0) to this bit location.

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Local Interrupt Control Register Bit Definitions (Concluded)

Bits 05 and 04: **Reserved** - These are reserved.

Bit 03: **Reset Node Request** – When this bit is high (1), another node on the network has requested that the local PCI bus master reset this board. The VMIPCI-5565 does not reset itself automatically.

Bit 02: **Pending Net. Int 3** – When this bit is high (1), one or more type 2 network interrupts have been received. To see the sender data and sender node ID(s), read the Interrupt Sender Data 3 (ISD3) FIFO at offset $30 and the Interrupt Sender ID (SID3) FIFO at offset $34 respectively.

Bit 01: **Pending Net. Int 2** – When this bit is high (1), one or more type 1 network interrupts have been received. To see the sender data and sender node ID(s), read the Interrupt Sender Data 2 (ISD2) FIFO at offset $2B and the Interrupt Sender ID (SID2) FIFO at offset $2C respectively.

Bit 00: **Pending Net. Int 1** – When this bit is high (1), one or more type 0 network interrupts have been received. To see the sender data and sender node ID(s), read the Interrupt Sender Data 1 (ISD1) FIFO at offset $20 and the Interrupt Sender ID (SID1) FIFO at offset $24 respectively.

Local Interrupt Enable Register

Table 3-64 Local Interrupt Enable Register Bit Map

Local Interrupt Enable Register (LIER): Offset $14, Read/Write, Lword, Word or Byte accesses							
Bit 31	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
Reserved							

Bit 23	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
Reserved							

Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
Auto Clear Enable	Reserved	Enable Int on Local Mem. Parity Error	Enable Int on Mem Write Inhibit	Enable Int on Latched Sync Loss	Enable Int on RX FIFO Full	Enable Int on RX FIFO Almost Full	Enable Int on Bad Data

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
Enable Int on Pending Init. Interrupt	Enable Int on Rogue Packet Fault	Reserved		Enable Int on Reset Node Request	Enable Int on Pending Net. Int 3	Enable Int on Pending Net. Int 2	Enable Int on Pending Net. Int 1

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Network Target Data Register (NTD)

The Network Target Data (NTD) register is a 32-bit register located at offset $18 that contains the data associated with one of the four network interrupts that will be sent to the target (destination) node. Writing data to this register does not initiate the actual interrupt; only writing to the Network Interrupt Command (NIC) register will do so. The NTD register is both read and write accessible.

Network Target Node Register (NTN)

The Network Target Node (NTN) register is an 8-bit register located at offset $1C that contains the node ID of the target (destination) node. Writing to the NTN register does not initiate the actual network interrupt. This register is both read and write accessible. The NTN register can be written or read with the NIC register as a single 16-bit word.

Network Interrupt Command Register (NIC)

The Network Interrupt Command (NIC) register is an 8-bit register located at offset $1D that contains a four bit code, which defines the type of network interrupt that is issued. See Table 3-65 below for a definition of the possible codes. The NIC is both read and write accessible. Writing to the NIC register, only initiates the network interrupt.

Table 3-65 Network Interrupt Command Register Interrupt Codes

Network Interrupt Command Register (NIC): Offset $1D, Read/Write Lword, Word or Byte accesses	
NIC[3,2,1,0]	**Function**
X000	Reset Node Request (sets LISR Bit 03 only, PCI master must perform actual reset)
X001	Network Interrupt 1 (stored in a 127 deep FIFO at the receiving node)
X010	Network Interrupt 2 (stored in a 127 deep FIFO at the receiving node)
X011	Network Interrupt 3 (stored in a 127 deep FIFO at the receiving node)
X100	Reserved (Setting to this type will only set the OWN DATA bit in the CSR1)
X101	Reserved (Setting to this type will only set the OWN DATA bit in the CSR1)
X110	Reserved (Setting to this type will only set the OWN DATA bit in the CSR1)
X111	Network Initialized Interrupt (stored in a 127 deep FIFO at the receiving node)
1XXX	Global enable. Send to all nodes regardless of the NTN register.

Upon any reset, all bits of the NIC register will be set high (1), which corresponds to the selection of a Network Initialized Interrupt. Further, upon power up or reset, the Network Initialized Interrupt will be issued automatically by the board over the network once the board initialization is complete and the network synchronization is established. Network Initialized Interrupt is globally issued.

The NTD, NTN and NIC registers described above are involved with the generation of network interrupts. Four pairs of registers described below are involved with receiving those network interrupts.

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Interrupt 1 Sender ID FIFO

Each time one node issues a network interrupt, it includes its own node ID as part of the packet. At each other network node, the interrupt packet is evaluated. If the network interrupt is directed to that node, and if the network interrupt is of type 1, then the sender's node ID is stored in a 127 location deep FIFO called the Interrupt 1 Sender ID FIFO or SID1. The SID1 is accessed at offset $24. Like any normal FIFO, each time the SID1 is read, the FIFO address pointer automatically increments to the next location in the FIFO. Therefore, each sender ID can only be read once from the SID1 FIFO. Writing any data to the SID1 FIFO causes the SID1 FIFO to be cleared to zero and set to empty. Note that the value of zero is NOT a true indicator that the FIFO is empty since zero is also a valid node ID. To see if network interrupts are pending, examine bits 07, 03, 02, 01 and 00 in the LISR register.

Interrupt 1 Sender Data FIFO

The 32 bit Interrupt 1 Sender Data (ISD1) FIFO is located at offset $20. It contains up to 127 Lwords of data, which have been sent to this node in type 1 network interrupt packets. The function of the 32 bits of data is user defined. The ISD1 is a 127 location deep FIFO, but it is coupled and slaved to the companion FIFO SID1. Essentially, there is only one address pointer for both FIFOs and that pointer is only affected by access to the Sender ID 1 (SID1) FIFO. For this reason, each location within the data (ISD1) FIFO can be read multiple times without incrementing the address pointer, while reading the companion SID1 FIFO increments the pointer for both FIFOs. For this same reason, the user must read the data (ISD1) before the Sender ID (SID1) or the corresponding data will be lost.

Interrupt 2 Sender ID FIFO

The Interrupt 2 Sender ID FIFO (SID2) is located at offset $2C and functions just like SID1, except it responds only to type 2 network interrupts.

Interrupt 2 Sender Data FIFO

The Interrupt 2 Sender Data (ISD2) FIFO is located at offset $28 and functions just like ISD1, except it responds only to type 2 network interrupts.

Interrupt 3 Sender ID FIFO

The Interrupt 3 Sender ID FIFO (SID3) is located at offset $34 and functions just like SID1, except it responds only to type 3 network interrupts.

Interrupt 3 Sender Data FIFO

The Interrupt 3 Sender Data (ISD3) FIFO is located at offset $30 and functions just like ISD1, except it responds only to type 3 network interrupts.

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Initialized Node ID FIFO

The Initialized Node ID (INITN) FIFO is located at offset $3C and, for the most part, functions just like SID1. However, it responds only to network interrupts for which the sender's NIC register is set to $F or $7. In many circumstances it may be used as a fourth network interrupt. However, the INITN FIFO has one additional function. Whenever any node is reset due to power-up or otherwise, the local processor can issue an "initialized" network interrupt indicating it has completed its own initialization. The initialized network interrupt is sent globally to all other nodes present on the network and is written into the INITN FIFO of each node. The user can designate one or more of these nodes as network master nodes within the user's system software routines. Upon receiving an initialized interrupt, the master node can refresh portions or all of the Reflective Memory in the initialized node by rewriting the selected areas of its own Reflective Memory.

Initialized Node Data FIFO

The Initialized Node Data (INITD) FIFO is located at offset $38 and functions, for the most part, just like SID1. However, like the INITN FIFO, it responds only to network interrupts for which the sender's NIC register is set to $F or $7. Also like the INITN FIFO, it also responds to initialized interrupts.

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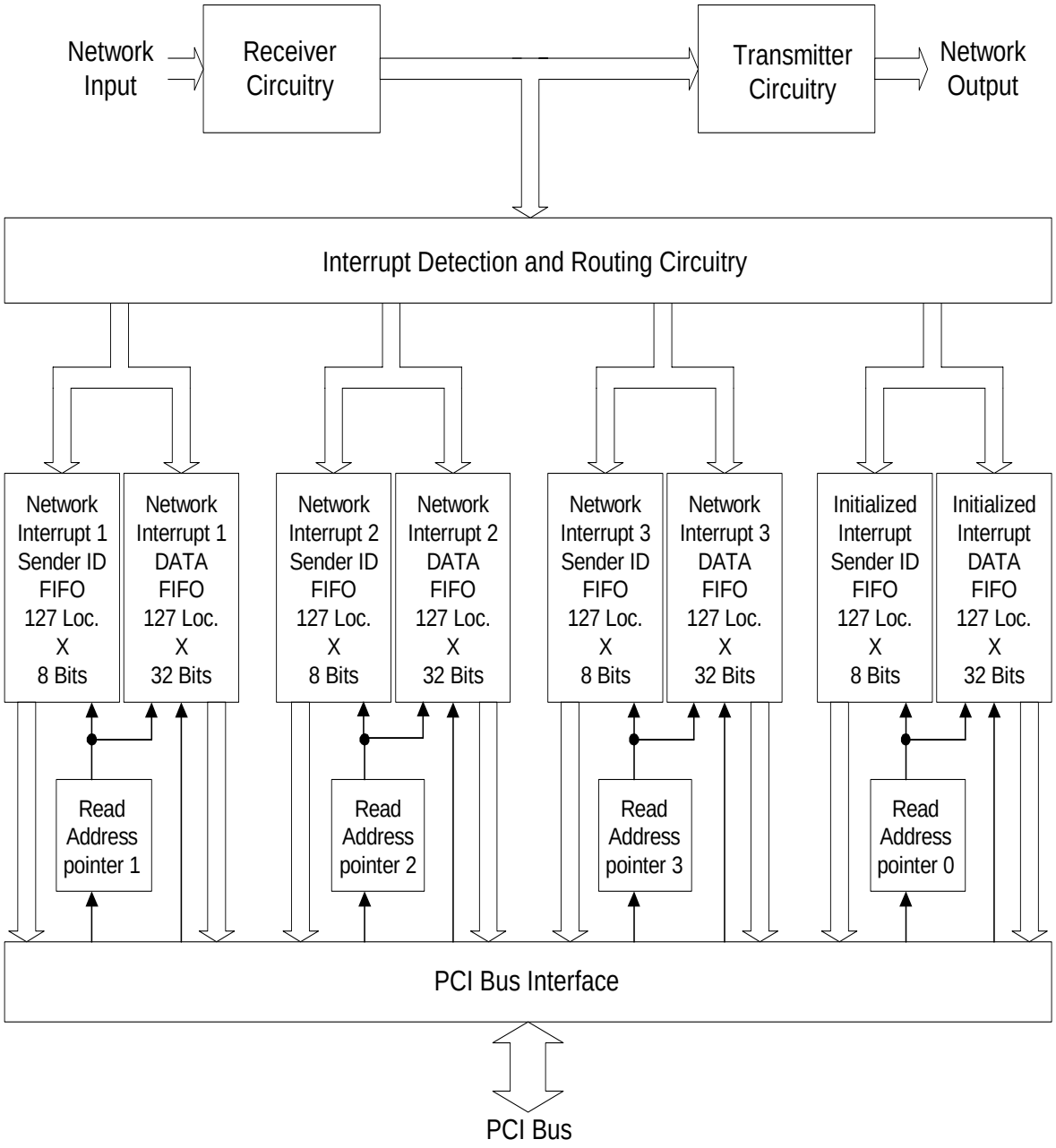


Figure 3-1 Block Diagram of the Network Interrupt Reception Circuitry

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Example of a DMA Operation for the VMIPCI-5565

1. Find the value stored in Base Address Register 0 (this is the starting address of the Local Control and Configuration registers, which include the DMA Control registers). The value in this register is BaseAddr0.
2. There are five DMA registers that must be written to set up the DMA cycle. All five registers will remain unchanged after the DMA cycle.

DMA channel 0 mode register: Set to $1C3.	**DMAMODE0 at BaseAddr0 + offset $80**
DMA channel 0 PCI starting address: Set to the starting address of the PC memory (for either source or destination transfer).	**DMAPADR0 at BaseAddr0 + offset $84**
DMA channel 0 local starting address: Set to the starting address of the local (RFM) memory (for either source or destination transfers) NOTE: For the VMIPCI-5565, the first local (RFM) memory location is at $00000.	**DMALADR0 at BaseAddr0 + offset $88**
DMA channel 0 transfer size: Set to the number of bytes to be transferred.	**DMASIZ0 at BaseAddr0 + offset $8C**
DMA channel 0 Descriptor Pointer: Set to $0 for PCI-to-Local or set to $8 for Local-to-PCI.	**DMADPR0 at BaseAddr0 + offset $90**

3. To initiate and monitor the transfer write to the following:

   DMA channel 0 Command/Status register:
   DMACSR0 at BaseAddr0 + offset $A8
   Write $0003 to start the transfer, then poll the same register. When it contains $xx11, the DMA cycle is complete.

NOTE: Polling read cycles take priority over the DMA cycles. Overly aggressive polling will slow down the DMA transfer.

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Example of Network Interrupt Handling

The following is an example of the steps necessary to set up the VMIPCI-5565 to generate a PCI interrupt in response to one of the three basic network interrupts. This example also lists the steps necessary to service that interrupt. When using this example, it is advisable to examine Figure 1-1 on page 26 and Figure 3-1 on page 83 to obtain a visual sense of the circuitry involved.

Setup:

1. Clear any prior unscheduled interrupts in the SID1 FIFO by writing zero (0) to the SID1 at BaseAddr2 + offset $24.
2. Clear any prior unscheduled interrupts in the SID2 FIFO by writing zero (0) to the SID2 at BaseAddr2 + offset $2C.
3. Clear any prior unscheduled interrupts in the SID3 FIFO by writing zero (0) to the SID3 at BaseAddr2 + offset $34.
4. Using a read-modify-write operation, set Bit 02, Bit 01 and Bit 00 high (1) in the LIER register at BaseAddr2 + offset $14. This allows any one of the three basic network interrupts to assert the onboard signal LINTi#, provided the global enable in the LISR is also high (1).
5. Write the value $4000 to the LISR register at BaseAddr2 + offset $10. The value $4000 sets the global interrupt enable (Bit 14) high (1) and clears any unrelated sources. You may prefer to use a read-modify-write operation if other sources in the LISR are to remain unchanged.
6. Using a read-modify-write operation, set Bit 8 and Bit 11 high (1) in the INTCSR register at BaseAddr0 + offset $68. Bit 8 is the PCI Interrupt Enable and Bit 11 is the Local Interrupt Input (LINTi#) Enable.

Servicing Network Interrupts:

1. Read the INTCSR register at BaseAddr0 + offset $68. Verify that the Local Interrupt Input Active (Bit 15) is high (1). If Bit 15 is not high, or if another interrupt source within the INTCSR has priorty, then the user's interrupt service routine would take different steps from this point on.
2. Read the LISR register at BaseAddr2 + offset $10. Determine if the Pending Network Interrupt 3 (Bit 02), the Pending Network Interrupt 2 (Bit 01) or the Pending Network Interrupt 1 (Bit 00) is high (1).
3. Assuming, for example, the previous step indicates Network Interrupt 2 is pending, read the Interrupt 2 Sender Data FIFO at BaseAddr2 + offset $28 and place the value in the desired user location. If the user is not passing data with the interrupt, then this step is unnecessary and may be skipped.
4. Read the Interrupt 2 Sender ID FIFO at BaseAddr2 + offset $2C and place the value in the desired user location. This value is the node ID of the source of the network interrupt. Provided that there are no additional network interrupts stored in the Sender ID FIFO, the act of reading this value will de-assert the Pending Network Interrupt 2 bit (Bit 01) in the LISR, which in turn de-asserts the LINTi# line. De-asserting the LINTi# line will de-assert the PCI interrupt.

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Maintenance

Maintenance

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1. Software resident on the product
2. System configuration
3. Electrical connections
4. Jumper or configuration options
5. Boards are fully inserted into their proper connector location
6. Connector pins are clean and free from contamination
7. No components or adjacent boards were disturbed when inserting or removing the board from the chassis
8. Quality of cables and I/O connections

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Maintenance Prints

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Compliance Information

This chapter provides the applicable information regarding regulatory compliance for the VMIPCI-5565.

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CE

GE Fanuc Embedded Systems VMIPCI-5565 has been evaluated to and has met the requirements for compliance to the following standards:

- EN55024
- EN55022, Class B
- EN61000-4-2
- EN61000-4-3
- EN61000-4-4
- EN61000-4-5
- EN61000-4-6

International Compliance

It has also met the following international levels.

European Union

- EN55024 (1998 w A1:01 & A2: 03)
- CISPR22, EN55022 (Class B)
- CISPR11, EN55011(Class B, Group 1)

United States

- FCC Part 15, Subpart B, Section 109, Class B
- CISPR 22 (1997), Class B
- ANSI C63.4 (2003) method

Australia/New Zealand

- AS/NZS CISPR 22 (2002) Class B using:
- EN55022 (1998) Class B

Japan

- VCCI (April 2005) Class B using:
- CISPR 22 (1997) Class B
- ANSI C63.4 (2003) method

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Canada

- ICES-003 Class B using:
- CISPR 22 (1997) Class B
- ANSI C63.4 (2003) Method

FCC Part 15

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

FCC Class B

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

NOTICE: Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Canadian Regulations

The VMIPCI-5565 Class B digital apparatus complies with Canadian ICES-003.

NOTE: Any equipment tested and found compliant with FCC Part 15 for unintentional radiators or EN55022 (previously CISPR 22) satisfies ICES-003.

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