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VMIVME-5532L VMEbus
FIBER-OPTIC REPEATER LINK

PRODUCT MANUAL

DOCUMENT NO. 500-005532-000 B

Revised December 21, 1995

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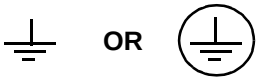
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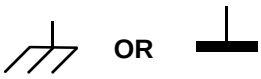
Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 volts are so marked).



Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.



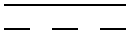
Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. Before operating the equipment, terminal marked with this symbol must be connected to ground in the manner described in the installation (operation) manual.



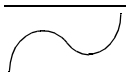
Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.



Alternating current (power line).



Direct current (power line).



Alternating or direct current (power line).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in injury or death to personnel.

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VMIVME-5532L VMEbus FIBER-OPTIC REPEATER LINK

TABLE OF CONTENTS

Page

SECTION 1. INTRODUCTION
1.1 FEATURES 1-1
1.2 FUNCTIONAL DESCRIPTION 1-2
1.3 REFERENCE MATERIAL LIST 1-2

SECTION 2. PHYSICAL DESCRIPTION AND SPECIFICATION

SECTION 3. THEORY OF OPERATION
3.1 OPERATIONAL OVERVIEW 3-1
3.2 THEORY OF OPERATION 3-2
3.3 REGISTERS 3-2
3.4 BUS ARBITRATION SIGNALS 3-2
3.5 ENABLING THE VMEbus IN A SLAVE CHASSIS 3-3
3.6 ENABLING SYSRESET* IN THE SLAVE CHASSIS 3-3
3.7 INTERRUPT SIGNALS 3-4

SECTION 4. PROGRAMMING
4.1 PROGRAMMING 4-1
4.2 VMIVME-5532L REGISTER MAP 4-1
4.2.1 Board ID Register (BIR) 4-1
4.2.2 Burst Mode Register (BMR) 4-2
4.2.3 Host Bus Grant Status Register (HBGSR) 4-3
4.2.4 VMEbus Activity Status Register (VASR) 4-3
4.2.5 Burst Mode Key Register (BMKR) 4-4
4.2.6 VMEbus Key Register (VMEKR) 4-4
4.2.7 Sysreset Enable Key Register (SEKR) 4-5
4.2.8 Slave Chassis Reset Key Register (SCRKR) 4-5

SECTION 5. CONFIGURATION AND INSTALLATION
5.1 UNPACKING PROCEDURES 5-1
5.2 PHYSICAL INSTALLATION 5-1
5.3 BOARD CONFIGURATION 5-1
5.3.1 All Jumpers Removed 5-2
5.3.2 Slot 1 Disable (E3) 5-2
5.3.3 Register Enable (E2) 5-2
5.3.4 Register Address (E1) 5-2
5.3.5 Burst Mode Enable (E4) 5-4
5.4 FRONT PANEL RESET SWITCH 5-4
5.5 CABLE INSTALLATION 5-4

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TABLE OF CONTENTS (Concluded)

SECTION 6. MAINTENANCE
6.1 MAINTENANCE 6-1
6.2 MAINTENANCE PRINTS 6-1

LIST OF FIGURES

Figure — Page
3.1-1 Single Link Application Configuration 3-5
3.1-2 Star Configuration 3-6
3.1-3 Redundant Link Configuration 3-7
3.1-4 Block Diagram of VMIVME-5532S Slave Chassis Repeater Link Board 3-8
3.1-5 Block Diagram of VMIVME-5532M Master Chassis Repeater Link Board 3-9
5.3-1 VMIVME-5532L Location of User-Configurable Jumpers 5-3
5.3.4-1 Register Address Jumper (E1) 5-4
5.5-1 VMIVME-5532L Cable Connection 5-5

LIST OF TABLES

Table — Page
4.2-1 VMIVME-5532L Register Map 4-1
4.2.1-1 Board ID Register Bit Map 4-2
4.2.2-1 Burst Mode Register Bit Map 4-2
4.2.3-1 Host Bus Grant Status Register Bit Map 4-3
4.2.4-1 VMEbus Activity Status Register Bit Map 4-3
4.2.5-1 Burst Mode Key Register Bit Map 4-4
4.2.6-1 VMEbus Key Register Bit Map 4-4
4.2.7-1 Sysreset Key Register Bit Map 4-5

APPENDIX

A Assembly Drawing, Parts List, and Schematic

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SECTION 1

INTRODUCTION

1.1 FEATURES

VMIC's VMIVME-5532L Fiber-Optic Repeater Link is a two-board set with interconnecting cables that allows the user to effectively extend a VMEbus chassis to more than 20 slots. The "extended" slots are operational for noninterrupting VMEbus slave modules and local master modules (for example, redundant repeater links from multiple master chassis to one slave chassis). When multiple master modules are used in the slave chassis, bus ownership remains in the slave chassis and does not proceed up the link into the master chassis.

The Repeater Link has several unique features, as listed below:

a. Software transparency, allows direct communication from master chassis to slave chassis with no software overhead (unidirectional link control with bidirectional data transfers).

b. Register enable allows operations as described above, but includes functional registers located in short I/O addressing space dealing with multiple master control of the VMEbus in the slave chassis.

c. VMIVME-5532S slave board includes the system controller functions of SYSRESET* on power up, SYSCLK, and a single level bus arbiter (SGL) when used in slot 1 of the slave chassis.

d. VMIVME-5532S slave board includes a Release-on-Request (ROR) bus requester which operates level 3 (BR3*) when used in slot 1 through slot 21 of the slave chassis.

e. A Burst Mode Register allowing the host CPU in the master chassis to request and hold the slave chassis VMEbus is available when the VMIVME-5532's registers are enabled.

f. Supports 8-, 16-, and 32-bit transfers.

g. Supports 16-, 24-, and 32-bit addressing.

h. Supports VMEbus slaves and local VMEbus masters in the "slave" chassis.

i. Supports fiber-optic cables up to 6,560 feet (2,000 meters) long.

j. Allows expansion to 19 x 19 slots using a 20-slot backplane in a star configuration.

k. Double Eurocard form factor.

l. Industry standard ST type I/O connectors.

m. Link includes one Model VMIVME-5532M, one VMIVME-5532S, and two interconnecting fiber-optic cables.

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1.2 FUNCTIONAL DESCRIPTION

The VMIVME-5532L is a two-board set that allows noninterrupting VMEbus slave I/O boards residing in one VMEbus chassis to be controlled by a VMEbus master residing in another chassis. The VMEbus chassis in which the VMEbus master resides is referred to as a master chassis, while the VMEbus slave board resides in a slave chassis. A master VMEbus chassis can communicate with several slave chassis and several slave chassis can communicate with one master chassis, both by using multiple repeater links.

1.3 REFERENCE MATERIAL LIST

For a detailed explanation of the VMEbus and its characteristics, the publication “The VMEbus Specification” is available from:

VITA
VFEA International Trade Association
10229 N. Scottsdale Road
Scottsdale, AZ 85253
(602) 951-8866

The following Application and Configuration Guides are available from VMIC to assist in the selection, specification, and implementation of systems based upon VMIC's products:

TITLE	DOCUMENT NO.
Digital Input Board Application Guide	825-000000-000
Change-of-State Application Guide	825-000000-002
Digital I/O (with Built-in-Test) Product Line Description	825-000000-003
Synchro/Resolver (Built-in-Test) Subsystem Configuration Guide	825-000000-004
Analog I/O Products (with Built-in-Test) Configuration Guide	825-000000-005
Connector and I/O Cable Application Guide	825-000000-006

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SECTION 2

PHYSICAL DESCRIPTION AND SPECIFICATIONS

REFER TO 800-005532-000 SPECIFICATION

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SECTION 3

THEORY OF OPERATION

3.1 OPERATIONAL OVERVIEW

The VMIVME-5532 Link is a high-performance, yet easy-to-use method of linking two or more VMEbus systems together using fiber-optic cables. The Repeater Link is a two-board set which allows VMEbus slave boards residing in one VMEbus chassis to be controlled by a VMEbus master residing in another chassis. The VMEbus chassis in which the VMEbus master resides is referred to as the master chassis, while the VMEbus slave boards reside in a slave chassis. The two-board set is configured as shown in Figure 3.1-1 on page 3-5, with one board designated for the master chassis while the other board is designated for the slave chassis. A master VMEbus chassis can communicate with several slave chassis by using multiple Repeater Links in a star configuration as shown in Figure 3.1-2 on page 3-6, or in a redundant repeater link configuration as shown in Figure 3.1-3 on page 3-7.

The link is software transparent (no registers requiring software initialization) when the repeater link's registers are disabled. Any VMEbus master in the master chassis may access (read or write) to any slave board in the slave chassis. Only noninterrupting slave and master boards are allowed in the slave chassis. The link between the master chassis and slave chassis is automatically established when a VMEbus master (typically a CPU board) addresses any board in the slave chassis (with AM codes 09, 0D, 29, 2D, 39, or 3D).

Any time a master in the master chassis initiates a read/write access it will be repeated to the slave chassis. If a slave board in the slave chassis responds to that address, the data transfer (read or write) will occur between the chassis and a Data Transfer Acknowledge (DTACK) will be returned to the master (in the master chassis) to complete the cycle.

The link includes registers that can be enabled using a jumper, allowing the user to gain more control over the bus arbitration operations occurring in the slave chassis. These registers are intended to support a redundant link configuration but allows a CPU to reside in the slave chassis for local control. These registers feature a Burst Mode bit which allows the host CPU in the master chassis to request and hold the VMEbus in the slave chassis.

A link consists of two boards (VMIVME-5532M and VMIVME-5532S) and the two fiber-optic cables which enable a VMEbus system to be expanded beyond a single chassis. Refer to Figures 3.1-4 and 3.1-5 on pages 3-8 and 3-9 for a block diagram of each board.

A link reset switch located on the front panel of the VMIVME-5532M allows the user to assert SYSRESET* in the slave chassis without resetting the master chassis (or additional slave chassis in a star configuration). When the registers are enabled, the

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host software can also reset the slave chassis by writing to a register. When SYSRESET* is asserted in the master chassis, it is repeated to all slave chassis whose repeater links have SYSRESET* enabled.

Both the VMIVME-5532M and VMIVME-5532S have a dual-color LED which indicates the status of the link. The LED is green when the local receiver has achieved phase-lock and frame synchronization with the remote transmitter. A red LED indicates that the link is not ready and can be due to damaged or miswired cables, unpowered remote chassis, or a damaged link. The LED is red momentarily during reset.

3.2 THEORY OF OPERATION

The VMIVME-5532M and VMIVME-5532S each consist of three state machines, Taxi Transmitter, Taxi Receiver, Fiber-Optic Transmitter, Fiber-Optic Receiver, random logic, and buffers. The three state machines control the VMEbus interface, the Taxi Transmitter, and the Taxi Receiver.

3.3 REGISTERS

The VMIVME-5532L registers become active when the register enable jumper (E2) is installed. The registers consist of an assortment of control and status registers whose master function is to support redundant repeater link operations in the slave chassis (multiple master chassis, only one slave chassis). The registers are described in detail in Section 4, the programming section. The registers and jumpers are physically located on the VMIVME-5532S (slave Board).

3.4 BUS ARBITRATION SIGNALS

The bus arbitration signals in the master chassis are not repeated over the link, but the VMIVME-5532L does provide an on-board bus requester and arbiter to support multiple VMIVME-5532S boards in the slave chassis.

In the master chassis, the VMIVME-5532M (the “M” designating master chassis where the CPUs reside) functions as a slave device, sending appropriate read/write accesses across the fiber-optic cable. The BGIN* signals are connected to the BGOUT* signals in order to maintain the BUS Grant daisy chain in the master chassis.

The VMIVME-5532S (the “S” designating slave chassis) actually functions as a bus master receiving VMEbus information over the fiber-optic cable, and then generating the appropriate VMEbus cycle in the slave chassis.

The bus arbiter located on the VMIVME-5532S board is a Single Level Arbiter (SGL) supporting bus requests in the slave chassis on level 3 (BR3*). The bus arbiter is enabled when the slot 1 disable jumper (E3) is omitted and the VMIVME-5532S board is installed in slot 1 of the slave chassis.

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The bus requester located on the VMIVME-5532S board is a Release-on-Request (ROR) type supporting bus requests in the slave chassis on level 3 (BR3*) only. The bus requester is always enabled, and allows the VMIVME-5532S board to be located in any of the slots of the slave chassis.

The VMIVME-5532L registers supplement the bus arbitration functions in the slave chassis. The Burst Mode bit located in the Burst Mode Register allows a host CPU located in a master chassis to request and hold the VMEbus when this bit is set. When set, the Burst Mode bit prevents another master located in the slave chassis from being granted the VMEbus by holding BBSY* active. Altering of the Burst Mode bit is enabled by the Burst Mode Enable jumper (E4) and the Burst Mode Key register which adds a layer of protection against inadvertent writes to this bit.

The Host Bus Grant Status register is a read-only register supporting the bus arbitration functions in the slave chassis. The host CPU can read this bit (for example, after setting the Burst Mode bit) to see if the repeater link has been granted the bus.

The bus arbitration functions of the VMIVME-5532S board are primarily present to support multiple repeater links to a single chassis for local control.

NOTE:

BUS ARBITRATION IN THE SLAVE CHASSIS DOES NOT PROCEED UP THE FIBER-OPTIC CABLES INTO THE MASTER CHASSIS. BUS OWNERSHIP REMAINS LOCAL IN THE SLAVE CHASSIS.

3.5 ENABLING THE VMEbus IN A SLAVE CHASSIS

The VMIVME-5532L fiber-optic repeater link will be ready to perform VMEbus transfers on power up when the repeater link's registers are **DISABLED** (Register Enable jumper E2 omitted).

The VMEbus in the slave chassis is not enabled on power up when the repeater link's registers are **ENABLED**. The host CPU must write $54XX to the VMEbus Key register to enable the repeater link to transfer master chassis cycles to the slave chassis. The system reset (SYSRESET*) function in the slave chassis requires an additional enable to be set before the host CPU can reset the slave chassis using the repeater link.

3.6 ENABLING SYSRESET* IN THE SLAVE CHASSIS

The VMIVME-5532L fiber-optic Repeater Link will generate a SYSRESET* pulse in the slave chassis on power up. When the Register Enable Jumper (E2) is omitted (registers disabled), the repeater link will generate a SYSRESET* pulse in the slave chassis when SYSRESET* is active in the master chassis (or the VMIVME-5532M front panel reset button is depressed) following power up.

If the repeater link's registers are enabled (jumper E2 installed), the host CPU must set the VMEbus Key Register equal to $54XX enabling the repeater link, and it must set the Sysreset Enable Key Register equal to $A6XX enabling the repeater link to generate a SYSRESET* pulse in the slave chassis. Under these conditions, a

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SYSRESET* pulse in the slave chassis can be generated by a SYSRESET* occurring in the master chassis (and passed along the link to the slave chassis), or by writing a $75XX to the slave chassis reset key (generating a reset in the slave chassis only) or by pressing the front panel reset button on the VMIVME-5532M (generating a reset in the slave chassis only).

NOTE:

THE VMIVME-5532L REGISTERS WILL BE RESET FOLLOWING A SYSRESET* OCCURRING IN THE SLAVE CHASSIS.

3.7 INTERRUPT SIGNALS

The interrupt signals are not repeated over the fiber-optic link. Therefore, the VMIVME-5532S regenerates the IACK* signal as a logic high in the slave chassis. In the master chassis, the VMIVME-5532M connects IACKIN* to IACKOUT* in order to maintain the Interrupt Acknowledge daisy chain.

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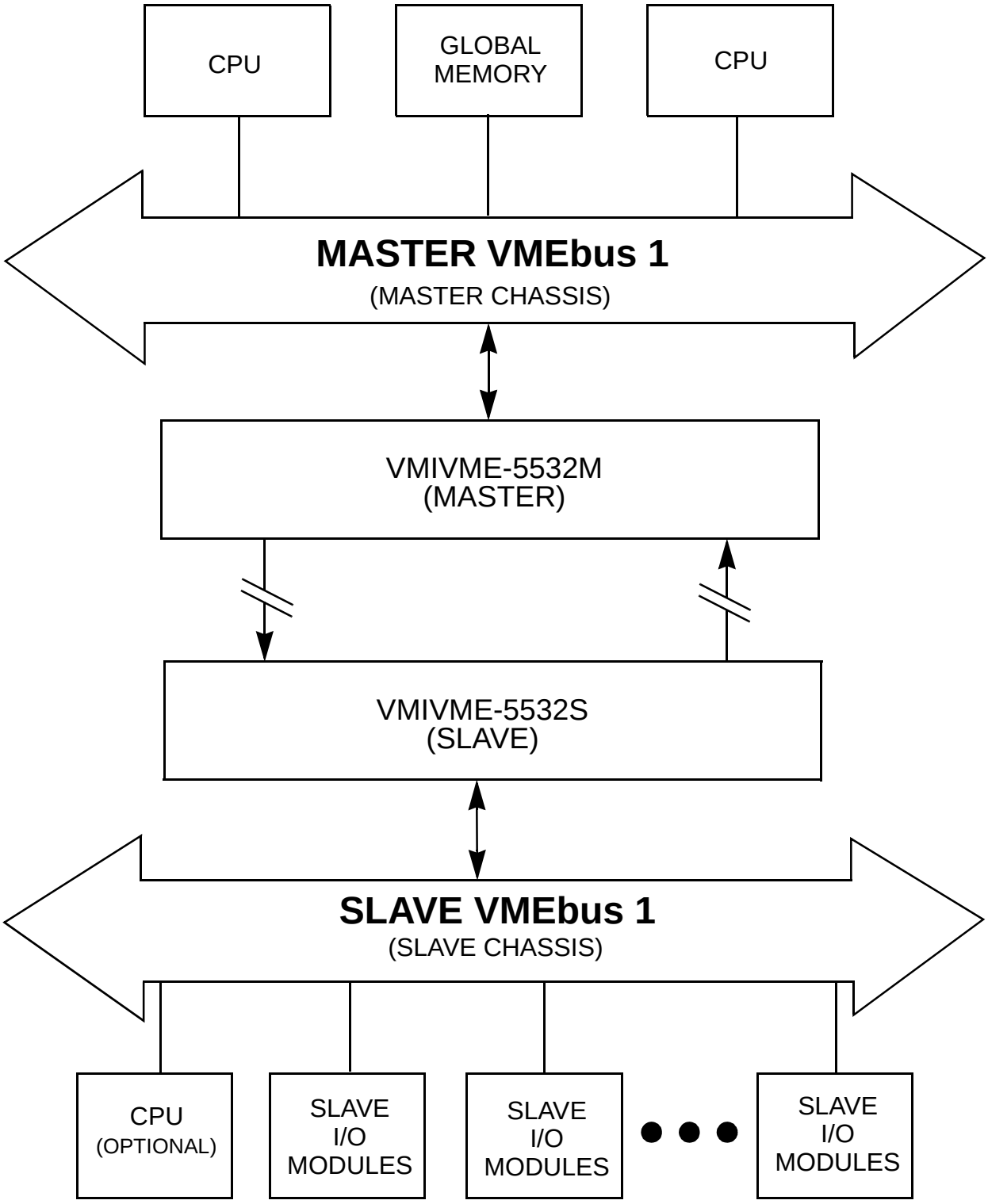


Figure 3.1-1. Single Link Application Configuration

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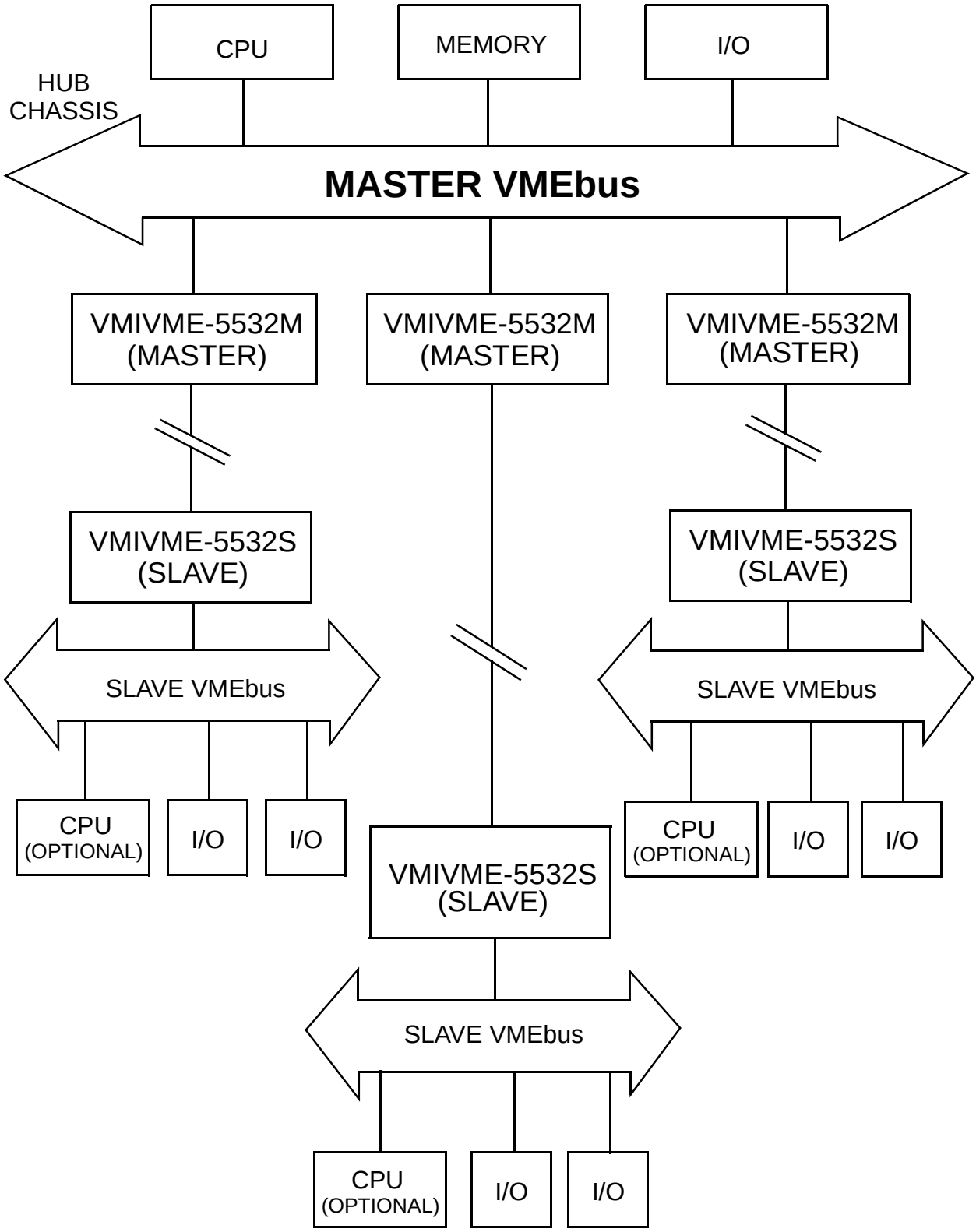
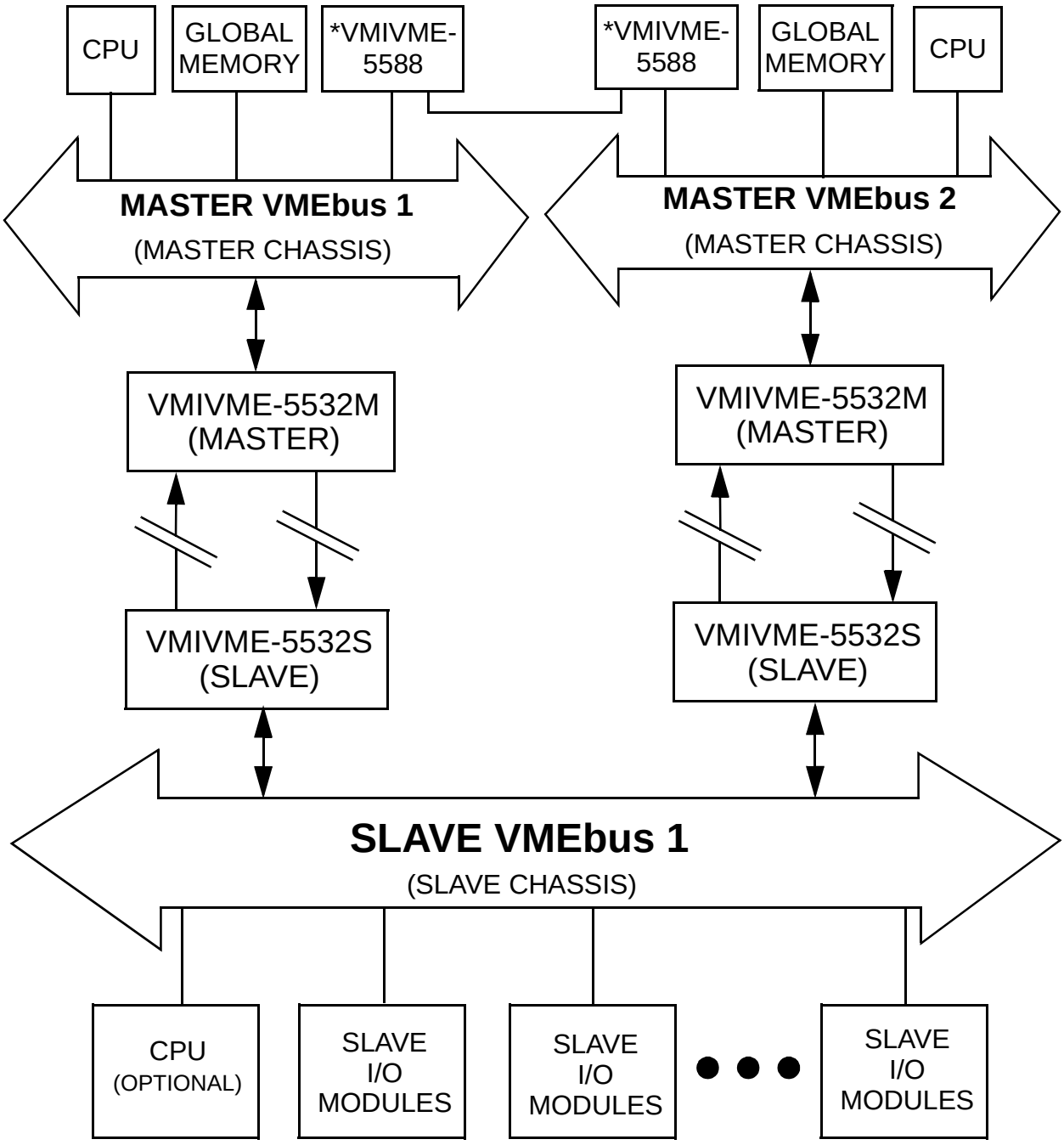


Figure 3.1-2. Star Configuration

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***VMIVME-5588 Reflective Memory is an effective way to synchronize memory for multiple master CPUs.

Figure 3.1-3. Redundant Link Configuration

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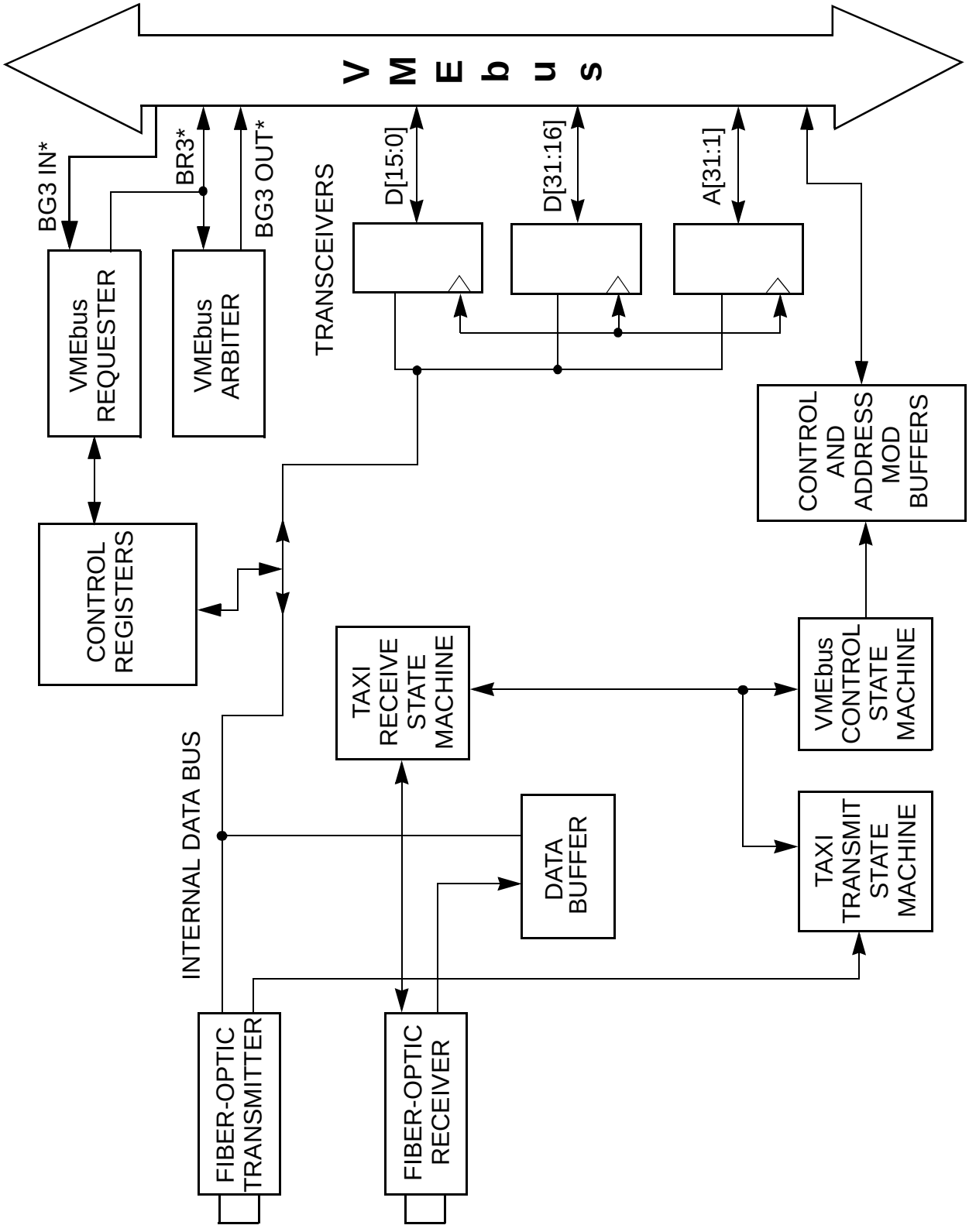


Figure 3.1-4. Block Diagram of VMIVME-5532S Slave Chassis Repeater Link Board

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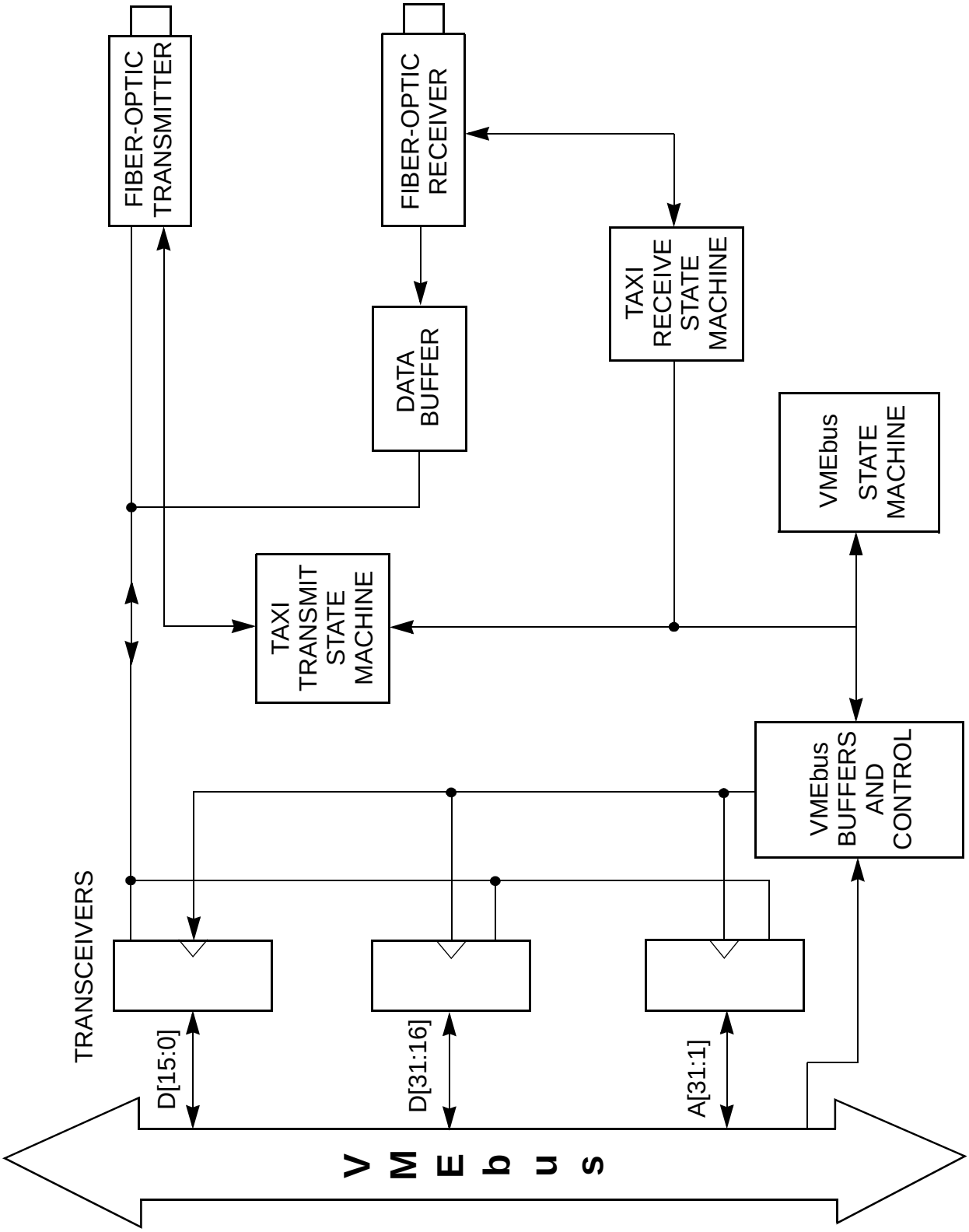


Figure 3.1-5. Block Diagram of VMIVME-5532M Master Chassis Repeater Link Board

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SECTION 4

PROGRAMMING

4.1 PROGRAMMING

The VMIVME-5532L Fiber-Optic Repeater Link functions as a software transparent link or as a semitransparent link containing registers in VMEbus short I/O space supporting various multimaster functions in the slave chassis. When jumper E2, the register enable jumper, is omitted (registers disabled) the repeater link is software transparent. Boards residing in the slave VMEbus chassis respond to VMEbus transfers as if they were located in the master VMEbus chassis. Therefore, the Repeater Link requires no special programming considerations, due to the fact that the address and data signals are transmitted to the slave chassis. Any VMEbus read/write access (with AM codes 09, 0D, 29, 2D, 39, or 3D) in the master chassis is transmitted across the link to the slave chassis.

When jumper E2 is installed (registers enabled), the registers listed in Table 4.2-1 become active and will reside in VMEbus short I/O space at the short I/O offset address determined by the E1 jumper field (Register Address Jumpers). The link operates as described in the previous paragraph, except it appears that a 256 byte short I/O space containing the registers resides in the slave chassis.

4.2 VMIVME-5532L REGISTER MAP

Table 4.2-1. VMIVME-5532L Register Map

SHORT I/O ADDRESS	FUNCTION	MNEMONIC	WIDTH	ACCESS
$00	BOARD ID REGISTER	BIR	BYTE/WORD	READ-ONLY
$02	BURST MODE REGISTER	BMR	BYTE/WORD	READ/WRITE
$04	HOST BUS GRANT STATUS REGISTER	HBGSR	BYTE/WORD	READ-ONLY
$06	VMEBUS ACTIVITY STATUS REGISTER	VASR	BYTE/WORD	READ-ONLY
$08	BURST MODE KEY REGISTER	BMKR	BYTE/WORD	READ/WRITE
$0A	VMEBUS KEY REGISTER	VMEKR	BYTE/WORD	READ/WRITE
$0C	SYSRESET ENABLE KEY REGISTER	SEKR	BYTE/WORD	READ/WRITE
$0E	SLAVE CHASSIS RESET KEY REGISTER	SCRKR	BYTE/WORD	READ/WRITE

4.2.1 Board ID Register (BIR)

The VMIVME-5532L Board ID Register is an 8-bit read-only register at offset $00 with a constant value set at $4AXX. This ID number uniquely identifies the board from other VMIC products.

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Table 4.2.1-1. Board ID Register Bit Map

BOARD ID REGISTER (OFFSET $00) READ-ONLY, BYTE/WORD							
BIT 15	**BIT 14**	**BIT 13**	**BIT 12**	**BIT 11**	**BIT 10**	**BIT 09**	**BIT 08**
0	1	0	0	1	0	1	0
BIT 07	**BIT 06**	**BIT 05**	**BIT 04**	**BIT 03**	**BIT 02**	**BIT 01**	**BIT 00**
Reserved							

Power up/Reset Default = $A400 M5532L/T4.2.1-1

4.2.2 Burst Mode Register (BMR)

Table 4.2.2-1. Burst Mode Register Bit Map

Burst Mode Register (Offset $02) Read/Write, Byte/Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
BURST MODE	X	X	X	X	X	X	X
BIT 07	**BIT 06**	**BIT 05**	**BIT 04**	**BIT 03**	**BIT 02**	**BIT 01**	**BIT 00**
X	X	X	X	X	X	X	X

Power up/Reset Default = $0000 M5532L/T4.2.2-1

Burst Mode Register Bit Definition

Bit 15, Burst Mode: The Burst Mode register contains a single bit allowing the host processor in the master chassis to put the repeater link in a VMEbus request and hold mode called Burst Mode. The Burst Mode Key Register must be set equal to $9DXX and the Burst Mode Enable jumper (E4) must be installed before this bit can be altered. When set to a logical “1,” the Burst Mode bit (bit 15) directs the on-board bus requester to perform a bus request in the slave chassis and after being granted the bus, the slave chassis will subsequently hold the bus until the Burst Mode bit is set to a logical “0.” When the slave chassis VMEbus has been granted to this repeater link, setting of the Burst Mode bit prevents deactivating the BBUSY* VMEbus signal in the slave chassis which is being driven by the slave repeater board.

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4.2.3 Host Bus Grant Status Register (HBGSR)

Table 4.2.3-1. Host Bus Grant Status Register Bit Map

HOST BUS GRANT STATUS REGISTER (OFFSET $04) READ-ONLY, BYTE/WORD							
BIT 15	**BIT 14**	**BIT 13**	**BIT 12**	**BIT 11**	**BIT 10**	**BIT 09**	**BIT 08**
HOST BUS GRANT	X	X	X	X	X	X	X

BIT 07	**BIT 06**	**BIT 05**	**BIT 04**	**BIT 03**	**BIT 02**	**BIT 01**	**BIT 00**
X	X	X	X	X	X	X	X

Power up /Reset Default =$0000 M5532L/4.2.3-1

Host Bus Grant Status Register Bit Definitions

Bit 15, Host Bus Grant: This register contains a single read-only bit allowing the host CPU in the master chassis to determine if the repeater link has been granted ownership of the slave chassis VMEbus. A logical “1” indicates that the repeater link has been granted ownership of the VMEbus and a logical “0” indicates that the link has not been granted ownership.

4.2.4 VMEbus Activity Status Register (VASR)

Table 4.2.4-1. VMEbus Activity Status Register Bit Map

VMEbus ACTIVITY STATUS REGISTER (OFFSET $06) READ-ONLY, BYTE/WORD							
BIT 15	**BIT 14**	**BIT 13**	**BIT 12**	**BIT 11**	**BIT 10**	**BIT 09**	**BIT 08**
VMEBUS ACTIVITY	X	X	X	X	X	X	X

BIT 07	**BIT 06**	**BIT 05**	**BIT 04**	**BIT 03**	**BIT 02**	**BIT 01**	**BIT 00**
X	X	X	X	X	X	X	X

Power up/Reset Defualt = $0000 M5532L/T4.2.4-1

VMEbus Activity Status Register Bit Definitions

Bit 15, VMEbus Activity: This register contains a single read-only bit indicating activity on the VMEbus in the slave chassis. A VMEbus DTACK* going active in the slave chassis will set the bit to a logical “1” and a read of this register will clear the bit to a logical “0.”

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4.2.5 Burst Mode Key Register (BMKR)

Table 4.2.5-1. Burst Mode Key Register Bit Map

BURST MODE KEY REGISTER (OFFSET $08) READ/WRITE, BYTE/WORD							
BIT 15	**BIT 14**	**BIT 13**	**BIT 12**	**BIT 11**	**BIT 10**	**BIT 09**	**BIT 08**
BURST MODE KEY BIT 7	BURST MODE KEY BIT 6	BURST MODE KEY BIT 5	BURST MODE KEY BIT 4	BURST MODE KEY BIT 3	BURST MODE KEY BIT 2	BURST MODE KEY BIT 1	BURST MODE KEY BIT 0
BIT 07	**BIT 06**	**BIT 05**	**BIT 04**	**BIT 03**	**BIT 02**	**BIT 01**	**BIT 00**
X	X	X	X	X	X	X	X

Power up/Reset Default = $0000 M5532L/T4.2.5-1

Burst Mode Key Register Bit Definitions

Bits 15 through 8, Burst Mode Key Bit [7..0]: The Burst Mode Key Register is used in conjunction with the Burst Mode Enable jumper E4 to allow altering of the Burst Mode bit. When the Burst Mode Enable jumper is installed (meaning Burst Mode can be enabled) and the Burst Mode Key equals $9DXX, the Burst Mode bit can be altered from its present state. When either the jumper or key are inactive (jumper E4 omitted or the key does not equal $9DXX), the Burst Mode bit cannot be altered. Burst Mode Key = $9DXX.

4.2.6 VMEbus Key Register

Table 4.2.6-1. VMEbus Key Register Bit Map

VMEBUS KEY REGISTER (OFFSET $A) READ/WRITE, BYTE/WORD							
BIT 15	**BIT 14**	**BIT 13**	**BIT 12**	**BIT 11**	**BIT 10**	**BIT 09**	**BIT 08**
VMEBUS KEY BIT 7	VMEBUS KEY BIT 6	VMEBUS KEY BIT 5	VMEBUS KEY BIT 4	VMEBUS KEY BIT 3	VMEBUS KEY BIT 2	VMEBUS KEY BIT 1	VMEBUS KEY BIT 0
BIT 07	**BIT 06**	**BIT 05**	**BIT 04**	**BIT 03**	**BIT 02**	**BIT 01**	**BIT 00**
X	X	X	X	X	X	X	X

Power up/Reset Default = $0000 M5532L/T4.2.6-1

VMEbus Key Register Bit Definitions

Bits 15 through 8, VMEbus Key Bits [7..0]: The VMEbus Key Register is used to enable the VMIVME-5532 Repeater Link (specifically the slave board) in the slave chassis. When this key is equal to $54XX and the link has been granted the bus in the slave chassis, the link can communicate on the slave chassis VMEbus lines. When this register is not equal to $54XX, the repeater link will not be able to perform bus request or bus

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transfers. The SYSRESET* function in the slave chassis uses the VMEbus Key Register as well as another register, the Sysreset Key Register, to enable it. VMEbus Key = $54XX

4.2.7 Sysreset Enable Key Register (SEKR)

Table 4.2.7-1. Sysreset Enable Key Register Bit Map

SYSRESET ENABLE KEY REGISTER (OFFSET $0C) READ/WRITE, BYTE/WORD							
BIT 15	**BIT 14**	**BIT 13**	**BIT 12**	**BIT 11**	**BIT 10**	**BIT 09**	**BIT 08**
SYSRESET ENABLE KEY BIT 7	SYSRESET ENABLE KEY BIT 6	SYSRESET ENABLE KEY BIT 5	SYSRESET ENABLE KEY BIT 4	SYSRESET ENABLE KEY BIT 3	SYSRESET ENABLE KEY BIT 2	SYSRESET ENABLE KEY BIT 1	SYSRESET ENABLE KEY BIT 0
BIT 07	**BIT 06**	**BIT 05**	**BIT 04**	**BIT 03**	**BIT 02**	**BIT 01**	**BIT 00**
X	X	X	X	X	X	X	X

Power up/Reset Default = $0000 M5532L/T4.2.7-1

Sysreset Enable Key Register Bit Definitions

Bits 15 through 8, Sysreset Enable Key Bit [7..0]: The Sysreset Key Register is used along with the VMEbus Key Register in allowing the host CPU in the master chassis to initiate system reset in the slave chassis. When the VMEbus Key is active (equal to $54XX), and the Sysreset Enable Key is set active by writing a $A6XX to the register, the host can initiate a SYSRESET* in the slave chassis by producing a SYSRESET* in the master chassis (the link will transfer it to the slave chassis) or by writing $75XX to the Slave Chassis Reset Key Register (offset $XX0E), or by pushing the reset button on the VMIVME-5532M. Sysreset Enable Key = $A6XX.

4.2.8 Slave Chassis Reset Key Register (SCRKR)

Table 4.2.8-1. Slave Chassis Reset Key Register Bit Map

SLAVE CHASSIS RESET KEY REGISTER (OFFSET $0E) READ/WRITE, BYTE/WORD							
BIT 15	**BIT 14**	**BIT 13**	**BIT 12**	**BIT 11**	**BIT 10**	**BIT 09**	**BIT 08**
SLAVE CHASSIS RESET KEY BIT 7	SLAVE CHASSIS RESET KEY BIT 6	SLAVE CHASSIS RESET KEY BIT 5	SLAVE CHASSIS RESET KEY BIT 4	SLAVE CHASSIS RESET KEY BIT 3	SLAVE CHASSIS RESET KEY BIT 2	SLAVE CHASSIS RESET KEY BIT 1	SLAVE CHASSIS RESET KEY BIT 0
BIT 07	**BIT 06**	**BIT 05**	**BIT 04**	**BIT 03**	**BIT 02**	**BIT 01**	**BIT 00**
X	X	X	X	X	X	X	X

Power up/Reset Default = $0000 M5532L/T4.2.8-1

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Slave Chassis Reset Key Register Bit Definitions

Bits 15 through 8, Slave Chassis Reset Key Bit [7..0]: The Slave Chassis Reset Key Register is used to produce the SYSRESET* function in the slave chassis under host software control. When the VMEbus Key is active (equal to $54XX) and the Sysreset Enable Key is set active (equal to $A6XX), the host can write a $75XX to this register and produce a SYSRESET* in the slave chassis. There will be no SYSRESET* generated in the master chassis. Slave Chassis Reset Key = $75XX.

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SECTION 5

CONFIGURATION AND INSTALLATION

5.1 UNPACKING PROCEDURES

CAUTION

SOME OF THE COMPONENTS ASSEMBLED ON VMIC's PRODUCTS CAN BE SENSITIVE TO ELECTROSTATIC DISCHARGE AND DAMAGE CAN OCCUR ON BOARDS THAT ARE SUBJECTED TO A HIGH ENERGY ELECTROSTATIC FIELD. UNUSED BOARDS SHOULD BE STORED IN THE SAME PROTECTIVE BOXES IN WHICH THEY WERE SHIPPED. WHEN THE BOARD IS TO BE PLACED ON A BENCH FOR CONFIGURING, ETC., IT IS SUGGESTED THAT CONDUCTIVE MATERIAL BE INSERTED UNDER THE BOARD TO PROVIDE A CONDUCTIVE SHUNT.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice about the disposition of the damaged item(s).

5.2 PHYSICAL INSTALLATION

CAUTION

DO NOT INSTALL OR REMOVE BOARDS WHILE POWER IS APPLIED.

De-energize the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the board is properly aligned and oriented in the supporting card guides, slide the board smoothly forward against the mating connector until firmly seated.

5.3 BOARD CONFIGURATION

The VMIVME-5532L fiber-optic repeater link requires a minimum amount of user configuration prior to operation. The VMIVME-5532M can be placed in slots 2 through 21 of the master VMEbus chassis. The VMIVME-5532M does not contain any jumpers for configuration. All of the configuration operations are contained on the VMIVME-5532S board. See Figure 5.3-1 on page 5-3 for location of jumpers.

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The VMIVME-5532S will occupy either slot 1 or slots 2 through 21 of the slave VMEbus chassis and is determined by jumper E3 (slot 1 disabled). This jumper function as well as the other jumpers are described below. All configuration operations are performed on the VMIVME-5532S.

5.3.1 All Jumpers Removed

The VMIVME-5532L Fiber-Optic Repeater Link operates as a transparent VMEbus repeater when all jumpers are removed. In this configuration, the VMIVME-5532S is required to occupy slot 1 of the slave chassis and the slave board's system controller functions are enabled. All VMIVME-5532L register functions are disabled. The VMIVME-5532L link boards can be placed in their respective chassis, fiber-optic cables properly connected, and the repeater link is ready to operate with no software setup required.

5.3.2 Slot 1 Disable (E3)

The Slot 1 Disable jumper is used to configure the VMIVME-5532S slave board as a slot 1 VMEbus master (enables system controller function) or as master residing in slots 2 through 21 of the slave chassis.

When the **JUMPER IS OMITTED**, the slave board's system controller functions are **ENABLED** and the board should be placed in slot 1 of the VMEbus slave chassis. System controller functions that are enabled/disabled by this jumper include the single level VMEbus bus arbiter, SYSCLK, and power up SYSRESET*. When the **JUMPER IS INSTALLED,** the slave board's system controller functions are **DISABLED** and the board should be placed in slots 2 through 21 of the slave chassis.

5.3.3 Register Enable (E2)

The Register Enable jumper is used to enable/disable the VMIVME-5532 link's on-board registers. When this **JUMPER IS OMITTED**, the repeater link's registers (residing on the VMIVME-5532S) will be **DISABLED** and the repeater link will function in a transparent manner passing all of the master chassis data transfers through to the slave chassis. Jumper E1 (Register Address) and E4 (Burst Mode Enable) become "don't care" functions when this jumper is omitted.

When this **JUMPER IS INSTALLED,** the repeater link's registers will be **ENABLED** and located at the VMEbus short I/O offset address determined by the jumper field at E1.

5.3.4 Register Address (E1)

The Register Address jumpers are used to set the VMEbus short I/O offset address when the user has enabled the VMIVME-5532 link's registers by installing the Register Enable jumper E2. The link's registers can reside on any 256 byte boundary and will respond to either short supervisory or short nonprivileged accesses. The jumper field is shown in Figure 5.3.4-1 on page 5-4.

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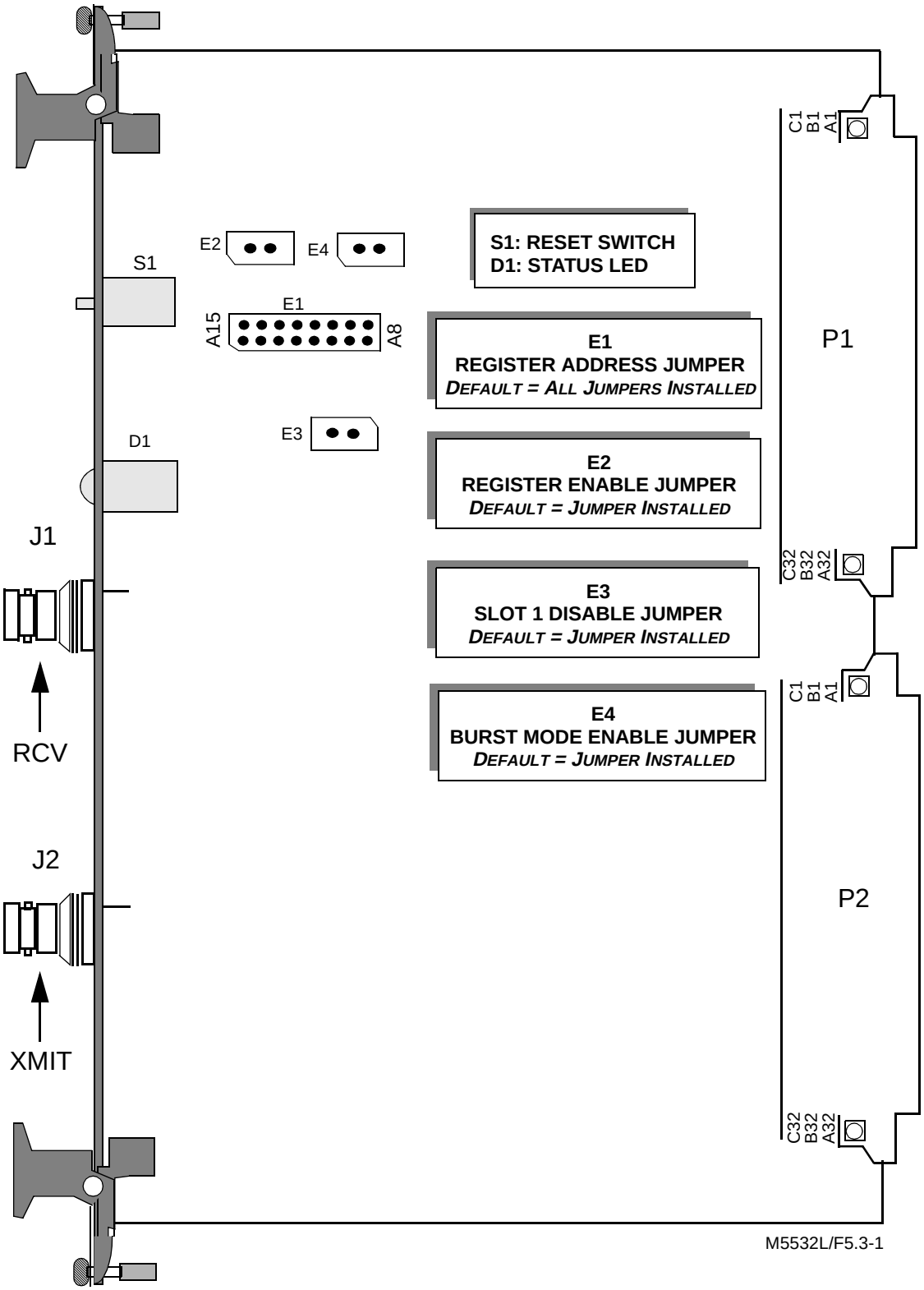


Figure 5.3-1. VMIVME-5532S Location of User-Configurable Jumpers

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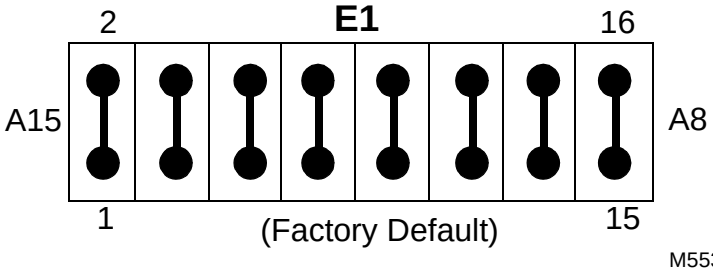


Figure 5.3.4-1. Register Address Jumper (E1)

5.3.5 Burst Mode Enable (E4)

The Burst Mode Enable jumper is used along with the Burst Mode Key register to enable altering of the Burst Mode bit. When this **JUMPER IS OMITTED**, the Burst Mode bit will be cleared to a logical "0" and the host CPU in the master chassis will not be able to alter it (Burst Mode is disabled). When this **JUMPER IS INSTALLED**, the Burst Mode bit can be altered when the Burst Mode Key is enabled (Key = $9DXX). Burst Mode is enabled (Burst Mode bit must be set for burst mode to be active).

NOTE:

JUMPER (E4) DOES NOT SET THE BURST MODE BIT TO A LOGICAL "1" OR "0." IT IS USED AS PART OF AN ENABLING PROCESS WITH THE BURST MODE KEY TO ALLOW THE HOST CPU TO ALTER THE BURST MODE BIT.

5.4 FRONT PANEL RESET SWITCH

A link reset switch located on the front panel of the VMIVME-5532M allows the user to assert SYSRESET* in the slave chassis without resetting the master chassis (or additional slave chassis in a star configuration). See Figure 5.3-1 for location of the switch.

5.5 CABLE INSTALLATION

The Fiber-Optic Repeater Link requires two multimode fiber-optic cables with 62.5 µm core. There must be an ST connector at each end of the cable. Refer to Figure 5.5-1 on page 5-6 for the cable connections.

1. Connect one cable from the VMIVME-5532M board connector (TX) to the VMIVME-5532S connector (RX).

2. Connect the other cable from the VMIVME-5532M board connector (RX) to the VMIVME-5532S connector (TX).

The VMIVME-5532L Repeater Link is ready to use when system power is applied.

NOTE:

THE RUBBER CAPS FOR THE FIBER-OPTIC CONNECTORS ON THE REPEATER BOARDS SHOULD BE ON THE CONNECTORS WHEN THE CABLES ARE NOT CONNECTED TO MINIMIZE CONTAMINATION OF THE FIBER-OPTIC TRANSCEIVERS. ALSO, FOR BEST RESULTS, AVOID SEVERE BENDS AND KINKS OF THE FIBER-OPTIC CABLE.

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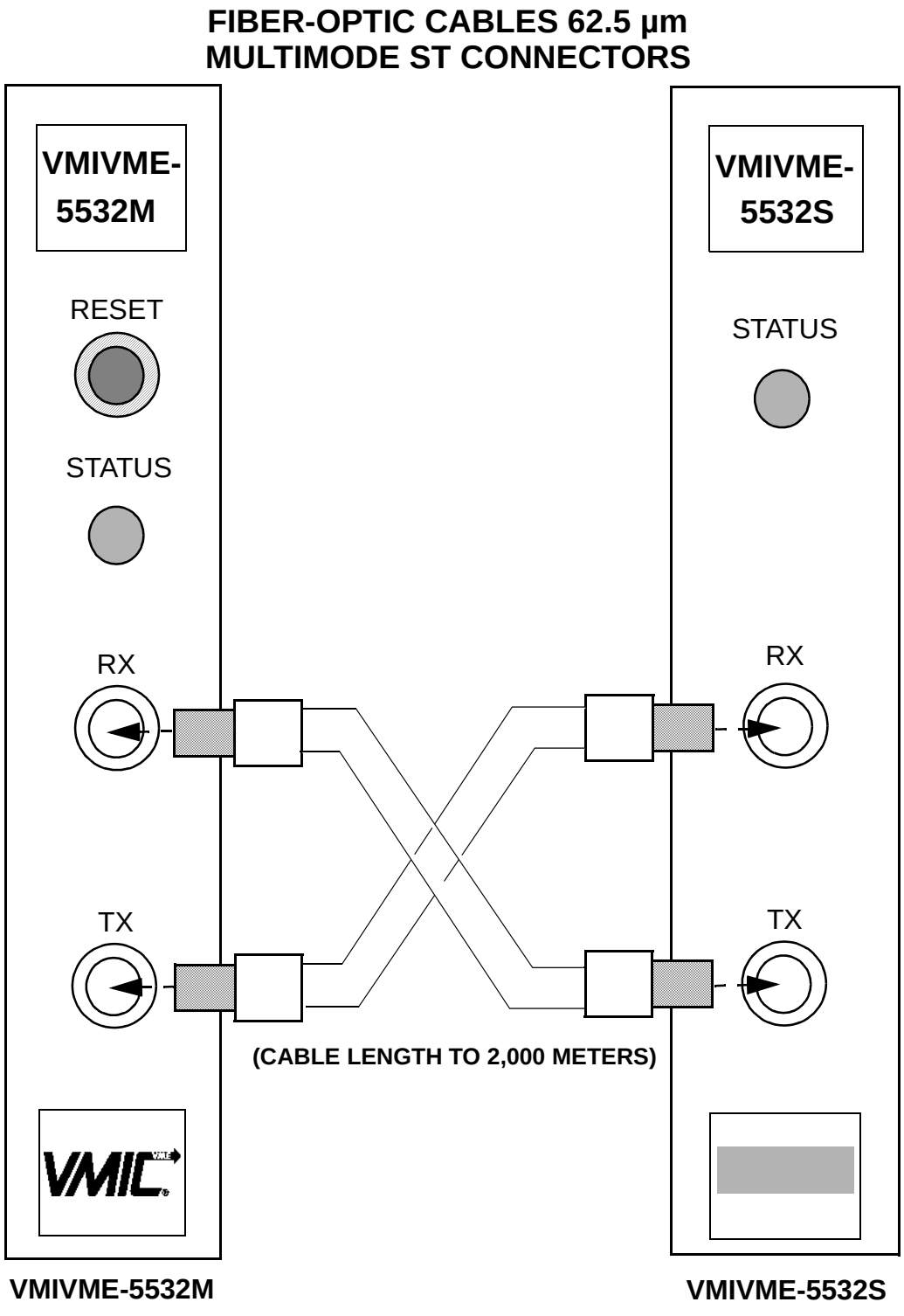


Figure 5.4-1. VMIVME-5532L Cable Connection

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SECTION 6

MAINTENANCE

6.1 MAINTENANCE

This section provides information relative to the care and maintenance of VMIC's products. If the products malfunction, verify the following:

a. Software
b. System configuration
c. Electrical connections
d. Jumper or configuration options
e. Boards are fully inserted into their proper connector location
f. Connector pins are clean and free from contamination
g. No components of adjacent boards are disturbed when inserting or removing the board from the chassis
h. Quality of cables and I/O connections

If products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return**.

6.2 MAINTENANCE PRINTS

User level repairs are not recommended. The appendix to this manual contains drawings and diagrams for reference purposes only.

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APPENDIX A

ASSEMBLY DRAWING, PARTS LIST, AND SCHEMATIC

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