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VMIPMC-5790
PMC Dual-Channel Ultra160 SCSI Host Adapter

Product Manual

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Huntsville, Alabama 35803-3308, USA
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500-755790-000 Rev. B

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Overview

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Introduction

The VMIPMC-5790 is an Dual-Channel Ultra160 SCSI Host Adapter built around the LSI Symbios® SYM53C1010 highly integrated PCI Dual-Channel Ultra160 SCSI controller. The IC is ideal for embedded applications that require high throughput. The VMIPMC-5790 maximizes throughput while minimizing transfer latency and host processor overhead. The host BIOS configures the VMIPMC-5790 as two independent Ultra160 SCSI channels.

The two independent Ultra160 channels support wide Ultra160 SCSI synchronous transfer rates up to 160 Mbyte/s on a Low Voltage Differential (LVD) SCSI bus. Integrated LVDlink™ transceivers support both LVD and single-ended signals with no external transceivers required. Fast SCSI, Ultra SCSI, Ultra2 SCSI, and Ultra160 SCSI are all supported by the VMIPMC-5790. The 8 Kbyte of internal RAM per channel for SCRIPTS™ instruction storage allow all accesses to remain internal, reducing the time spent on the PCI bus. A 944-byte DMA FIFO on each channel allows the VMIPMC-5790 to efficiently burst up to 512 bytes across the PCI bus. SCSI bus phase mismatches are handled in SCRIPTS, reducing CPU utilization.

Ultra160 SCSI Hardware Features:

- 64-bit, 33/66 MHz PCI interface
- No external memory required
- Double transition clocking for 160 Mbyte/s throughput on each channel
- 64-bit addressing supported through Dual Address Cycles (DACs)
- Complaint with PCI 2.2, PCI Power Management 1.1 and PC99
- Cyclic Redundancy Check (CRC)
- Domain validation
- Asynchronous Information Protection (AIP)

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- CRC protects data
- Covers all non-data, including command, status and messages
- High-performance PCI multifunction device
- Represents one electrical load to the PCI bus
- Two independent wide Ultra160 SCSI channels
- SCSI Interrupt Steering Logic (SISL) alternate interrupt routing for RAID applications
- Supports Nextreme ™ RAID

OS Support Ultra160 SCSI:

- WindowsNT and 95/98
- Novell NetWare
- Linux
- Solaris
- UnixWare
- OS/2

Targeted Applications:

- SANs
- Server clustering environments
- Embedded RAID
- Low cost PCI host adapters
- Host motherboards

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Functional Description

The VMIPMC-5790 Dual-Channel Ultra160 SCSI Host Adapter incorporates the Symbios® SYM53C1010, which is a highly integrated PCI Dual-Channel Ultra160 SCSI controller. The SYM53C1010 is 100 percent compatible with the Ultra160 SCSI initiative and provides additional features that ensure robust Ultra160 system operation. Fast SCSI, Ultra SCSI, Ultra2 SCSI and Ultra160 SCSI are all supported by the SYM53C1010. Double transition clocking enables throughput of up to 160 Mbyte/s on each channel for a total of 320 MBps, without increasing the interface clock rate.

The SYM53C1010 uses the same proven CRC algorithm used by FDDI, Ethernet and Fibre Channel, and detects all single bit errors, double bit errors, odd number of errors, and all burst errors up to 32 bits long. To provide complete end-to-end protection of the SCSI I/O, AIP protects all non-data phases, augmenting the CRC feature of Ultra160. SureLINK™ domain validation technology detects the configuration of the SCSI bus and automatically tests and adjusts the SCSI transfer rate to optimize inter-operability. The SYM53C1010 controller and Ultra160 provide Basic (Level 1) and Enhanced (Level 2) domain validation, while the SYM53C1010 has an added feature of Margining (Level 3) domain validation. Figure 1 on page 16 shows the functional block diagram for the SYM53C1010.

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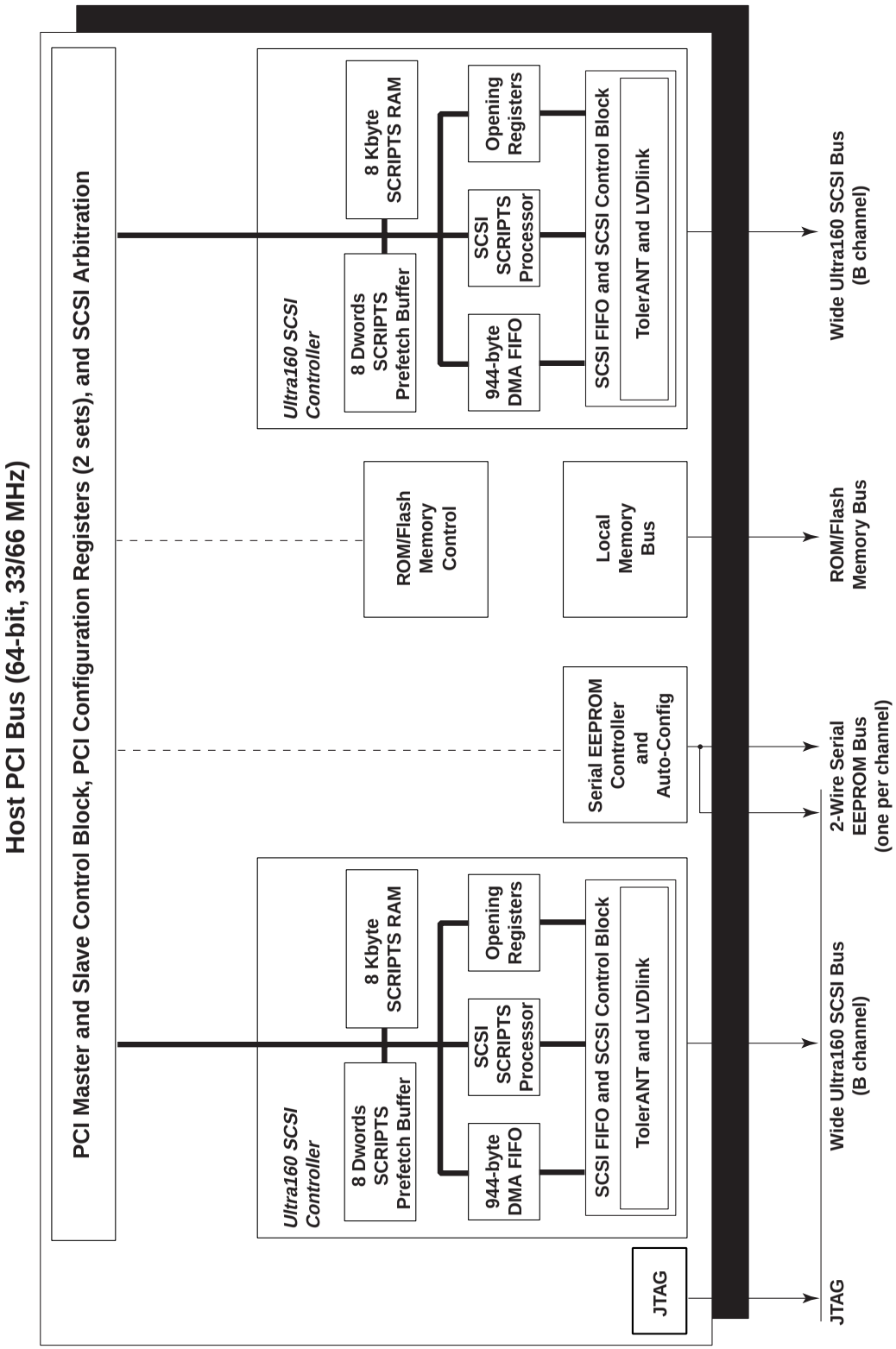


Figure 1 SYM53C1010 Functional Block Diagram

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PCI Interface

The Ultra160 SCSI PCI Interface complies with *PCI Local Bus Specification Revision 2.2*, and implements a 64-bit/66 MHz PCI bus. It is backward compatible with 32-bit/33 MHz buses. The SYM53C1010 is a true PCI multifunction device in that it presents one electrical load to the PCI bus. It uses one REQ/-GNT/ pair to arbitrate for PCI bus mastership, and separate interrupt signals are generated for SCSI Function A and SCSI Function B for maximum performance. The SYM53C1010 complies with *PCI Power Management Interface Specification Revision 1.1* and *PC 99*, supporting power states D0, D1, D2, D3hot and D3cold, power management capabilities registers, and programmable values for PCI Subsystem Vendor ID and Subsystem ID. Extended access cycles (Memory Read Line, Memory Read Multiple, and Memory Write and Invalidate) are also supported.

Ultra160 SCSI Memory

The SYM53C1010 supports up to 1 Mbyte of external expansion ROM through a parallel interface. For ease of software development and field upgrades of the ROM, the interface supports local programming of FLASH memory. A serial 2-wire interface on each SCSI channel provides a connection to an external serial EEPROM for storing the Subsystem Vendor ID and Subsystem ID.

Ultra160 SCSI Processor

The SYM53C1010 provides two independent Ultra160 SCSI controllers on a single chip. Each controller supports wide Ultra160 SCSI synchronous transfer rates up to 160 Mbyte/s on a LVD SCSI bus. Integrated LVDlink™ transceivers support both LVD and single-ended signals with no external transceivers required. Fast SCSI, Ultra SCSI, Ultra2 SCSI and Ultra160 SCSI are all supported by the SYM53C1010. An on-chip SCSI clock quadrupler allows the chip to achieve Ultra160 SCSI transfer rates with an input frequency of 40 MHz. The 8 Kbytes of internal RAM per channel for SCRIPTS instruction storage allow all accesses to remain internal, reducing the time spent on the PCI bus. A 944-byte DMA FIFO on each channel allows the device to efficiently burst up to 512 bytes across the PCI bus. SCSI bus phase mismatches are handled in SCRIPTS, reducing CPU utilization.

Ultra160 SCSI Termination

All SCSI buses require a termination network at each end to function properly. Specific termination requirements differ, depending on which types of SCSI devices are present on the bus. The SCSI Host Adapter uses the UCC5630A termination ICs to automatically sense the SCSI bus and switch the termination to either single ended (SE) or low voltage differential (LVD) SCSI, dependent on which type of devices are connected to the bus. The UCC5630A termination IC is used in multi-mode active termination applications, where single ended (SE) and low voltage differential (LVD) devices might coexist. The UCC5630A has both SE and LVD termination networks integrated into a single monolithic component. The correct network is automatically determined by the SCSI bus “DIFSENS” signal. The SCSI bus DIFSENS signal line is used to identify which types of SCSI devices are present on the bus. On power-up, the UCC5630A DIFSENS drivers will attempt to deliver 1.3V to the DIFSENS line.

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If only LVD devices are present, the DIFSENS line will be successfully driven to 1.3 V and the terminators will configure for LVD operation. If any single ended devices are present, they will present a short to ground on the DIFSENS line, signaling the UCC5630A(s) to configure into the SE mode, accommodating the SE devices. Or, if any high voltage differential (HVD) devices are present, the DIFSENS line is pulled high and the terminator will enter a high impedance state, effectively disconnecting from the bus. Header E1 pins 3 & 4 enables automatic termination on the SCSI Host Adapter to disable the termination remove the shorting strap.

Media Connection

The VMIPMC-5790 supports dual 68-pin VHDCI external connectors.

Software Drivers

To optimize performance of this PCI-based adapter card, the VMIPMC-5790 is available with software drivers compatible with the Windows NT operating system.

The software drivers for the VMIPMC-5790 are available through the VMIC website (see web address below). After downloading the driver of choice, go to the readme.txt file for instructions on how to load the driver.

VMIC website: www.vmicnet.com

For drivers that are not available on the website, contact VMIC Customer Service.

VMIC Customer Service is available at: 1-800-240-7782.
Or E-mail VMIC at customer.service@vmic.com

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Reference Material List

Refer to PCI Local Bus Specification for a detailed explanation of the PCI Local bus. The *PCI Local bus Specification* is available from the following source:

PCI Special Interest Group
P.O. Box 14070
Portland, OR 97214
U.S.: (800) 433-5177
International: (503) 797-4207
FAX: (503) 234-6762

For a detailed explanation of SCSI, refer to *'Basics of SCSI' Fourth Edition*.

Ancot Corporation
115 Constitution Dr.
Mento Park, CA 94025
(650) 322-5322
fax (650) 322-0455

For a detailed explanation of the SYM5301010 Dual Channel Ultra3 SCSI Controller refer to *'Symbios® SYM53C1010 PCI to Dual Channel Ultra3 SCSI Multifunction Controller'*.

Document DB14-000083-000, First Edition Version 1.0

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1551 McCarthy Blvd.
Milpitas, CA 95035
800.433.8778 (in the United States)
408.433.8000 (outside the United States)
Fax 408.433.8989

For a detailed explanation of the UNITRODE UCC5630A Multimode SCSI 9 Line Terminator, refer to: '*UCC5630A Data Sheet'*, Document Number: SLUS322A.

UNITRODE Corporation
7 Continental Blvd.
Merrimack, NH 03054
(603) 424-2410
FAX (603) 424-3460

Physical Description and Specifications

Refer to Product Specification, 800-855790-000 available from:

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Safety Summary

The following general safety precautions must be observed during all phases of the operation, service and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture and intended use of this product.

VMIC assumes no liability for the customer's failure to comply with these requirements.

Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VMIC for service and repair to ensure that safety features are maintained.

Dangerous Procedure Warnings

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

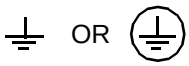
STOP: Dangerous voltages, capable of causing death, are present in this system. Use extreme caution when handling, testing, and adjusting.

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Safety Symbols Used in This Manual



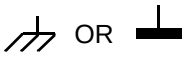
Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 V are so marked).



Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.



Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. Before operating the equipment, terminal marked with this symbol must be connected to ground in the manner described in the installation (operation) manual.



Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.



Alternating current (power line).



Direct current (power line).



Alternating or direct current (power line).

STOP: This symbol informs the operator that a practice or procedure should not be performed. Actions could result in injury or death to personnel, or could result in damage to or destruction of part or all of the system.

WARNING: This sign denotes a hazard. It calls attention to a procedure, a practice or a condition, which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION: This sign denotes a hazard. It calls attention to an operating procedure, a practice or a condition, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE: Calls attention to a procedure, a practice, a condition or the like, which is essential to highlight.

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CHAPTER 1

Theory of Operation

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Introduction

The VMIPMC-5790 is a PMC Dual-Channel Ultra160 SCSI Host Adapter that provides the host system with complete SCSI command and data transport capabilities, thus freeing the host system from the simultaneous execution of SCSI traffic. This chapter provides a description of the registers in the SYM53C1010 PCI to Dual Channel Ultra3 SCSI Multifunction Controller chip.

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PCI Addressing

There are three types of PCI-defined address spaces:

- Configuration space
- Memory space
- I/O space

Configuration space is a contiguous 256 x 8-bit set of addresses dedicated to each “slot” or “stub” on the bus. The Ultra160 SCSI contains two sets of configuration registers, one for each channel. Each SCSI function contains the same register set with identical default values except for the Interrupt Pin. The BIOS uses this configuration space to initialize the VMIPMC-5790. Decoding C_BE[7:0]/ determines if a PCI cycle is intended to access configuration register space. The IDSEL bus signal is a “chip select” that allows access to the configuration register space only. A configuration read/write cycle without IDSEL will be ignored. The eight lower order addresses are used to select a specific 8-bit register. According to the PCI specification, since AD[10:8] are to be used for multifunction devices bits AD[10:8] decode either SCSI Function A Configuration register (AD[10:8] = 0b000) or SCSI Function B Configuration register (AD[10:8] = 0b001). At initialization time, each PCI device is assigned a base address for memory accesses and I/O accesses. On every access, the VMIPMC-5790 compares its assigned base addresses with the value on the Address/Data bus during the PCI address phase. A decode of C_BE[7:0]/ determines which registers and what type of access is to be performed.

PCI Bus Commands Supported

Bus Commands indicate to the target the type of transaction the master is requesting. Bus Commands are encoded on the C_BE[7:0]/ lines during the address phase. PCI Bus Command encoding and types appear in Table 1-1 on page 25.

The Memory Read and Memory Read Multiple commands are used to read data from an agent mapped in memory address space. All 64 address bits are decoded.

The Memory Write, and Memory Write and Invalidate commands are used to write data to an agent when mapped in memory address space. All 64 address bits are decoded.

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Table 1-1 PCI bus Commands and Encoding Types

C_BE[3:0]	Command Type	Supported as Master	Supported as Slave
0000	Special Interrupt Acknowledge	No	No
0001	Special Cycle	No	No
0010	I/O Read Cycle	Yes	Yes
0011	I/O Write Cycle	Yes	Yes
0100 and 0101	Reserved	N/A	N/A
0110	Memory Read	Yes	Yes
0111	Memory Write	Yes	Yes
1000 and 1001	Reserved	N/A	N/A
1010	Configuration Read	No	Yes
1011	Configuration Write	No	Yes
1100	Memory Read Multiple	Yes	Yes
1101	Dual Address Cycle	Yes	Yes
1110	Memory Read Line	Yes	Yes
1111	Memory Write and Invalidate	Yes	Yes

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PCI Bus Configuration Registers

The Configuration registers are accessible only by the system BIOS during PCI configuration cycles, and are not available to the user at any time. No other cycles can access these registers.

NOTE: The Configuration register descriptions, which provide general information only, indicate which PCI configuration addresses are supported in the SYM53C1010 controller. Table 1-2 below shows the PCI Configuration registers implemented by the VMIPMC-5790. Addresses $48 through $7F are not defined.

Note the following:

- Register bits are set to one (1) and reset or cleared to zero (0) unless otherwise noted. A reset value of X indicates an indeterminate value.
- Reserved bits are reset to zero (0) unless otherwise noted. Register bits allow read and write access unless otherwise noted.

Table 1-2 PCI Configuration Register Map

31	16	15	0	
Device ID		Vendor ID		$00
Status		Command		$04
Class Code			Revision ID	$08
BIST	Head Type	Latency Timer	Cache Line Size	$0C
I/O Base Address				$10
Mem0 Base Address Low				$14
Mem0 Base Address High				$18
Mem1 Base Address Low				$1C
Mem1 Base Address High				$20
Reserved				$24
Reserved				$28
Subsystem ID (SID)		Subsystem Vendor ID (SVID)		$2C
Expansion ROM Base Address				$30
Reserved			Capabilities Pointer	$34
Reserved				$38
Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	$3C
Power Management Capabilities		Next Item Pointer	Capability ID	$40
Data	Bridge Support Extensions	Power Management Control/Status		$44
Reserved				$48 - $7F

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PCI Vendor ID Register

This 16-bit register identifies the manufacturer of the SCSI chip, and also contains the hardwired value of $1000 for SCSI. This register is accessed by the system software to identify the SYM53C1010 on the PCI bus. The register bits are shown in Table 1-3.

Table 1-3 PCI SCSI Vendor ID (VID) Register Bit Map

Ultra160 SCSI: Configuration Address Space $00 (R)		
Bit	**Name**	**Reset Value**
15 through 0	PCI Vendor ID	$1000

PCI Device ID Register

This 16-bit register identifies the particular device. This register contains the hardwired value of $0020. The system software accesses this register to identify the SYM53C1010 on the PCI bus. The register bits are shown in Table 1-4.

Table 1-4 PCI SCSI Device ID (DID) Register Bit Map

Ultra160 SCSI: Configuration Address Space $02 (R)		
Bit	**Name**	**Reset Value**
15 through 0	PCI Device ID	$0020

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PCI Status/Command Register

The most significant half of the Status / Command register is used to record status information for PCI bus-related events. Reads to this register behave normally. Writes are slightly different in that bits can be cleared, but not set. A bit is reset whenever the register is written, and the data in the corresponding bit location is a one (1). For instance, to clear Bit 31 and not affect any other bits, write the value $8000 to the register.

The least significant half of the Status / Command register provides coarse control over a device's ability to generate and respond to PCI cycles. When a zero is written to this register, the VMIPMC-5790 is logically disconnected from the PCI bus for all accesses except configuration accesses.

Table 1-5 PCI Status/Command Register Bit Map

Status/Command: Offset $04, Read/Write							
Bit 31	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
DPE	SSE	MA	RTA	Reserved	DevSel / Tim		DPR
Bit 23	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
Reserved							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
Reserved							SERR
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
Reserved	EPER	Reserved	WIM	Reserved	EBM	EMS	EIOS

PCI Status/Command Register Bit Definitions

Bit 31: **Detected Parity Error (DPE) -** This bit will be set by the VMIPMC-5790 whenever it detects a data parity error, even if parity error handling is disabled.

Bit 30: **Signal System Error (SSE)** - This read / write bit is set whenever a device asserts the SERR / signal.

Bit 29: **Master Abort (MA)** - This read / write bit should be set by a master device whenever its transaction (except for Special Cycle) is terminated with master abort. All master devices should implement this bit.

Bit 28: **Received Target Abort (RTA)** - This read / write bit should be set by a master device whenever its transaction is terminated with a target abort. All master devices should implement this bit.

Bit 27: **Reserved** - Reserved for future use.

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PCI Status/Command Register Bit Definitions (Continued)

Bits 26 and 25: **DevSel/Timing (DevSel/Tim)** - These read / write bits encode the timing of DevSel/. They are encoded as follows:

0b00	Fast
0b01	Medium
0b10	Slow
0b11	Reserved

Bit 24: **Data Parity Reported (DPR)** - This read / write bit is set when the following conditions are met:

1. The bus agent asserted PERR itself or observed PERR/ asserted.
2. The agent setting this bit acted as the bus master for the operation in which the error occurred.
3. The Parity Error Response bit in the Command register is set.

Bits 23 through 09: **Reserved** - Reserved for future use.

Bit 08: **SERR/Enable (SERR)** - This read / write bit enables the SERR/ driver. SERR/ is disabled when this bit is clear. The default value of this bit is zero (0). This bit and Bit 6 must be set to report address parity errors.

Bit 07: **Reserved** - Reserved for future use.

Bit 06: **Enable Parity Error Response (EPER)** - This read / write bit allows the VMIPMC-5790 to detect parity errors on the PCI bus and report these errors to the system. Only data parity checking is enabled. The SYM53C1010 will always generate parity errors for the PCI bus.

Bit 05: **Reserved** - Reserved for future use.

Bit 04: **Write and Invalidate Mode (WIM)** - This read / write bit, when set, will cause Memory Write and Invalidate cycles to be issued on the PCI bus after certain conditions have been met.

Bit 03: **Reserved** - Reserved for future use.

Bit 02: **Enable Bus Mastering** - This read / write bit controls the VMIPMC-5790's ability to act as a master on the PCI bus. A value of zero (0) disables the device from generating PCI bus master accesses. A value of one (1) allows the VMIPMC-5790 to behave as a bus master.

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PCI Status/Command Register Bit Definitions (Continued)

Bit 01: **Enable Memory Space** - This read / write bit controls the VMIPMC-5790 response to Memory Space accesses. A value of zero (0) disables the device response. A value of one (1) allows the VMIPMC-5790 to respond to Memory Space accesses at the address specified by Base Address One.

Bit 00: **Enable I/O Space** - This read-only bit controls the VMIPMC-5790 response to I / O Space accesses. A value of zero (0) disables the device response. A value of one (1) allows the VMIPMC-5790 to respond to I / O Space accesses at the address specified by Base Address Zero.

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PCI Class Code/Revision ID Register ($08)

Table 1-6 PCI Class Code/Revision ID Register Bit Map

Class Code/Revision ID: Offset $08, Read/Write							
Bit 31	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
CLCode (Most Significant)							
Bit 23	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
CLCode (Most Significant)							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
CLCode (Least Significant)							
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
RevID							

PCI Class Code/Revision ID Register Bit Definitions

Bits 31 through 08: **Class Code (CLCode)** - These read-only bits are used to identify the generic function of the device. The upper byte of this register is a base class code, the middle byte is a subclass code, and the lower byte identifies a specific register level programming interface. The value defaults to $010000 for Ultra160 SCSI unless firmware programs it to a different value prior to PCI configuration, or it gets changed using a serial EEPROM. This default value indicates that this is an I_2O compliant device.

Bits 07 through 00: **Revision ID (RevID)** - These read-only bits specify device and revision identifiers.

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PCI BIST/Header/Latency/Cache Line Size Register ($0C)

Table 1-7 PCI BIST/Header/Latency/Cache Line Size Register Bit Map

BIST/Header/Latency/Cache Line Size: Offset $0C, Read/Write							
Bit 31	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
BIST							
Bit 23	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
HdTyp							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
LatTim							
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
Cache							

PCI BIST/Header/Latency/Cache Line Size Register Bit Definitions

Bits 31 through 24: **Built-In Self Test (BIST)** - Read-only.

Bits 23 through 16: **Header Type (HdTyp)** - These read-only bits identify the layout of bytes $10 through $3F in configuration space and also whether or not the device contains multiple functions. The value of this register is $80 for Ultra160 SCSI.

Bits 15 through 08: **Latency Timer (LatTim)** - The Latency Timer are read / write bits that specify, in units of PCI bus clocks, the value of the Latency Timer for this PCI bus master. The VMIPMC-5790 supports this timer. All eight bits are writable, allowing latency values of 0-255 PCI clocks. Use the following equation to calculate an optimum latency value for the VMIPMC-5790:

Latency = 2 + (Burst Size * (typical wait states + 1)).

Values greater than optimum are also acceptable.

Bits 07 through 00: **Cache Line Size (Cache)** - This read / write register specifies the system cache line size in units of 32-bit words. Cache mode is enabled and disabled by the Cache Line Size Enable (CLSE) bit, Bit 7 in the DCNTL register. Setting this bit causes the VMIPMC-5790 to align to cache line boundaries before allowing any bursting, except during Memory Moves in which the read and write addresses are not aligned to a burst size boundary.

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PCI I/O Base Address Register ($10)

Table 1-8 I/O Base Address Register Bit Map

I/O Base Address Register: Offset $10, Read/Write							
Bit 31	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
IOBAdd (Most Significant)							
Bit 23	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
IOBAdd (Most Significant)							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
IOBAdd (Least Significant)							
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
Reserved							IOMemSp

NOTE: This register is only 32 bits, because I/O must be mapped into the lower 4 Gbytes of address space.

PCI I/O Base Address Register Bit Definitions

Bits 31 through 08: **I/O Base Address (IOBAdd)** - Indicates location of I/O space required by the device and is fixed at a size of 256 bytes.

Bits 07 through 01: **Reserved** - Reserved for future use.

Bit 00: **I/O or Memory Space Indicator** - This read-only bit is set to one (1) to indicate I/O space mapping.

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PCI Mem0 Base Address Low Register ($14)

Table 1-9 Mem0 Base Address Low Register Bit Map

Mem0 Base Address Low: Offset $14, Read/Write							
Bit 31	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
Mem0BAddL (Most Significant)							
Bit 23	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
Mem0BAddL (Most Significant)							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
Mem0BAddL (Least Significant)							
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
Mem0BaddL (Least Significant)				Prefetch	Type		IOMemSp

PCI Mem0 Base Address Low Register Bit Definitions

Bits 31 through 04: **Mem0 Base Address Low (Mem0BaddL)** - Indicates lower 32 bits of the 64-bit memory address width, and the location of memory required by the device. Its size is programmable from 16 Kbytes (2^{14}) through 512 Kbytes (2^{19}) in steps of powers of 2 (based on bits [27:24] of the PCI Config0 register). The default value indicated is 64 Kbytes, unless firmware programs a different value prior to PCI configuration, or if programmed with the serial EEPROM.

Bit 03: **Prefetchable Memory Block (Prefetch)** - With this bit set, there are no side effects to prefetching. For reads, all bytes can be sent regardless of the state of the byte enables. For writes, sequential writes can be combined into a burst.

Bits 02 and 01: **Location of Memory (Type)** - When Bit 2 = 1 and Bit 1 = 0, the user can map this device anywhere in the 64-bit space.

Bit 00: **I/O or Memory Space Indicator (IOMemSp)** - This bit is set to zero (0) to indicate Memory Space mapping.

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PCI Mem0 Base Address High Register ($18)

Table 1-10 Mem0 Base Address High Register Bit Map

Mem0 Base Address High: Offset $18, Read/Write							
Bit 31	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
Mem0BAddH (Most Significant)							
Bit 23	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
Mem0BAddH (Most Significant)							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
Mem0BAddH (Least Significant)							
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
Mem0BaddH (Least Significant)							

PCI Mem0 Base Address High Register Bit Definitions

Bits 31 through 00: **Mem0 Base Address High (Mem0BaddH)** - Indicates upper 32 bits of the 64-bit memory address width, and the location of memory required by the device. This allows the VMIPMC-5790 to be mapped above the 4 Gbyte boundary.

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PCI Subsystem Vendor ID (SVID: $2C and $2D)

Table 1-11 Subsystem Vendor ID Register Bit Map

Subsystem Vendor ID Register: Offsets $2C and $2D, Read-Only							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
SVID (If MAD7 is HIGH)							
0	0	0	1	0	0	0	0

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
SVID (If MAD7 is HIGH)							
0	0	0	0	0	0	0	0

Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
SVID (If MAD7 is LOW)							
X	X	X	X	X	X	X	X

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
SVID (If MAD7 is LOW)							
X	X	X	X	X	X	X	X

PCI Subsystem Vendor ID Register Bit Definitions

Bits 15 through 00:

Subsystem Vendor ID - This 16-bit register is used to uniquely identify the vendor manufacturing the add-in board or subsystem where this PCI device resides. It provides a mechanism for an add-in card vendor to distinguish its card from another vendor's cards, even if the cards have the same PCI controller installed on them (and therefore the same Vendor ID and Device ID).

If the external serial EEPROM interface is enabled (MAD[7] LOW), this register is automatically loaded at power up from the external serial EEPROM and will contain the value downloaded from the serial EEPROM or a value of $0000 if the download fails.

If the external serial EEPROM interface is disabled (MAD[7] HIGH), this register returns a value of $1000. The 16 bit value stored in the vendor's PCI Vendor ID register must be obtained from the PCI Special Interest Group (SIG). See the '*Reference Material List*' on Page 17.

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PCI Subsystem ID (SID: $2E and $2F)

Table 1-12 Subsystem ID Register Bit Map

Subsystem ID Register: Offsets $2E and $2F, Read-Only							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
SID (If MAD7 is HIGH)							
0	0	0	1	0	0	0	0
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
SID (If MAD7 is HIGH)							
0	0	0	0	0	0	0	0
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
SID (If MAD7 is LOW)							
X	X	X	X	X	X	X	X
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
SID (If MAD7 is LOW)							
X	X	X	X	X	X	X	X

PCI Subsystem ID Register Bit Definitions

Bits 15 through 00:

Subsystem ID - This 16-bit register is used to uniquely identify the vendor manufacturing the add-in board or subsystem where this PCI device resides. It provides a mechanism for an add-in card vendor to distinguish its card from another vendor's cards, even if the cards have the same PCI controller installed on them (and therefore the same Vendor ID and Device ID).

If the external serial EEPROM interface is enabled (MAD[7] LOW), this register is automatically loaded at power up from the external serial EEPROM and will contain the value downloaded from the serial EEPROM or a value of $0000 if the download fails.

If the external serial EEPROM interface is disabled (MAD[7] HIGH), this register returns a value of $1000. The 16 bit value stored in the vendor's PCI Vendor ID register must be obtained from the PCI Special Interest Group (SIG). See the '*Reference Material List*' on Page 17.

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PCI Expansion ROM Base Address ($30)

Table 1-13 Expansion ROM Base Address Register Bit Map

Expansion ROM Base Address: Offset $30, Read/Write							
Bit 31	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
ExpROMBAdd (Most Significant)							
Bit 23	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
ExpROMBAdd (Most Significant)							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
ExpROMBAdd (Least Significant)				Reserved			

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
Reserved							ExpROMEn

PCI Expansion ROM Base Address Bit Definitions

Bits 31 through 11: **Expansion ROM Base Address (ExpROMBadd)** - indicates location of Expansion ROM device and is programmable from 256 Kbytes (2^{18}) through 1 Mbyte (2^{20}) in steps of powers of 2 (using the ROMSIZE[1:0] input bus).

Bits 10 through 01: **Reserved** - Reserved for future use.

Bit 00: **Expansion ROM Enable (ExpROMEn)** - Memory access must be enabled using the MemSpace bit in the Command register, unless ROMSIZE[1:0] = 11 (in which case there is no Expansion ROM).

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PCI Capability Pointer Register ($34)

Table 1-14 Capability Pointer Register Bit Map

Capability Pointer: Offset $34, Read-Only							
Bit 31	**Bit 30**	**Bit 29**	**Bit 28**	**Bit 27**	**Bit 26**	**Bit 25**	**Bit 24**
Reserved							
Bit 23	**Bit 22**	**Bit 21**	**Bit 20**	**Bit 19**	**Bit 18**	**Bit 17**	**Bit 16**
Reserved							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
Reserved							
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
CapPtr							

PCI Capability Pointer Register Bit Definitions

Bits 31 through 08: **Reserved** - These read-only bits are reserved for future use.

Bits 07 through 00: **Capabilities Pointer (CapPtr)** - These read-only bits indicate that the first Extended Capability register is located at offset $40 in the PCI Configuration registers.

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PCI Interrupt Line Register (IL: $3C)

Table 1-15 Interrupt Line Register Bit Map

Latency/Interrupt Register: Offset $3C, Read/Write							
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
IL							

PCI Interrupt Line Register Bit Definitions

Bits 07 through 00: **Interrupt Line** - This register is used to communicate interrupt line routing information. POST software writes the routing information into this register as it configures the system. The value in this register identifies which input of the system interrupt controller(s) the device's interrupt pin is connected to. Values in this register are specified by system architecture.

PCI Interrupt Pin Register (IP: $3D)

Table 1-16 Interrupt Pin Register Bit Map

Interrupt Pin Register: Offset $3D, Read-Only							
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
IP (SCSI Function A)							
0	0	0	0	0	0	0	1

IP (SCSI Function B if MAD[4] is pulled LOW							
0	0	0	0	0	0	1	0

IP (SCSI Function B if MAD[4] is pulled HIGH)							
0	0	0	0	0	0	0	1

PCI Interrupt Pin Register Bit Definitions

Bits 07 through 00: **Interrupt Pin** - This register is unique to each SCSI function. It identifies which interrupt pin the device uses. Its value is set to $01 for the Function A (INTA /) signal, and $02 for the Function B (INTB /) signal at power up MAD[4] is pulled LOW. The Function B value is set to $02 (INTA /) if MAD[4] is pulled HIGH.

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PCI Capability ID Register ($40)

Table 1-17 Capability ID Register Bit Map

Capability ID Register: Offset $40, Read-Only							
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
CID							

PCI Capability ID Register Bit Definitions

Bits 07 through 00: **Capability ID (CID)** - This register indicates the type of data structure currently being used. A value of $01 indicates the Power Management Data Structure.

PCI Next Item Pointer Register ($41)

Table 1-18 Next Item Pointer Register Bit Map

Next Item Pointer Register: Offset $41, Read-Only							
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
NIP							

PCI Next Item Pointer Register Bit Definitions

Bits 07 through 00: **Next Item Pointer (NIP)** - Bits[7:0] contain the offset location of the next item in the function's capabilities list. Default value is $00.

PCI Power Management Capabilities Register ($42 and $43)

Table 1-19 Power Management Capabilities Register Bit Map

Power Management Capabilities Register: Offsets $42 and $43, Read-Only							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
PMES					D2S	D1S	AUXC

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
AUXC		DSI	APS	PMEC	VER[2:0]		

PCI Power Management Capabilities Register Bit Definitions

Bits 15 through 11: **PME_Support (PMES)** - Bits[15:11] define the power management states in which the VMIPMC-5790 will assert the PME pin. These bits are all set to zero (0) because the VMIPMC-5790 does not provide a PME signal.

Bit 10: **D2_Support (D2S)** - The VMIPMC-5790 sets this bit to indicate support for power management state D2. Bits 9 and 10 are set to one (1), indicating support for the D2 and D1 power states.

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PCI Power Management Capabilities Register Bit Definitions (Continued)

Bit 09: **D1_Support (D1S)** - The VMIPMC-5790 sets this bit to indicate support for power management state D1. Bits 9 and 10 are set to one (1), indicating support for the D2 and D1 power states.

Bits 08 through 06: **Aux_Current (AUXC)** - The VMIPMC-5790 will always return zero (0). This feature is not supported.

Bit 05: **Device Specific Initialization (DSI)** - This bit is cleared to indicate that the VMIPMC-5790 requires no special initialization before the generic class device driver is able to use it.

Bit 04: **Aux_Power Source (APS)** - This bit is set to zero to indicate the VMIPMC-5790 does not require an auxiliary power source.

Bit 03: **PME Clock (PMEC)** - Bit 03 is cleared because the VMIPMC-5790 does not provide a PME pin.

Bits 02 through 00: **Version (VER[2:0])** - These three bits are set to 0b010 to indicate that the VMIPMC-5790 complies with Revision 1.1 of the PCI Power Management Interface Specification.

PCI Power Management Control/Status Register ($44 and $45)

Table 1-20 Power Management Control/Status Register Bit Map

Power Management Control/Status Register: Offsets $44 and $45, Read/Write							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
PST	DSCL		DSLT				PEN

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
Reserved						PWS[1:0]	

PCI Power Management Control/Status Register Bit Definitions

Bit 15: **PME_Status (PMES)** - The VMIPMC-5790 always returns a zero for this bit, indicating that PME signal generation is not supported from D3cold.

Bits 14 and 13: **Data_Scale (DSCL)** - The VMIPMC-5790 does not support the data register. Therefore, these two bits are always cleared.

Bits 12 through 09: **Data_Select (DSLT)** - The VMIPMC-5790 does not support the data register. Therefore, these four bits are always cleared.

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PCI Power Management Control/Status Register Bit Definitions (Continued)

Bit 08: **PME_Enable (PEN)** - The VMIPMC-5790 always returns a zero (0) for this bit to indicate that PME assertion is disabled.

Bits 07 through 02: **Reserved** - These bits are reserved for future use.

Bits 01 and 00: **Power State (PWS[1:0])** - Bits[1:0] are used to determine the current power state of the VMIPMC-5790. They are used to place the VMIPMC-5790 in a new power state. Power states are defined as:

0b00	D0
0b01	D1
0b10	D2
0b11	D3 hot

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SCSI Interface Registers

The control registers for the SCSI core are directly accessible from the PCI bus using Memory or I/O mapping. SCSI Function A and SCSI Function B contain the same register set with identical default values, except the Interrupt Pin registers. The address map of the SCSI registers is shown in Table 1-21 starting below.

The eight, 32-bit, phase mismatch registers contain the byte count and addressing information required to update the Direct, Indirect or Table.

The phase mismatch registers are:

- Phase Mismatch Jump Address One (PMJAD1)
- Phase Mismatch Jump Address Two (PMJAD2)
- Remaining Byte Count (RBC)
- Updated Address (UA)
- Entry Storage Address (ESA)
- Instruction Address (IA)
- SCSI Byte Count (SBC)
- Cumulative SCSI Byte Count (CSBC)
- Indirect BMOV instructions with new byte counts and addresses

All the phase mismatch registers can be read / written using the Load and Store SCRIPTS instructions, or the CPU with SCRIPTS not running.

NOTE: The only registers that the host CPU can access while the SYM53C1010 is executing SCRIPTS are the Interrupt Status Zero (ISTAT0), Interrupt Status One (ISTAT1), Mailbox Zero (MBOX0), and Mailbox One (MBOX1) registers. Attempts to access the other registers will interfere with the operation of the chip. However, all operating registers are accessible with SCRIPTS. All read data is synchronized and stable when presented to the PCI bus.

NOTE: Do not access reserved bits.

Table 1-21 SCSI Register Map

31 16	15 0			Address
SCNTL3	SCNTL2	SCNTL1	SCNTL0	$00
GPREG	SDID	SXFER	SCID	$04
SBCL	SSID	SOCL	SFBR	$08
SSTAT2	SSTAT1	SSTAT0	DSTAT	$0C
DSA				$10 - $13
MBOX1	MBOX0	ISTAT1	ISTAT0	$14
CTEST3	CTEST2	CTEST1	CTEST0	$18
TEMP				$1C - $1F
CTEST6	CTEST5	CTEST4	Reserved	$20
DCMD	DBC			$24 - $26
DNAD				$28 - $2B

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Table 1-21 SCSI Register Map (Continued)

31	16 15		0	Address
DSP				$2C - $2F
DSPS				$30 - $33
SCRATCH A				$34 - $37
DCNTL	SBR	DIEN	DMODE	$38
ADDER				$3C - $3F
SIST1	SIST0	SIEN1	SIEN0	$40
GPCNTL	Reserved	SWIDE	Reserved	$44
RESPID1	RESPID0	STIME1	STIME0	$48
STEST3	STEST2	STEST1	STEST0	$4C
CSO	STEST4	SIDL		$50 - $51
CCNTL1	CCNTL0	SODL		$54 - $55
CCNTL3	Reserved	SBDL		$58 - $59
SCRATCH B				$5C - $5F
SCRATCH C - SCRATCH R				$60 - $9F
MMRS				$A0 - $A3
MMWS				$A4 - $A7
SFS				$A8 - $AB
DRS				$AC - $AF
SBMS				$B0 - $B3
DBMS				$B4 - $B7
DNAD64				$B8 - $BB
AIPCNTL1	AICNTL0	Reserved	SCNTL4	$BC
PMJAD1				$C0 - $C3
PMJAD2				$C4 - $C7
RBC				$C8 - $CB
UA				$CC - $CF
ESA				$D0 - $D3
IA				$D4 - $D7
Reserved	SBC			$D8 - $DA
CSBC				$DC - $DF
CRCCNTL1	CRCCNTL0	CRCPAD		$E0 - $E1
CRCD				$E4 - $E7
Reserved				$E8 - $EF
Reserved		DFBC		$F0 - $F1
Reserved				$F4 - FF

NOTE: Refer to document DB14-000083-00 First Edition from LSI Corp. for detailed explanation of each individual SCSI register.

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CHAPTER 2

Configuration and Installation

Contents

Unpacking Procedures 48
Physical Installation. 49
Cable Configuration 51

Introduction

This chapter describes the installation and configuration of the board. Cable configuration and board layout are illustrated in this chapter.

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Unpacking Procedures

CAUTION: Some of the components assembled on VMIC's products may be sensitive to electrostatic discharge and damage may occur on boards that are subjected to a high-energy electrostatic field. When the board is placed on a bench for configuring, etc., it is suggested that conductive material should be inserted under the board to provide a conductive shunt. Unused boards should be stored in the same protective boxes in which they were shipped.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice concerning the disposition of the damaged item(s).

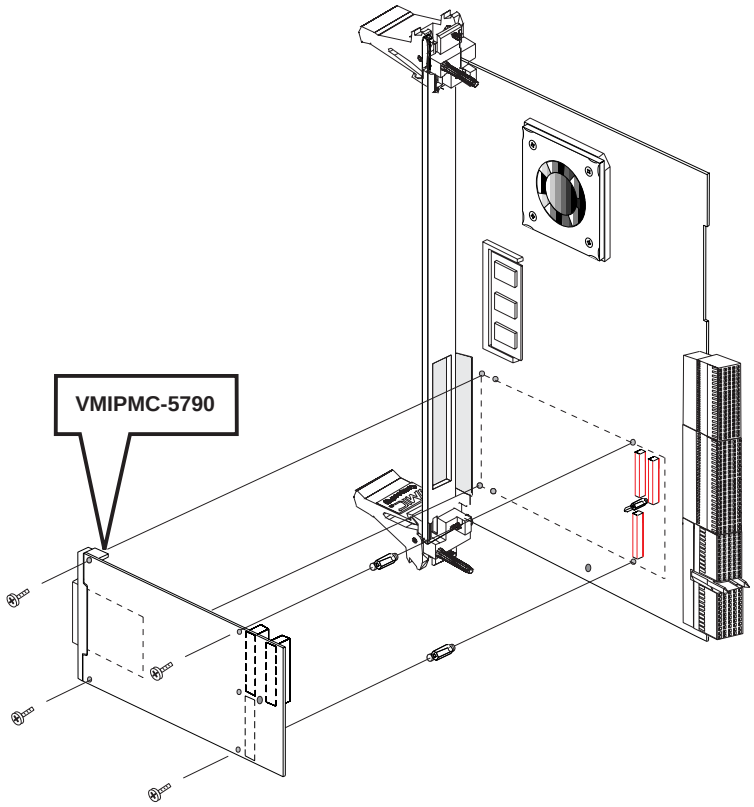
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Physical Installation

CAUTION: Do not install or remove the board while power is applied.

Host systems containing PMC sites vary widely in appearance and board installation procedures. VMIC recommends examining the host system installation procedures prior to installing this board. The following procedure outlines the installation of the VMIPMC-5790 onto a suitable PCI bus motherboard with an available PMC site.

1. Remove the motherboard from the chassis.
2. Install the VMIPMC-5790 firmly onto the PMC connectors (refer to Figure 2-1 for installation of the VMIPMC-5790). Install the screws to secure the VMIPMC-5790 to the motherboard (see Figure 2-2 on page 50).
3. Re-install the motherboard in the chassis, apply power.



NOTE: The VMIPMC-5790 is designed to interface with any suitable PCI compliant motherboard using a direct PCI bus interface, compliant with v2.2 of the PCI signalling specification as defined by *IEEE P1386.1 Draft 2.0.*

Figure 2-1 Installing the VMIPMC-5790

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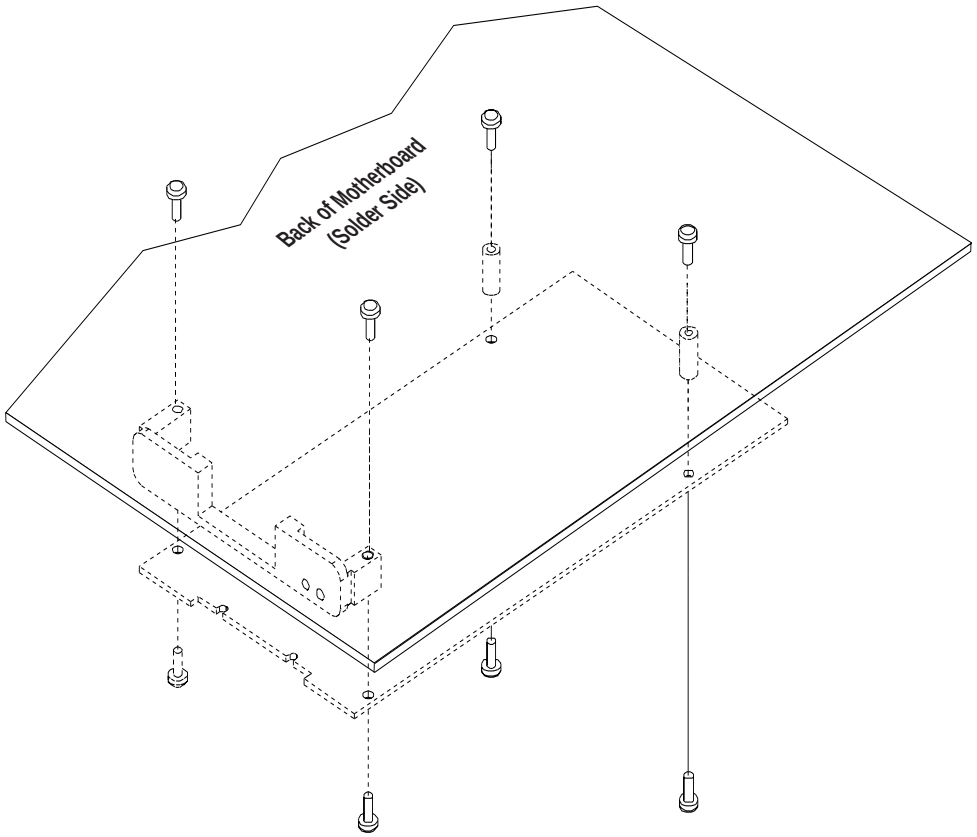


Figure 2-2 Securing the VMIPMC-5790 to the motherboard

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Cable Configuration

SCSI Connections

The VMIPMC-5790 Ultra160 SCSI connection is made using dual-channel 68-pin VHDCI external connectors.

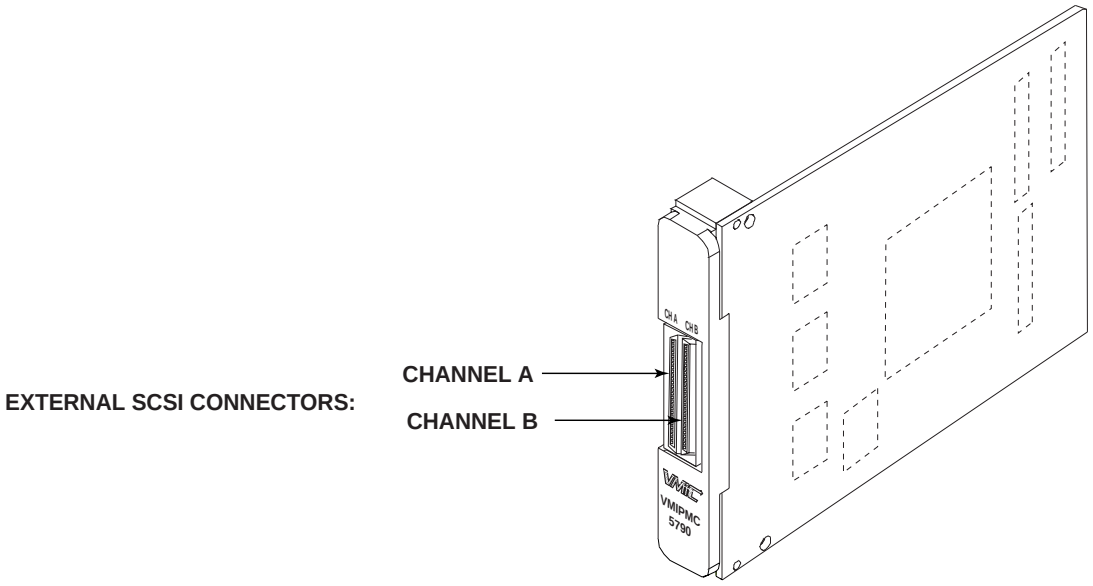


Figure 2-3 VMIPMC-5790 Front Panel and Internal Connections

External SCSI (Front Panel):

- VMIC Part Number - 321-000370-068
- AMP - 787962-1
- CHAMP 0.8mm High Density Interconnection System
- 68-Position, Right-angle, Stacked Receptacle
- Housing and Pin Spacer - UL 94V-0 rated thermoplastic, black, SMT compatible
- Inserts-UL 94V-0 rated thermoplastic, natural, SMT compatible
- Shell-Steel, plated 0.00500 min. bright tin over 0.00250 min. copper
- Contacts-Phosphor bronze, duplex plated 0.000076 min. gold over 0.00076 min. palladium nickel on mating end, 0.00375 min. bright tin-lead on solder end, all over 0.00127 min. nickel under plating
- Boardlocks-Brass, plated 0.00375 min. bright tin-lead over 0.00127 min. nickel
- Durability-500 insertion cycles

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SCSI Connectivity

The VMIPMC-5790 allows you to connect up to 16 SCSI devices per channel without any degradation of signal. The front panel SCSI connector is two 68-position VHDCI (very high density connectors), right-angle, stacked receptacles representing Channels A and B. See Figure 2-6 on page 53 for an illustration of connecting SCSI devices.

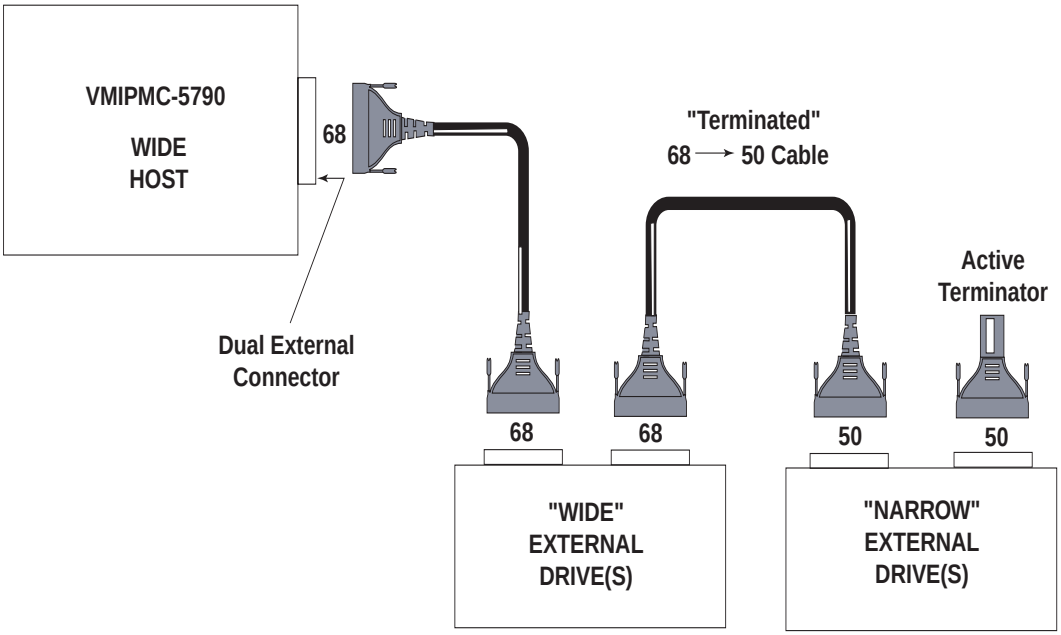


Figure 2-4 SCSI Connectivity

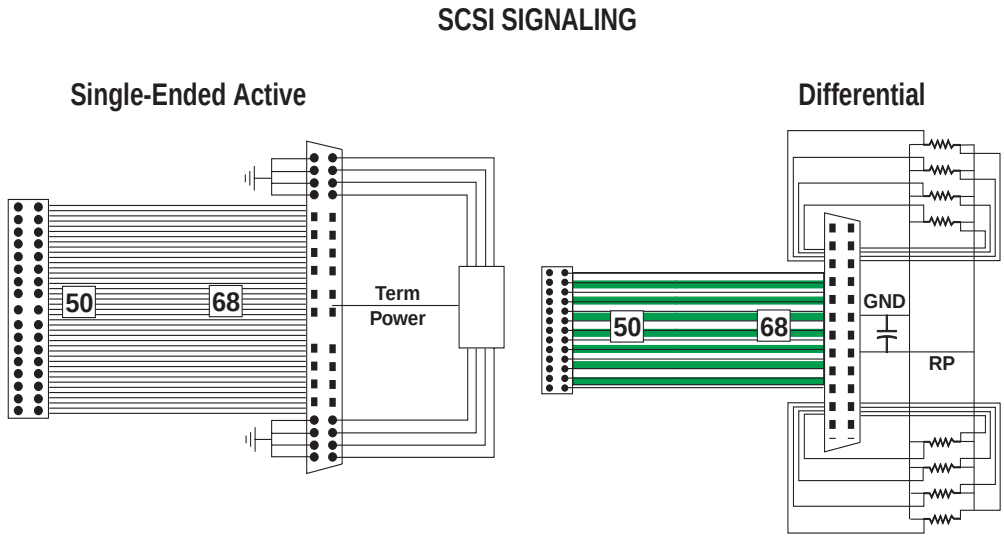


Figure 2-5 SCSI Single-Ended and Differential Schematic

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Ultra160

When Ultra160 SCSI is used with low-voltage differential (LVD) signalling, cable lengths of 12 meters are maintained to provide full backward compatibility. Ultra160 SCSI can connect up to 16 devices on a single channel. Table 2-1 is a comparative matrix comparing Ultra160 SCSI against other connectivity technologies.

Table 2-1 Comparative Matrix

	Maximum Transfer Speed	Maximum Cable Length	Maximum Number of Devices	Application Performance
IDE / UDMA 33	33MB / sec.	18 inches	2	Low
IDE / UMDA 66	66MB / sec.	18 inches	2	Low / Medium
Wide Ultra SCSI	40MB / sec.	1.5 meters	16	Low / Medium
Wide Ultra2 SCSI	80MB / sec.	12 meters	16	High
Fibre Channel	100MB / sec.	10K meters	126	High
Ultra160 SCSI	**160MB/sec.**	**12 meters**	**16**	**High**

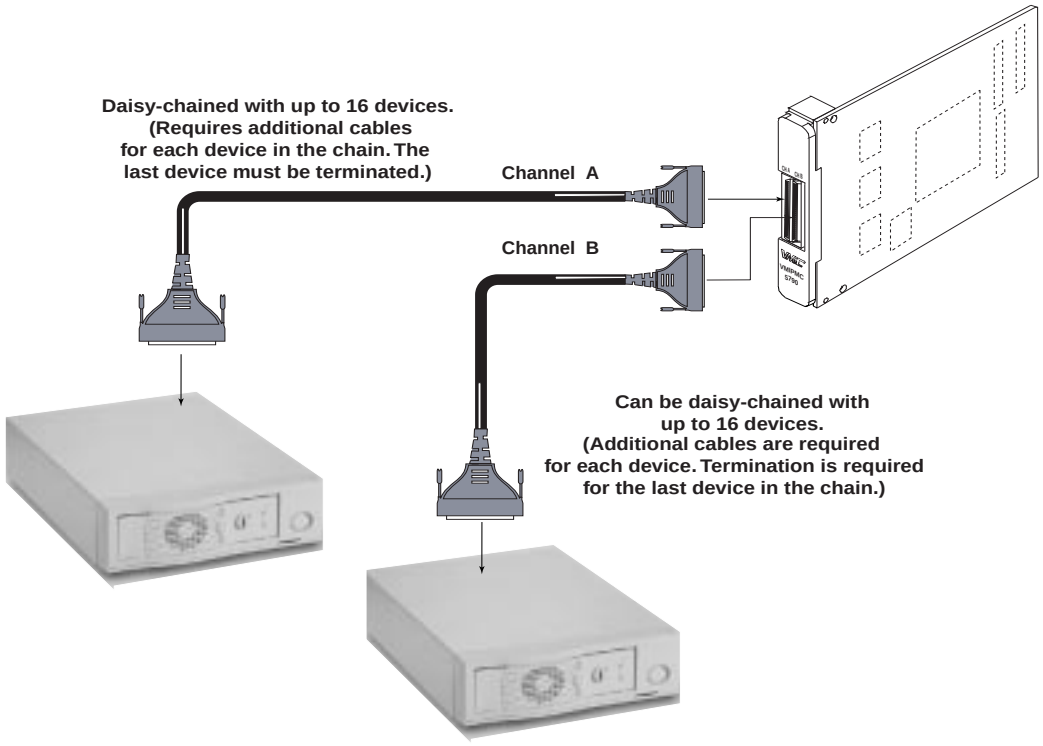


Figure 2-6 Connecting SCSI Devices

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Maintenance

Maintenance

This section provides information relative to the care and maintenance of VMIC's products. If the product malfunctions, verify the following:

- Software
- System configuration
- Electrical connections
- Jumper or configuration options
- Boards are fully inserted into their proper connector location
- Connector pins are clean and free from contamination
- No components of adjacent boards are disturbed when inserting or removing the board from the chassis
- Quality of cables and I/O connections

If the product must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return**.

Contact VMIC customer Service at 1-800-240-7782, or
E-mail: customer.service@vmic.com .

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Maintenance Prints

User level repairs are not recommended. The drawings and tables in this manual are for reference purposes only.

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Appendix

A

SCSI BIOS and Configuration Utility

Introduction

This section presents general information about the SCSI BIOS and Configuration Utility. The following SCSI information is divided into these sections:

SCSI BIOS

- Starting the SCSI BIOS Configuration Utility
- Using the Configuration Utility
- Main Menu
- Boot Adapter List
- Global Properties
- Adapter Properties
- Device Properties
- Quitting the SCSI Configuration Utility

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SCSI BIOS

A SCSI BIOS is the bootable ROM code that manages SCSI hardware resources. The SCSI BIOS integrates with a standard system BIOS, extending the standard disk service routine provided through INT13h. During the boot time initialization, the SCSI BIOS determines if there are other hard disks, such as an IDE drive, already installed by the system BIOS. If there are, the SCSI BIOS maps any SCSI drives it finds behind the drive(s) already installed. Otherwise, the SCSI BIOS installs drives starting with the system boot drive. In this case, the system boots from a drive controlled by the SCSI BIOS.

Starting the SCSI BIOS Configuration Utility

During the boot sequence you can change the default configuration of your SCSI host adapters by using the SCSI BIOS Configuration Utility. You may decide to alter these default values if there is a conflict between device settings or if you need to optimize system performance. The version number of the SCSI BIOS and the following message are displayed on your computer monitor during boot.

"Press Ctrl-C to start Symbios Configuration Utility..."

This message remains on your screen for about five seconds, giving you time to start the utility. If you decide to press "Ctrl-C", the message changes to:

"Please wait, invoking Symbios Configuration Utility..."

After a brief pause, your computer monitor displays the Main Menu of the Storage Device Management System (SDMS) PCI SCSI BIOS Configuration Utility.

CAUTION: The SCSI BIOS Configuration Utility is a powerful tool. If, while using it, you somehow disable all of your controllers, pressing Ctrl-A (or Ctrl-E on version 4.04 or later) after memory initialization during reboot allows you to re-enable and reconfigure.

NOTE: Not all devices detected by the Configuration Utility can be controlled by the BIOS. Devices such as tape drives and scanners require that a device driver specific to that peripheral be loaded. The SCSI BIOS Configuration Utility does allow parameters to be modified for these devices.

These messages may also appear during the boot process:

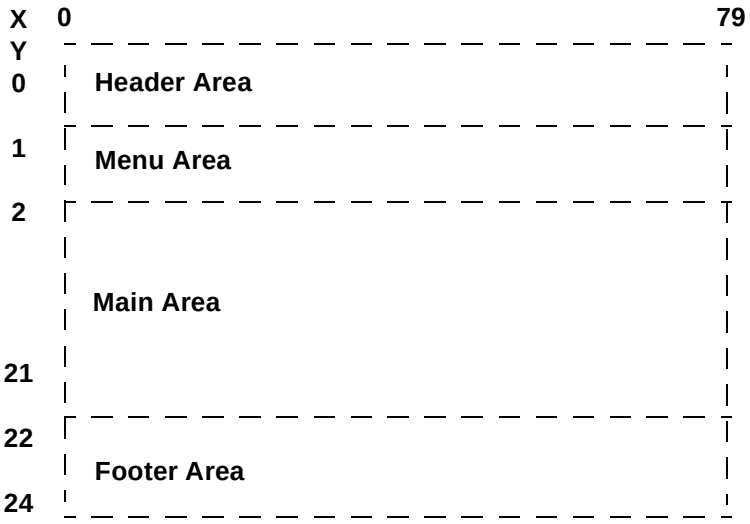
1. "**Adapter removed from boot order, parameters will be updated accordingly**" appears when an adapter is removed from the system or relocated behind a PCI bridge.
2. "**Configuration data invalid, saving default configuration!**" appears if none of the information in the NVRAM is valid.
3. "**Found SCSI Controller not in following Boot Order List, to Add: Press Ctrl-C to start Symbios Configuration Utility...**" appears when less than four adapters are in the boot order and more adapters exist than are shown.

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Using the Configuration Utility

* * * Screen Format * * *

All SCSI BIOS Configuration Utility screens are partitioned into fixed areas as shown below.



Header Area

This area provides static information text, which is typically the product title and version.

Menu Area

This area provides the current Main Area's menu, if any. This area has a cursor for menu item selection.

Main Area

This is the main area for presenting data. This area has a cursor for item selection, horizontal scrolling and vertical scrolling. The horizontal and vertical scroll bars appear here.

Footer Area

This area provides general help information text.

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* * * User Input * * *

Throughout the GUI, selections that are not permissible are grayed out.

F1 = Help

Context sensitive help for the cursor-resident field.

F2 = Menu

Sets cursor context to the menu selection area. Select a menu item and press Enter.

Arrow Keys = Select Item
Home/End = Select Item

Up, down, left, right movement to position the cursor.

+/- = Change [Item]

Items with values in [] brackets are modifiable. Numeric keypad '+' and numeric keypad '-', update a modifiable field to its next relative value.

Esc = Abort/Exit

Escape aborts the current context operation and / or exits the current screen. User confirmation is solicited as required.

Enter = Execute <Item>

Items with values in <> brackets are executable. Press Enter to execute the field's associated function.

Main Menu

When you invoke the SDMS SCSI BIOS Configuration Utility, the Main Menu appears. This screen displays a scrolling list of up to 256 LSI Logic PCI to SCSI host adapters in the system and information about each of them.

Use the arrow keys to select an adapter, then press Enter to view and modify the selected adapter's properties (and to gain access to the attached devices). Only adapters with LSI Logic Control enabled can be accessed. After selecting an adapter and pressing Enter, the adapter's SCSI bus is scanned and the Adapter Properties screen appears. An example is shown below.

On the Main Menu, two selections are: Boot Adapter List and Global Properties.

- Boot Adapter List allows selection and ordering of boot adapters. Refer to *"Boot Adapter List"* on page 76.
- Global Properties allows changes to global scope settings. Refer to *"Global Properties"* on page 77.

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To execute an item, select it and press Enter. The following is an example of the Main Menu:

```
|-------------------------------------------------------------------|
| Symbios SDMS PCI SCSI Configuration Utility Version PCI -x.xx     |
| <Boot Adapter List>  <Global Properties>                          |
|                                                                   |
| Symbios Host Bus Adapters                                         |
| Adapter          PCI  Dev/   Port    IRQ  NVM  Boot   LSI Logic   |
|                  Bus  Func   Number           Order  Control     |
| <SYM53C1010-66   0   60>     E400    10   ---  0      Enabled     |
| <SYM53C1010-66   0   88>     E000    12   Yes  1      Enabled     |
| <SYM53C896       0   90>     F800     9   Yes  2      Enabled     |
| <SYM53C896       0   A0>     E800    11   Yes  3      Enabled     |
|-------------------------------------------------------------------|
```

* * * Field Descriptions * * *

Adapter: Indicates the specific family of LSI Logic Host Adapters.

PCI Bus: Indicates the PCI Bus number (range 0x00 - 0xFF, 0 - 255 decimal) assigned by the system BIOS to an adapter.

Dev/Func: Indicates the PCI Device / Function assigned by the system BIOS to an adapter.

An 8-bit value mapped as follows:

```
Bit # 7  6  5  4  3  2  1  0
      |___________|  |_____|
            |           |> Bits 2-0: Function (range 0-7)
            |> Bits 7-3: Device (range 0x00-0x1F, 0-31 decimal)
```

Port Number: Indicates the I/O Port Number that communicates with an adapter. The system BIOS assigns this number.

IRQ: Indicates the Interrupt Request Line used by an adapter. The system BIOS also assigns this value.

NVM: Indicates whether an adapter has non-volatile memory (NVM) associated with it. An adapter's configuration is stored in its associated NVM. NVM can refer to NVRAM that is resident on a host adapter or to system NVM.

Boot Order: Indicates the relative boot order (0 to 3) of an adapter. The SDMS SCSI BIOS traverses up to four adapters in the specified order in search of bootable media. Access the "Boot Adapter List" Menu to modify this item.

LSI Logic: Indicates whether an adapter is eligible for LSI Logic software control or is reserved for control by non-LSI Logic software.

Global: Indicates global properties that are not associated with a properties specific adapter or device.

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Boot Adapter List

The adapter boot order specifies the order in which adapters will boot when more than one OS adapter is in a system.

Up to four of the total adapters in a system may be selected as bootable.

To add an adapter to the boot list, press Insert while on the Boot Adapter List. This puts the cursor on the adapter select list. Use the arrow keys to select the desired adapter and press Enter to add it to the end of Boot Adapter List.

To remove an adapter from the boot list, press Delete while on the desired adapter in the Boot Adapter List. An example of the Boot Adapter List Menu is shown below.

```
|-------------------------------------------------------------|
| Symbios SDMS PCI SCSI Configuration Utility Version PCI x.xx|
|                                                             |
| Boot Adapter List                                           |
| Insert=Add an adapter    Delete=Remove an adapter           |
|                                                             |
|           Adapter     PCI  Dev/    Boot   Current  Next     |
|                       Bus  Func    Order  Status   Boot     |
|       <SYM53C1010-66   0   60>     [0]    On       [On]     |
|       <SYM53C1010-66   0   61>     [1]    On       [On]     |
|       <SYM53C896       0   98>     [2]    On       [On]     |
|       <SYM53C896       0   A0>     [3]    On       [On]     |
|                                                             |
| Press Insert to select an adapter from this list:           |
|       <SYM53C1010-66   0   60>                              |
|       <SYM53C1010-66   0   61>                              |
|       <SYM53C896       0   98>                              |
|       <SYM53C896       0   A0>                              |
|-------------------------------------------------------------|
```

Field Descriptions

Adapter: Indicates the specific family of LSI Logic Host Bus Adapters.

PCI Bus: Indicates the PCI Bus number (range 0x00 - 0xFF, 0 - 255 decimal) assigned by the system BIOS to an adapter.

Dev/Func: Indicates the PCI Device / Function assigned by the system BIOS to an adapter.

An 8-bit value mapped as follows:

```
Bit # 7  6  5  4  3  2  1  0
      |___________|  |_____|
            |           |> Bits 2-0: Function (range 0 - 7)
              |> Bits 7-3: Device (range 0x00-0x1F, 0-31 decimal)
```


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Boot Order: Specifies the relative boot order (0 to 3) of an adapter.

-: decreases an adapter's relative boot order.

+: increases an adapter's relative boot order.

Current Status: Indicates whether an adapter in the boot list was enabled during the most recent boot. Disabled adapters and their attached devices are ignored by the SDMS PCI SCSI BIOS, although they are still visible to the Configuration Utility.

Next Boot: Specifies whether to enable an adapter upon the next boot. The SDMS SCSI BIOS ignores disabled adapters and their attached devices although they are still visible to the Configuration Utility.

Global Properties

The Global Properties option on the Main Menu allows you to set Display and Video modes, as well as a pause if an alert message has been displayed. An example of the Global Properties Menu is shown below.

```
Symbios SDMS PCI SCSI Configuration Utility Version x.xx
Global Properties


Pause When Boot Alert Displayed        [Yes]
Boot Information Displayed Mode        [Verbose]
Negotiate with devices                 [Supported]
Video Mode                             [Color]
Support Interrupt                      [Hook interrupt, the default]

            <Restore Defaults>
```

* * * Field Descriptions * * *

Pause When Boot Alert Displayed: This option specifies whether to pause for user acknowledgement after displaying an alert message during boot. The Boot Alert setting can be either No or Yes.

To continue after displaying a message, specify No.

To wait for any key after displaying a message, specify Yes.

Boot Information Display Mode: This option specifies the information display mode of the BIOS during boot. It controls how much information about adapters and devices are displayed during boot. The Display Mode setting can be either Terse or Verbose.

To display minimum information, specify Terse mode.

To display detailed information, specify Verbose mode.

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Negotiate with devices: This option sets the default value for synchronous and wide negotiations with specified devices. Options are: All, None, or Supported.

Video Mode: This option specifies the default video mode for the Configuration Utility. The Video Mode setting can be either Color or Monochrome. The monochrome setting enhances readability on a monochrome monitor.

Support Interrupt: This option allows the ability to prevent a hook on INT40, if required.

<Restore Defaults>: Press Enter to obtain default settings**.**

Adapter Properties

The Adapter Properties Menu allows you to view and modify adapter settings.

It also provides access to an adapter's device settings. An example of the Adapter Properties Menu is shown below:

```
Symbios SDMS PCI SCSI Configuration Utility Version PCI x.xx

 Adapter Properties

 Adapter              PCI    Dev/
                      Bus    Func
 53C1010-66            0      60

      <Device Properties>

       SCSI Parity               [Yes]
       Host SCSI ID              [ 7]
       SCSI Bus Scan Order       [Low to High (0..Max)]
       Removable Media Support   [None]
       CHS Mapping               [SCSI Plug and Play Mapping]
       Spinup Delay (Secs)       [ 2]
       Secondary Cluster Server  [No]
       Termination Control       [Auto]

      <Restore Defaults>
```

* * * Field Descriptions * * *

<Device Properties>: To view and modify device properties, press Enter.

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SCSI Parity: This field indicates whether SCSI parity is enabled for an adapter. When disabled, it is also necessary to disable disconnects for all devices, as parity checking for the reselection phase is NOT disabled. If a non-parity generating device disconnects, its operation will never complete because the reselection fails due to parity error.

Host SCSI ID: This field indicates the SCSI identifier of an adapter [0-7] or [0-15]. It is recommended that this field be set to the highest priority SCSI identifier, which is 7.

NOTE: 8-bit SCSI devices cannot see identifiers greater than 7.

SCSI Bus Scan Order: This field indicates the order in which to scan SCSI identifiers on an adapter. Changing this item will affect drive letter assignment(s) if more than one device is attached to an adapter.

NOTE: Changing this item may conflict with an operating system that automatically assigns drive order.

Removable Media Support: This field specifies the removable media support option for an adapter. Three settings are allowed:

- **None** indicates no removable media support whether the drive is selected as first (BBS), or is first in the scan order (non-BBS).
- **Boot Drive Only** provides removable media support for a removable hard drive if it is first in the scan order.
- **With Media Installed** provides removable media regardless of the drive ordering.

CHS Mapping: This field defines how the Cylinder Head Sector values are mapped onto a disk without pre-existing partition information. CHS Mapping allows two settings: SCSI Plug and Play Mapping (default value), and Alternate CHS Mapping.

SCSI Plug and Play Mapping automatically determines the most efficient and compatible mapping.

Alternate CHS Mapping utilizes an alternate, possibly less efficient mapping that may be required if a device is moved between adapters from different vendors.

NOTE: Neither of these options has any effect after a disk has been partitioned using the FDISK command. To change the CHS Mapping on a partitioned disk, use FDISK command to delete all partitions. Next, reboot the system to clear memory or the old partitioning data will be reused, thus nullifying the previous operation.

CAUTION: Ensure that the correct disk is the target of an FDISK command.

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Spinup Delay (Secs): This field indicates the number of seconds to wait between spinups of devices attached to an adapter. Staggered spinups will balance the total electrical current load on the system during boot. The default value is 2 seconds, with choices between 1 and 10 seconds.

Secondary Cluster Server: This field indicates whether an adapter has one or more devices attached that are shared with one or more other adapters and therefore, the SDMS PCI SCSI BIOS should avoid SCSI Bus resets as much as possible.

This option allows you to enable an adapter to join a cluster of adapters without doing any SCSI bus resets. This is a requirement for Microsoft Cluster Server. The default value is No with an alternate option of Yes.

Termination Control: This field indicates whether an adapter has automatic termination control, and if so, its current status. Two settings are:

- **Auto:** The adapter automatically determines whether it should enable or disable its termination.
- **Off:** Termination at the adapter is off, the devices at the ends of the SCSI bus must terminate the bus.

NOTE: If Auto is grayed out, it means that termination is automatic, not programmable.

Restore Defaults: To obtain default settings, press Enter.

Device Properties

The Device Properties screen provides viewing and updating of individual device settings for an adapter.

Changing a setting for the host device (for example, SCSI ID 7) changes the setting for all devices. An example of the Device Properties screen is shown on the following page:

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Symbios SDMS PCI SCSI Configuration Utility Version PCI- x.xx

SCSI ID	Device Identifier	MB/sec	MT/sec	Data Width	Scan ID	Scan LUNs>0	Dis-connect
0		[160]	[80]	[16]	[Yes]	[Yes]	[On]
1		[160]	[80]	[16]	[Yes]	[Yes]	[On]
2		[160]	[80]	[16]	[Yes]	[Yes]	[On]
3	SEAGATE ST31055N	[160]	[80]	[16]	[Yes]	[Yes]	[On]
4		[160]	[80]	[16]	[Yes]	[Yes]	[On]
5		[160]	[80]	[16]	[Yes]	[Yes]	[On]
6		[160]	[80]	[16]	[Yes]	[Yes]	[On]
7	SYM53C1010-66	[160]	[80]	[16]	[Yes]	[Yes]	[On]
8		[160]	[80]	[16]	[Yes]	[Yes]	[On]
9		[160]	[80]	[16]	[Yes]	[Yes]	[On]
10		[160]	[80]	[16]	[Yes]	[Yes]	[On]
11		[160]	[80]	[16]	[Yes]	[Yes]	[On]
12		[160]	[80]	[16]	[Yes]	[Yes]	[On]
13		[160]	[80]	[16]	[Yes]	[Yes]	[On]
14		[160]	[80]	[16]	[Yes]	[Yes]	[On]
15		[160]	[80]	[16]	[Yes]	[Yes]	[On]

<< Scroll Indicator>>

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```
SCSI  Device Identifier              SCSI    Queue  Boot    Format
 ID                                 Timeout Tags  Choice
  0    -                              <10>    [On]   [No]    <Format>
  1    -                              <10>    [On]   [No]    <Format>
  2    -                              <10>    [On]   [No]    <Format>
  3    SEAGATE ST31055N               <10>    [On]   [No]    <Format>
  4    -                              <10>    [On]   [No]    <Format>
  5    -                              <10>    [On]   [No]    <Format>
  6    -                              <10>    [On]   [No]    <Format>
  7    SYM53C1010-66                  <10>    [On]   [No]    <Format>
  8    -                              <10>    [On]   [No]    <Format>
  9    -                              <10>    [On]   [No]    <Format>
 10    -                              <10>    [On]   [No]    <Format>
 11    -                              <10>    [On]   [No]    <Format>
 12    -                              <10>    [On]   [No]    <Format>
 13    -                              <10>    [On]   [No]    <Format>
 14    -                              <10>    [On]   [No]    <Format>
 15    -                              <10>    [On]   [No]    <Format>
                                    << Scroll Indicator >>

SCSI  Device Identifier               Verify    Restore
ID                                              Defaults
 0    -                               <Verify>  <Defaults>
 1    -                               <Verify>  <Defaults>
 2    NEC     CD-ROM DRIVE:4621.15    <Verify>  <Defaults>
 3    SEAGATE ST31055N        0594    <Verify>  <Defaults>
 4    -                               <Verify>  <Defaults>
 5    -                               <Verify>  <Defaults>
 6    -                               <Verify>  <Defaults>
 7    SYM53C1010-66                   <Verify>  <Defaults>
 8    -                               <Verify>  <Defaults>
 9    -                               <Verify>  <Defaults>
10    -                               <Verify>  <Defaults>
11    -                               <Verify>  <Defaults>
12    -                               <Verify>  <Defaults>
13    -                               <Verify>  <Defaults>
14    -                               <Verify>  <Defaults>
15    -                               <Verify>  <Defaults>
                                     << Scroll Indicator>>
```


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* * * Field Descriptions * * *

SCSI ID: This field indicates the device's SCSI Identifier.

Device Identifier: This field indicates the ASCII device identifier string extracted from the device's Inquiry Data.

Sync Rate: This field indicates the maximum synchronous data transfer rate, in Mega Transfers per second.

Mega Transfers/ Second	Data Width= 8 MBytes/s	Data Width=16 MBytes/s	Synchronous Period nsec
0=Async	0=Async	0=Async	0=Async
5	5	10	200
10	10	20	100
20	20	40	50
40	40	80	25

Data Width: This field indicates the maximum data width in bits.

Scan ID: This field indicates whether to scan for this SCSI identifier at boot time. This item can be used to ignore a device and to decrease boot time by disabling the inquiry of unused SCSI identifiers.

Set this option to "No" if there is a device that you do not want to be available to the system. Also, on a bus with only a few devices attached, the user can speed up boot time by changing this setting to "No" for all unused SCSI IDs.

Scan LUNs > 0: This field indicates whether to scan for LUNs greater than zero for a device. LUN zero is always queried. This option should be used if a multi-LUN device responds to unoccupied LUNs, or if it is desired to reduce the visibility of a multi-LUN device to LUN zero only.

Set this option to "No" if you have problems with a device that responds to all LUNs (occupied or not). Also, if a SCSI device with multiple LUNs exists on your system but you do not want all of those LUNs to be available to the system, set this option to "No." This will limit the scan to LUN 0 only.

Disconnect: This field indicates whether to allow a device to disconnect during SCSI operations. Some (mostly newer) devices run faster with disconnect enabled, while some (mostly older) devices run faster with disconnect disabled.

SCSI Timeout: This field indicates the maximum amount of time [0 to 9999] in seconds to wait for a SCSI operation to complete.

Since timeouts provide a safeguard that allows the system to recover should an operation fail, it is recommended that a value greater than zero be used. A value of zero allows unlimited time for an operation to complete and could result in the system hanging (waiting forever) should an operation fail.

Press Enter, type in a value, and then press Enter again to specify a new timeout value.

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Queue Tags: This field indicates whether to allow the use of queue tags for a device. Currently the BIOS does not use queue tags. This item specifies queue tag control to higher level device drivers.

Boot Choice: This field indicates whether this device may possibly be selected as the boot device. This option is only applicable to devices attached to adapter number zero (in the boot list) on non-BBS systems. It provides primitive BBS flexibility to non-BBS systems.

Format: Press Enter to low-level format the device.

If enabled, this option allows low-level formatting on a disk drive. Low-level formatting will completely and irreversibly erase all data on the drive.

NOTE: Formatting will default the drive to a 512-byte sector size even if the drive had previously been formatted to another sector size.

Verify: Press Enter to verify all sectors on the device and to reassign defective Logical Block Addresses (LBAs).

Restore Defaults: Press Enter to obtain default settings.

Quitting the SCSI BIOS Configuration Utility

Since some changes only take effect after your system reboots, it is important that you exit this configuration utility properly. To exit, press Esc (Escape key) and respond to the verification prompts that follow.

CAUTION: If you reboot the system without properly exiting from this utility, some changes may not take effect.

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