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VMICPCI-7611

Single Board Embedded Module Processor-Based System Slot CompactPCI® CPU

Product Manual

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Huntsville, Alabama 35803-3308, USA
(256) 880-0444 ◆ (800) 322-3616 ◆ Fax: (256) 882-0859

500-657611-000 Rev.A

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Table of Contents

Overview 13

Organization of the Manual 14
References 15
Safety Summary 17
Safety Symbols Used in This Manual 18

Chapter 1 - Features and Options 19

CompactPCI Features 22
VMICPCI-7611 Product Options 23

Chapter 2 - Installation and Setup 25

Unpacking Procedures 25
Hardware Setup 26
Installation 31
BIOS Setup 32
Front Panel Connectors 32
PMC Site Connector 33
LED Definition 34

Chapter 3 - PC/AT Functions 35

CPU Socket 36
Physical Memory 36
I/O Port Map 37
PCI-to-PCI Bridge 39
PC/AT Interrupts 39
PCI Interrupts 42
Integrated Peripherals 45

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Ethernet Controller 46
10BaseT 46
100BaseTx 46
Video Graphics Adapter 47

Chapter 4 - Embedded PC/RTOS Features 49

DiskOnChip (Optional) 50
Installing the DiskOnChip 50
Configuring the DiskOnChip as the Boot Device 50
Using the DiskOnChip with Other Operating Systems 51
Watchdog Timer 52
Time of Day Registers 54
Time of Day Alarm Registers 55
Watchdog Alarm Registers 56
Command Register 56

Chapter 5 - Maintenance 59

Maintenance Prints 59

Appendix A - Connector Pinouts 61

J1 Connector Pinout 63
J2 Connector and Pinout 64
J3 Connector Pinout 65
J5 Connector and Pinout 66
Ethernet Connector Pinout (J14) 67
Video Connector Pinout (J11) 68
Parallel Port Connector Pinout (P2) 69
Keyboard and Mouse Connectors and Pinout (J10) 70
USB Connector (J9) 71
PMC Connector Pinout 72
PMC J7 Connector and Pinout 72
PMC J6 Connector and Pinout 73
PMC J4 Connector and Pinout 74

Appendix B - Phoenix BIOS 75

System BIOS Setup Utility 75
Help Window 75
First Boot 76

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Main Menu 77
QuickBoot 77
Setting The Time 77
Setting The Date 77
Legacy Diskette 78
Floppy Drive A 78
Floppy Drive B 78
Primary Master/Slave 78
Secondary Master 79
Keyboard Features 79
NumLock 79
Key Click 79
Keyboard Auto-Repeat Rate (Chars/Sec) 79
Keyboard Auto-Repeat Delay (sec) 80
Keyboard Test 80
System Memory 80
Extended Memory 80
Extended Memory 80
Console Redirection 80
Com Port Address 81
Baud Rate 81
Console Type 81
Flow Control 81
Console Connection 81
Continue C.R. After POST 81
Advanced Menu 82
Installed O/S 82
Reset Configuration Data 82
Cache Memory 82
I/O Device Configuration 83
Large Disk Access Mode 84
Local Bus IDE Adapter 84
Advanced Chipset Control 84
Graphics Aperture 84
Enable Memory Map 85
ECC Config 85
SERR Signal Configuration 85
Clear Watchdog Timer Reset 85

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Assign Interrupt To USB 85
Legacy Keyboard/Mouse 85
Power 86
Boot Menu 87
Exit Menu 88
Exit Saving Changes 88
Exit Discarding Changes 88
Load Setup Defaults 88
Discard Changes 88
Save Changes 88

Appendix C - Device Configuration: I/O and Interrupt Control 89

BIOS Operations 90
BIOS Control Overview 90
Functional Overview 90
Data Book References 92
Device Address Definition 94
ISA Devices 94
PCI Devices 95
Device Interrupt Definition 96
PC/AT Interrupt Definition 96
ISA Device Interrupt Map 96
PCI Device Interrupt Map 98

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List of Figures

Figure 1-1 VMICPCI-7611 Block Diagram 21
Figure 2-1 VMICPCI-7611 Embedded Module, and Jumper Locations 27
Figure 2-2 Installing a PMC Card on the VMICPCI-7611 33
Figure 2-3 Front Panel LED Positions 34
Figure 3-1 Connections for the PC Interrupt Logic Controller 44
Figure 4-2 Watchdog Alarm Block 52
Figure A-1 VMICPCI-7611 Connector and Jumper Locations 62
Figure A-2 J1 Connector and Pinout 63
Figure A-3 J2 Connector and Pinout 64
Figure A-4 J3 Connector and Pinout 65
Figure A-5 J5 Connector and Pinout 66
Figure A-6: Ethernet Connector and Pinout 67
Figure A-7 Video Connector and Pinout 68
Figure A-8 P2 Connector and Pinout 69
Figure A-9 Keyboard/Mouse Connector and Pinout 70
Figure A-10 USB Connector Pinout 71
Figure C-1 VMICPCI-7611 Block Diagram 91
Figure C-2 BIOS Default Connections for the PC Interrupt Logic Controller 97

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List of Tables

Table 1-1	PC/AT I/O Features	20
Table 2-1	CPU Board Connectors	28
Table 2-2	Password Clear (User Configurable) - Jumper (E3)	28
Table 2-3	Factory Configured - PIIX4E Battery Jumper (E6)	29
Table 2-4	Factory Configured - Watchdog Timer jumper (E7)	29
Table 2-5	Factory Configured - Clock Speed Select Jumper (E8)	29
Table 2-6	Factory Configured - Watchdog Battery Jumper (E10)	29
Table 2-7	Factory Configured - Reserved Jumper (E12)	29
Table 2-8	Factory Configured - DiskOnChip Address SEL Jumper (E13)	30
Table 2-9	Factory Configured - Boot Block Lock Jumper (E17)	30
Table 2-10	Factory Configured - Boot Block Lock (E18)	30
Table 3-1	VMICPCI-7611 I/O Address Map	37
Table 3-2	PC/AT Hardware Interrupt Line Assignments	39
Table 3-3	PC/AT Interrupt Vector Table	40
Table 3-4	NMI Register Bit Descriptions	43
Table 3-5	Supported Graphics Video Resolutions	47
Table 4-6	Watchdog Registers	53
Table 4-7	Time of Day Alarm Registers	55
Table A-1	Keyboard/Mouse Y Splitter Cable	70
Table A-2	PMC J7 Connector Pinout	72
Table A-3	PMC J6 Connector Pinout	73
Table A-4	PMC J4 Connector Pinout	74
Table C-1	ISA Device Mapping Configuration	94
Table C-2	PCI Device Mapping Configuration	95
Table C-3	PCI Device Interrupt Mapping by the BIOS	98

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Overview

Introduction

VMIC's VMICPCI-7611 is a complete IBM PC / AT-compatible Pentium II / III Embedded Module processor-based computer with the additional benefits of Eurocard construction and full compatibility with the CompactPCI Specification Rev. 2.1. The VMICPCI-7611 with advanced CPCI interface and SDRAM that is dual-ported to the CPCI bus, is ideal for CPCI system controller applications.

The single-slot CPU board functions as a standard PC / AT, executing a PC / AT-type power-on self-test, then boots up MS-DOS, Windows 3.11, Windows 95, Windows NT, or any other PC / AT-compatible operating system. The PC / AT mode of the VMICPCI-7611 is discussed in Chapter 3 of this manual.

The VMICPCI-7611 also operates as a CPCI system slot CPU and interacts with other CPCI modules via the on-board embedded bridge.

The VMICPCI-7611 also provides capabilities beyond the features of a typical PC / AT compatible CPU including a programmable watchdog timer and a bootable flash disk system. These features makethe unit ideal for embedded applications. These nonstandard PC / AT functions are discussed in Chapter 4 of this manual.

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Organization of the Manual

This manual is composed of the following chapters and appendices:

Chapter 1 - Features and Options describes the features of the base unit followed by descriptions of the associated features of the unit in operation on a CPCI bus.

Chapter 2 - Installation and Setup describes unpacking, inspection, hardware jumper settings, connector definitions, installation, system setup, and operation of the VMICPCI-7611.

Chapter 3 - PC/AT Functions describes the unit design in terms of the standard PC memory and I/O maps, along with the standard interrupt architecture.

Chapter 4 - Embedded PC/RTOS Features describes the unit features that are beyond standard PC/AT functions.

Chapter 5 - Maintenance provides information relative to the care and maintenance of the unit.

Appendix A - Connector Pinouts illustrates and defines the connectors included in the unit's I/O ports.

Appendix B - Phoenix BIOS describes the menus and options associated with the Phoenix BIOS.

Appendix D - Device Configuration: I/O and Interrupt Control provides the user with the information needed to develop custom applications such as the revision of the current BIOS configuration to a user-specific configuration.

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References

For the most up-to-date specifications for the VMICPCI-7611, please refer to:

Pentium II/III Processor with MMX™ Technology
Intel Corporation
2200 Mission College Blvd.
P.O. Box 58119
Santa Clara, CA 95052-8119
(408) 765-8080

Intel 82440BX AGP set: 82443BX Host Bridge/Controller
Intel Corporation
2200 Mission College Boulevard
P.O. Box 58119
Santa Clara, CA 95052-8119

Intel 21154 PCI-to-PCI Bridge
Intel Corporation
2200 Mission College Boulevard
P.O. Box 58119
Santa Clara, CA 95052-8119

Intel 82559 10/100 Mb/s Ethernet LAN Controller
Intel Corporation
2200 Mission College Boulevard
P.O. Box 58119
Santa Clara, CA 95052-8119

Intel 82440BX PCIset ISA Bridge
82371EB PCI ISA IDE Xcellerator (PIIX4E)
2200 Mission College Boulevard
P.O. Box 58119
Santa Clara, CA 95052-8119

PCI Local Bus Specification, Rev. 2.1
PCI Special Interest Group
P.O. Box 14070
Portland, OR 97214
(800) 433-5177 (U.S.)
(503) 797-4207 (International)
(503) 234-6762 (FAX)

SMC FDC37C67X Enhanced Super I/O Controller
SMC Component Products Division
300 Kennedy Drive
Hauppauge, NY 11788
(516) 435-6000
(516) 231-6004 (FAX)

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ISA & EISA, Theory and Operation
Solari, Edward
Annabooks
15010 Avenue of Science, Suite 101
San Diego, CA 92128 USA
ISBN 0-929392 -15-9

DS 1284 Watchdog Timekeeping Controller
Dallas Semiconductor
4461 South Beltwood Pwky.
Dallas, TX 75244-3292

M-Systems Corporate Headquarters
USA Office
39899 Balentine Dr.
Suite 335
Newark, CA 94560
Tel: 510-413-5950
Fax: 510-413-5980
Email: info@m-sys.com

Intel 69000AGP Video Controller
Intel Corporation
P.O. Box 58119
Santa Clara, CA 95052-8119
(408) 765-8080
www.intel.com

CMC Specification, P1386/Draft 2.0 from:
IEEE Standards Department
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Piscataway, NJ 08855-1331, USA

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Piscataway, NJ 08855-1331, USA

For a detailed description and specification of the CompactPCI bus, please refer to:

CompactPCI™ Specification PICMG 2.0 R2.1
PCI Industrial Computer Manufactures' Group
301 Edgewater Place
Suite 220
Wakefield, MA 01880
(617) 224-1100
(617) 224-1239 (FAX)
www.picmg.org (Web)

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Safety Summary

The following general safety precautions must be observed during all phases of the operation, service, and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of this product.

VMIC assumes no liability for the customer's failure to comply with these requirements.

Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person capable of rendering first aid and resuscitation is present.

Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VMIC for service and repair to ensure that safety features are maintained.

Dangerous Procedure Warnings

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

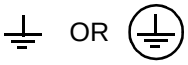
WARNING

Dangerous voltages, capable of causing death, are present in this system. Use extreme caution when handling, testing, and adjusting.

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Safety Symbols Used in This Manual

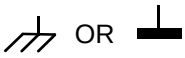
Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 V are so marked).



Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.



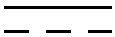
Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. Before operating the equipment, terminal marked with this symbol must be connected to ground in the manner described in the installation (operation) manual.



Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.



Alternating current (power line).



Direct current (power line).



Alternating or direct current (power line).

STOP: informs the operator that a practice or procedure should not be performed. Actions could result in injury or death to personnel, or could result in damage to or destruction of part or all of the system.

WARNING: denotes a hazard. It calls attention to a procedure, a practice, or condition, which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION: calls attention to an operating procedure, a practice, or a condition, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE: denotes important information. It calls attention to a procedure, a practice, or condition which is essential to highlight.

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CHAPTER 1

Features and Options

Contents

CompactPCI Features 22
VMICPCI-7611 Product Options 23

Introduction

The VMICPCI-7611 performs all the functions of a standard IBM PC / AT motherboard with the following features:

- Single-slot CPCI bus 6U Eurocard form factor
- Includes a high-performance Intel Pentium II / III Embedded Module processor
- Up to 256 Mbyte of Synchronous DRAM
- AGP video with 2 Mbyte SDRAM
- Real-time clock / calendar
- Front panel reset switch
- Onboard port for keyboard and mouse
- UltraEIDE hard drive, floppy drive through the CPCI J3 connector
- Onboard fast Ethernet controller supporting 10BaseT and 100BaseTX interfaces
- Front panel “vital sign” indicators (power, UltraEIDE hard drive activity, Ready, and Ethernet status)
- Software-selectable watchdog timer with reset
- Optional M-Systems DiskOnChip flash memory (12 to 72 Mbyte available)
- Two Serial ports, one available by way of the front panel RJ11 connector and both available through the CPCI J3 connector
- One enhanced parallel port available on the front panel and through the CPCI J3 connector
- Two USB Ports: one available on the front panel, and one through the CPCI J3 connector (rear I / O)

The VMICPCI-7611 supports standard PC / AT I / O features such as those listed in Table 1-1. Figure 1-1 on page 21 shows a block diagram of the VMICPCI-7611 emphasizing the I / O features, including the PCI-to-PCI bridge. The serial, parallel, IDE, and floppy signals are also routed through the backplane.

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Table 1-1 PC/AT I/O Features

I/O FEATURE	IDENTIFIER	PHYSICAL ACCESS
Two high-performance 16550-compatible serial port	COM1, COM2	One through the front panel RJ11, both through CPCI J3 Connector (See Note)
One Enhanced Parallel Port, Supports ECP / EPP Modes	Parallel	Through front panel and CPCI J3 connector (See Note)
AT-Style Keyboard / Mouse Controller	M / K	Front Panel PS / 2-Style Connector, Mini-DIN Circular (female)
AGP Video Controller with 2 Mbyte SDRAM	SVGA	Front Panel DB15HD High Density (female)
Real-Time Clock / Calendar	Date, Time	
On-board fast Ethernet controller supporting 10BaseT and 100BaseTX interfaces	LAN	Front Panel R-J45
Floppy Disk Controller	Drive A	Through CPCI J3
Ultra EIDE Hard Drive Controller	Drive C	Through CPCI J3
Two USB Ports	USB	One through the front panel, the other through CPCI J3
Hardware Reset	RST	Front Panel Push-Button
Power Status, Hard Drive Activity, Ready, and Ethernet Status for each controller	LED Indicators	Front Panel

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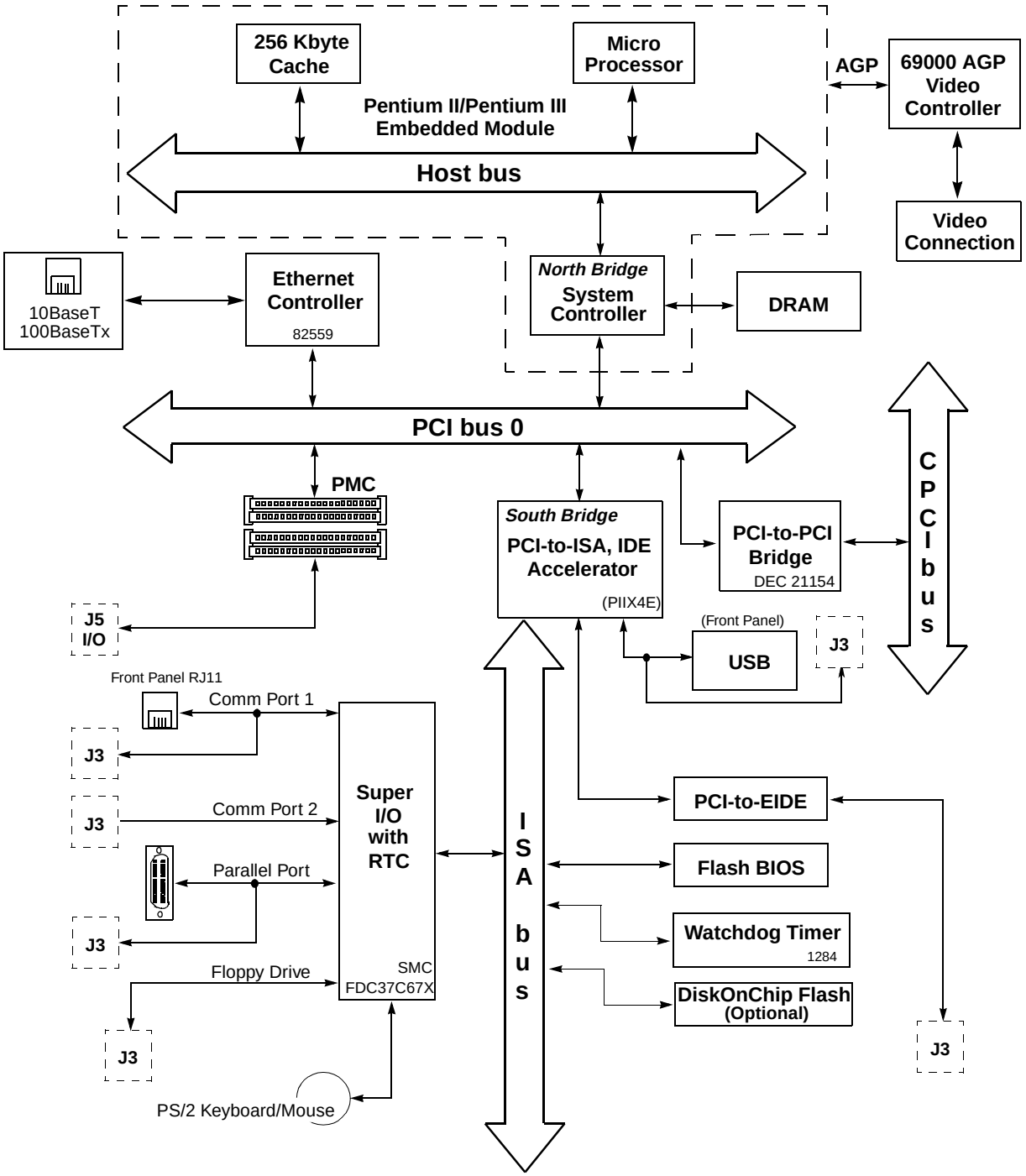


Figure 1-1 VMICPCI-7611 Block Diagram

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CompactPCI Features

In addition to its PC / AT functions, the VMICPCI-7611 has the following CompactPCI features:

- Single-slot, 6U height CPCI board
- Complies fully with Revision 2.1 of the *PCI Local Bus Specification*
- Complies fully with Revision 1.1 of the *PCI-to-PCI Bridge Architecture Specification*
- Complies with Revision 2.1 of the *CompactPCI Specification*
- Implements delayed transactions for all PCI configuration, I / O, and memory read commands-up to three transactions simultaneously in each direction
- Allows 152 bytes of buffering (data and address) for upstream posted memory write commands and 88 bytes of buffering for downstream posted memory write commands- up to nine upstream and five downstream posted write transactions simultaneously
- Allows 152 bytes of read data buffering upstream and 72 bytes of read data buffering downstream
- Provides concurrent primary and secondary bus operation to isolate traffic
- Provides enhanced address decoding
- Includes addressing and VGA palette snooping support
- Supports PCI transaction forwarding for the following commands
  - All I / O and memory commands
  - Type 1 to Type 1 configuration commands
  - Type 1 to Type 0 configuration commands (downstream only)
  - All Type 1 to special cycle configuration commands
- Includes downstream lock support
- Supports both 5 and 3.3 V signaling environments

The VMICPCI-7611 is a versatile single-board solution for CPCI control with familiar PC / AT operation.

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VMICPCI-7611 Product Options

VMIC's VMICPCI-7611 is built around three fundamental hardware configurations. These involve processor power, RAM memory, and the optional DiskOnChip flash memory size. *These options are subject to change based on emerging technologies and availability of vendor configurations.*

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CHAPTER 2

Installation and Setup

Contents

Unpacking Procedures 3-25
Hardware Setup 3-26
Installation 3-31

Introduction

This chapter describes the hardware jumper settings, connector descriptions, installation, system setup, and operation of the VMICPCI-7611.

Unpacking Procedures

Any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC Customer Service together with a request for advice concerning the disposition of the damaged item(s).

CAUTION: Some of the components assembled on VMIC's products may be sensitive to electrostatic discharge and damage may occur on boards that are subjected to a high energy electrostatic field. When the board is placed on a bench for configuring, etc., it is suggested that conductive material be inserted under the board to provide a conductive shunt. Unused boards should be stored in the same protective boxes in which they were shipped.

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Hardware Setup

The VMICPCI-7611 is factory populated with user-specified options as part of the VMICPCI-7611 ordering information. The CPU speed, RAM size, and flash memory size are not user-upgradable. To change CPU speeds, RAM / flash size, contact customer service to receive a Return Material Authorization (RMA).

VMIC Customer Service is available at: 1-800-240-7782.

The VMICPCI-7611 is tested for system operation and shipped with factory-installed header jumpers. The physical location of the jumpers and connectors for the single board CPU are illustrated in Figure 2-1 on page 27. The definitions of the CPU board jumpers and connectors are included in Table 2-1 through Table 2-10.

CAUTION: All jumpers are factory configured and should not be modified by the user. There are two exceptions: the Password Clear (E3), and the Watchdog Timer (E7). Modifying any other jumper will void the Warranty and may damage the unit. The default jumper condition of the VMICPCI-7611 is expressed in Table 2-1 through Table 2-10 with **bold text** in the table cells.

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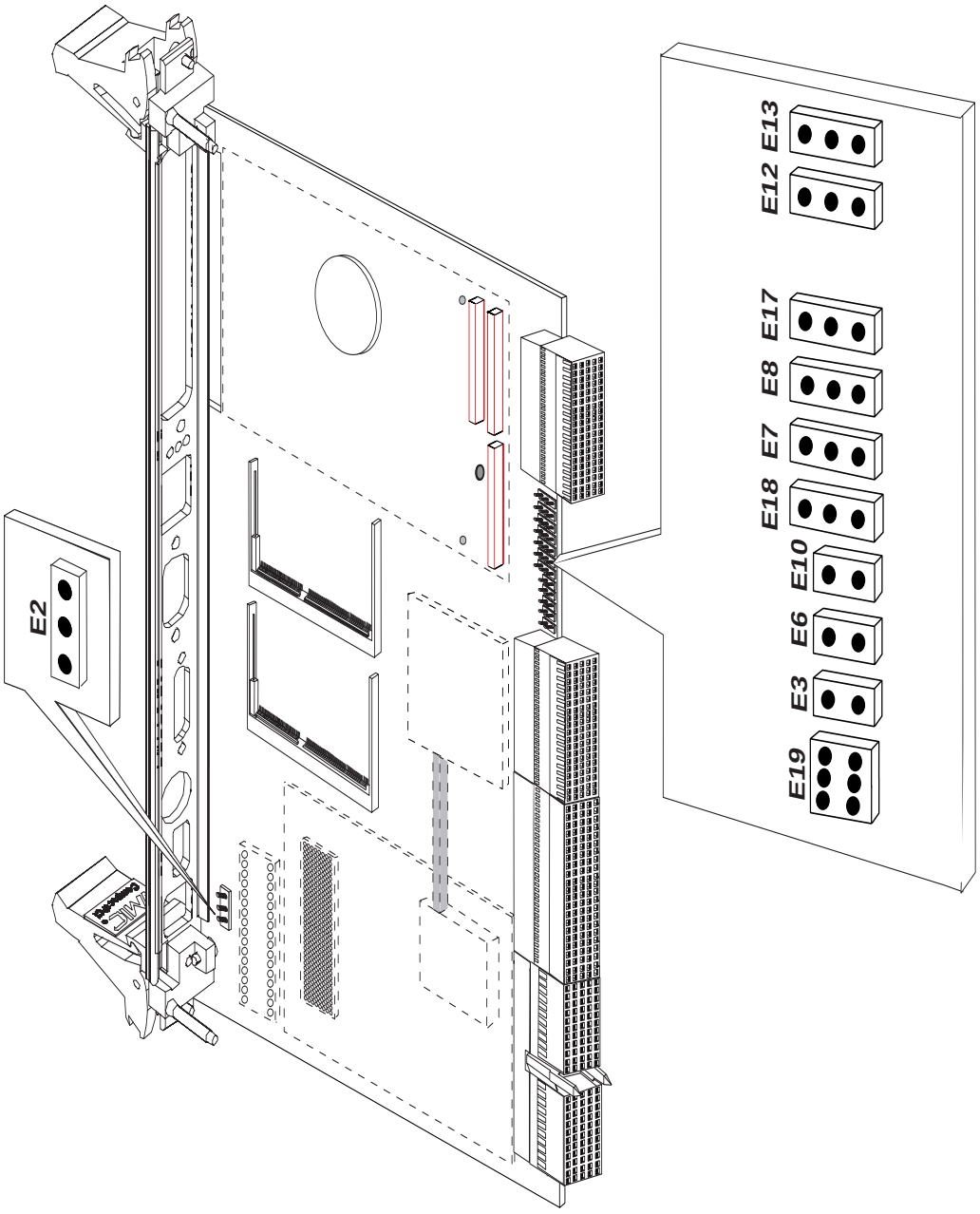


Figure 2-1 VMICPCI-7611 Embedded Module, and Jumper Locations

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Table 2-1 CPU Board Connectors

Connector	Function
J10	Mouse/Keyboard Connector
J9	USB Connector
J13	COM1
J3	COM1/COM2
J3, P2	Parallel Port Connector
J14	Ethernet Connector
J11	Video Connector
J3	Floppy Interface Connector
E15	ITP Test Header
E16	Port 80 Test Header
J3	EIDE Connector
E2	Fan Connector
J6, J7, J4	PMC Slot
J1, J2	Compact PCI Connectors

Table 2-2 Password Clear (**User Configurable**) - Jumper (E3)

	Jumper Position
Normal	**Out**
Clear NVRAM/CMOS/Password	In

NOTE: The BIOS has the capability (not currently enabled) of password protecting casual access to the unit's CMOS set-up screens. The Password Clear jumper allows for a means to clear the password feature, this might be necessary to perform in the case of a forgotten password.

To clear the CMOS password:

1. Turn off power to the unit
2. Install a jumper at E3
3. Power up the unit
4. Turn off the power to the unit and remove the jumper from E3

When power is reapplied to the unit, the CMOS password will be cleared.

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Table 2-3 Factory Configured - PIIX4E Battery Jumper (E6)

PIIX4E Battery	Jumper Position
Enabled	**In**
Disabled	Out

Table 2-4 Factory Configured - Watchdog Timer jumper (E7)

Select	Jumper Position
Watchdog Timer Reset	1-2
No Watchdog Timer Reset or SERR#	**Out**
Watchdog Timer SERR#	2-3

Table 2-5 Factory Configured - Clock Speed Select Jumper (E8)

CPU Bus Frequency (MHz)	PCI Bus Frequency (MHz)	E8 Position
66.6	**33.3**	**2-3**
100	25	1-2

Table 2-6 Factory Configured - Watchdog Battery Jumper (E10)

SRAM Battery	Jumper Position
Enabled	In
Disabled	**Out**

Table 2-7 Factory Configured - Reserved Jumper (E12)

Reserved	1 - 2	Out
Reserved	2 - 3	Out

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Table 2-8 Factory Configured - DiskOnChip Address SEL Jumper (E13)

DiskOnChip	Jumper Position	
D000	**1 - 2**	**In**
E000	2 - 3	In

Table 2-9 Factory Configured - Boot Block Lock Jumper (E17)

Select	Jumper Position
Boot Block Programming	1 - 2
No Program	**2 - 3**

Table 2-10 Factory Configured - Boot Block Lock (E18)

Select	Jumper Position
Reserved	1-2
Reserved	2 -3
Reserved	**Omitted**

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Installation

The VMICPCI-7611 conforms to the CompactPCI physical specification for a 6U board. The VMICPCI-7611 is a system slot only board. It can be plugged directly into any standard chassis accepting this type of board. The following picture illustrates the symbol use to identify the slots in a standard CPCI chassis.



This symbol identifies the System Controller slot



This symbol identifies peripheral slot

CAUTION: Do not install or remove the board while power is applied.

The following steps describe the VMIC recommended method for installation and powerup of the VMICPCI-7611:

1. Make sure power to the equipment is off.
2. If a PMC module such as VMIC's VMIPMC-7441 is to be used, connect it to the VMICPCI-7611 prior to board installation. Refer to the Product Manual for that particular board for configuration and setup.
3. The VMICPCI-7611 must be installed in the designated system slot of the CompactPCI backplane (See symbols above for selection of the correct slot).

NOTE: The VMICPCI-7611 requires forced air cooling. It is advisable to install blank panels over any exposed slots. This will allow for better air flow over the VMICPCI-7611 board.

4. Insert the VMICPCI-7611 into the CompactPCI chassis system slot. While ensuring that the board is properly aligned and oriented in the supporting board guides, slide the board smoothly forward against the mating connector. Use the ejector handles to firmly seat the board.
5. All needed peripherals can be accessed from the front panel and the rear I/O VMIACC-0576 Rear Transition utility board. Each connector is clearly labeled on the front panel, and detailed pinouts are in Appendix A.
6. The VMICPCI-7611 features a Flash Disk resident on the board. Refer to Chapter 4 for set up details.
7. If an external drive module is installed, the BIOS Setup program must be run to configure the drive types. See Appendix B to properly configure the system.

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8. If a drive module is present, install the operating system according to the manufacturer's instructions.
9. A keyboard and a mouse are required if the user has not previously configured the system

BIOS Setup

The VMICPCI-7611 has an on-board BIOS Setup program that controls many configuration options. These options are saved in a special nonvolatile, battery-backed memory chip and are collectively referred to as the board's "CMOS configuration." The CMOS configuration controls many details concerning the behavior of the hardware from the moment power is applied.

The VMICPCI-7611 is shipped from the factory with hard drive type configuration set to AUTO in the CMOS.

Details of the VMICPCI-7611 BIOS setup program are included in Appendix B.

Front Panel Connectors

The front panel connections, including connector pinouts and orientation, for the VMICPCI-7611 are defined in detail in Appendix A.

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PMC Site Connector

The VMICPCI-7611 supports IEEE-P1386 Common Mezzanine Card Specification with a 5 V PMC site. Figure 2-2 shows the installation of the PMC card on the VMICPCI-7611.

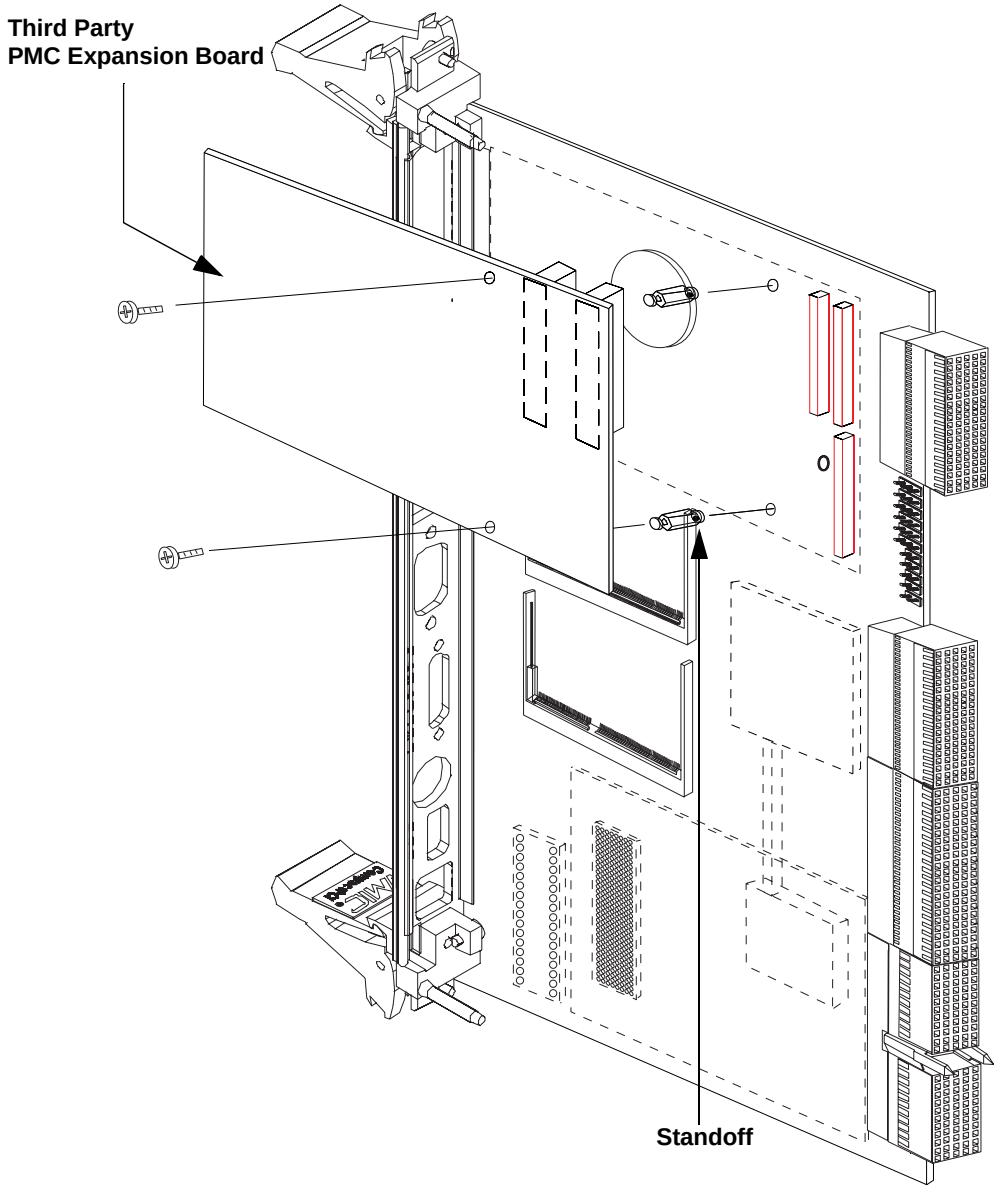
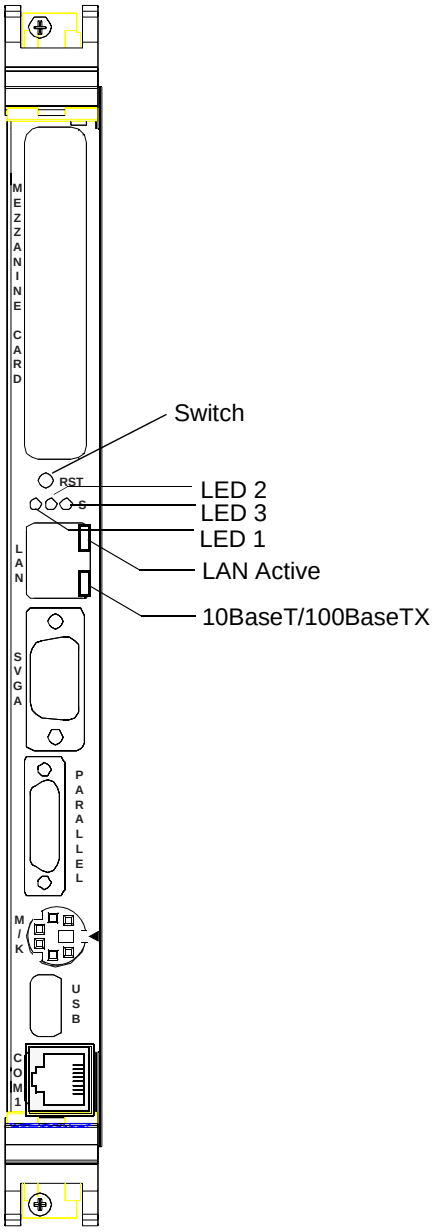


Figure 2-2 Installing a PMC Card on the VMICPCI-7611

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LED Definition



LED 1	*Power* - Indicates when power is applied to the board.
LED 2	*Hard Drive Indicator* - Indicates when hard drive activity is occurring.
LED 3	*Ready* - Indicates BIOS Boot is complete, and module is ready
Switch	*Reset* - Allows the system to be reset from the front panel.
LAN Active	Indicates the Ethernet is active, (yellow LED).
10/100BaseTX	Indicates whether 10BaseT or 100BaseTX mode. Yellow LED for 10BaseT, and Green LED for 100BaseTX.

Figure 2-3 Front Panel LED Positions

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CHAPTER

3

PC/AT Functions

Contents

CPU Socket 3-36
Physical Memory 3-36
I/O Port Map 3-37
Integrated Peripherals 3-45
Ethernet Controller 3-46
Video Graphics Adapter 3-47

Introduction

The VMICPCI-7611 is a complete IBM PC/AT-compatible Pentium II/III embedded module processor-based computer. The design includes a high-speed microprocessor with current technology memory, and optional M-Systems DiskOnChip flash. Reference the VMIC product specifications for available component options.

Because the design is PC/AT compatible, it retains standard PC memory and I/O maps along with standard interrupt architecture. Furthermore, the VMICPCI-7611 includes a PCI-compatible Ethernet controller.

The following sections describe in detail the PC/AT functions of the VMICPCI-7611.

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CPU Socket

The VMICPCI-7611 CPU socket is factory populated with a , high-speed Pentium II or Pentium III processor. The CPU speed and RAM / flash size are user-specified as part of the VMICPCI-7611 ordering information. The CPU speed is not user-upgradable.

To change CPU speeds, RAM size, or flash size contact customer service to receive a Return Material Authorization (RMA).

VMIC Customer Service is available at: 1-800-240-7782.

Physical Memory

The VMICPCI-7611 provides Synchronous DRAM (SODIMM) as on-board system memory. Memory can be accessed as bytes, words, or longwords.

The VMICPCI-7611 accepts two 144-pin SODIMM DRAM modules for a maximum memory capacity of 256 Mbyte. The on-board DRAM is dual-ported to the CPCI bus through the PCI-to-PCI bridge. The memory is addressable by the local processor.

The VMICPCI-7611 is also available with an optional M-Systems DiskOnChip flash up to 72 Mbytes. Reference the VMICPCI-7611 Product Specification for available flash memory options.

NOTE: Memory capacity may be extended as parts become available.

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I/O Port Map

The Pentium II/III processor-based CPU includes special input/output instructions that access I/O peripherals residing in I/O addressing space (separate and distinct from memory addressing space). Locations in I/O address space are referred to as *ports*. When the CPU decodes and executes an I/O instruction, it produces a 16-bit I/O address on lines A00 to A15 and identifies the I/O cycle with the M/I/O control line. Thus, the CPU includes an independent 64 Kbyte I/O address space which is accessible as bytes, words, or longwords.

Standard PC/AT hardware circuitry reserves only 1,024 byte of I/O addressing space from I/O $000 to $3FF for peripherals. All standard PC I/O peripherals such as serial and parallel ports, hard and floppy drive controllers, video system, real-time clock, system timers, and interrupt controllers are addressed in this region of I/O space. The BIOS initializes and configures all these registers properly; adjusting these I/O ports directly is not normally necessary.

The assigned and user-available I/O addresses are summarized in the I/O Address Map, Table 3-1.

Table 3-1 VMICPCI-7611 I/O Address Map

I/O ADDRESS RANGE	SIZE IN BYTES	HW DEVICE	PC/AT FUNCTION
$000 - $00F	16		DMA Controller 1 (Intel 8237A Compatible)
$010 - $01F	16		Reserved
$020 - $021	2		Master Interrupt Controller (Intel 8259A Compatible)
$022 - $03F	30		Reserved
$040 - $043	4		Programmable Timer (Intel 8254 Compatible)
$044 - $05F	30		Reserved
$060 - $064	5		Keyboard, Speaker, Eqpt. Configuration (Intel 8042 Compatible)
$065 - $06F	11		Reserved
$070 - $071	2		Real-Time Clock
$072 - $07F	14		Reserved
$080 - $08F	16		DMA Page Registers
$090 - $091	2		Reserved
$092	1		Alt. Gate A20/Fast Reset Register
$093	1		Reserved

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Table 3-1 VMICPCI-7611 I/O Address Map (Continued)

I/O ADDRESS RANGE	SIZE IN BYTES	HW DEVICE	PC/AT FUNCTION
$094	1		
$095 - $09F	11		Reserved
$0A0 - $0A1	2		Slave Interrupt Controller (Intel 8259A Compatible)
$0A2 - $0BF	30		Reserved
$0C0 - $0DF	32		DMA Controller 2 (Intel 8237A Compatible)
$0E0 - $16F	142		Reserved
$170 - $177	8	PIIX4E	Secondary Hard Disk Controller
$178 - $1EF	120		User I/O
$1F0 - $1F7	8	PIIX4E	Primary Hard Disk Controller
$1F8 - $277	128		User I/O
$278 - $27F	8	I/O Chip*	LPT2 Parallel I/O*
$280 - $2E7	104		Reserved
$2E8 - $2EE	7	UART*	COM4 Serial I/O*
$2EF - $2F7	9		User I/O
$2F8 - $2FE	7	Super-I/O Chip	COM2 Serial I/O (16550 Compatible)
$2FF - $36F	113		Reserved
$370 - $377	8	Super-I/O Chip	Secondary Floppy Disk Controller
$378 - $37F	8	Super-I/O Chip	LPT1 Parallel I/O
$380 - $3E7	108		Reserved
$3E8 - $3EE	7	UART*	COM3 Serial I/O*
$3F0 - $3F7	8	Super-I/O Chip	Primary Floppy Disk Controller
$3F8 - $3FE	7	Super-I/O Chip	COM1 Serial I/O (16550 Compatible)
$3FF - $4FF			Reserved
$500 - $503	4	Watchdog Timer	Programmable Watchdog Timer
$504 - CFF			Reserved

* While these I/O ports are reserved for the listed functions, they are not implemented on the VMICPCI-7611. They are listed here to make the user aware of the standard PC/AT usage of these ports.

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PCI-to-PCI Bridge

The VMICPCI-7611 uses the Intel 21154 PCI-to-PCI bridge to interface between the primary PCI bus of unit and the CompactPCI (CPCI) bus. The CompactPCI bus appears as a secondary PCI bus, and all devices in the seven peripheral slots of the CPCI chassis are auto detected by the BIOS and respond to normal PCI accesses.

PC/AT Interrupts

In addition to an I/O port address, an I/O device has a separate hardware interrupt line assignment. Assigned to each interrupt line is a corresponding interrupt vector in the 256-vector interrupt table at $00000 to $003FF in memory. The 16 maskable interrupts and the single Non-Maskable Interrupt (NMI) are listed in Table 3-2 along with their functions. Table 3-3 on page 40 details the vectors in the interrupt vector table. The interrupt number in HEX and decimal are also defined for real and protected mode in Table 3-3 on page 40.

The interrupt hardware implementation on the VMICPCI-7611 is standard for computers built around the PC/AT architecture, which evolved from the IBM PC/XT. In the IBM PC/XT computers, only eight interrupt request lines exist, numbered from IRQ0 to IRQ7 at the PIC. The IBM PC/AT computer added eight more IRQx lines, numbered IRQ8 to IRQ15, by cascading a second slave PIC into the original master PIC. IRQ2 at the master PIC was committed as the cascade input from the slave PIC. This architecture is represented in Figure 3-1 on page 44.

To maintain backward compatibility with PC/XT systems, IBM chose to use the new IRQ9 input on the slave PIC to operate as the old IRQ2 interrupt line on the PC/XT Expansion Bus. Thus, in AT systems, the IRQ9 interrupt line connects to the old IRQ2 pin (pin B4) on the AT Expansion Bus (or ISA bus).

Table 3-2 PC/AT Hardware Interrupt Line Assignments

IRQ	AT FUNCTION	COMMENTS
NMI	Parity Errors (Must be enabled in BIOS Setup)	Used by VMICPCI-7611 PCIbus Interface
0	System Timer	Set by BIOS Setup
1	Keyboard	Set by BIOS Setup
2	Duplexed to IRQ9	
3	COM2/COM4	
4	COM1/COM3	
5	LPT2	
6	Floppy Controller	
7	LPT1	
8	Real-Time Clock	

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Table 3-2 PC/AT Hardware Interrupt Line Assignments (Continued)

IRQ	AT FUNCTION	COMMENTS
9	Old IRQ2	SVGA or Network I/O
10	Not Assigned	Determined by BIOS
11	Not Assigned	Determined by BIOS
12	Mouse	
13	Math Coprocessor	
14	AT Hard Drive	
15	Flash Drive	

Table 3-3 PC/AT Interrupt Vector Table

INTERRUPT NO.		IRQ LINE	REAL MODE	PROTECTED MODE
HEX	DEC			
00	0		Divide Error	Same as Real Mode
01	1		Debug Single Step	Same as Real Mode
02	2	NMI	Memory Parity Error, CompactPCI Interrupts	Same as Real Mode (Must be enabled in BIOS Setup)
03	3		Debug Breakpoint	Same as Real Mode
04	4		ALU Overflow	Same as Real Mode
05	5		Print Screen	Array Bounds Check
06	6			Invalid OpCode
07	7			Device Not Available
08	8	IRQ0	Timer Tick	Double Exception Detected
09	9	IRQ1	Keyboard Input	Coprocessor Segment Overrun
0A	10	IRQ2	BIOS Reserved	Invalid Task State Segment
0B	11	IRQ3	COM2 Serial I/O	Segment Not Present
0C	12	IRQ4	COM1 Serial I/O	Stack Segment Overrun
0D	13	IRQ5	Timer	Same as Real Mode
0E	14	IRQ6	Floppy Disk Controller	Page Fault
0F	15	IRQ7	LPT1 Parallel I/O	Unassigned
10	16		BIOS Video I/O	Coprocessor Error

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Table 3-3 PC/AT Interrupt Vector Table (Continued)

INTERRUPT NO.		IRQ LINE	REAL MODE	PROTECTED MODE
HEX	DEC			
11	17		Eqpt Configuration Check	Same as Real Mode
12	18		Memory Size Check	Same as Real Mode
13	19		XT Floppy / Hard Drive	Same as Real Mode
14	20		BIOS Comm I/O	Same as Real Mode
15	21		BIOS Cassette Tape I/O	Same as Real Mode
16	22		BIOS Keyboard I/O	Same as Real Mode
17	23		BIOS Printer I/O	Same as Real Mode
18	24		ROM BASIC Entry Point	Same as Real Mode
19	25		Bootstrap Loader	Same as Real Mode
1A	26	IRQ8	Real-Time Clock	Same as Real Mode
1B	27		Control/Break Handler	Same as Real Mode
1C	28		Timer Control	Same as Real Mode
1D	29		Video Parameter Table Pntr	Same as Real Mode
1E	30		Floppy Parm Table Pntr	Same as Real Mode
1F	31		Video Graphics Table Pntr	Same as Real Mode
20	32		DOS Terminate Program	Same as Real Mode
21	33		DOS Function Entry Point	Same as Real Mode
22	34		DOS Terminate Handler	Same as Real Mode
23	35		DOS Control/Break Handler	Same as Real Mode
24	36		DOS Critical Error Handler	Same as Real Mode
25	37		DOS Absolute Disk Read	Same as Real Mode
26	38		DOS Absolute Disk Write	Same as Real Mode
27	39		DOS Program Terminate, Stay Resident	Same as Real Mode
28	40		DOS Keyboard Idle Loop	Same as Real Mode
29	41		DOS CON Dev. Raw Output	Same as Real Mode
2A	42		DOS 3.x+ Network Comm	Same as Real Mode

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Table 3-3 PC/AT Interrupt Vector Table (Continued)

INTERRUPT NO.		IRQ LINE	REAL MODE	PROTECTED MODE
HEX	DEC			
2B	43		DOS Internal Use	Same as Real Mode
2C	44		DOS Internal Use	Same as Real Mode
2D	45		DOS Internal Use	Same as Real Mode
2E	46		DOS Internal Use	Same as Real Mode
2F	47		DOS Print Spooler Driver	Same as Real Mode
30-60	48-96		Reserved by DOS	Same as Real Mode
61-66	97-102		User Available	Same as Real Mode
67-71	103-113		Reserved by DOS	Same as Real Mode
72	114	IRQ10	Not Assigned	
73	115	IRQ11	Not Assigned	
74	116	IRQ12	Mouse	
75	117	IRQ13	Math Coprocessor	
76	118	IRQ14	AT Hard Drive	
77	119	IRQ15	Flash Drive	
78-7F	120-127		Reserved by DOS	Same as Real Mode
80-F0	128-240		Reserved for BASIC	Same as Real Mode
F1-FF	241-255		Reserved by DOS	Same as Real Mode

PCI Interrupts

Interrupts on Peripheral Component Interconnect (PCI) Local Bus are optional and defined as “level sensitive,” asserted low (negative true), using open drain output drivers. The assertion and de-assertion of an interrupt line, INTx#, is asynchronous to CLK. A device asserts its INTx# line when requesting attention from its device driver. Once the INTx# signal is asserted, it remains asserted until the device driver clears the pending request. When the request is cleared, the device de-asserts its INTx# signal.

PCI defines one interrupt line for a single function device and up to four interrupt lines for a multifunction device or connector. For a single function device, only INTA# may be used while the other three interrupt lines have no meaning. Figure 3-1 on page 44 depicts the VMICPCI-7611 interrupt logic pertaining to CompactPCI operations and the PMC site.

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Any function on a multifunction device can be connected to any of the INTx# lines. The Interrupt Pin register defines which INTx# line the function uses to request an interrupt. If a device implements a single INTx# line, it is called INTA#; if it implements two lines, they are called INTA# and INTB#; and so forth. For a multifunction device, all functions may use the same INTx# line or each may have its own (up to a maximum of four functions) or any combination thereof. A single function can never generate an interrupt request on more than one INTx# line.

The slave PIC accepts the CompactPCI interrupts through lines that are defined by the BIOS. The BIOS defines which interrupt line to utilize depending on which system requires the use of the line.

The PCI-to-PCI Bridge has the capability of generating a Non-Maskable Interrupt (NMI) via the PCI SERR# line. Table 3-4 describes the register bits that are used by the NMI. The SERR interrupt is routed through logic back to the NMI input line on the CPU. The CPU reads the NMI Status Control register to determine the NMI source (bits set to 1). After the NMI interrupt routine processes the interrupt, software clears the NMI status bits by setting the corresponding enable / disable bit to 1. The NMI Enable and Real-Time Clock register can mask the NMI signal and disable / enable all NMI sources.

Table 3-4 NMI Register Bit Descriptions

Status Control Register (I/O Address $061, Read/Write, Read Only)	
Bit 7	SERR# NMI Source Status (Read Only) - This bit is set to 1 if a system board agent detects a system board error. It then asserts the PCI SERR# line. To reset the interrupt, set bit 2 to 0 and then set it to 1. When writing to port $061, bit 7 must be 0.
Bit 2	PCI SERR# Enable (Read/Write) - 1 = Clear and Disable, 0 = Enable
Enable and Real-Time Clock Address Register (I/O Address $070, Write Only)	
Bit 7	NMI Enable - 1 = Disable, 0 = Enable

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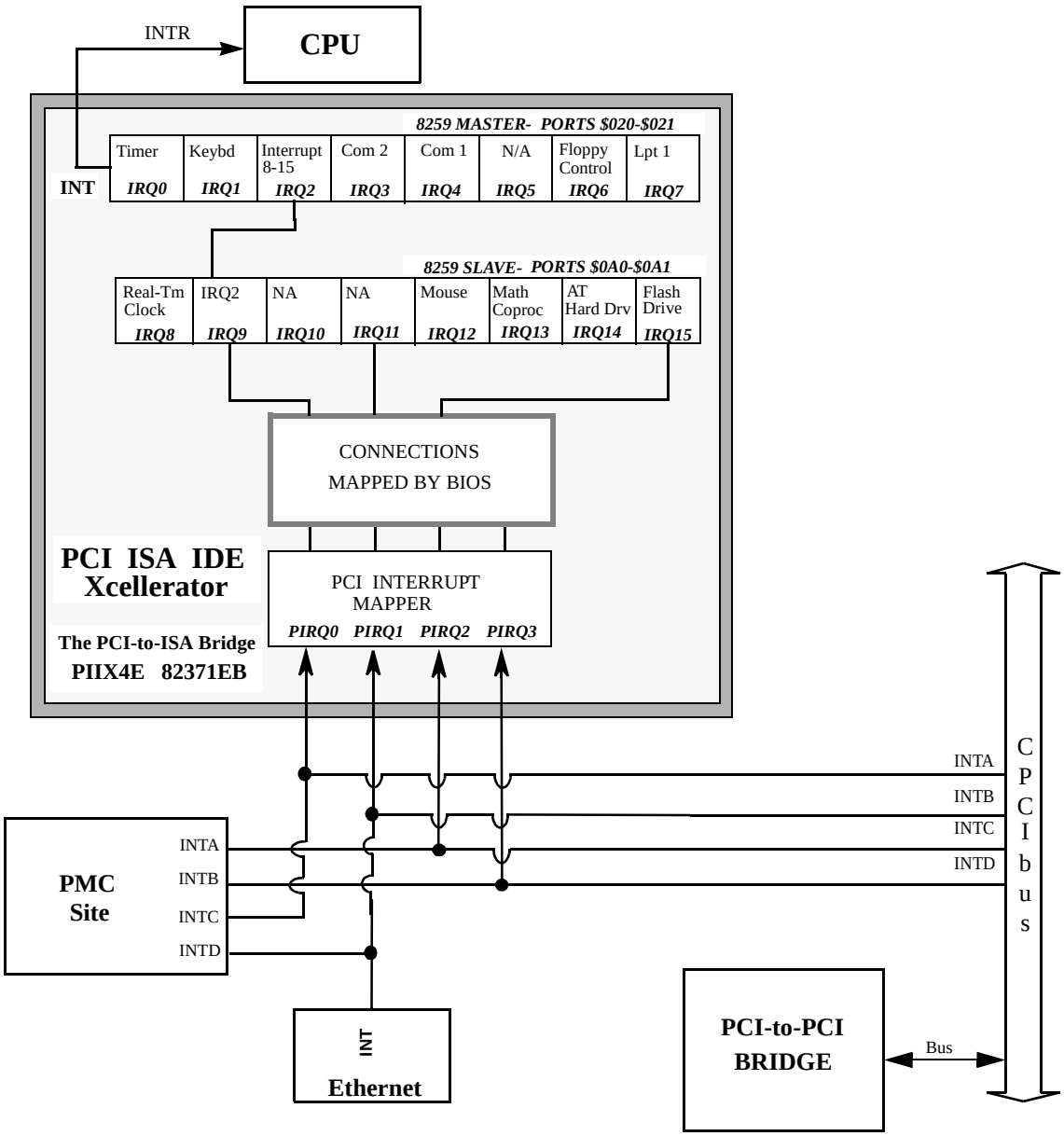


Figure 3-1 Connections for the PC Interrupt Logic Controller

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Integrated Peripherals

The VMICPCI-7611 incorporates the SMC Super-I/O chip. The SMC chip provides the VMICPCI-7611 with a standard floppy drive controller, two 16550 UART-compatible serial ports, and one enhance parallel port with ECP/EPP modes. The Ultra-EIDE hard drive interface and two USB ports are provided by the Intel 82371EB (PIIX4E) PCI ISA IDE Xcelerator chip. All ports are located on the CPCI J3 connector.

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Ethernet Controller

The network capability is provided by the Intel 82559 Ethernet Controller. This Ethernet controller is PCI bus based and is software configurable. The VMICPCI-7611 supports 10BaseT and 100BaseTx Ethernet.

10BaseT

A network based on the 10BaseT standard uses unshielded twisted-pair cables, providing an economical solution to networking by allowing the use of existing telephone wiring and connectors. The RJ-45 connector is used with the 10BaseT standard. 10BaseT has a maximum length of 100 meters from the wiring hub to the terminal node.

100BaseTx

The VMICPCI-7611 also supports the 100BaseTx Ethernet. A network based on a 100BaseTx standard uses unshielded twisted-pair cables and a RJ-45 connector. The 100BaseTx has a maximum deployment length of 100 meters.

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Video Graphics Adapter

The monitor port on the VMIPMC-7611 is controlled by a Chips and Technology 69000 video adapter chip with 2 Mbyte video SDRAM. The video controller chip is hardware and BIOS compatible with the IBM EGA and SXGA standards and also supports VESA high-resolution and extended video modes. Table 3-5 shows the graphics video modes supported by the VMICPCI-7611.

Table 3-5 Supported Graphics Video Resolutions

SCREEN RESOLUTION	MAXIMUM COLORS	REFRESH RATES (Hz)
640 x 480	16 M	60, 75, 85
800 x 600	16 M	60, 75, 85
1024 x 768	64 K	60, 75, 85
1280 x 1024	256	60, 75

Not all SVGA monitors support resolutions and refresh rates beyond 640 x 480 at 60 Hz. Do not attempt to drive a monitor to a resolution or refresh rate beyond its capability.

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CHAPTER

4

Embedded PC/RTOS Features

Contents

DiskOnChip (Optional) 50
Watchdog Timer 52

Introduction

VMIC's VMICPCI-7611 features additional capabilities beyond those of a typical IBM PC / AT-compatible CPU. The unit provides a programmable Watchdog timer for synchronizing and controlling multiple events in embedded applications. The VMICPCI-7611 also provides a bootable Flash Disk system. These features make the unit ideal for embedded applications, particularly applications where standard hard drives and floppy disk drives cannot be used.

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DiskOnChip (Optional)

The VMICPCI-7611 is available with an optional single DiskOnChip which is plugged into a standard 32-pin EEPROM socket. The DiskOnChip is mapped into an 32 Kbyte window in the BIOS expansion address space of the PC, which is located between address 0xD0000 to 0xD1FFF.

The DiskOnChip contains a built-in copy of the M-Systems industry-standard TrueFFS software, which makes the DiskOnChip operate as a standard disk drive. The DiskOnChip can contain the operating system in it to allow systems to boot without a hard disk. The DiskOnChip can also be configured as the boot device in systems with a hard disk.

Installing the DiskOnChip

1. To install the DiskOnChip as drive C on a system without a hard disk, set the CMOS setup of the Primary Master and Primary Slave to Not Installed (indicating that no physical magnetic disk is installed), and reboot the computer. The DiskOnChip will install as drive C. The DiskOnChip needs to be formatted with the System files in order for it to be a bootable drive. See “Configuring the DiskOnChip as the Boot Device” below.
2. To install the DiskOnChip as a logical drive on a system with a hard disk, just reboot the system, and the DiskOnChip will install as the last drive.
3. To install the DiskOnChip as drive C on a system with a hard disk, see “Configuring the DiskOnChip as the First Drive”.

NOTE: The active (bootable) partition will always be drive C.

Configuring the DiskOnChip as the Boot Device

In order to configure the DiskOnChip as the boot device, the operating system files need to be copied into the chip. Copying the operating system files into the DiskOnChip should be done in the same manner as any other hard disk. The following is a example of a typical initialization process:

1. Set the DiskOnChip as a regular drive in your system (not a boot drive).
2. Insert a bootable floppy diskette in drive A and boot the system.
3. At the DOS prompt, type SYS C: to transfer the DOS system files to the DiskOnChip (assuming the DiskOnChip is installed as drive C).
4. Copy any files needed into the DiskOnChip.
5. Remove the floppy diskette and reboot the system. The system will boot from the DiskOnChip and will allow you to run and access any files that have been copied into the DiskOnChip.

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Using the DiskOnChip with Other Operating Systems

If the VMICPCI-7611 is to be used with a DiskOnChip running an operating system other than DOS, the user should access the M-Systems website at www.m-sys.com for information on installation and other details.

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Watchdog Timer

The VMICPCI-7611 utilizes a Dallas DS1284 Watchdog Timekeeping Controller as its Watchdog Timer. The device provides a Time of Day feature and a Watchdog Alarm. The Time of Day feature found within the DS1284 device is explained in this section. The actual Time of Day registers used by the VMICPCI-7611 are located at the standard PC/AT I/O address. The Time of Day feature in the DS1284 Watchdog Timer is available for use by the user at their discretion.

The Watchdog Timer provides a Watchdog alarm window and interval timing between 0.01 and 99.99 seconds. If enabled, and if jumper E7 pins 1 and 2 are loaded, the Watchdog alarm will reset the CPU to a known state if not accessed during the alarm window.

Figure 4-2 shows a generalized block diagram of how the Watchdog Timer is used in the VMICPCI-7611. The Watchdog Timer registers are I/O-mapped at address $500 through $50D. Table 4-6 on page 53 shows the address, content and the range of each Watchdog Register.

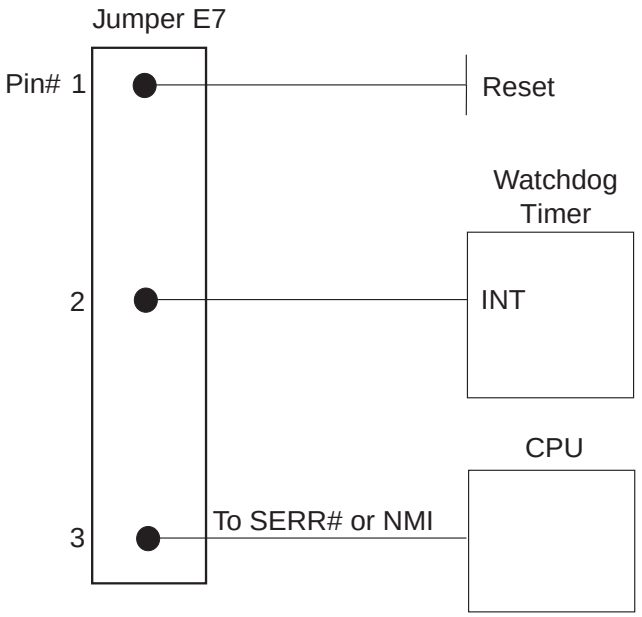


Figure 4-2 Watchdog Alarm Block

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Table 4-6 Watchdog Registers

Register	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Range
0	$500	0.1 Seconds (BCD)				0.01 Seconds (BCD)				00 - 99
1	$501	10 Seconds (BCD)				Seconds (BCD)				00 - 59
2	$502	10 Minutes (BCD)				Minutes (BCD)				00 - 59
3	$503	M	10 Minute Alarm (BCD)			Minute Alarm (BCD)				00 - 59
4	$504	0	12 / 24	AM / PM *	10 Hr	Hours (BCD)				
5	$505	M	12 / 24	AM / PM *	10 Hr	Hour Alarm (BCD)				
6	$506	0	0	0	0	Days (BCD)				01 - 07
7	$507	M	0	0	0	Day Alarm (BCD)				01 - 07
8	$508	0	0	10 Date (BCD)		Date (BCD)				01 - 31
9	$509	Eosc	1**	0	10 Mo	Months (BCD)				01 - 12
A	$50A	10 Years (BCD)				Years (BCD)				00 - 99
B	$50B	Te	Ipsw	Ibh / lo	Pu / lvl	Wam	Tdm	Waf	Tdf	
C	$50C	0.1 Seconds (BCD)				0.01 Seconds (BCD)				00 - 99
D	$50D	10 Seconds (BCD)				Seconds (BCD)				00 - 99

* In the 12 hour mode bit 5 determines AM (0) or PM (1). In the 24 hour mode bit 5 combines with Bit 4 to represent the 10 hour value.
** Bit 6 of Register 9 must be set to a 1. If set to a 0, an unused square wave will be generated in the circuit.

Registers 0 through A are Clock, Calendar, Time of Day Registers.
Register B is the Command Register.
Registers C and D are Watchdog Alarm Registers.

The Watchdog Timer contains 14 registers which are 8-bits wide. These registers contain all of the Time of Day, Alarm, Watchdog, Control, and Data information. The Clock Calendar, Alarm, and Watchdog Registers have both external (user accessible) and internal memory locations containing copies of the data. The external memory locations are independent of the internal functions except that they are updated periodically by the transfer of the incremented internal values. Registers 0, 1, 2, 4, 6, 8, 9, and A contain Time of Day and Data information in Binary Coded Decimal (BCD). Registers 3, 5, and 7 contain the Time of Day Alarm information in BCD. The Command Register (Register B) contains data in binary. The Watchdog Alarm Registers are Registers C and D and information stored in these registers is in BCD.

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Time of Day Registers

Registers 0, 1, 2, 4, 6, 8, 9, and A contain Time of Day data in BCD.

Register 0 contains two Time of Day values. Bits 3 - 0 contain the 0.01 Seconds value with a range of 0 to 9 in BCD while Bits 7 - 4 contain the 0.1 Seconds value with a range of 0 to 9 in BCD. This Register has a total range of 0.00 to 0.99 Seconds.

Register 1 contains two Time of Day values. Bits 3 - 0 contain the 1 Seconds value with a range of 0 to 9 in BCD while Bits 7 - 4 contain the 10 Seconds value with a range of 0 to 5 in BCD. This Register has a total range of 0.0 to 59.0 Seconds. Bit 7 of this register will always be zero regardless of what value is written to it.

Register 2 contains two Time of Day values. Bits 3 - 0 contain the 1 Minutes value with a range of 0 to 9 in BCD while Bits 7 - 4 contain the 10 Minutes value with a range of 0 to 5 in BCD. This Register has a total range of 0 to 59 Minutes. Bit 7 of this register will always be zero regardless of what value is written to it.

Register 4 contains the Hours value of the Time of Day. The Hours can be represented in either 12 or 24 hour format depending on the state of Bit 6. When Bit 6 is set to a one (1) the format is 12 hour. When Bit 6 is set to a zero (0) the format is 24 hour. For the 12 hour format Bits 3 - 0 contain the 1 Hour value with a range of 0 to 9 in BCD and Bit 4 contains the 10 Hour value with a range of 0 to 1. In the 12 hour format Bit 5 is used as the AM / PM bit. When AM Bit 5 is a zero (0) and when PM bit 5 is a one (1). The total range of this register in the 12 hour format is 01 AM to 12 AM and 01 PM to 12 PM.

When Register 4 is in 24 hour format (Bit 6 is set to a zero (0)) Bits 3 - 0 contain the 1 Hour value with a range of 0 to 9 in BCD, Bit 5 combines with 4 to represent the 10 Hour value. The 10 Hour range is from 0 to 2. The total range of register 4 in the 24 hour format is 00 to 23 hours. Bit 7 of register 4 will always be zero regardless of what value is written to it and regardless of format (12 or 24 hour).

Register 6 contains the Days value of the Time of Day. Bits 2 - 0 contain the Days value with a range of 1 to 7 in BCD.

Register 8 contains two Time of Day values. Bits 3 - 0 contain the Date value with a range of 0 to 9 in BCD while Bits 5 - 4 contain the 10 Date value with a range of 0 to 3. This Register has a total range of 01 to 31. Bits 7 - 6 of this register will always be zero regardless of what value is written to it.

Register 9 contains two Time of Day values. Bits 3 - 0 contain the Months value with a range of 0 to 9 in BCD while Bits 4 contain the 10 Date value with a range of 0 to 1. This Register has a total range of 01 to 12. Bit 5 will always be zero regardless of what value is written to it. Bit 6 is unused but must be set to a 1. Bit 7, $\overline{\text{Eosc}}$, is the clock oscillator enable bit. When this bit is set to a zero (0) the oscillator is internally enabled. When set to a one (1) the oscillator is internally disabled. The oscillator via this bit is usually turned on once during system initialization but can be toggled on and off at the users discretion.

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There are two techniques for reading the Time of Day from the Watchdog Timer. The first is to halt the External Time of Day Registers from tracking the Internal Time of Day Registers by setting the Te bit (Bit 7 of the Command Register) to a logic zero (0) then reading the contents of the Time of Day Registers. Using this technique eliminates the chance of the Time of Day changing while the read is taking place. At the end of the read, the Te bit is set to a logic one (1) allowing the external Time of Day Registers to resume tracking the internal Time of Day Registers. No time is lost as the internal Time of Day Registers continue to keep time while the external Time of Day Registers are halted. This is the recommended method.

The second technique for reading the Time of Day from the Watchdog Timer is to read the external Time of Day Registers without halting the tracking of the Internal Registers. This is not recommended as the registers may be updated while the reading is taking place, resulting in erroneous data being read.

Time of Day Alarm Registers

Registers 3, 5, and 7 are the Time of Day Alarm Registers and are formatted similar to Register 2, 4, and 6 respectively. Bit 7 of registers 3, 5, and 7 is a mask bit. The mask bits, when active (logic one (1)), disable the use of the particular Time of Day Alarm Register in the determination of the Time of Day Alarm (see Table 4-7). When all the mask bits are low (0) an alarm will occur when Registers 2, 4, and 6 match the values found in registers 3, 5, and 7. When Register 7's mask bit is set to a logic one (1) Register 6 will be disregarded in the determination of the Time of Day alarm and an alarm will occur everyday. When Registers 7 and 5's mask bit is set to a logic one (1), Register 6 and 4 will be disregarded in the determination of the Time of Day alarm and an alarm will occur every hour. When Registers 7, 5 and 3's mask bit is set to a logic one (1), Register 6, 4, and 2 will be disregarded in the determination of the Time of Day alarm and an alarm will occur every minute (when Register 1's seconds step from 59 to 00).

Table 4-7 Time of Day Alarm Registers

Register			Comment
Minutes	Hours	Days	
1	1	1	Alarm once per minute
0	1	1	Alarm when minutes match
0	0	1	Alarm when hours and minutes match
0	0	0	Alarm when hours, minutes, and days match

The Time of Day Alarm registers are read and written to in the same format as the Time of Day registers. The Time of Day alarm flag and interrupt are cleared when the alarm registers are read or written.

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Watchdog Alarm Registers

Register C contains two Watchdog alarm values. Bits 3 - 0 contain the 0.01 Seconds value with a range of 0 to 9 in BCD while Bits 7 - 4 contain the 0.1 Seconds value with a range of 0 to 9 in BCD. This Register has a total range of 0.00 to 0.99 Seconds.

Register D contains two Watchdog Alarm values. Bits 3 - 0 contain the 1 Second value with a range of 0 to 9 in BCD while Bits 7 - 4 contain the 10 Seconds value with a range of 0 to 9 in BCD. This Register has a total range of 00.0 to 99.0 Seconds.

The Watchdog Alarm Registers can be read or written in any order. When a new value is entered or the Watchdog registers are read, the Watchdog Timer will start counting down from the entered value. When zero is reached the Watchdog Interrupt Output will go active. If jumper E7 is loaded, the CPU will reset to a known state, refer to Figure 4-2 on page 52. The Watchdog Timer count is reinitialized back to the entered value, the Watchdog flag bit is cleared, and the Watchdog interrupt output is cleared every time either of the registers are accessed. Periodic accesses to the Watchdog Timer will prevent the Watchdog Alarm from occurring. If access does not occur, the alarm will be repetitive. The Watchdog Alarm Register always reads the entered value. The actual countdown value is internal and not accessible to the user. Writing zero's to Registers C and D will disable the Watchdog Alarm feature.

Command Register

Register B is the Command Register. Within this register are mask bits, control bits, and flag bits. The following paragraphs describe each bit.

Te - Bit 7 Transfer Enable - This bit enables and disables the tracking of data between the internal and external registers. When set to a logic zero (0), tracking is disabled that is the data in the external register is frozen. When set to a logic one (1), tracking is enabled. This bit must be set to a logic one (1) to allow the external register to be updated.

Ipsw - Bit 6 Interrupt Switch - This bit toggles the Interrupt Output between the Time of Day Alarm and the Watchdog Alarm. When set to a logic zero (0), the Interrupt Output is from the Watchdog Alarm. When set to a logic one (1), the Interrupt Output is from the Time of Day Alarm.

Ibh/lo - Bit 5 Reserved - This bit should be set to a logic low (0).

Pu/lvl - Bit 4 Interrupt Pulse Mode or Level Mode - This bit determines whether the Interrupt Output will output as a pulse or a level. When set to a logic zero (0), Interrupt Output will be a level. When set to a logic one (1), Interrupt Output will be a pulse. In pulse mode the Interrupt Output will sink current for a minimum of 3 ms. This bit should be set to a logic one (1).

Wam - Bit 3 Watchdog Alarm Mask - Enables / Disables the Watchdog Alarm to Interrupt Output when Ipsw (Bit 6, Interrupt Switch) is set to logic zero (0). When set to a logic zero (0), Watchdog Alarm Interrupt Output will be enabled. When set to a logic one (1), Watchdog Alarm Interrupt Output will be disabled.

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Tdm - Bit 2 Time of Day Alarm Mask - Enables / Disables the Time of Day Alarm to Interrupt Output when Ipsw (see Bit 6, Interrupt Switch) is set to logic one (1). When set to a logic zero (0), Time of Day Alarm Interrupt Output will be enabled. When set to a logic one (1), Time of Day Alarm Interrupt Output will be disabled.

Waf - Bit 1 Watchdog Alarm Flag - This is a read-only bit set to a logic one (1) when a Watchdog Alarm Interrupt occurs. This bit is reset when any of the Watchdog Alarm registers are accessed. When the Interrupt Output is set to Pulse Mode (see Bit 4, Interrupt Pulse Mode or Level Mode), the flag will be set to a logic one (1) only when the Interrupt Output is active.

Tdf - Bit 0 Time of Day Alarm Flag - This is a read-only bit set to a logic one (1) when a Time of Day Alarm Interrupt occurs. This bit is reset when any of the Time of Day Alarm registers are accessed. When the Interrupt Output is set to Pulse Mode (see Bit 4, Interrupt Pulse Mode or Level Mode), the flag will be set to a logic one (1) only when the Interrupt Output is active.

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CHAPTER 5

Maintenance

If a VMIC product malfunctions, please verify the following:

1. Software resident on the product
2. System configuration
3. Electrical connections
4. Jumper or configuration options
5. Boards are fully inserted into their proper connector location
6. Connector pins are clean and free from contamination
7. No components or adjacent boards were disturbed when inserting or removing the board from the chassis
8. Quality of cables and I/O connections

If products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return**.

VMIC Customer Service is available at: 1-800-240-7782.
Or E-mail us at customer.service@vmic.com

Maintenance Prints

User level repairs are not recommended. The drawings and diagrams in this manual are for reference purposes only.

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Appendix

A

Connector Pinouts

Contents

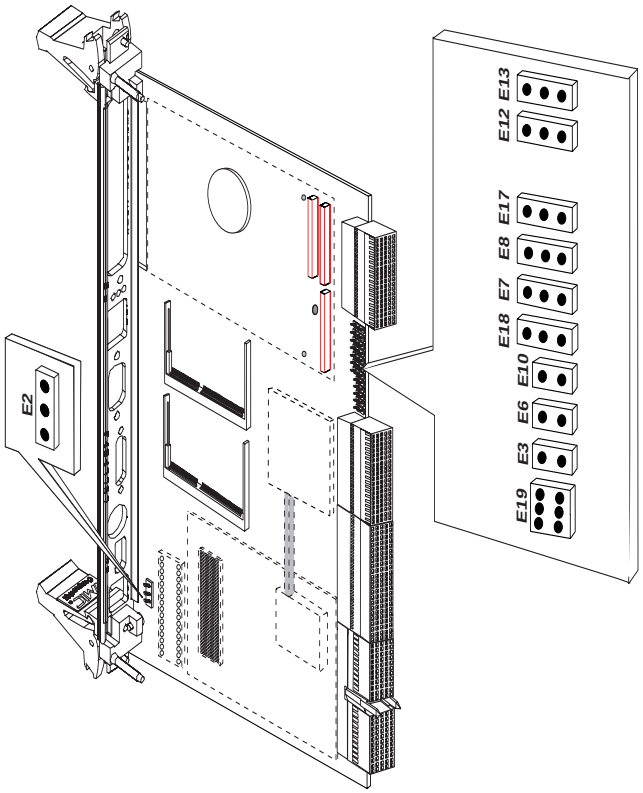
J1 Connector Pinout 63
J2 Connector and Pinout 64
J3 Connector Pinout 65
J5 Connector and Pinout 66
Keyboard and Mouse Connectors and Pinout (J10) 70
PMC Connector Pinout 72

Introduction

The VMICPCI-7611 PC / AT-Compatible CompactPCI® Controller has several connectors for its I / O ports. Figure A-1 shows the locations of the connectors on the VMICPCI-7611. Wherever possible, the VMICPCI-7611 uses connectors and pinouts typical for any desktop PC. This ensures maximum compatibility with a varity of systems.

Connector diagrams in this appendix are generally shown in a natural orientation with the controller board mounted in a CPCI bus chassis.

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VMICPCI-7611 Jumper Configuration	
E18: Boot Block Lock Pins 1 and 2 Reserved Pins 2 and 3 Reserved **Omitted = Reserved**	**E8: CPU Clock Speed SEL** Pins 1 and 2 IN = 100 MHz **Pins 2 and 3 IN = 66 MHz**
E17: BIOS Mode Option Pins 1 and 2 = Boot Block Prgm **Pins 2 and 3 = Boot Block No Prgm**	**E7: Watchdog Timer SEL** Pins 1 and 2 IN = RTCRESET# Pins 2 and 3 IN = SERR#
E13: DiskOnChip Address SEL **Pins 1 and 2 IN = D000** Pins 2 and 3 IN = E000	**E6: PIIX4E Battery** **Pins 1 and 2 IN = Battery Enabled** Pins 1 and 2 OUT = Battery Disabled
E12: Reserved	**E3: Password Clear** Pins 1 and 2 IN = Clear Password
E10: Watchdog Battery SEL **Pins 1 and 2 OUT = Disabled**	**E2: Fan Connector**

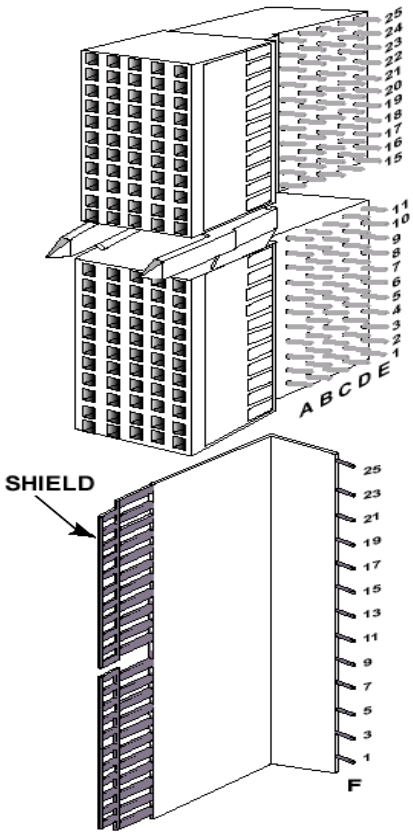
Bold = Default Factory Configuration

Figure A-1 VMICPCI-7611 Connector and Jumper Locations

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J1 Connector Pinout

The VMICPCI-7611 utilitizes a high-density 110-pin, low inductance, and controlled impedance connector. This connector meets the IEC-1076 international standard for CompactPCI connectors. An additional external metal shield is required. The large number of ground pins ensures adequate shielding and grounding for low ground bounce and reliable operation in noisy environments. The key prevents mis-alignment of the board when installing in the chassis. Figure A-2 below depicts the J1 connector and the connector pinout.



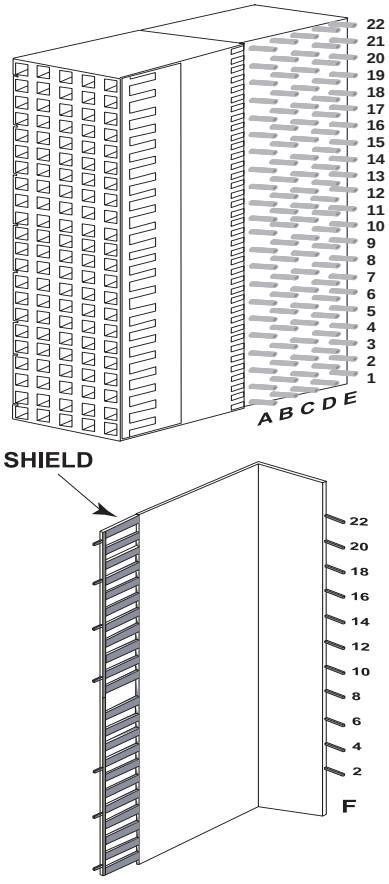
Pin No.	Row A	Row B	Row C	Row D	Row E	Row F
25	+5 V	C_REQ64#	C_ENUM	CPCI_3.3	+5 V	GND
24	C_AD[1]	+5 V	CPCI_VIO	C_AD[0]	C_ACK64#	N/C
23	CPCI_3.3	C_AD[4]	C_AD[3]	+5 V	C_AD[2]	GND
22	C_AD[7]	GND	CPCI_3.3	C_AD[6]	C_AD[5]	N/C
21	CPCI_3.3	C_AD[9]	C_AD[8]	GND	C_C/BE0#	GND
20	C_AD[12]	GND	CPCI_VIO	C_AD[11]	C_AD[10]	N/C
19	CPCI_3.3	C_AD[15]	C_AD[14]	GND	C_AD[13]	GND
18	C_SERR#	GND	CPCI_3.3	C_PAR	C_C/BE1#	N/C
17	CPCI_3.3	C_SDONE	C_SB0#	GND	C_PERR#	GND
16	C_DEVSEL#	GND	CPCI_VIO	C_STOP#	C_LOCK#	N/C
15	CPCI_3.3	C_FRAME	C_IRDY#	GND	C_TRDY#	GND
14 lost to the keying area						N/C
13 lost to the keying area						GND
12 lost to the keying area						N/C
11	C_AD[18]	C_AD[17]	C_AD[16]	GND	C_C/BE2#	GND
10	C_AD[21]	GND	CPCI_3.3	C_AD[20]	C_AD[19]	N/C
9	C_CBE3#	N/C	C_AD[23]	GND	C_AD[22]	GND
8	C_AD[26]	GND	CPCI_VIO	C_AD[25]	C_AD[24]	N/C
7	C_AD[30]	C_AD[29]	C_AD[28]	GND	C_AD[27]	GND
6	C_REQ#	GND	CPCI_3.3	C_CLK	C_AD[31]	N/C
5	N/C	N/C	C_RST#	GND	C_GNT#	GND
4	N/C	GND	CPCI_VIO	N/C	N/C	N/C
3	C_INTA#	C_INTB#	C_INTC#	+5 V	C_INTD#	GND
2	C_TCK	+5 V	C_TMS	N/C	C_TDI	N/C
1	+5 V	-12 V	C_TRST#	+12 V	+5 V	GND

Figure A-2 J1 Connector and Pinout

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J2 Connector and Pinout

The VMICPCI-7611 J2 connector is a 2mm “Hard Metric” CompactPCI connector, with 5 rows, of 22 pins each. J2 is required for system slot CPUs. An additional external metal shield is also used, labeled row F. This connector’s controlled impedance minimizes unwanted signal reflections. Figure A-3 illustrates the J2 connector and the connector pinout.



Pin No.	Row A	Row B	Row C	Row D	Row E	Row F
22	N/C	N/C	N/C	N/C	N/C	GND
21	C_CLK[6]	GND	N/C	N/C	N/C	N/C
20	C_CLK[5]	GND	N/C	GND	N/C	GND
19	GND	GND	N/C	N/C	N/C	N/C
18	N/C	N/C	N/C	GND	N/C	GND
17	N/C	GND	C-PRST#	C_REQ6#	C_GNT6#	N/C
16	N/C	N/C	C_DEG#	GND	N/C	GND
15	N/C	GND	C_FAL#	C_REQ5#	C_GNT5#	N/C
14	N/C	N/C	N/C	GND	N/C	GND
13	N/C	GND	CPCI_VIO	N/C	N/C	N/C
12	N/C	N/C	N/C	GND	N/C	GND
11	N/C	GND	CPCI_VIO	N/C	N/C	N/C
10	N/C	N/C	N/C	GND	N/C	GND
9	N/C	GND	CPCI_VIO	N/C	N/C	N/C
8	N/C	N/C	N/C	GND	N/C	GND
7	N/C	GND	CPCI_VIO	N/C	N/C	N/C
6	N/C	N/C	N/C	GND	N/C	GND
5	C_C/BE5#	GND	CPCI_VIO	C_C/BE4#	C_PAR64	N/C
4	CPCI_VIO	N/C	C_C/BE7#	GND	C_C/BE6#	GND
3	C_CLK[4]	GND	C_GNT3#	C_REQ4#	C_GNT4#	N/C
2	C_CLK[2]	C_CLK[3]	GND	C_GNT2#	C_REQ3#	GND
1	C_CLK[1]	GND	C_REQ1#	C_GNT1#	C_REQ2#	N/C

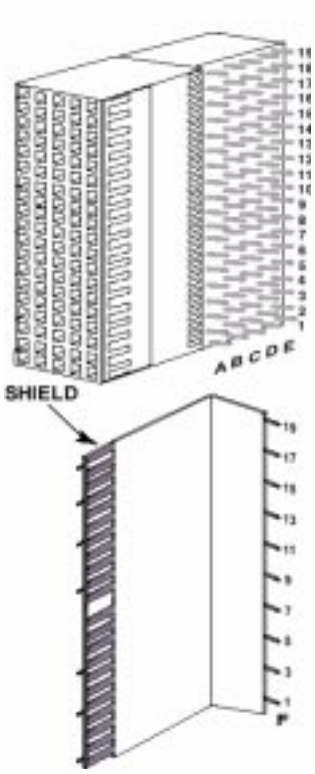
* CPCI_VIO - The VMICPCI-7611 is a universal VIO design.
* The VMICPCI-7611 supports a 32-bit CPCI bus.
* J2 Row C pins 15 and 16 are not supported.

Figure A-3 J2 Connector and Pinout

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J3 Connector Pinout

The J3 connector is 5 rows of 19 pins each, 2mm “Hard Metric” CompactPCI connector. An additional external metal shield is also used, labeled row F. Figure A-4 illustrates the J3 connector and the connector pinout. This connector is also used to route the serial, floppy, and harddrive signals to the backplane I/O.



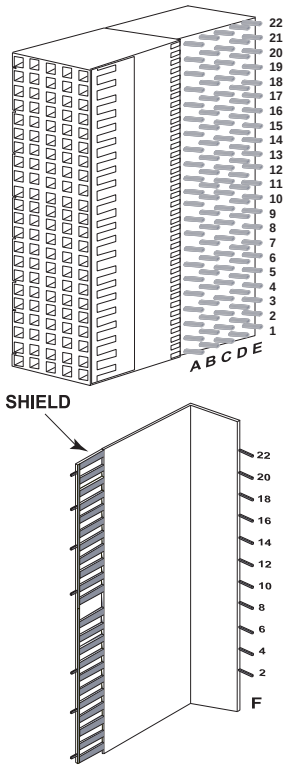
Pin No.	Row A	Row B	Row C	Row D	Row E	Row F
19	GND	ACK#	BUSY	PE	SLCT	GND
18	PD4	PD5	PD6	PD7	GND	N/C
17	PD1	INIT#	PD2	SLIN#	PD3	GND
16	N/C	STB#	AFD#	PD0	ERR#	N/C
15	USBP1+RTC	USBP1-RTC	USB0C1#	DATA	CLK	GND
14	GND	SP0_R1#B	SP0_DTR#B	SP0_CTS#B	SP0_TXB	N/C
13	SP0_RTS	SP0_RXB	SP0_DSR#B	SP0_DCD#B	N/C	GND
12	SP1_RTS	N/C	+5 V	N/C	+12 V	N/C
11	GND	SP1_R1#B	SP1_DTR#B	SP1_CTS#B	SP1_TXB	GND
10	DAP0	SP1_RXB	SP1_DSR#B	SP1_DCD#	DAP2PR	N/C
9	DAP1	REDWC#	IDEIORDY	IDESELA	IDEIOW0#	GND
8	DIR#	INDEX#	IDECS01#	DOP[8]	DOP[6]	N/C
7	SIDE1#	IDEIOR0#	HD_ACTA#	DOP[9]	DOP[7]	GND
6	RDATA#	TRK0#	IDECS03#	DOP[10]	DOP[2]	N/C
5	DRATE0#	WDATA#	IDEIRQ14	DOP[11]	DOP[3]	GND
4	DRVSB#	STEP#	IDE0ACK0#	DOP[12]	DOP[4]	N/C
3	DSKCHG#	MOTEB#	+5 V	DOP[13]	DOP[5]	GND
2	WPT#	DRVSA#	IDEDRQ0	DOP[14]	DOP[0]	N/C
1	WGATE#	MOTEA#	IDERST#	DOP[15]	DOP[1]	GND

Figure A-4 J3 Connector and Pinout

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J5 Connector and Pinout

The VMICPCI-7611 J5 connector is a 2mm “Hard Metric” CompactPCI connector, with 5 rows, of 22 pins each. An additional external metal shield is also used, labeled row F. This connector’s controlled impedance minimizes unwanted signal reflections. Figure A-5 illustrates the J5 connector and the connector pinout.



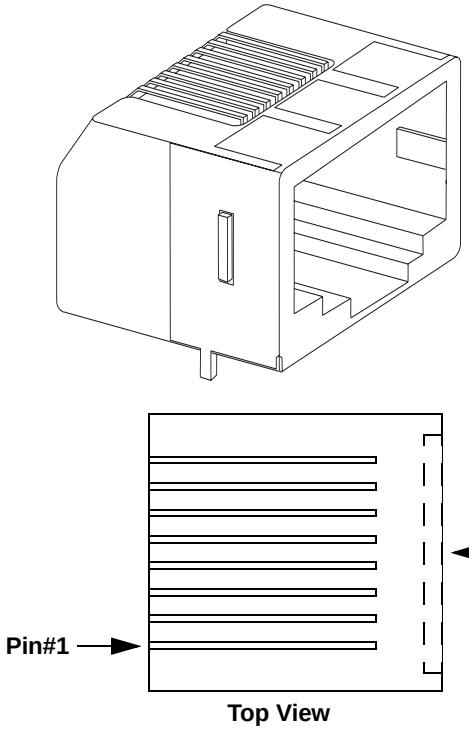
Pin No.	Row A	Row B	Row C	Row D	Row E	Row F
22	PMC_A22_5	PMC_B22_4	PMC_C22_3	PMC_D22_2	PMC_E22_1	GND
21	PMC_A21_10	PMC_B21_9	PMC_C21_8	PMC_D21_7	PMC_E21_6	N/C
20	PMC_A20_15	PMC_B20_14	PMC_C20_13	PMC_D20_12	PMC_E20_11	GND
19	PMC_A19_20	PMC_B19_19	PMC_C19_18	PMC_D19_17	PMC_E19_16	N/C
18	PMC_A18_25	PMC_B18_24	PMC_C18_23	PMC_D18_22	PMC_E18_21	GND
17	PMC_A17_30	PMC_B17_29	PMC_C17_28	PMC_D17_27	PMC_E17_26	N/C
16	PMC_A16_35	PMC_B16_34	PMC_C16_33	PMC_D16_32	PMC_E16_31	GND
15	PMC_A15_40	PMC_B15_39	PMC_C15_38	PMC_D15_37	PMC_E15_36	N/C
14	PMC_A14_45	PMC_B14_44	PMC_C14_43	PMC_D14_42	PMC_E14_41	GND
13	PMC_A13_50	PMC_B13_49	PMC_C13_48	PMC_D13_47	PMC_E13_46	N/C
12	PMC_A12_55	PMC_B12_54	PMC_C12_53	PMC_D12_52	PMC_E12_51	GND
11	PMC_A11_60	PMC_B11_59	PMC_C11_58	PMC_D11_57	PMC_E11_56	N/C
10	VIO	PMC_B10_64	PMC_C10_63	PMC_D10_62	PMC_E10_61	GND
9	GND	3.3V	N/C	GND	GND	GND
8	GND	GND	GND	GND	GND	GND
7	GND	GND	TXOUT0+	GND	GND	GND
6	GND	TXOUT1+	TXOUT0-	GND	GND	GND
5	GND	TXOUT1-	TXOUT2+	GND	GND	GND
4	GND	TXCLKOUT+	TXOUT2-	GND	GND	GND
3	GND	TXCLKOUT-	TXOUT3+	GND	GND	GND
2	GND	GND	TXOUT3-	GND	GND	GND
1	THERM#	GND	GND	GND	GND	GND

Figure A-5 J5 Connector and Pinout

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Ethernet Connector Pinout (J14)

The pinout diagram for the Ethernet 10BaseT and 100BaseTx connector is shown in Figure A-6.



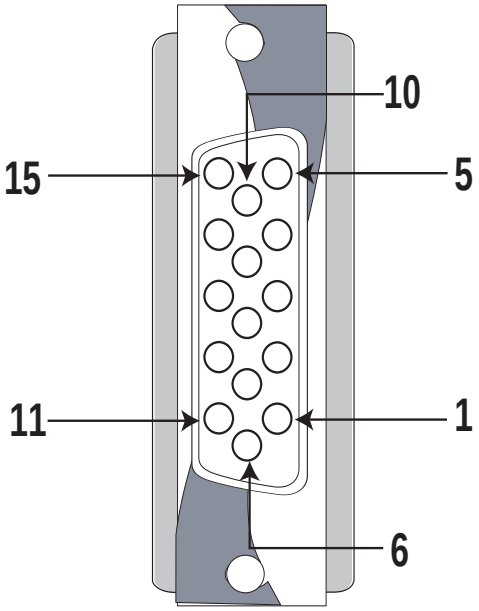
ETHERNET CONNECTOR (10BaseT, 100BaseTx)		
PIN	**Signal Name**	
1	TD+	Transmit Data
2	TD-	Transmit Data
3	RD+	Receive Data
4	NC	No Connection
5	NC	No Connection
6	RD-	Receive Data
7	NC	No Connection
8	NC	No Connection

Figure A-6: Ethernet Connector and Pinout

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Video Connector Pinout (J11)

The video port uses a standard high-density DB15 SVGA connector. Figure A-7 illustrates the connector and pinout.



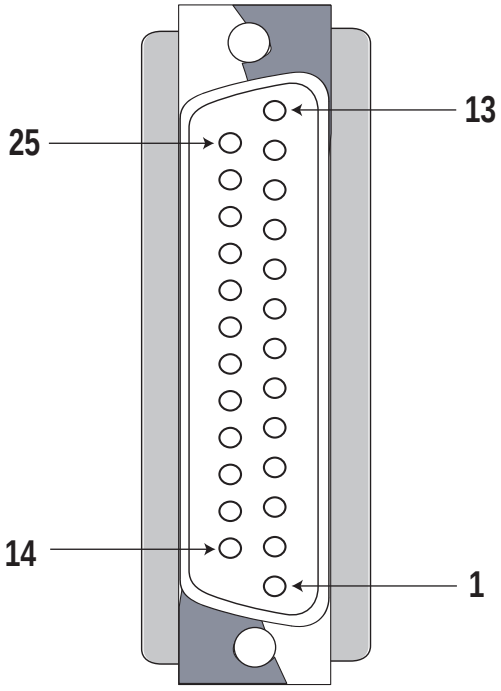
Video Connector		
Pin	**Direction**	**Function**
1	Out	Red
2	Out	Green
3	Out	Blue
4		Reserved
5		Ground
6		Ground
7		Ground
8		Ground
9		5 V
10		Ground
11		Reserved
12		I2 Data
13	Out	Horizontal SYNC
14	Out	Vertical SYNC
15		I2 Clock
Shield		Chassis Ground

Figure A-7 Video Connector and Pinout

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Parallel Port Connector Pinout (P2)

The parallel port shown in Figure A-8 uses a Microminiature DB25 female connector typical of any PC / AT system. An adapter to connect standard DB25 parallel port products to the Microminiature connector is available. Please refer to the "VMICPCI-7611 Product Specification" for ordering information.



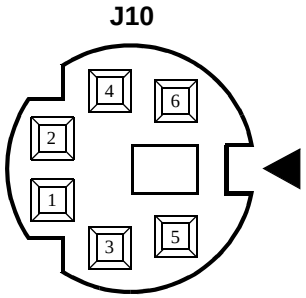
Parallel Port Connector		
Pin	**Direction**	**Function**
1	In / Out	Data Strobe
2	In / Out	Bidirectional Data D0
3	In / Out	Bidirectional Data D1
4	In / Out	Bidirectional Data D2
5	In / Out	Bidirectional Data D3
6	In / Out	Bidirectional Data D4
7	In / Out	Bidirectional Data D5
8	In / Out	Bidirectional Data D6
9	In / Out	Bidirectional Data D7
10	In	Acknowledge
11	In	Device Busy
12	In	Out of Paper
13	In	Device Selected
14	Out	Auto Feed
15	In	Error
16	Out	Initialize Device
17	In	Device Ready for Input
18		Signal Ground
19		Signal Ground
20		Signal Ground
21		Signal Ground
22		Signal Ground
23		Signal Ground
24		Signal Ground
25		Signal Ground
Shield		Chassis Ground

Figure A-8 P2 Connector and Pinout

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Keyboard and Mouse Connectors and Pinout (J10)

The keyboard and mouse connectors are standard 6-pin female mini-DIN PS/2 connectors as shown in Figure A-9 and Table A-1.



Keyboard/Mouse Connector*		
Pin	**Dir**	**Function**
1	In/Out	Mouse Data
2	In/Out	Keyboard Data
3		Ground
4		+5 V
5	Out	Mouse Clock
6	Out	Keyboard Clock
Shield		Chassis Ground
An adapter cable is included with the VMICPCI-7611 to separate the keyboard and mouse connector.		

Figure A-9 Keyboard/Mouse Connector and Pinout

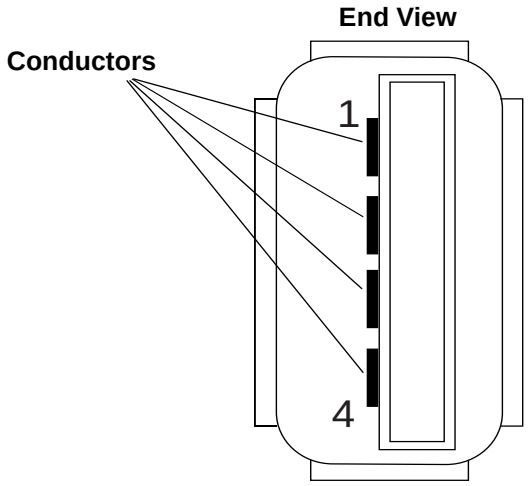
Table A-1 Keyboard/Mouse Y Splitter Cable

Keyboard			Mouse		
Pin	**Dir**	**Function**	**Pin**	**Dir**	**Function**
1	In/Out	Keyboard Data	1	In/Out	Mouse Data
2		Unused	2		Unused
3		Ground	3		Ground
4		+5 V	4		+5 V
5	Out	Keyboard Clock	5	Out	Mouse Clock
6		Unused	6		Unused
Shield		Chassis Ground	Shield		Chassis Ground

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USB Connector (J9)

The Universal Serial Bus (USB) port uses an industry standard four position shielded connector. Figure A-10 shows the pinout of the USB connector.



Pin	Signal	Function
1	USBV	USB Power
2	USB-	USB Data -
3	USB+	USB Data +
4	USBG	USB Ground

Figure A-10 USB Connector Pinout

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PMC Connector Pinout

PMC J7 Connector and Pinout

The PCI Mezzanine Card (PMC) carries the same signals as the PCI standard; however, the PMC standard uses a completely different form factor. Tables A-1 through A-3 are the pinouts for the PMC connectors (J6, J7, and J4).

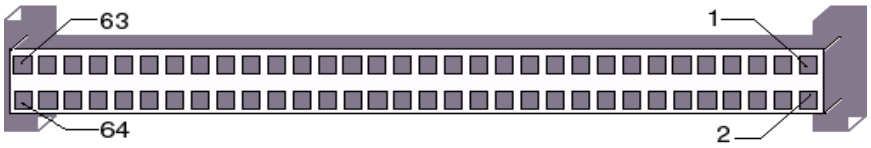


Table A-2 PMC J7 Connector Pinout

PMC Connector (J7)				PMC Connector (J7)			
Left Side		Right Side		Left Side		Right Side	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	GND	2	-12	33	FRAME#	34	GND
3	GND	4	INTC#	35	GND	36	IRDY#
5	INTD#	6	INTA#	37	DEVSEL#	38	+5 V
7	BMODE1A	8	+5 V	39	GND	40	LOCK#
9	INTB#	10	NC	41	SDONE#	42	NC
11	GND	12	NC	43	PAR	44	GND
13	CLK	14	GND	45	+5 V	46	AD[15]
15	GND	16	GNT#	47	AD[12]	48	AD[11]
17	REQ#	18	+5 V	49	AD[9]	50	+5 V
19	+5 V	20	AD[31]	51	GND	52	C/BE0#
21	AD[28]	22	AD[27]	53	AD[6]	54	AD[5]
23	AD[25]	24	GND	55	AD[4]	56	GND
25	GND	26	C/BE3#	57	+5 V	58	AD[3]
27	AD[22]	28	AD[21]	59	AD[2]	60	AD[1]
29	AD[19]	30	+5 V	61	AD[0]	62	+5 V
31	+5 V	32	AD[17]	63	GND	64	REQ64#

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PMC J6 Connector and Pinout

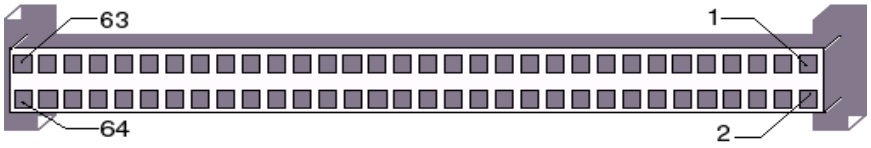


Table A-3 PMC J6 Connector Pinout

PMC Connector (J6)				PMC Connector (J6)			
Left Side		Right Side		Left Side		Right Side	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	+12 V	2	+5 V	33	GND	34	NC
3	GND	4	NC	35	TRDY	36	+3.3 V
5	+5 V	6	GND	37	GND	38	STOP#
7	GND	8	NC	39	PERR#	40	GND
9	NC	10	NC	41	+3.3 V	42	SERR#
11	PRSNT2	12	+3.3 V	43	C/BE1#	44	GND
13	RST#	14	GND	45	AD[14]	46	AD[13]
15	+3.3 V	16	GND	47	GND	48	AD[10]
17	NC	18	GND	49	AD[8]	50	+3.3 V
19	AD[30]	20	AD[29]	51	AD[7]	52	NC
21	GND	22	AD[26]	53	+3.3 V	54	NC
23	AD[24]	24	+3.3 V	55	NC	56	GND
25	IDSEL	26	AD[23]	57	NC	58	NC
27	+3.3 V	28	AD[20]	59	GND	60	NC
29	AD[18]	30	GND	61	ACK64#	62	+3.3 V
31	AD[16]	32	C/BE2#	63	GND	64	NC

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PMC J4 Connector and Pinout

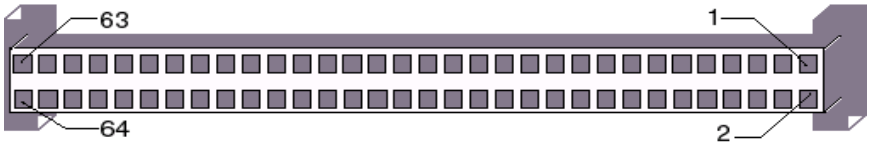


Table A-4 PMC J4 Connector Pinout

PMC Connector (J4)				PMC Connector (J4)			
Left Side		Right Side		Left Side		Right Side	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	J5_PMC_E22_1	2	J5_PMC_D22_2	33	J5_PMC_C16_33	34	J5_PMC_B16_34
3	J5_PMC-C22_3	4	J5_PMC_B22_4	35	J5_PMC_A16_35	36	J5_PMC_E15_36
5	J5_PMC_A22_5	6	J5_PMC_E21_6	37	J5_PMC_D15_37	38	J5_PMC_C15_38
7	J5_PMC_D21_7	8	J5_PMC_C21_8	39	J5_PMC_B15_39	40	J5_PMC_A15_40
9	J5_PMC_B21_9	10	J5_PMC_A21_10	41	J5_PMC_E14_41	42	J5_PMC_D14_42
11	J5_PMC_E20_11	12	J5_PMC_D20_12	43	J5_PMC_C14_43	44	J5_PMC_B14_44
13	J5_PMC_C20_13	14	J5_PMC_B20_14	45	J5_PMC_A14_45	46	J5_PMC_E13_46
15	J5_PMC_A20_15	16	J5_PMC_E19_16	47	J5_PMC_D13_47	48	J5_PMC_C13_48
17	J5_PMC_D19_17	18	J5_PMC_C19_18	49	J5_PMC_B13_49	50	J5_PMC_A13_50
19	J5_PMC_B19_19	20	J5_PMC_A19_20	51	J5_PMC_E12_51	52	J5_PMC_D12_52
21	J5_PMC_E18_21	22	J5_PMC_D18_22	53	J5_PMC_C12_53	54	J5_PMC_B12_54
23	J5_PMC_C18_23	24	J5_PMC_B18_24	55	J5_PMC_A12_55	56	J5_PMC_E11_56
25	J5_PMC_A18_25	26	J5_PMC_E17_26	57	J5_PMC_D11_57	58	J5_PMC_C11_58
27	J5_PMC_D17_27	28	J5_PMC_C17_28	59	J5_PMC_B11_59	60	J5_PMC_A11_60
29	J5_PMC_B17_29	30	J5_PMC_A17_30	61	J5_PMC_E10_61	62	J5_PMC_D10_62
31	J5_PMC_E16_31	32	J5_PMC_D16_32	63	J5_PMC_C10_63	64	J5_PMC_B10_64

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Appendix

B

Phoenix BIOS

Contents

First Boot 76
Main Menu 77
Advanced Menu 82
Power 86
Boot Menu 87
Exit Menu 88

Introduction

The VMICPCI-7611 utilizes the BIOS (Basic Input / Output System) in the same manner as other PC / AT compatible computers. This appendix describes the menus and options associated with the VMICPCI-7611 BIOS.

System BIOS Setup Utility

During system bootup, press the F2 key to access the Phoenix BIOS Main screen. From this screen, the user can select any section of the Phoenix (system) BIOS for configuration, such as floppy drive configuration or system memory. The parameters shown throughout this section are the default values.

Help Window

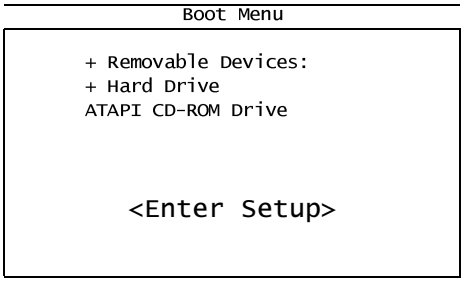
The help window on the right side of each menu displays the help text for the currently selected field. It updates as you move the cursor to each field. Pressing F1 or Alt- H on any menu brings up the General Help window that describes the legend keys and their alternates. The scroll bar on the right of any window indicates that there is more than one page of information in the window. Use PgUp and PgDn to display all the pages. Pressing Home and End displays the first and last page. Pressing Enter displays each page and then exits the window. Press Esc to exit the current window.

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First Boot

The VMICPCI-7611 has a First Boot menu to enable the user to, on a one time basis, select a drive device to boot from. This feature is useful when installing from a bootable disk. For example, when installing Windows NT from a CD enter the First Boot menu and using the arrows keys highlight ATAPI CD-ROM Drive then press “ENTER” to continue with system boot.

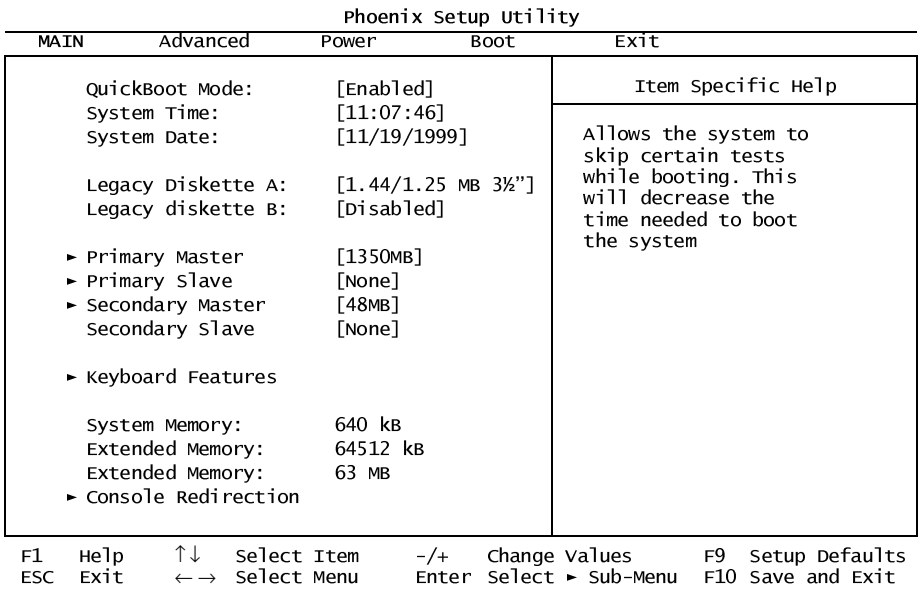
This feature is accessed by pressing the “ESC” at the very beginning of the boot cycle. The selection made from this screen applies to the current boot only, and will not be used during the next boot-up of the system. If you have trouble accessing this feature, disable the QuickBoot Mode in the Main BIOS setup screen. Exit, saving changes and retry accessing the First Boot menu.



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Main Menu

The Main menu allows the user to select QuickBoot, set the system clock and calendar, record disk drive parameters, and set selected functions for the keyboard.



QuickBoot

When enabled, certain checks normally performed during the POST are omitted, decreasing the time required to run the POST. The default is Enabled.

Setting The Time

The time format is based on the 24-hour military-time clock. For example, 1 PM is 13:00:00. Press the left or right arrow key to move the cursor to the desired field (hour, minute, seconds). Press the PgUp or PgDn key to step through the available choices, or type in the information.

Setting The Date

Press the left or right arrow key to move the cursor to the desired field (month, day, year). Press the PgUp or PgDn key to step through the available choices, or type in the information.

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Legacy Diskette

Floppy Drive A

The VMICPCI-7611 supports one floppy disk drive. The options are:

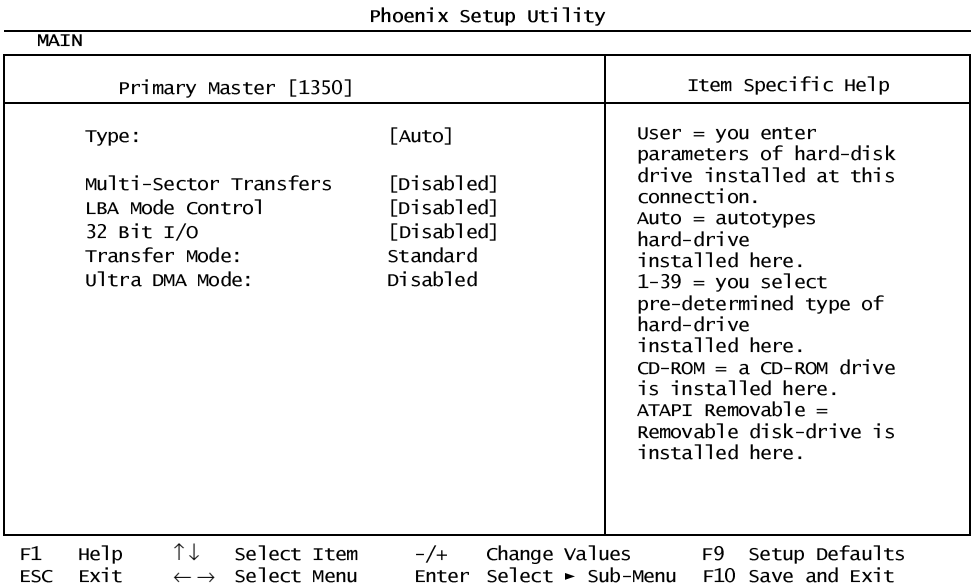
- None — No diskette drive installed
- 360K, 5.25 in — 5-1/4 inch PC-type standard drive; 360 kilobyte capacity
- 1.2M, 5.25 in — 5-1/4 inch AT-type high-density drive; 1.2 megabyte capacity
- 720K, 3.5 in — 3-1/2 double-sided drive; 720 kilobyte capacity
- 1.44M, 3.5 in — 3-1/2 inch double-sided drive; 1.44 megabyte capacity
- 2.88M, 3.5 in — 3-1/2 inch double-sided drive; 2.88 megabyte capacity
- Use PgUp or Pgdn to select the floppy drive. The default is 1.44M, 3.5 inch.

Floppy Drive B

The VMICPCI-7611 does not support a second floppy drive. The default is Disabled.

Primary Master/Slave

The VMICPCI-7611 has the capability of utilizing one IDE hard disk drive on the Primary Master bus. The default setting is Auto. The Primary Slave is assigned to the CD-ROM (if installed).



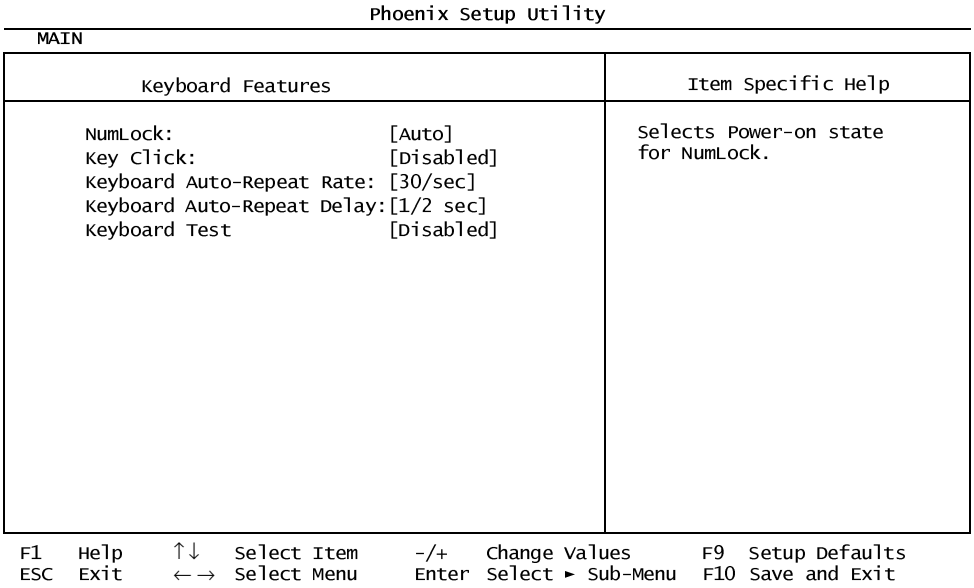
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Secondary Master

The Secondary Master is the resident Flash Disk (if installed). The default setting is Auto.

Keyboard Features

The Keyboard Features allows the user to set several keyboard functions.



NumLock

The NumLock can be set to Auto, On, or Off to control the state of the NumLock key when the system boots. When set to Auto or On, the numeric keypad generates numbers instead of controlling the cursor operations. The default is On.

Key Click

This option enables or disables the Keyboard Auto-Repeat Rate and Delay settings. When disabled the values in the Typematic Rate and Delay are ignored. The default is Disabled.

Keyboard Auto-Repeat Rate (Chars/Sec)

If the Key Click is enabled this determines the rate a character is repeated when a key is held down. The options are: 30, 26.7, 21.8, 18.5, 13.3, 10, 6, or 2 characters per second. The default is 30.

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Keyboard Auto-Repeat Delay (sec)

If the Key Click is enabled this determines the delay before a character starts repeating when a key is held down. The options are: 1/4, 1/2, 3/4, or 1 second. The default is 1/2.

Keyboard Test

When enabled this feature will test the keyboard during boot-up.

System Memory

The System Memory field is for informational purposes only and cannot be modified by the user. This field displays the base memory installed in the system.

Extended Memory

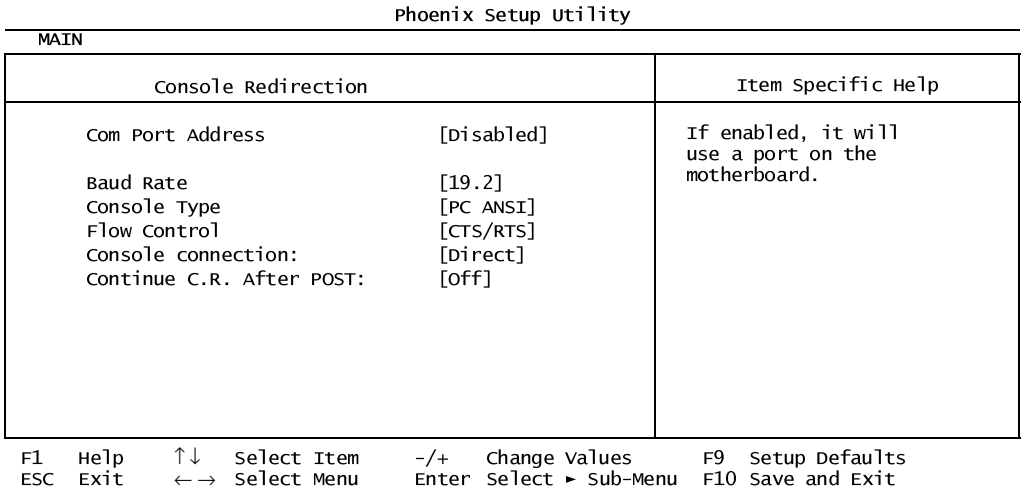
The Extended Memory field is for informational purposes only and cannot be modified by the user. This field displays the total amount of memory installed in the system in Kbytes.

Extended Memory

The Extended Memory field is for informational purposes only and cannot be modified by the user. This field displays the total amount of memory installed in the system in Mbytes.

Console Redirection

Console Redirection allows for remote access and control of the PC functions to a remote terminal via the serial port. Selecting Console Redirection provides addition menus used to configure the console.



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Com Port Address

If enabled, it will allow remote access through the serial port. The options are: Disabled, Motherboard Com A, and Motherboard Com B. The default is Disabled.

Baud Rate

Selects a baud rate for the serial port. The options are: 600, 1200, 2400, 4800, 9600, 19.2, 38.4, and 115.2. The default is 19.2.

Console Type

Selects the type of console to be used. The options are: PC ANSI or VT100. The default is PC ANSI.

Flow Control

Enables are disables Flow Control. The options are No Flow Control, XON / XOFF, or CTS / RTS. The default is CTS / RTS.

Console Connection

Indicates whether the console is connected directly to the system or if a modem is being used to connect. The options are: Direct or Via Modem. The default is Direct.

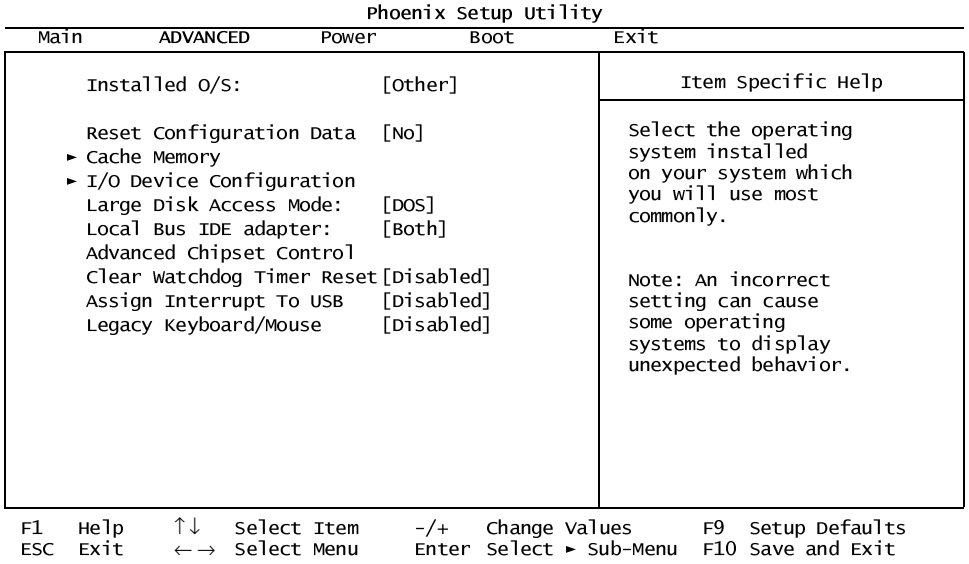
Continue C.R. After POST

This enables console redirection after the operating system has loaded. The options are Off or ON. The default setting is OFF.

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Advanced Menu

Selecting Advanced from the Main menu will display the screen shown below.



Installed O/S

Use this feature to select the operating system to use with your system.

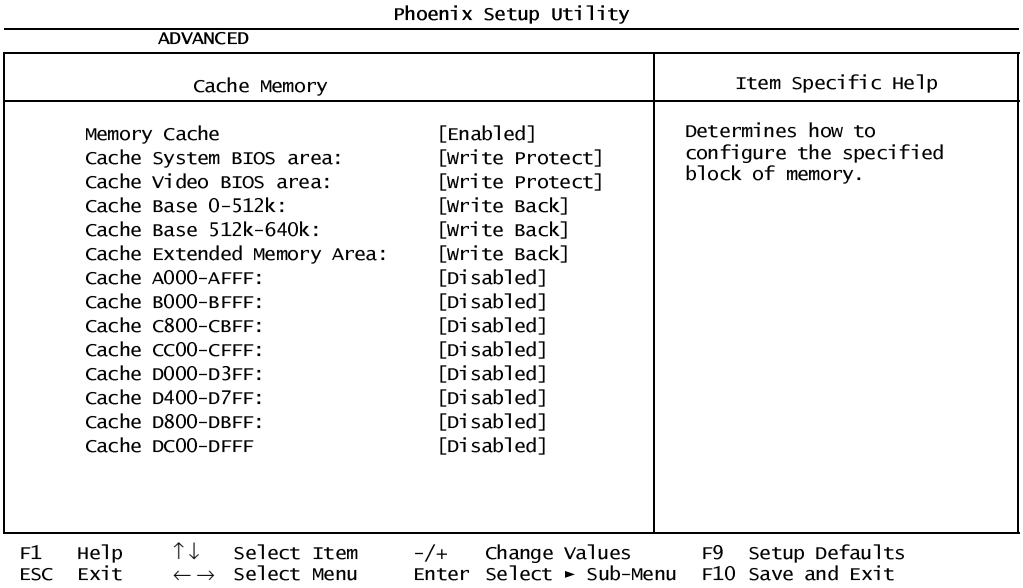
Reset Configuration Data

Select Yes if you want to clear the extended system configuration data. The default is No.

Cache Memory

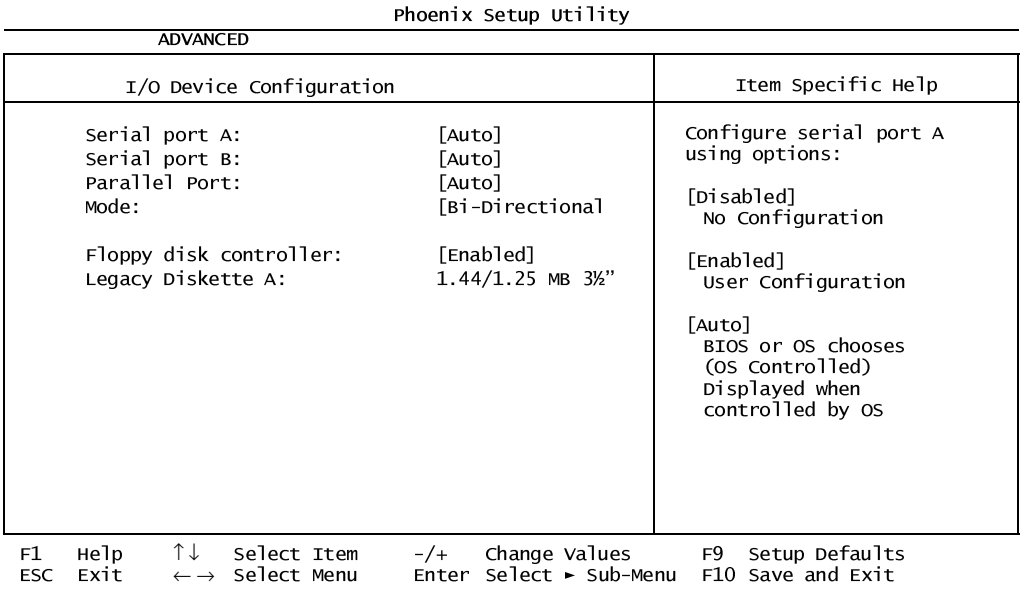
Enabling the cache memory enhances the speed of the processor. When the CPU requests data, the system transfers the requested data from the main DRAM into the cache memory were it is stored until processed by the CPU. The default is Enabled.

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I/O Device Configuration

Select this menu to configure your I/O devices, if required.



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Large Disk Access Mode

The options for the Large Disk Access Mode are: UNIX Novell Netware or Other.

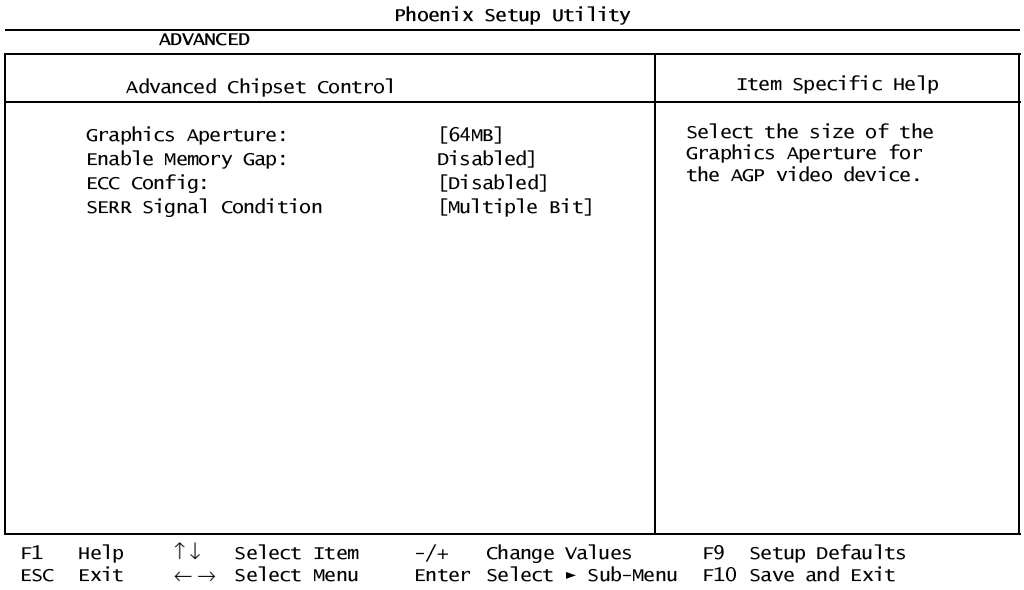
If you are installing new software and the drive fails, change this selection and try again. Different operating systems require different representations of drive geometries. The default is Other.

Local Bus IDE Adapter

This enables or disables the intergrated local bus IDE adapter. The options are: Disabled, Primary, Secondary, or Both. The default is both.

Advanced Chipset Control

Selecting Advanced Chipset Control opens the menu below. Use this menu to change the values in the chipset register for optimizing your system's performance.



Graphics Aperture

Select the size of the graphics aperture for the ACP video device. The options are 4MB, 8MB, 16MB, 32MB, 64MB, 128MB, or 256MB. The default is 64MB.

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Enable Memory Map

If enabled, turn system RAM off to free address space for use with an option card. Either a 128KB conventional memory gap, starting at 512KB, or a 1MB extended memory gap, starting at 15MB, will be created in the system RAM. The options are Disabled, Conventional, or Extended. The default is Disabled.

ECC Config

If all memory in the system supports ECC (x72) the ECC Config selects from No ECC (Disabled), Checking Only (EC), Checking and Correction (ECC), or Checking, Correction with Scrubbing (ECC Scrub). The default is Disabled.

SERR Signal Configuration

Select ECC error conditions that SERR# will be asserted. The options are: None, Single Bit, Multiple Bit, or Both. The default is Both.

Clear Watchdog Timer Reset

If enabled, after power-up or reset, the BIOS will clear the onboard Watchdog Timer so it will not generate a Watchdog Reset or NMI. The default is Disabled.

Assign Interrupt To USB

Enabled assigns an interrupt to the USB. The default is Disabled.

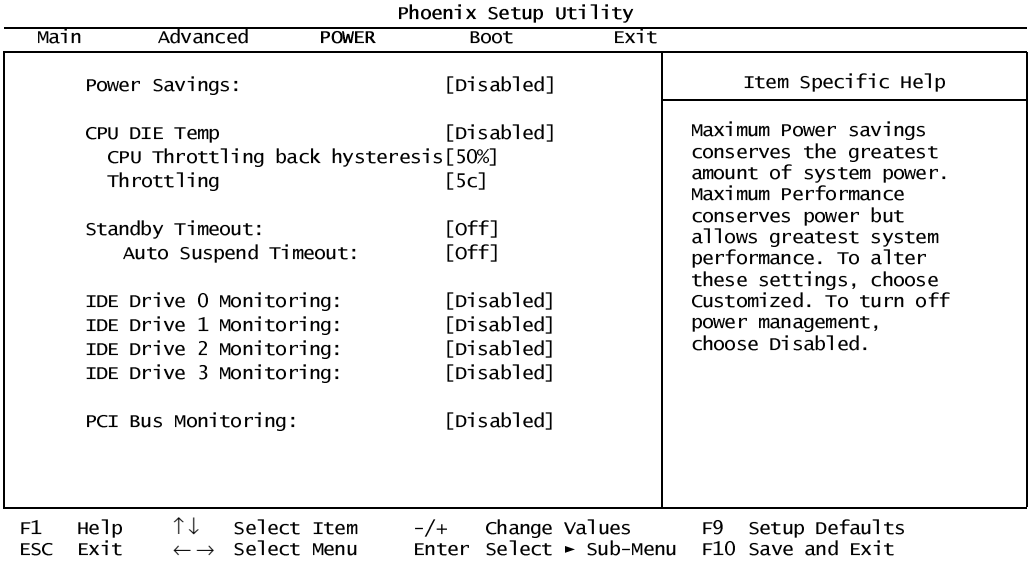
Legacy Keyboard/Mouse

Enabled supports a legacy keyboard and mouse on the USB. The default is Disabled.

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Power

This screen, selected from the Main screen, allows the user to configure power saving options on the VMICPCI-7611.

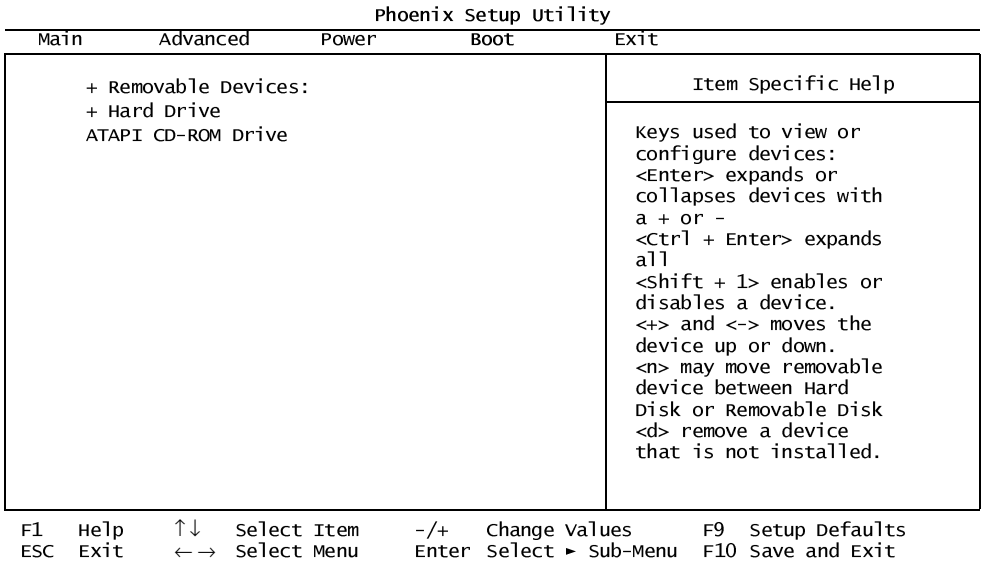


The Throttling and CPU Throttling back hysteresis selections will only be shown if CPU DIE Temp is enabled. The default for Throttling is 50%. The default for CPU Throttling back hysteresis is 5c.

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Boot Menu

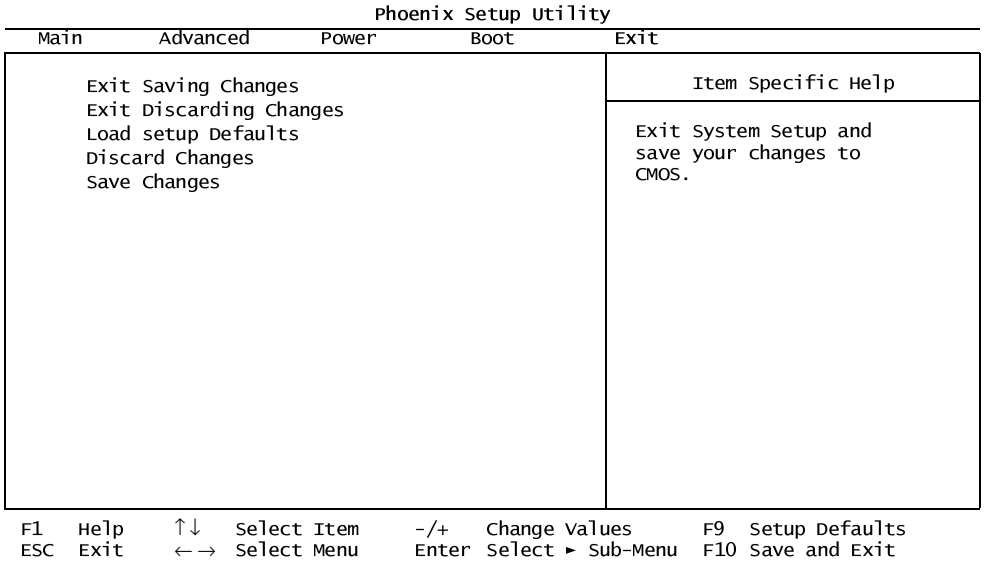
The Boot priority is determined by the stack order, with the top having the highest priority and the bottom the least. The order can be modified by highlighting a device and, using the <+> or <-> keys, moving it to the desired order in the stack. A device can be boot disabled by highlighting the particular device and pressing <Shift 1>. <Enter> expands or collapses devices with a + or - next to them.



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Exit Menu

The Exit menu allows the user to exit the BIOS program, while either saving or discarding any changes. This menu also allows the user to restore the BIOS defaults if desired.



Exit Saving Changes

Exit System Setup and save your changes to CMOS.

Exit Discarding Changes

Exit System Setup, discarding any changes to CMOS.

Load Setup Defaults

Load System defaults as defined at the factory.

Discard Changes

Discard any changes without exiting the setup program.

Save Changes

Save any changes made without exiting the Setup program.

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Appendix

C

Device Configuration: I/O and Interrupt Control

Contents

BIOS Operations 90
Device Address Definition. 94
Device Interrupt Definition 96

Introduction

This appendix provides the user with the information needed to develop custom applications for the VMICPCI-7611. The CPU board on the VMICPCI-7611 is unique in that the BIOS can not be removed; it must be used in the initial boot cycle. A custom application, like a revised operating system for example, can only begin to operate after the BIOS has finished initializing the CPU. The VMICPCI-7611 will allow the user to either maintain the current BIOS configuration or alter this configuration to be more user specific, but this alteration can only be accomplished after the initial BIOS boot cycle has completed.

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BIOS Operations

When the VMICPCI-7611 is powered on, control immediately jumps to the BIOS. The BIOS initiates a Power-on Self-Test (POST) program, which instructs the microprocessor to initialize system memory as well as the rest of the system. The BIOS establishes the configuration of all on-board devices by initializing their respective I/O and Memory addresses and interrupt request lines. The BIOS then builds an interrupt vector table in main memory, which is used for interrupt handling. The default interrupt vector table and the default address map are described in Chapter 3 of this manual. Finally, the BIOS jumps to the hard drive or floppy drive to execute the operating system's boot program. This is the point at which a custom operating system may take control of the board and proceed with a custom configuration and/or custom application. A user application may override the configuration set by the BIOS and reconfigure the system or it may accept what the BIOS initialized.

BIOS Control Overview

There are two areas on the VMICPCI-7611 in which the user must be familiar in order to override the initial BIOS configuration. These include the device addresses and the device interrupts. This appendix reviews the details of these addresses and interrupts, and provides a reference list for the individual devices used on the board.

The VMICPCI-7611 utilizes the high-performance Peripheral Component Interconnect (PCI) bus along with the Industrial Standard Architecture (ISA) bus. In general, the PCI bus is plug-and-play compatible. The components that are connected to the PCI bus are not always placed at a standard I/O or Memory address, nor are they connected to a standard interrupt request line as is the case with ISA bus devices. These PCI bus devices are re-established by the BIOS, meaning that these devices will not always be located at the same address or connected to the same interrupt request line every time the CPU is booted. This appendix lists the defaults that are found by powering up a specific VMICPCI-7611.

Functional Overview

The block diagram included in Figure C-1 on page 91 illustrates the VMICPCI-7611 emphasizing the I/O features, including the PCI-to-PCI bridge.

The circled number in the corner of a function block references the appropriate data book necessary for the programming of the function block.

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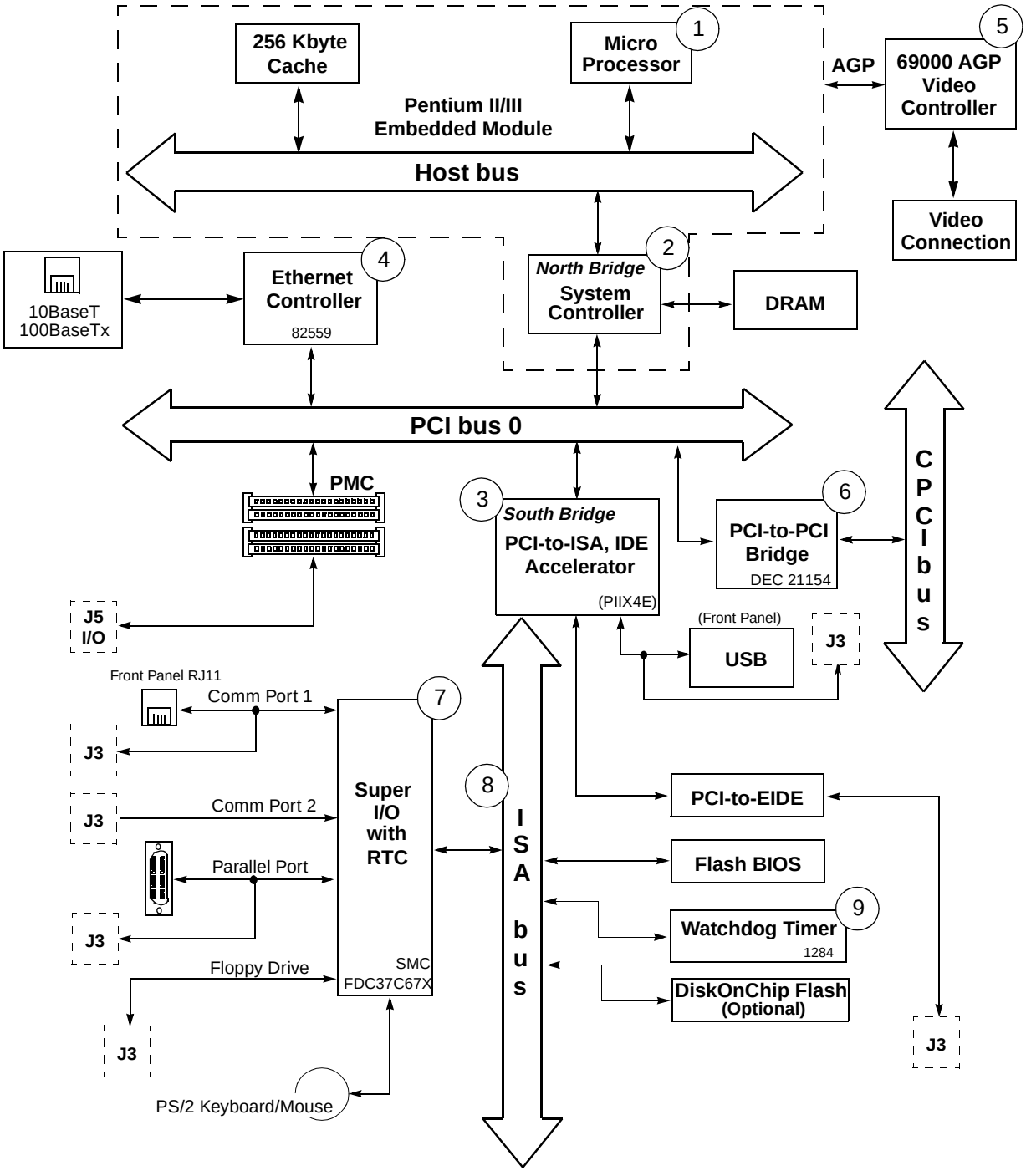


Figure C-1 VMICPCI-7611 Block Diagram

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Data Book References

1. *Pentium II/Pentium III Processor Developer's Manual*
   Intel Corporation
   2200 Mission College Blvd.
   P.O. Box 58119
   Santa Clara, CA 95052-8119
   (408) 765-8080
   www.intel.com
2. *Intel 440BX PCISet 82443BX Host Bridge/Controller*
   Intel Corporation
   2200 Mission College Boulevard
   P.O. Box 58119
   Santa Clara, CA 95052-8119
3. *Intel PIIX4E*
   82371EB PCI ISA IDE Xcellerator (PIIX4E)
   2200 Mission College Boulevard
   P.O. Box 58119
   Santa Clara, CA 95052-8119
4. *Intel 82559 10/100 Mb/s Ethernet LAN Controller*
   Intel
   www.intel.com
5. *Intel 69000 Technical Reference Manual*
   Intel Corporation
   2200 Mission College Blvd.
   P.O. Box 58119
   Santa Clara, CA 95052-8119
   (408) 765-8080
   www.intel.com
6. *PCI Local Bus Specification, Rev. 2.1*
   PCI Special Interest Group
   P.O. Box 14070
   Portland, OR 97214
   (800) 433-5177 (U.S.)
   (503) 797-4207 (International)
   (503) 234-6762 (FAX)
7. *SMC FDC37C67X Enhanced Super I/O Controller*
   SMC Component Products Division
   300 Kennedy Drive
   Hauppauge, NY 11788
   (516) 435-6000
   (516) 231-6004 (FAX)

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8. *ISA & EISA, Theory and Operation*
Solari, Edward
Annabooks
15010 Avenue of Science, Suite 101
San Diego, CA 92128 USA
ISBN 0-929392 -15-9

9. *DS 1284 Watchdog Timekeeping Controller*
Dallas Semiconductor
4461 South Beltwood Pwky
Dallas, TX 75244-3292

10. *IEEE P1386 PMC Specification*
The Institute of Electrical and Electronics Engineers, Inc.
345 East 47th Street
New York, NY 10017-2394
www.ieee.com

11. *Vita 29 Draft 0.92b PC-MIP Specification*
Vita Standards Organization
7825 East Gelding Drive
Suite 104
Scottsdale, AZ 85260
(602) 951-8866
www.vita.com

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Device Address Definition

The standard PC / AT architecture defines two distinctive types of address spaces for the devices and peripherals on the CPU board. These spaces have typically been named Memory address space and I / O address space. The boundaries for these areas are limited to the number of address bus lines that are physically located on the CPU board. The VMICPCI-7611 has 32 address bus lines located on the board, thereby defining the limit of the address space as 4 Gbyte. The standard PC / AT architecture defines Memory address space from zero to 4 Gbyte and the separate I / O address space from zero to 64 Kbyte.

ISA Devices

The ISA devices on the VMICPCI-7611 are configured by the BIOS at boot-up and adhere to the standard PC / AT architecture. They are mapped in I / O address space within standard addresses and their interrupts are mapped to standard interrupt control registers. However, all of the ISA devices with the exception of the real-time clock, keyboard, and programmable timer are relocatable to almost anywhere within the standard 1 Kbyte of I / O address space. Table C-1 defines the spectrum of addresses available for reconfiguration of ISA devices.

As previously stated, in the standard PC / AT system, all I / O devices are mapped in I / O address space. On the VMICPCI-7611, however, the Dynamic Random Access Memory (DRAM), is addressed in Memory address space. The BIOS places DRAM at address zero and extends to the physical limit of the on-board DRAM.

Table C-1 ISA Device Mapping Configuration

Device	Memory Space	I/O Address Space	PIC Interrupt Options	Byte Address Boundary	Default
Floppy	N / A	[0x100 - 0xFF8]	IRQ1 - IRQ15	8	$3F0
Serial Port 1	N / A	[0x100 - 0xFF8]	IRQ1 - IRQ15	8	$3F8
Serial Port 2	N / A	[0x100 - 0xFF8]	IRQ1 - IRQ15	8	$2F8
Real-Time Clock	Nonrelocatable				$070
Keyboard	Nonrelocatable				$060
Auxiliary I / O	N / A	- Primary I / O [0x000 - 0xFFF] - Secondary I / O [0x000 - 0xFFF]	IRQ1, IRQ3-IRQ15	1 1	
Watchdog Timer		0x500-50D	N / A	0xD	$500

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PCI Devices

PCI devices are fully configured under I/O and/or Memory address space. Table C-2 describes the PCI bus devices that are on-board the VMICPCI-7611 along with each device's configuration spectrum.

The PCI bus includes three physical address spaces. As with ISA bus, PCI bus supports Memory and I/O address space, but PCI bus includes an additional Configuration address space. This address space is defined to support PCI bus hardware configuration (refer to the PCI bus Specification for complete details on the configuration address space). PCI bus targets are required to implement Base Address registers in configuration address space to access internal registers or functions. The BIOS uses the Base Address register to determine how much space a device requires in a given address space and then assigns where in that space the device will reside. This functionality enables PCI devices to be located in either Memory or I/O address space.

Table C-2 PCI Device Mapping Configuration

Device	Memory Space	I/O Address Space	PIC Interrupt Options
Ethernet	Anywhere	Anywhere	PCI Defined
PMC Site	Anywhere	Anywhere	PCI Defined

** *Refer to the VMICPCI-7611-001 User's Manual.*

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Device Interrupt Definition

PC/AT Interrupt Definition

The interrupt hardware implementation on the VMICPCI-7611 is standard for computers built around the PC / AT architecture. The PC / AT evolved from the IBM PC / XT architecture. In the IBM PC / XT systems, only eight Interrupt Request (IRQ) lines exist, numbered from IRQ0 to IRQ7. These interrupt lines were included originally on a 8259A Priority Interrupt Controller (PIC) chip.

The IBM PC / AT computer added eight more IRQx lines, numbered IRQ8 to IRQ15, by cascading a second slave 8259A PIC into the original master 8259A PIC. The interrupt line IRQ2 at the master PIC was committed as the cascade input from the slave PIC. This master / slave architecture, the standard PC / AT interrupt mapping, is illustrated in Figure C-2 on page 97 within the PCI-to-ISA Bridge PIIX4E 82371EB section of the diagram.

To maintain backward compatibility with PC / XT systems, IBM chose to use the new IRQ9 input on the slave PIC to operate as the old IRQ2 interrupt line on the PC / XT Expansion Bus. Thus, in AT systems, the IRQ9 interrupt line connects to the old IRQ2 pin on the AT Expansion Bus (or ISA bus).

The BIOS defines the PC / AT interrupt line to be used by each device. The BIOS writes to each of the two cascaded 8259A PIC chips an 8-bit vector, which maps each IRQx to its corresponding interrupt vector in memory.

ISA Device Interrupt Map

The VMICPCI-7611 BIOS maps the IRQx lines to the appropriate device per the standard ISA architecture. Reference Figure C-2 on page 97. This initialization operation cannot be changed; however, a custom application could reroute the interrupt configuration after the BIOS has completed the initial configuration cycle.

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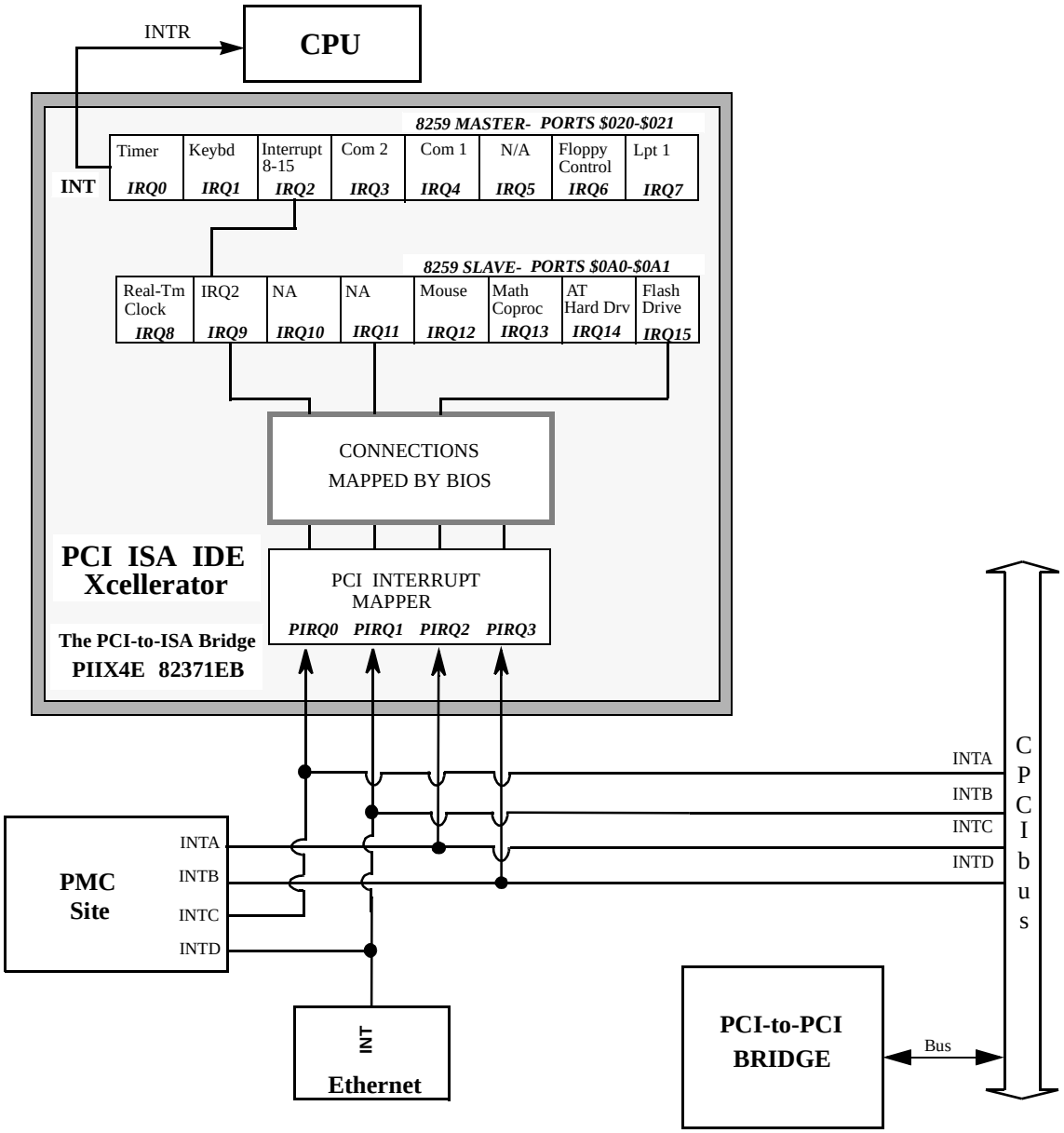


Figure C-2 BIOS Default Connections for the PC Interrupt Logic Controller

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PCI Device Interrupt Map

The PCI bus-based external devices include the two PCI expansion sites, the PCI-to-VMEbus bridge, and the VGA reserved connection. The default BIOS maps these external devices to the PCI Interrupt Request (PIRQx) lines of the PIIX4E. This mapping is illustrated in Figure C-2 on page 97 and is defined in Table C-3.

The device PCI interrupt lines (INTA through INTD) that are present on each device *cannot* be modified.

Table C-3 PCI Device Interrupt Mapping by the BIOS

DEVICE	COMPONENT	VENDOR ID	DEVICE ID	CPU ADDRESS MAP ID SELECT	DEVICE PCI INTERRUPT	MOTHER-BOARD PCI INTERRUPT MAPPER	DATA BOOK REF. #	Arbitration Level
Power Management	PIIX4E 82371EB Function	0x8086	0x7113	AD18	N / A	N / A	5	N / A
PCI-to-ISA Bridge	PIIX4E 82371EB Function 00	0x8086	0x7000	AD18	N / A	N / A	5	N / A
Ethernet Controller	Intel	0x8086	0x1229	AD22	INTA	PIRQ1	4	REQ1
PCI IDE Controller	PIIX4E 82371EB Function 01	0x8086	0x7111	AD18	N / A	N / A	5	N / A
PCI Host Bridge	Intel 440BX	0x8086	0x7190	N / A	N / A	N / A	2	N / A
PMC	N / A	N / A	N / A	AD31	INTA	PIRQ2	14	REQ3
Compact PCI Bridge	DEC 21154	0x1011	0x0026	AD26	N / A	N / A	3	REQ0

The motherboard accepts these PCI device interrupts through the PCI interrupt mapper function. The BIOS default maps the PCI Interrupt Request (PIRQx) external device lines to one of the available slave PIC Interrupt Request lines, IRQ (9, 10, 11, 12, 14, or 15).

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Index

100BaseTX 46, 67
10BaseT 46, 67
A
address map 90
B
BIOS 32, 43, 90
BIOS setup screens 75
block diagram 21
C
CMOS configuration 32
Configuring the DiskOnChip 50
Customer Service 26, 59
D
DiskOnChip 50
DMA controller 37
DMA page registers 37
DRAM 94
E
E-mail 59
Ethernet
  controller 98
  Intel 82559 Ethernet Controller 46
F
First Boot 76
Flash Disk 50
Floppy Disk Drive 78
Floppy Drive A 78
Floppy Drive B 78
G
graphics, video resolutions 47
I
I/O
  address space 37, 94
  features 19
  port map 37
installation 31
Interrupt Level Mode 56, 57
interrupt line assignment 39
Interrupt Output 56
Interrupt Pulse Mode 56, 57
Interrupt Switch 56
interrupt vector table 90
ISA bus 90
ISA device interrupt mapping 96
ISA devices 94
J
Jumper Locations 27
L
LPT1 Parallel I/O 38
LPT2 Parallel I/O 38
M
Maintenance 59
master interrupt controller 37
memory address space 94
N
Non-Maskable Interrupt (NMI) 39, 43
P
PC interrupt logic controller 44
PCI
  interrupt lines 42
  local bus 42
PCI bus 90
PCI host bridge 98
PCI IDE controller 98
PCI ISA bridge 98
Pentium CPU 36
Pentium III 36

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PIIX4E 98
Power Management 98
Power-on Self Test 90
programmable timer 37
protected mode 40
R
real mode 40
real-time clock 37
refresh rates 47
Return Material Authorization (RMA) number 59
RMA Number 59
S
screen resolutions 47
Serial I/O (COM1,2,3 & 4) 38
serial ports 45
SERR interrupt 43
SMC Super-I/O chip 45
System BIOS Setup Utility 75
T
Time of Day Alarm Flag 57
Time of Day Alarm Mask 57
Time of Day Registers 54
Transfer Enable 56
U
unpacking procedures 25
V
vector interrupt table 39
Video SDRAM 47
W
Watchdog Alarm 56
Watchdog Alarm Flag 57
Watchdog Alarm Mask 56
Watchdog Interrupt Output 56
Watchdog Registers 53
Watchdog Timer 52

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